CMOS Sensors for the Nominal DESY Beam Telescope

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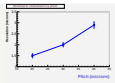
on behalf of DAPNIA-Saclay, LPSC-Grenoble, LPC-Clermont, IPHC-Strasbourg

OUTLINE

- Reminder (from transparencies shown in Oct. ’06 in Munich):
  - Basic improvements provided by final sensors
  - Development strategy
- Status of the development :
  - Column // r.o. architecture with integ. discri.
  - ADC
  - $\emptyset$ micro-cicuits
- Next steps :
  - Spatial resolution
  - Read-out frequency
  - Availability
- Summary

Introductory Remarks

  -

Essential Improvements Provided by Final Sensors

⇛ **Improvements focus on sensors equipping the arms (not DUT surface) :**

- **Increase of read-out speed by one order of magnitude :**
  - **Demonstrator provides frame read-out time of 1.6 ms (possibly 800 μs)**
  - **Final sensors will provide frame read-out time $\sim$ 100 μs (possibly $\sim$ 50 μs)**

- **Extension of sensitive area by factor 3.5 :**
  - **Demonstrator sensitive area : 7.68 x 7.68 mm^2**
  - **Final sensor sensitive area : 20.48 x 10.24 mm^2**
    $\longmapsto$ encompasses width of ILC-VD sensors

- **Integrate several other improvements resulting from R&D progress**
  ($\longmapsto$ signal amplification, data compression, etc.)

- **3 micro-circuit components developed in parallel :**
  - column // architecture with binary output
  - ADCs to be integrated at end of columns
  - ∅ micro-circuits to be integrated besides ADCs

- **Sharing of tasks :**
  - Col. // architecture design : DAPNIA & IPHC
  - ADC designs : LPC-Clermont, LPSC-Grenoble, DAPNIA, IPHC
  - ∅ micro-circuit design : IPHC (or nearly so ...)
  - chips characterisation : IN2P3 (several labs), DAPNIA, DESY et al., INFN (several labs)
    - ★ likely to be a bottle neck ...

- **2 design options under consideration :**
  - Sensors with binary encoding of signal charge : most straightforward
  - Sensors with 4- or 5-bit ADC encoding : will provide twice better spatial resolution

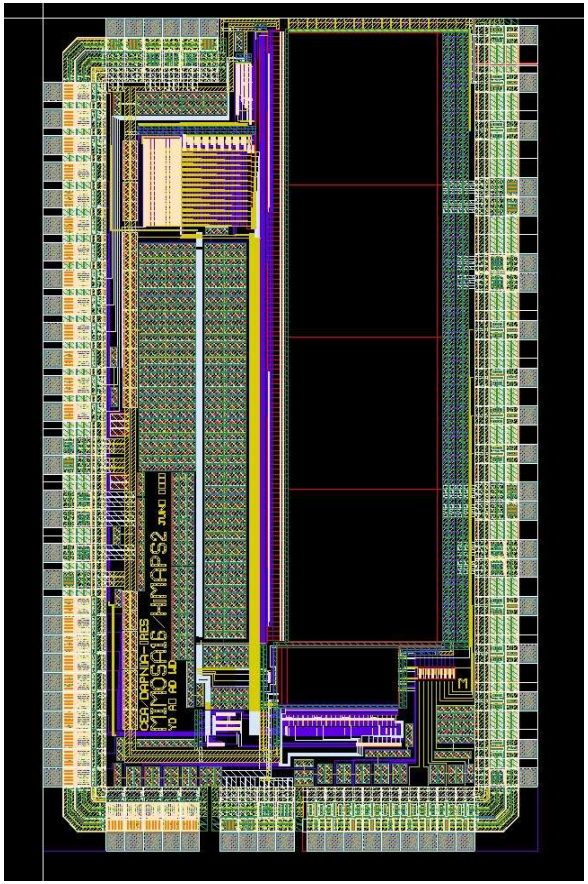
⇒ **Discussion needed to refine sensor requirements**

Status of the Development

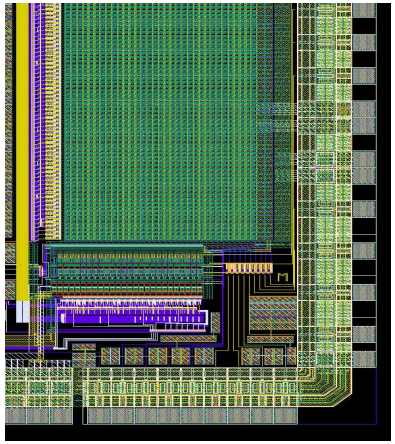
Fast Column Parallel Architecture

MIMOSA-16 design features :

- Fab. via STAR engin. run (Summer '06)
- AMS-0.35 OPTO translation of MIMOSA-8
  - $\hookrightarrow \sim$ 11–16 μm epitaxy instead of $\lesssim$ 7 μm
- 32 // columns of 128 pixels (pitch: 25 μm)
- on-pixel CDS (repeated at end of each column)
- discriminator at end of each column
- 4 sub-arrays :
  - ※ 2 like MIMO-8: 1.7x1.7 & 2.4x2.4μm^2 diodes
  - ※ 1 with ionising radiation tol. pixels
  - ※ 1 with enhanced in-pixel amplification (against noise of r.o. chain) & 4.5x4.5 μm^2 diode



$\Rightarrow$



24 col. with discri.

Status and Plans :

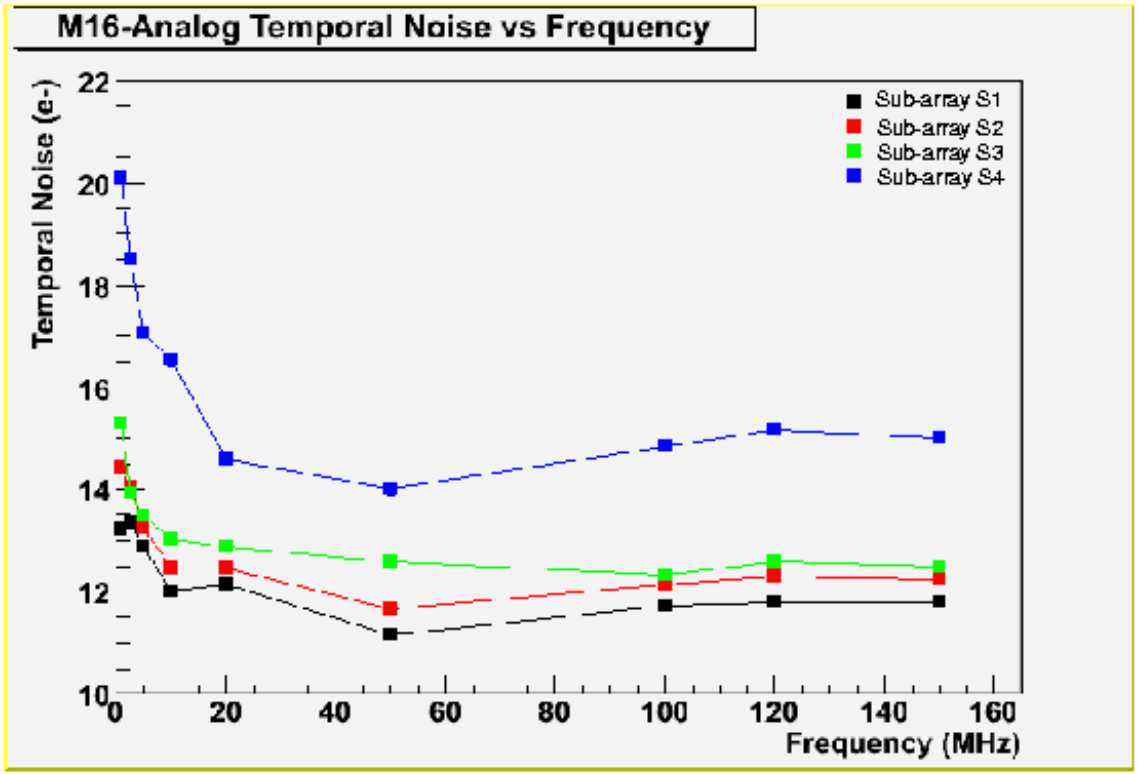
- back from foundry $<$ end Oct. '06 $\longmapsto$ lab tests $\gtrsim$ Nov. '06 (DAPNIA) $\longmapsto$ beam tests $\gtrsim$ Summer 2007
- next generations :
  - ※ small prototype (48+16 col. ? of 256 pixels, $\gtrsim$ 16 μm pitch, optimised pixels)
  - ※ small prototypes with ADCs replacing or downstream of discriminators

MIMOSA-16 Lab Test Results (Analog Part)

Temporal noise vs Frequency

Chip#0 (old mezzanine board)

Columns 28-31



08/01/07 Résumé résultats Mimosa-16 chip#0 2

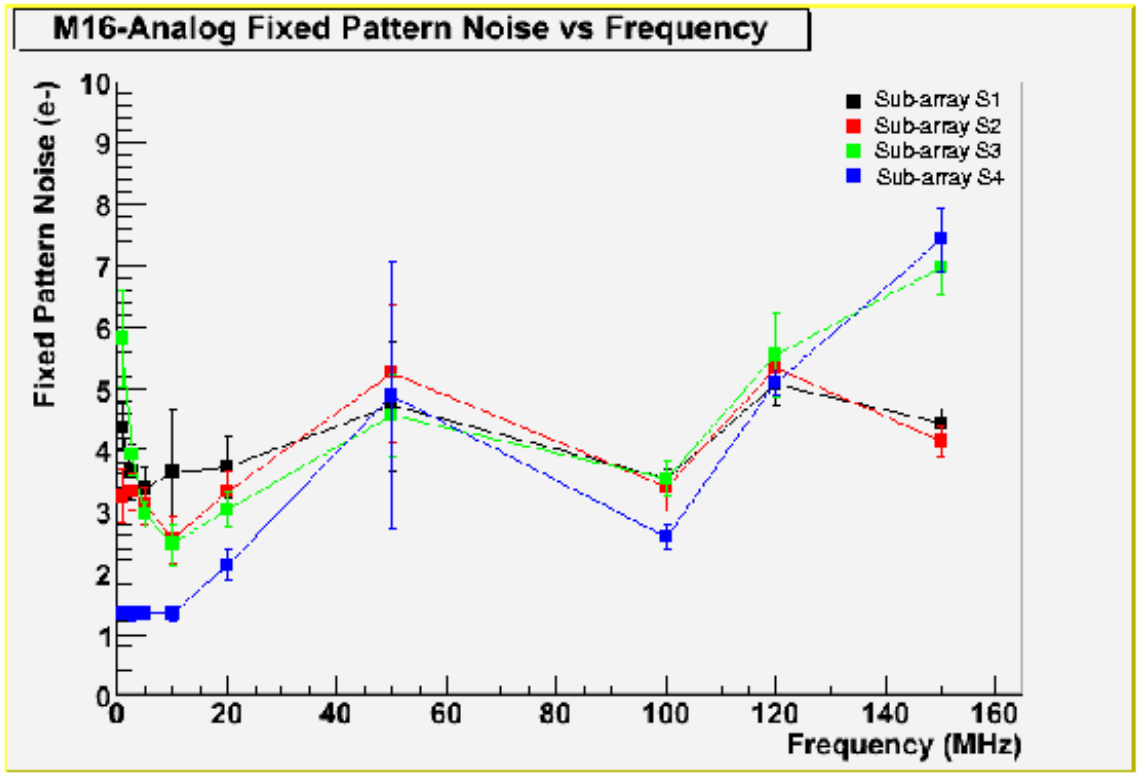
⇒ **Results compatible with MIMOSA-8 and -15 performances**

MIMOSA-16 Lab Test Results (Analog Part)

FPN (dispersion of pedestal) vs Frequency

Chip#0 (old mezzanine board)

Columns 28-31



08/01/07 Résumé résultats Mimosa-16 chip#0 1

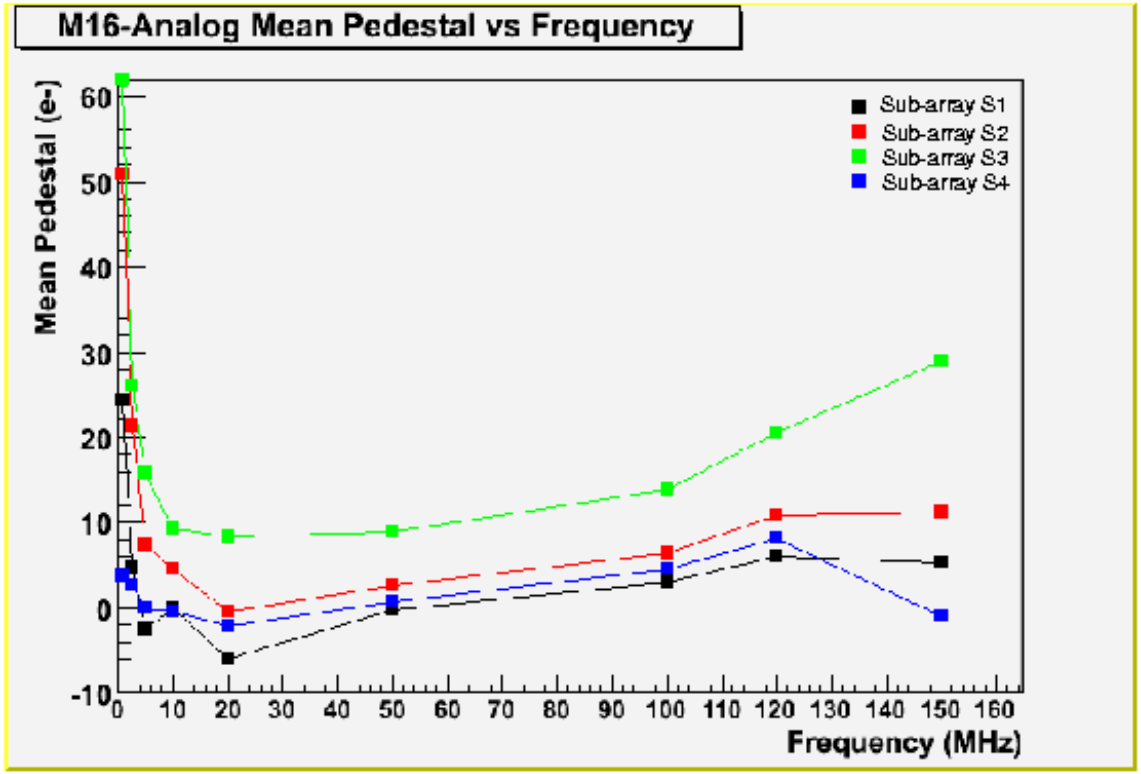
$\Rightarrow$ **FPN $<<$ pixel noise (as wanted)**

MIMOSA-16 Lab Test Results (Analog Part)

Pedestal Mean vs Frequency

Chip#0 (old mezzanine board)

Columns 28-31



08/01/07 Résumé résultats Mimosa-16 chip#0 3

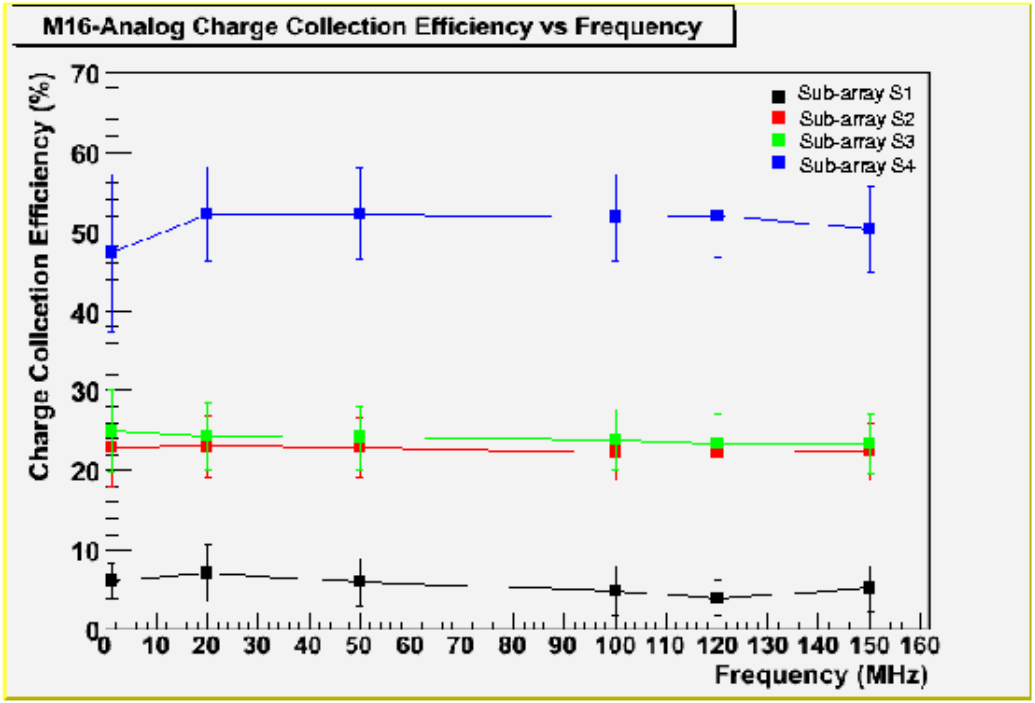
⇒ **No feature observed**

MIMOSA-16 Lab Test Results (Analog Part)

Charge Collection Efficiency vs Frequency

Chip#0 (old mezzanine board)

Columns 28-31



⇛ **Poor charge coll. efficiency for S1 (1.7x1.7 μm^2) and S2/S3 (2.4x2.4 μm^2)**

↪ **already observed with MIMOSA-15 (suspected origin in diffusion of P-well reducing the contact surface between N-well and epitaxy) ⟼ seems confirmed by S4 (4.5x4.5 μm^2 diode)**

- Several different ADC architectures under development at IN2P3 and DAPNIA (most for ILC)
  - LPSC (Grenoble): Ampli + semi-flash (pipe-line) 5- and 4-bit ADC for a column pair
  - LPCC (Clermont) : flash 4+1.5-bit ADC for a column pair
  - DAPNIA (Saclay) : Ampli + SAR (4- and) 5-bit ADC
  - IPHC (Strasbourg) : SAR 4-bit and Wilkinson 4-bit ADCs

Lab	proto.	phase	bits	chan.	$F_{r.o.}$(MHz)	dim. (μm^2)	P_{diss}	eff. bits	Problems
LPSC	ADC1	tested	5	8	15-25	43x1500	1700 μW	4	Offset & N
	ADC2	fab	4	8	25	40x943	800 μW		
	ADC3	design	4	> 8	25				
LPCC	ADC1	tested	5.5	1	5(T)–10(S)	230x400	20 000 μW	2.5	P_{diss} & bits
	ADC2	fab	5.5	1	10	40x1100	1000 μW		
DAPNIA	ADC1	tested	5	4	4	25x1000	300 μW	$\gtrsim 2$	Missing bits
	ADC2	fab	5	4	4	25x1000	300 μW		
IPHC	ADC1	fab	4	16	10	25x1385	660 μW		
	ADC2	fab	4	16	10	25x1540	545 μW		

$\Rightarrow$ 1st mature ADC design expected to come out in 2007

$\Rightarrow$ Submission of 1st col. // pixel array proto equipped with ADCs & $\varnothing \gtrsim$ end 2007

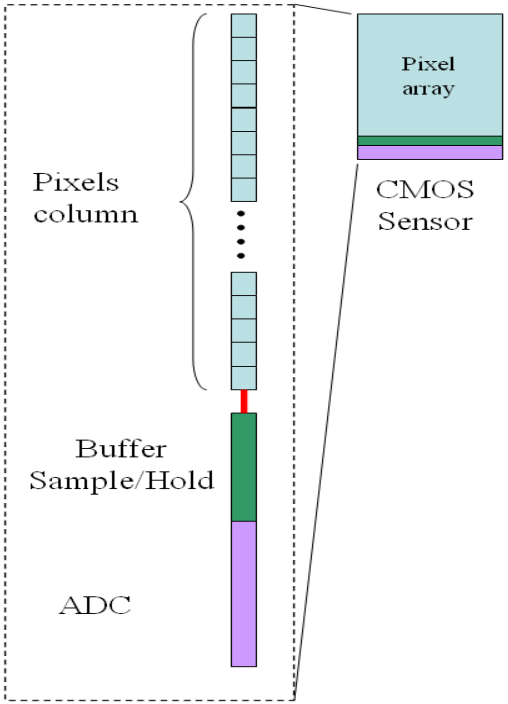
- **Study started end ’06 (triggered by STAR HFT) $\mapsto$ design started :**
  - **∅ logic restricted to one line at once (no clustering)**
  - **∅ micro-circuit identify discriminated pixels inside a line and give it an address**
  - **logic applied to subgroups of 64 (?) columns for data flow optimisation**

- **Plans :**
  - **1st prototype submission $\lesssim$ end April 2007**
  - **final prototype $\lesssim$ Summer 2008**

Prospect on Development of Final Sensors

Baseline Architecture with Integrated ADCs

- **Geometry :**
  - 1024 columns of 512 pixels
  - 20 μm pitch ($\longmapsto \sigma_{sp} < 2.5\ \mu m$)
  - Sensitive area = 20.48 x 10.24 mm^2



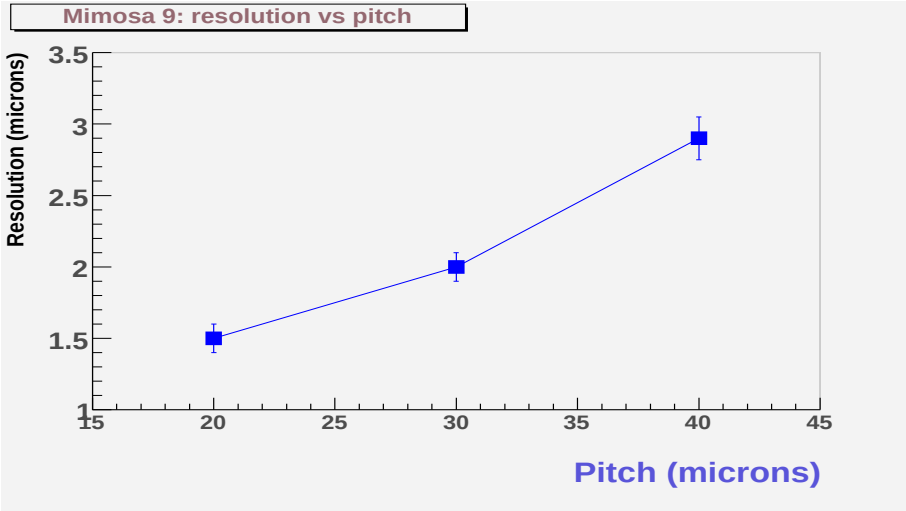
- **Functionnalities :**
  - pixels with integrated CDS (possibly repeated at end of column)
  - sensor with integrated 4-/5-bit ADC
    - ▷ ADC possibly preceded by discri. $\longmapsto$ 1 ADC for $\leq$ 64 col.
  - $\emptyset$ micro-circuit integrated inbetween (?) ADCs

- **Read-out speed (adapted to DESY beam) :**
  - default $\mathbf{t_{r.o.}}$ = 512 lines / 5 MHz $\sim$ 100 μs
  - flexible clock frequency : e.g. 1 – 10 MHz $\longmapsto$ $\mathbf{t_{r.o.}} \sim$ 500 – 50 μs

Spatial Resolution

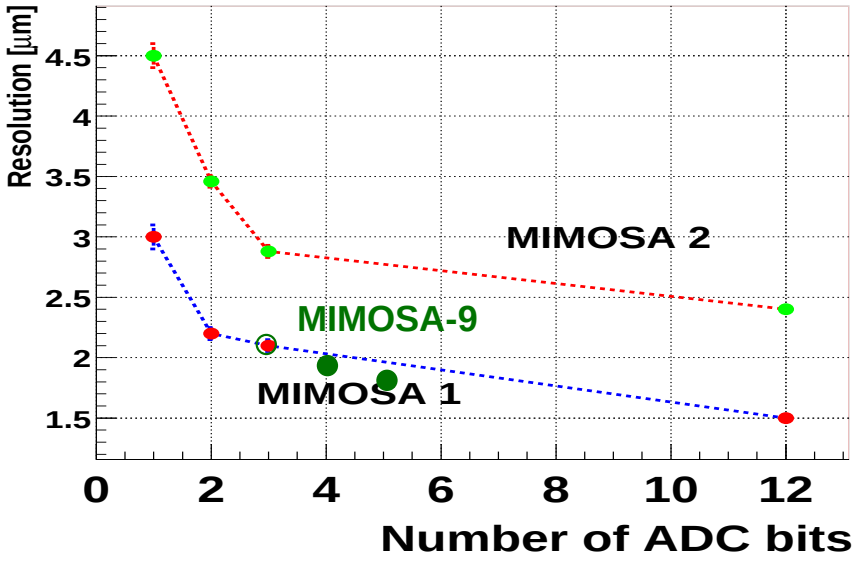
Single point resolution versus pixel pitch:

- clusters reconstructed with eta-function, exploiting charge sharing between pixels
- $\sigma_{sp} \sim 1.5\ \mu m$ (20 μm pitch)
  $\longmapsto \sigma_{sp} \lesssim 2\ \mu m$ (30 μm pitch)
- obtained with signal charge encoded on 12 bits



σ_{sp} dependence on ADC granularity:

- minimise number of ADC bits
  $\longmapsto$ minimise dimensions, $t_{r.o.}$ & P_{diss}
- effect simulated on real MIMOSA data
  (20 μm pitch ; 120 GeV/c π^- beam)

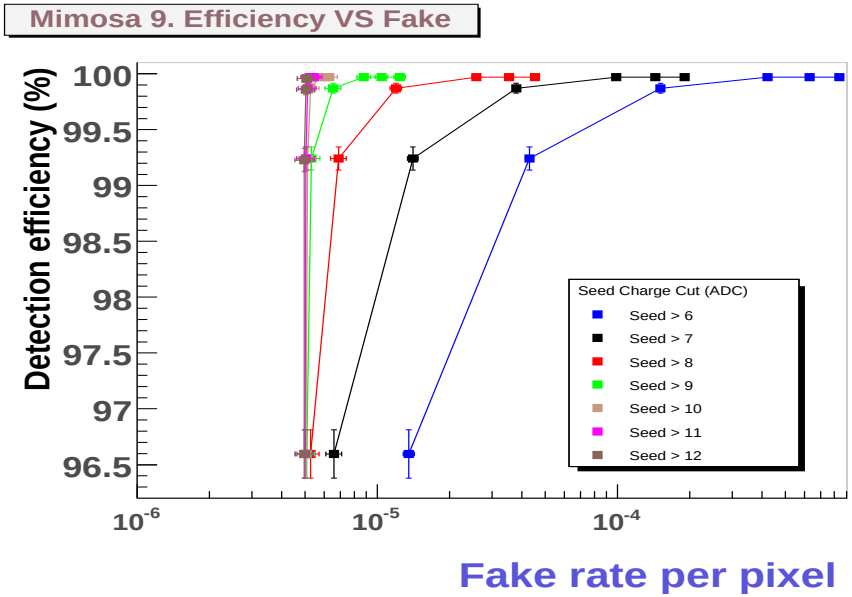


▷▷ $\sigma_{sp} < 2\ \mu m$ (4 bits) $\longmapsto$ 1.7–1.6 μm (5 bits)
(MIMOSA-9 : 20 μm pitch; T= + 20 °C)

- Warning : results based on simple pixel (N $\lesssim$ 10 e^- ENC)
  $\Rightarrow$ rad. tol. pixel integrating CDS (N $\lesssim$ 15 e^- ENC) not yet evaluated

- Expected Data Rate per Sensor

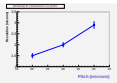
- **Baseline assumptions :**
  - sensor made of 1024 col. of 512 pixels $\longmapsto \sim 5{\cdot}10^5$ pixels / frame
  - $t_{r.o.}$ = 100 μs $\longmapsto$ 10 kfps (can be twice more or twice less)
  - $\lesssim$ 5 hits / frame
  - noisy pixel rate $>$ threshold $\lesssim 10^{-4}$ $\longmapsto$
  - pixel data size = 2 Bytes
    (10 bits of address & 5 bits for charge)



- **Data rate from pixel noise :**
  - 50 pixels / frame $\longmapsto$ 1 MB/s

- **Data rate from beam particle hits :**
  - 5 hits of 9 pixels / frame $\longmapsto$ 1 MB/s

$\Rightarrow$ **Total $<$ 1 kB/frame $\longmapsto$ few MB/s only**

  -

Simplified Architecture with Binary Output

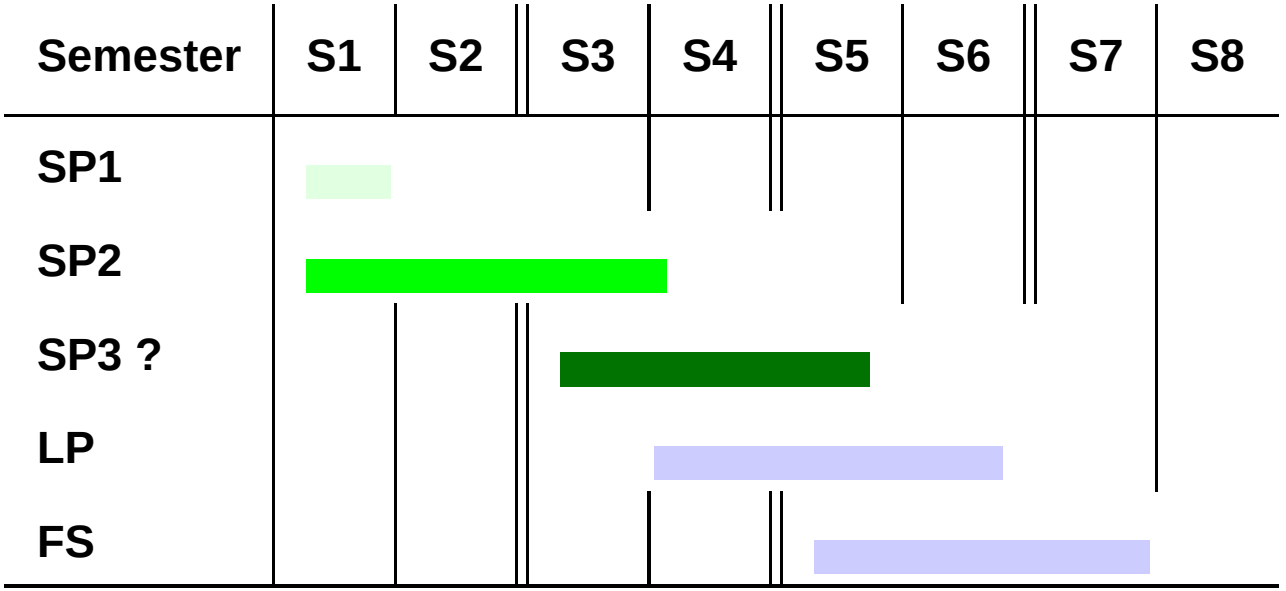
- **Geometry :**
  - 1280 columns of 640 pixels
  - 16 μm pitch ($\longrightarrow$ $\sigma_{sp} < 5\ \mu m$)
    - $\hookrightarrow$ MIMOSA-8 tests at CERN-SPS (Aug. '06) $\rightarrowtail \sigma_{sp} \sim$ 7 – 8 μm (25 μm pitch : 7.2 μm)
  - Sensitive area = 20.48 x 10.24 mm^2

- **Functionnalities :**
  - pixels with integrated CDS (possibly repeated at end of column)
  - column ended with integrated discriminator $\rightarrowtail$ binary encoding of charge
  - $\emptyset$ micro-circuit integrated downstream of discriminators

- **Read-out speed (adapted to DESY beams):**
  - default $\mathbf{t_{r.o.}}$ = 640 lines / 6.4 MHz = 100 μs
  - flexible clock frequency : e.g. 1 – 10 MHz $\rightarrowtail \mathbf{t_{r.o.}}$ = 640 – 64 μs

$\Rrightarrow$ **Less development needed to finalise sensor than with integ. ADC $\Rrightarrow$ available earlier**

Tentative Schedule of Sensor Delivery



- **Sensor production based on 5 steps (perhaps only 4, i.e. SP3 included in LP) :**
  - **MIMOSA-8 $\equiv$ SP-1 : 25 μm pitch, epi $<$ 7 μm**
  - **MIMOSA-16 $\equiv$ SP-2 : 25 μm pitch, epi $\sim$ 11 or 16 μm, rad. tol., enhanced ampli.**
  - **M16+ $\equiv$ SP-3 : like SP-2 but 16–18 μm pitch, optimised pixels, 48+16 col. of 256/320 pix. ?**
  - **M16++ $\equiv$ LP : like SP-3 but 320 col. of 256/320 pixels and integ. $\emptyset$**
  - **M16+++ $\equiv$ FS : like LP but 1280 col. of 640 pixels**

- **Which single point resolution over which area ?**
  - **Arms : $< 2.5\ \mu m$ or $< 5\ \mu m$ over 2 x 1 cm^2 ?**
  - **DUT surface : $\sim 1\ \mu m$ over 5 x 5 mm^2 ?**
- **Is t$_{r.o.}$ $\sim 100\ \mu s$ all right ? with how much flexibility ?**
- **When should the (final) sensors be delivered ?**
- **How do we organise ourselves w.r.t. sensor characterisation ?**

Development of final sensors for BT arm is progressing :

- Column // archi. : M16 analog part tested at DAPNIA (thick epi., no HRES)
  $\longmapsto$ results $\sim$ OK but poor charge coll. eff. with M8-like diode $\Rrightarrow$ enlarge sensing diode
- Compact & fast ADCs : in good progress $\longmapsto$ 1st mature concept/design expected $\sim$ end '07
- $\emptyset$ micro-circuits design starting

Need to agree on :

- σ_{sp}
- Frame r.o. speed
- Delivery date

$\Rrightarrow$ In particular : integrated ADC ($\sigma_{sp} < 2.5\ \mu m$) vs integrated discri. alone ($\sigma_{sp} < 5\ \mu m$)