UNIVERSITÄT
HEIDELBERG
ZUKUNFT
SEIT 1386

ALICE

Super-ALPIDE: Development of Electromechanical Integration Demonstrators for the ALICE ITS3

Alperen YÜNCÜ

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BMBF Forschungsschwerpunkt
ErUM-FSP T01
ALICE

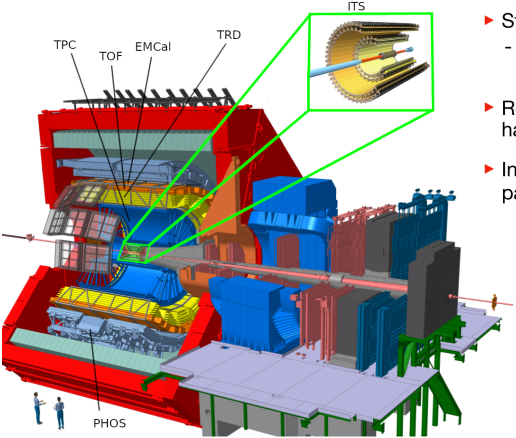
HighRR

HIGH-D

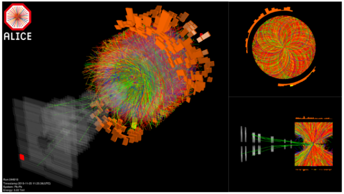
FSP ALICE
Erforschung von
Universum und Materie

ALICE

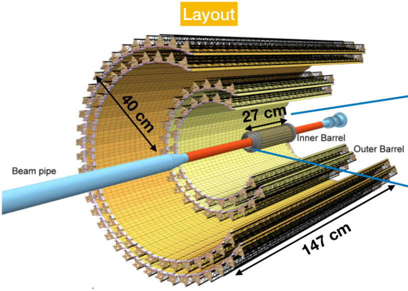
Detector and main goals

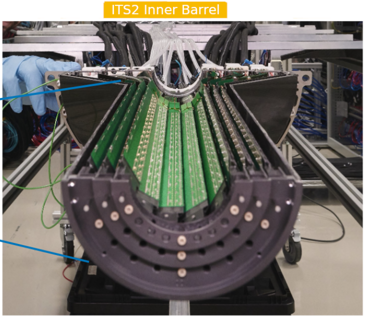


- Study of QGP in heavy-ion collisions at LHC
  - i.e. up to O(10k) particles to be tracked in a single event
- Reconstruction of charm and beauty hadrons
- Interest in low momentum (≲1 GeV/c) particle reconstruction



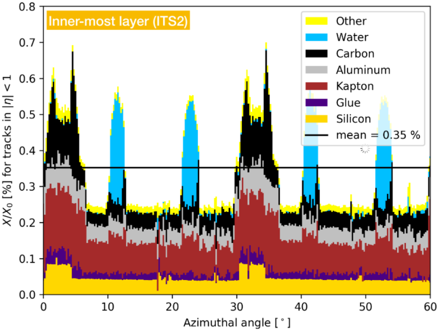
Current Inner Tracking System (ITS2)





- ITS2 is expected to perform according to specifications or even better
- The inner barrel is ultra-light ($0.35\%\,X_0$ per layer) but still most of the material comes from supports $\Longrightarrow$ further improvements seem possible
- Key questions:
  - Can we get closer to the interaction point?
  - Can we reduce the meterial budget even further?

Motivation for ITS3



- Observations:
  - $0.35\,\%$ X_0 per layer
  - Si makes only 1/7th of total material
  - Irregularities due to support/cooling

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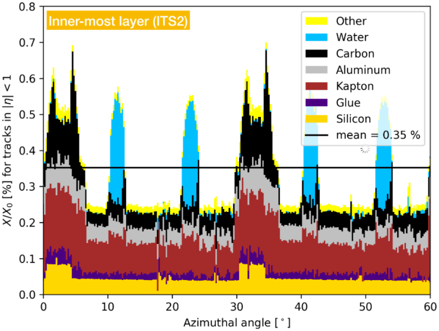

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  - Possible if power consumption stays below 20 mW/cm^2
  - Air cooling

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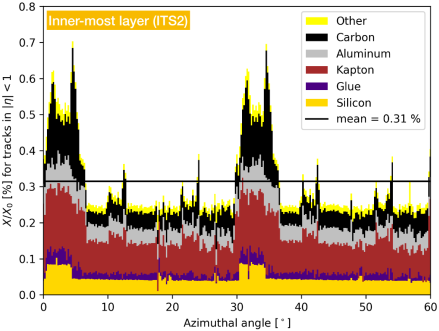

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  - $0.31\,\%$ X_0 per layer

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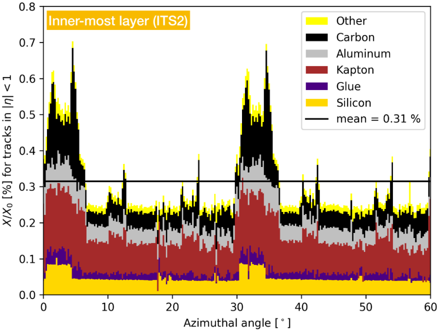

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  - Possible if integrated on chip

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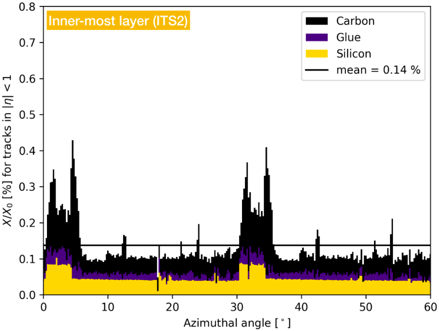

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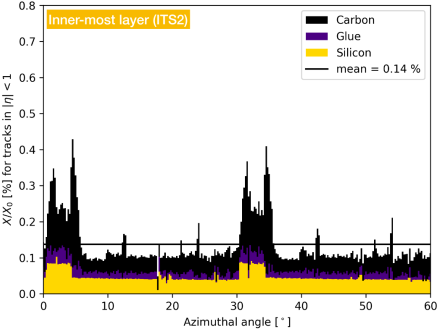
  - $0.14\ \%$ X_0 per layer

Motivation for ITS3



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- Removal of the circuit boards (power+data)
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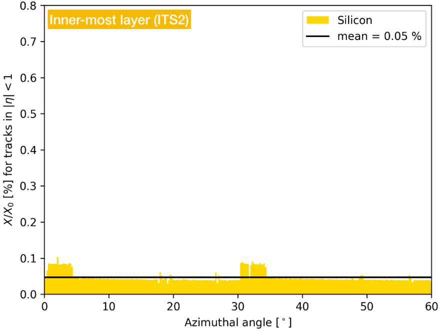
- Removal of mechanical support
  - Benefit from increased stiffness by bending Si wafers into cylinderical shape

Motivation for ITS3



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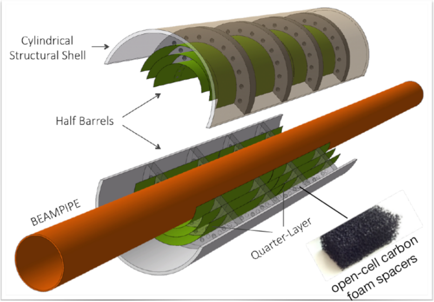
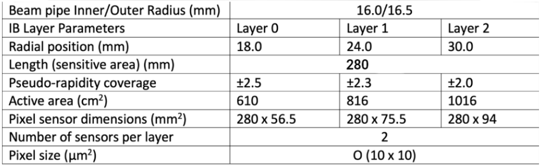
  - $0.14\,\%$ X_0 per layer
- Removal of mechanical support
  - Benefit from increased stiffness by bending Si wafers into cylinderical shape
  - $0.05\,\%$ X_0 per layer

ITS3 detector concept



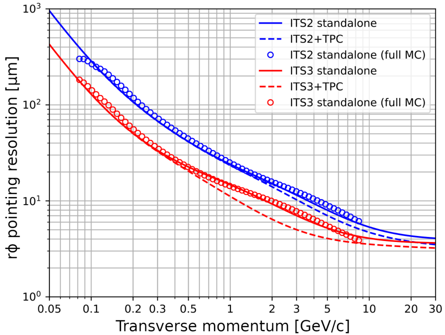


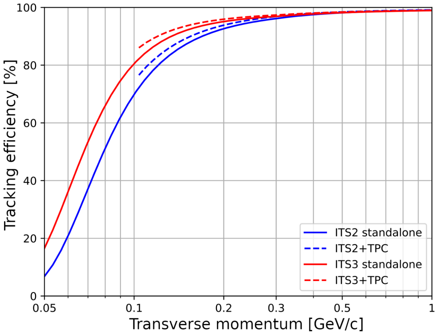
Beam pipe Inner/Outer Radius (mm)	16.0/16.5		
IB Layer Parameters	Layer 0	Layer 1	Layer 2
Radial position (mm)	18.0	24.0	30.0
Length (sensitive area) (mm)	280		
Pseudo-rapidity coverage	±2.5	±2.3	±2.0
Active area (cm²)	610	816	1016
Pixel sensor dimensions (mm²)	280 x 56.5	280 x 75.5	280 x 94
Number of sensors per layer	2		
Pixel size (µm²)	O (10 x 10)		

- Key ingredients:
  - 280 mm wafer-scale sensors, fabricated using stitching (Tower Partners Semiconductor (TPSCo) 65 nm CMOS Imaging Sensor (CIS) process)
  - Thinned down to 20-40 μm (0.02-0.04% X_0), making them flexible
  - Bent to the target radii
  - Mechanically held in place by carbon foam ribs
- Key benefits:
  - Extremely low material budget: 0.02-0.04% X_0 (beampipe: 500 μm Be: 0.14% X0)
  - Homogeneous material distribution: negligible systematic error from material distribution

THE WHOLE DETECTOR WILL COMPRISE SIX (!) SENSORS (CURRENT ITS IB: 432) AND BARELY ANYTHING ELSE

ITS3 performance

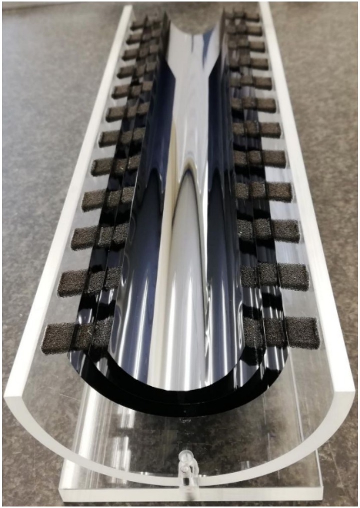




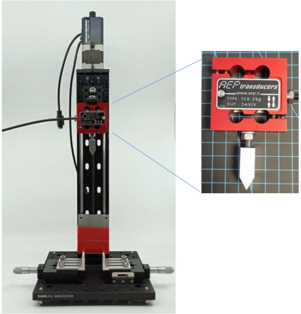
- Improvement on pointing resolution is factor of 2 over all momenta.
- Large improvement on tracking efficiency especially for low momenta.

Challenges

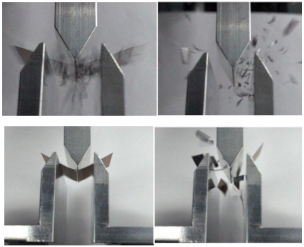
- Questions:
  - Can silicon be bent without breaking?
  - Are ASICs still functional in bent chip?
  - Can wafer-scale, thinned sensors be integrated without additional support structure?
  - Can 280 mm long silicon sensor be produced?



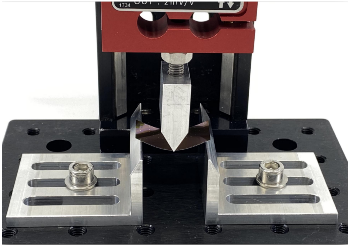
Bending Test

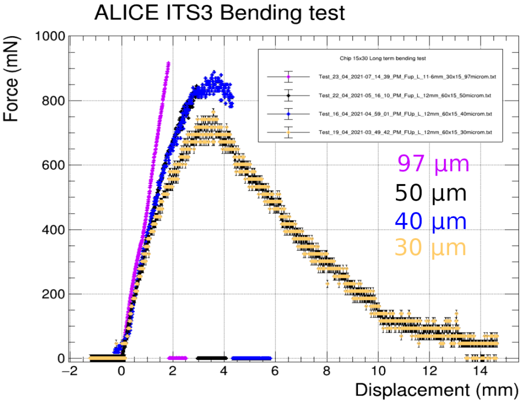


- Bending modulus
- Elastic - plastic region
- Breaking point
- Minimum radius



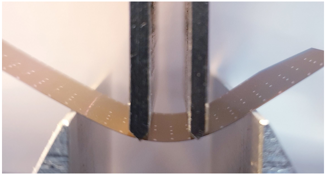
Bending Test (3-point test)

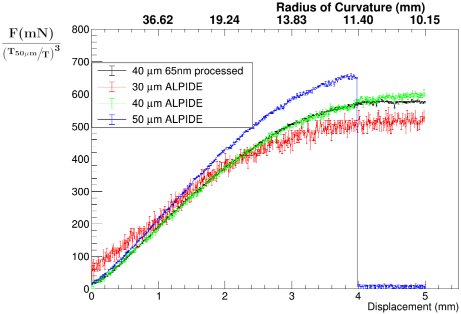




Bending Test (4-point test)

- Monolithic Active Pixel Sensors are quite flexible
  - already at thicknesses that are used for current detectors
- Bending force scales as $(\text{thickness})^{-3}$
  - large benefit from thinner sensors
- Breakage at smaller radii for thinner chips
  - again benefit from thinner sensors





ITS3 TARGET RADIUS AND THICKNESS ARE VERY FEASIBLE

bent ALPIDE

doi.org/10.1016/j.nima.2021.166280

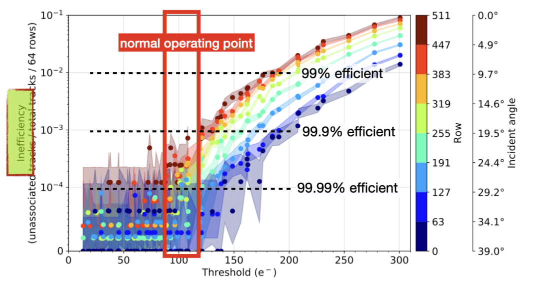
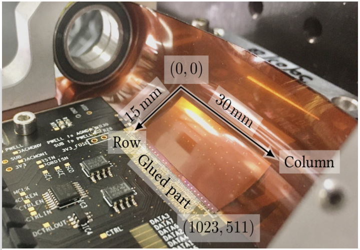
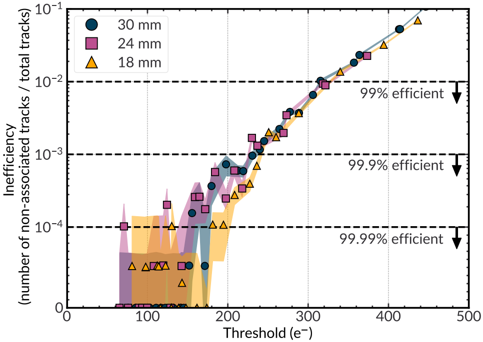


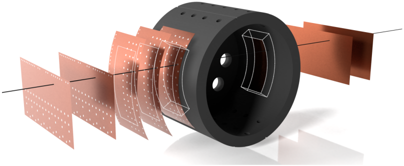
Fig. 10: Inefficiency as a function of threshold for different rows and incident angles with partially logarithmic scale (10^{-1} to 10^{-5}) to show fully efficient rows. Each data point corresponds to at least 8k tracks.

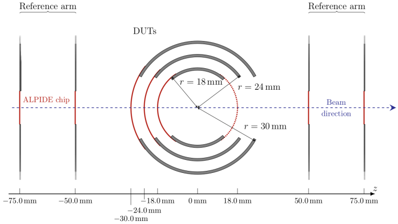


- Bent ALPIDE has high efficiency
- ASICs are functional in bent ALPIDE

bent ALPIDE

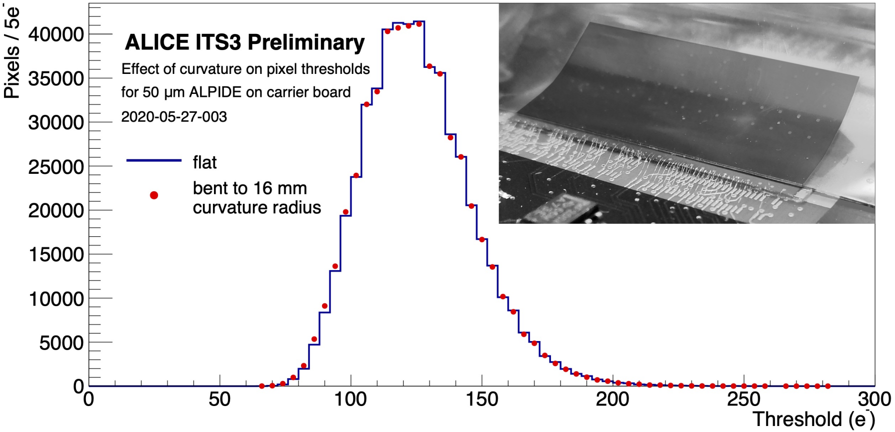




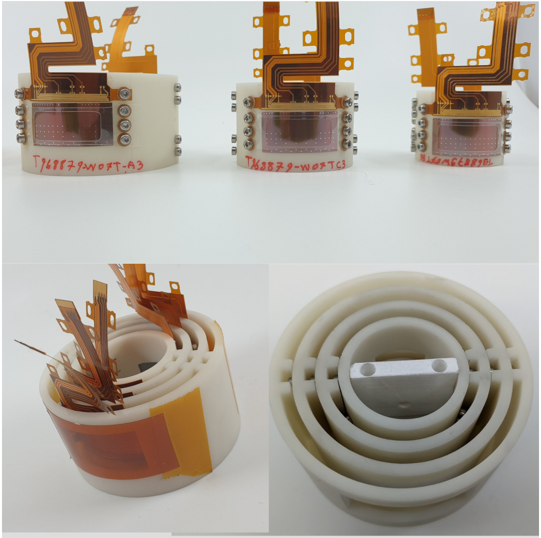


- Still has high efficiency on target radii

Chip bending performance



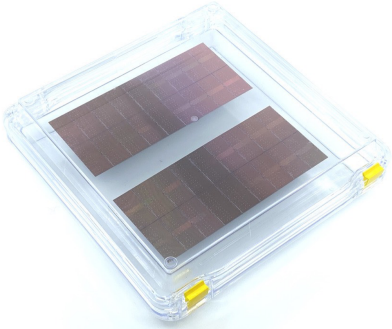
μITS3

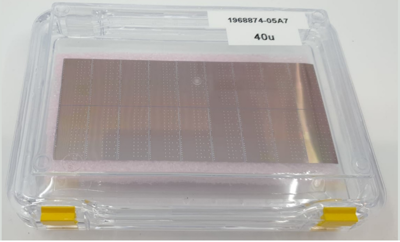


- μITS3 a mock-up of final ITS3
  - 6 ALPIDE bent to ITS3 target radii
  - Experience with handling thin, bent silicon was gained
- Also used with Cu target in the center, expect to see 120 GeV p-Cu collisions
- Analysis of μITS3 is in progress.

μITS Preperation Setup

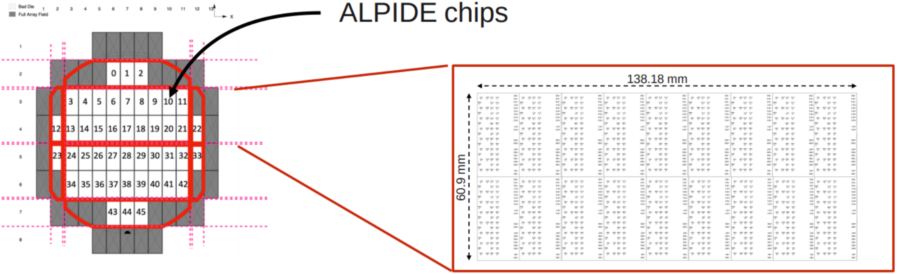
Super ALPIDE



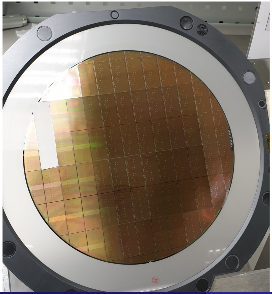


- To study the bending and interconnection of large pieces of processed chips, ”super-ALPIDE” is built.
- Comprises of **1 silicon piece cut** from an ALPIDE wafer size of $14\,\mathrm{cm} \times 6\,\mathrm{cm}$

Super ALPIDE

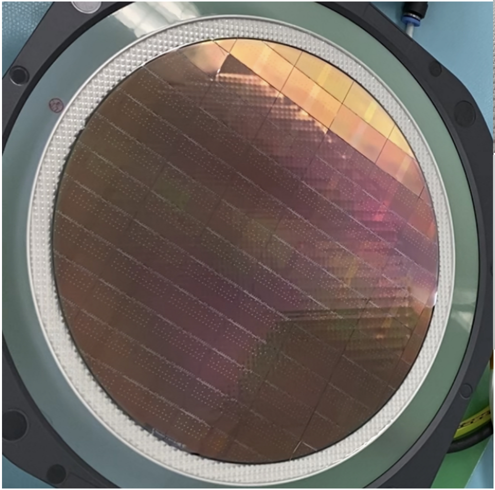


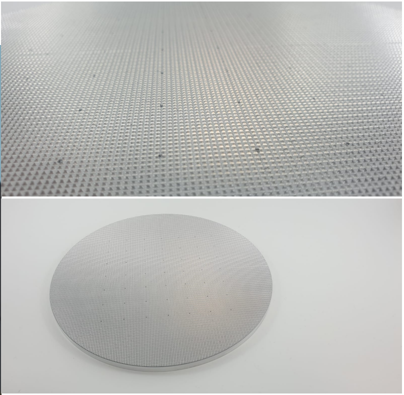
18 ALPIDE chips, covering about a half of an ITS3 half-Layer0



- Super-ALPIDEs are actually an array of ALPIDES.
- They consist 9×2 ALPIDE chips.

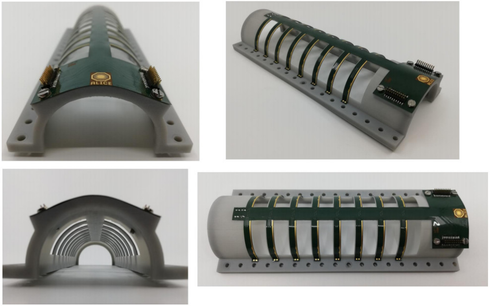
Picking up Super ALPIDE Chips





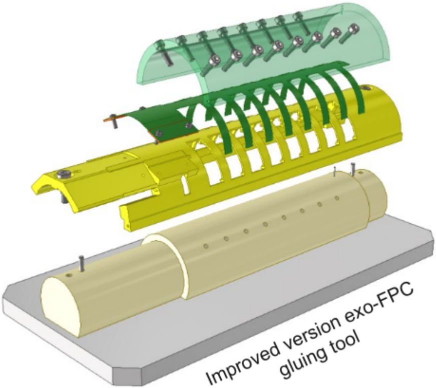
- Tested different methods how to pick large and very thinned chips
- Die-ejector with fine grid is quite efficient.

Exoskeleton

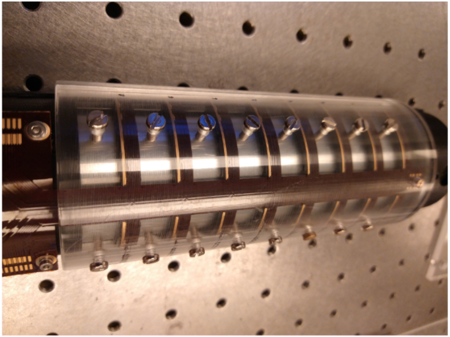


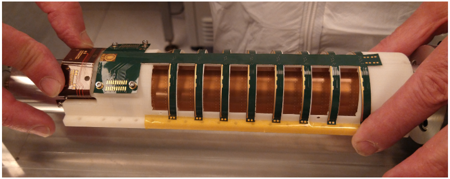
- 3-D printed.
- Designed to support super-ALPIDEs after bending.
- Windows to reach interconnection points at middle of super-ALPIDE
- FPC glued for connections

Gluing FPC

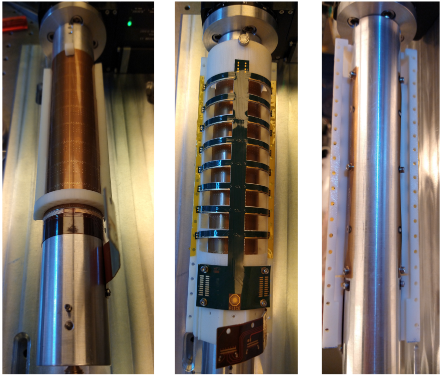


Improved version exo-FPC gluing tool

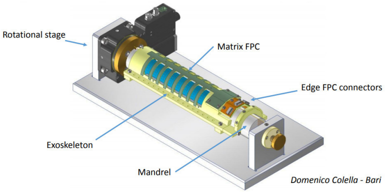




Bending Super ALPIDEs



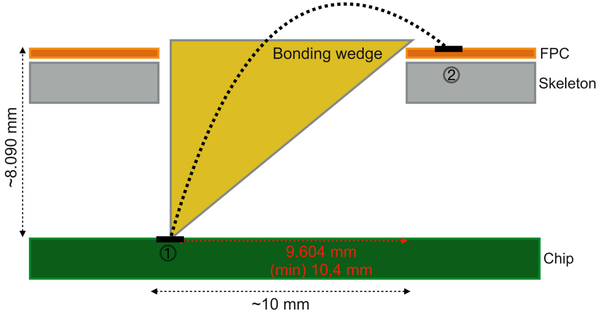
Super-ALPIDE wire-bonding setup

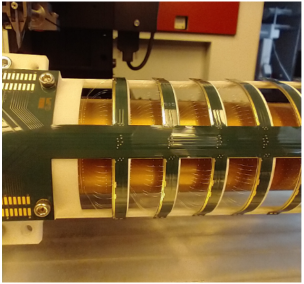


Domenico Colella - Bari

- Super ALPIDE is being rolled on mandrel
- Longerons are placed gently
- Exoskeleton is placed on top of the Super APIDE
- prepare for bonding

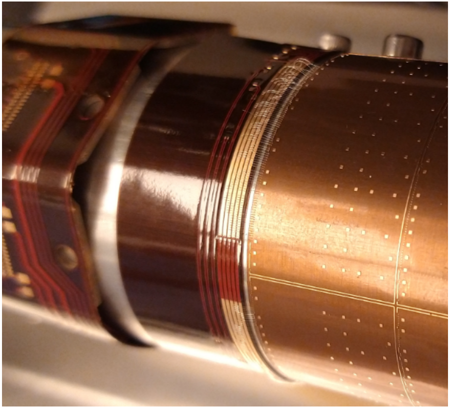
Bonding





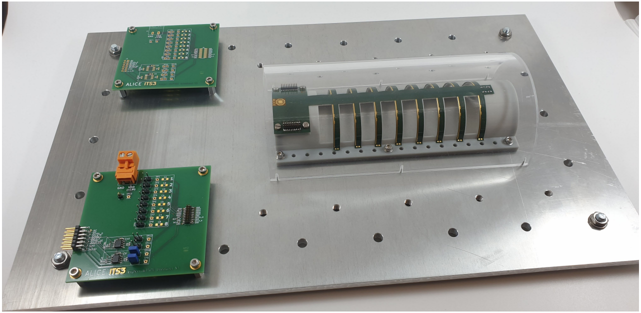
- The most of the ALPIDEs will be bonded to FPC on Exoskeleton via long wires

Bonding



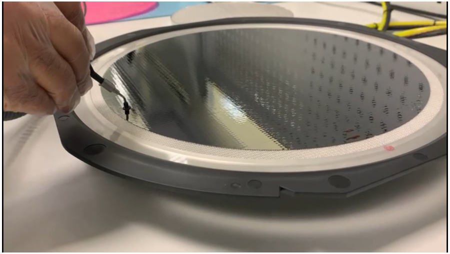
- The first row of ALPIDEs will be wire-bonded to an edge-FPC (just like final ITS3)
- The rest will be bonded to FPC on exoskeleton via long wires

Super ALPIDE Test Setup

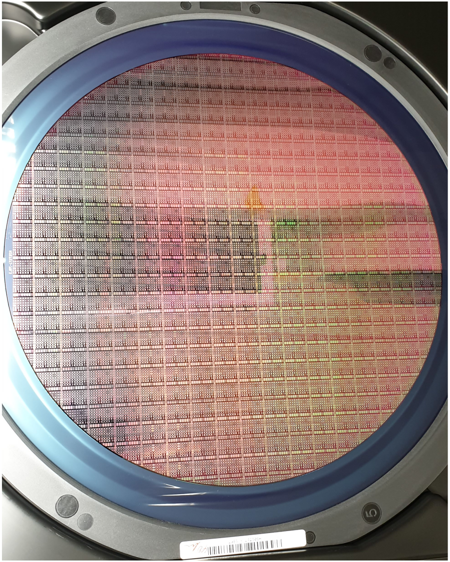


- Bonding and asembly of super ALPIDE is still ongoing at Bari.
- Meanwhile, Front-end readout circuitry is being built at CERN
- Test setup is ready.
- Tests of Super-ALPIDEs will start in November

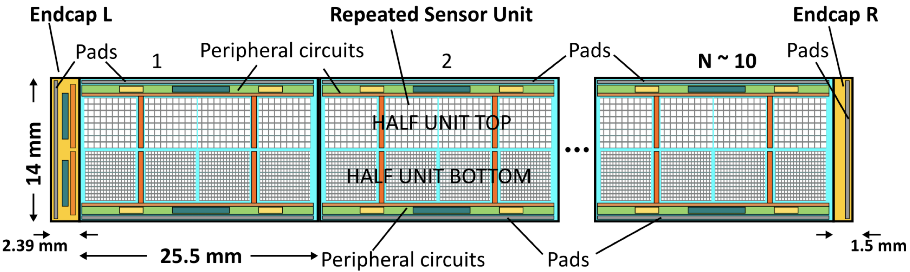
MLR1 Chips picking



- For **MLR1 chips on 12-inch wafers**, Die Ejector didn't help to remove chip
- After some number of methods failed we ask the prudoction company change the tape they use
- New blue tape is much **less adhesive** and MLR1 chips easily can be removed by die ejector.



Stiching



- Stitching used to connect metal traces for **power distribution** and **long range on-chip interconnect busses for control and data readout**
- Primary goals:
  - Learn stitching to make a charged-particle detector
  - Interconnect power and signals on wafer scale design
  - Learn about yield
  - Study power, leakage, spread, noise, speed

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Summary

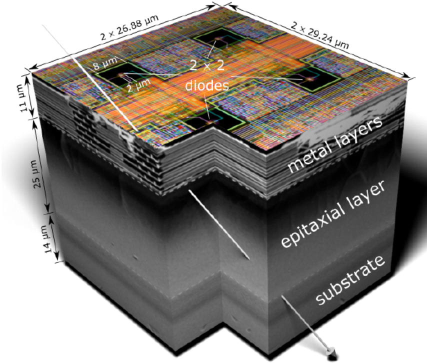
- Slicon is flexible enough to achieve targeted radii
- There is almost **no effeciency loss** at ASIC on bent chips
- Thanks to Super-ALPIDE study we have the know-how about how to deal with large and thin chips
- Almost ready for the production of the first prototypes of wafer-scale chips

THANK YOU

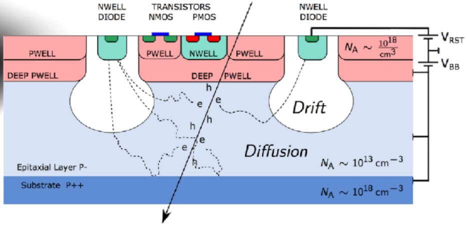
BACKUP

ALPIDE- ALice PIxel DEtector

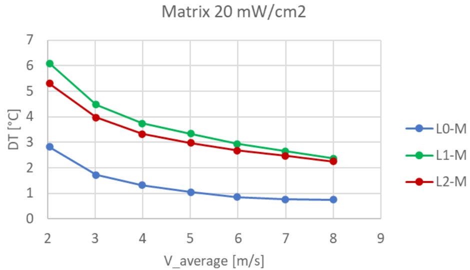
ALPIDE
Technology

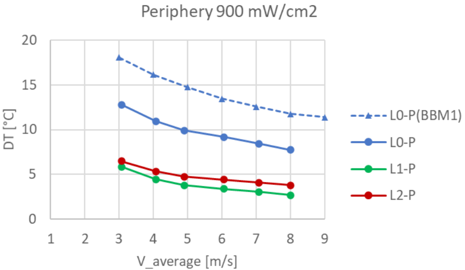


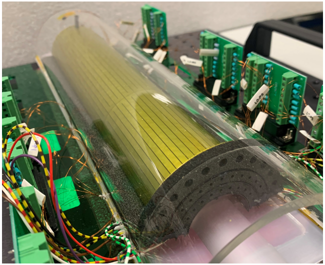
- **Process:** TowerJazz 180 nm CIS
  - deep p-well to allow CMOS circuitry inside matrix
  - reverse-substrate bias
- **Detection layer:** 25 µm high-resistive (>1kΩcm) epitaxial layer
- **Thickness:** 100 µm (OB) or 50 µm (IB)



Wind Tunnel Cooling Studies







- Different power & air speed
- Carbon foam radiator are key for heat removal at periphery
  - L1 and L2 DT $< 10^\circ$C
  - L0 has relatively larger temperature DT to air (further optimization on L0 Carbon foam layout)
  - Power density concentrated on 2.5 mm periphery