CMS BTL power distribution
proposal for LV, BV and TEC

07/03/2022
Agenda

1. Introduction – LVPS tender
2. Powering chain form LVPS to BTL tray
3. BTL power needs (LV, BV, TEC)
4. LVPS proposal
5. PP1 interconnections design
6. BTL supertray seal cabling
In August 2021 a tender for radiation tolerant LV power supplies for a few CMS subdetectors (including BTL) was finalized and a contract was placed.

At the very last moment, additional modules complaint with BV and TEC needs were added to the tender as variants, meaning ordering them is not required. This way we have received a quotation for development and production of these variants which turned to be exceptionally good offer (in our opinion).

BTL may place orders for development and production of BTL and BV modules at any moment.

If BTL follows this path, BV and TEC power modules would be placed in the LV power supply racks (towers next to the detector, 20 – 40 m away following cable path).
What do we need to power?

BTL tray is composed of:

- 6 x LV channel (60 W)
- 6 x BV channel (60/120 W)
- 6 x TEC channel (60 W)
- 12 x monitoring channels
- 1 x pre-heater channel (30 W) (NEW!)

We have assigned four cables of 13 mm OD to bring that power from PP1 to BTL tray.
BTL powering overview

LVPS
- LV module 12 x 60W
  - 12 V, 6 A
  - 8 x 6 mm², OD: 15 mm
  - 8 x 6 mm², OD: 15 mm
  - 8 x 6 mm², OD: 15 mm
- BV module 12 x 60W
  - 24 x 0.75 mm², OD: 12 mm
  - 24 x 0.75 mm², OD: 12 mm
- TEC module 12 x 60W
  - 24 x 0.75 mm², OD: 12 mm
  - 24 x 0.75 mm², OD: 12 mm
- Pre-heaters (BV module) 12 x 60W
  - 24 x 0.75 mm², OD: 12 mm
  - 48 x 0.22 mm², OD: 15 mm

Legend:
- D-SUB high current contacts 8W8
- D-SUB standard density 25 pins
- D-SUB standard density 50 pins

BTL tray 1
- CC 2
- CC 3
- CC 4
- CC 5
- CC 6

BTL tray 2
- CC 2
- CC 3
- CC 4
- CC 5
- CC 6

BTL tray 3

BTL tray 4

BTL tray 5

BTL tray 6
- CC 2
- CC 3
- CC 4
- CC 5
- CC 6
LVPS: LV power needs*

LV power consumption depends on the main consumer: TOFHIR.

- **34 W** - our best guess of today for a power consumption of a single RU with TOFHIR 2B (based on simulations)
- **50.4 W** - with contingency factor 1.4

<table>
<thead>
<tr>
<th></th>
<th>Power/ch [mW]</th>
<th>Power at PCCs [W]</th>
<th>FEAST 1.8 V current [A]</th>
<th>Power at LVPS</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOFHIR 2B</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(no contingency)</td>
<td>17.35</td>
<td>30.5</td>
<td>2.8</td>
<td>34 W</td>
</tr>
<tr>
<td>TOFHIR 2B</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(1.06 contingency)</td>
<td>18.6</td>
<td>32.5</td>
<td>3</td>
<td></td>
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<tr>
<td>TOFHIR 2B</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(1.27 contingency)</td>
<td>22.4</td>
<td>38.7</td>
<td>3.6</td>
<td></td>
</tr>
<tr>
<td>TOFHIR 2B</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(1.4 contingency)</td>
<td>24.8</td>
<td>42.7</td>
<td>4</td>
<td>50.4 W</td>
</tr>
</tbody>
</table>

* As of November 2020

60 W channel covers all scenarios.
LVPS: BV and TEC power needs

After assessment of power needs in December 2021, the following recommendations were published by us concerning BV and TEC power supply operating areas [1].

Modification of the TEC PS specs may be considered to enlarge operating area for anealing operation mode.

Present TEC PS specs:
- $V = 35 \text{ V}$
- $I = 2 \text{ A}$
- $P = 60 \text{ W}$

Potential change:
- $V = 42 \text{ V}$
- $I = 2 \text{ A}$
- $P = 60 \text{ W}$

Modification of the BVPS specs is recommended as present operating area is too large.

<table>
<thead>
<tr>
<th>Present BVPS specs</th>
<th>Suggested BVPS specs</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_B = 60 \text{ V}$</td>
<td>$V_B = 60 \text{ V}$</td>
</tr>
<tr>
<td>$I = 3 \text{ A}$</td>
<td>$I = 1.5 \text{ A}$</td>
</tr>
<tr>
<td>$P_B = 120 \text{ W}$</td>
<td>$P_B = 60 \text{ W}$</td>
</tr>
</tbody>
</table>

LVPS: modular design

- BTL modules may be mixed within one chassis. That opens a possibility to power entire BTL super-tray with a single chassis of power supply.
- 12 chassis will cover the needs of the entire BTL
- This approach would ease maintenance and interlocking – in case of power supply failure it is easy to implement interlock in a way that only a small fraction of the detector is disabled.

Single LVPS chassis may power 6 BTL trays (called super-tray)

Example modules distribution within a single chassis.
### LVPS: racks space for EB and BTL

<table>
<thead>
<tr>
<th>Parameters</th>
<th>EB+ X3 rack 1</th>
<th>EB+ X3 rack 2</th>
<th>EB+ X2 rack 1</th>
<th>EB+ X2 rack 2</th>
<th>EB- X3 rack 1</th>
<th>EB- X3 rack 2</th>
<th>EB- X2 rack 1</th>
<th>EB- X2 rack 2</th>
<th>X0 rack 1</th>
<th>X0 rack 2</th>
<th>X0 rack 3</th>
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</thead>
<tbody>
<tr>
<td>LVPS stage</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
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<td>0</td>
</tr>
<tr>
<td>BTL stage</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

#### EB LV power supplies

- EB+ X3
- EB+ X2
- EB- X3
- EB- X2

#### BTL power supplies

- X0
BTL powering overview

Legend:
- D-SUB high current contacts 8W8
- D-SUB standard density 25 pins
- D-SUB standard density 50 pins
PP1: 3D model [1]

[1] Credits to Axel Filenius and Tracker Integration team for sharing screenshots!
**PP1: number of cables reserved**

- Each PP1-half serves 2 BTL trays
- 4 cables / BTL tray reserved
- Constraints:
  - 1 PCB available, dimensions: 160.3 mm x 160 mm
  - Heights over a PCB available: 45 mm on the PS side; 30 mm on the detector side. This may be altered, a total of 80 mm available
  - Preference to have a connector on the detector side, no such a need on the other side
  - Minimum bending radius for cables on the detector side: 70 mm

---

**System** | **IN (PS side)** | **OUT (BTL side)**
--- | --- | ---
LV | 3 (8 x 6 mm2, 15 mm OD) | 2 (24 x 0.75 mm2)
BV | 3 (24 x 0.75 mm2, 13 mm OD) | 2 (24 x 0.75 mm2) [before: 3]
TEC | 3 (24 x 0.75 mm2, 13 mm OD) | 2 (24 x 0.75 mm2)
Monitoring | 1 (48 x 0.22 mm2, 15 mm OD) | 1 (48 x 0.22 mm2)
Pre-heaters | 1 (24 x 0.75 mm2, 13 mm OD) [before: 0] | 1 (24 x 0.75 mm2) [before: 0]
TOTALS | 11 cables | 8 cables

*Patch panel 1 PCB: space available. Credits: Axel Filenius.*
PP1: PCB design

- V1.1 designed in 2021. BTL LV, BV, TEC and monitoring included
- Pre-heaters not included.
- The PCB may be updated according to needs

Legend:
- Front PCB side
- Back PCB side
BTL powering overview

Legend:
- D-SUB high current contacts 8W8
- D-SUB standard density 25 pins
- D-SUB standard density 50 pins

LVPS
- 12 V, 6 A
- 8 x 6 mm², OD: 15 mm
- 8 x 6 mm², OD: 15 mm
- 8 x 6 mm², OD: 15 mm

LV module 12 x 60W
- 24 x 0.75 mm², OD: 12 mm
- 24 x 0.75 mm², OD: 12 mm
- 24 x 0.75 mm², OD: 12 mm
- 24 x 0.75 mm², OD: 12 mm

BV module 12 x 60W
- 24 x 0.75 mm², OD: 12 mm
- 24 x 0.75 mm², OD: 12 mm
- 24 x 0.75 mm², OD: 12 mm
- 24 x 0.75 mm², OD: 12 mm

TEC module 12 x 60W
- 24 x 0.75 mm², OD: 12 mm
- 24 x 0.75 mm², OD: 12 mm
- 24 x 0.75 mm², OD: 12 mm
- 24 x 0.75 mm², OD: 12 mm

Pre-heaters (BV module) 12 x 60W
- 48 x 0.22 mm², OD: 15 mm

BTL tray 1
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- CC 5
- CC 6

BTL tray 3

BTL tray 4

BTL tray 5

BTL tray 6

T. Gadek, W. Lustermann, K. Stachon | 07/03/2022 | 14
Supertray: BTL connectors

Connectors arrangement - before reduction of BV connections

Connectors arrangement - after reduction of BV connections

CMS BTL supertray seal overview. Credits: Axel Filenius.
Supertray: wiring diagram
Conclusions

- The presented concept assumes usage of radiation-tollerant power supplies
- To profit from current LVPS tender, actions must be taken:
  - Modification of specification of BV and TEC modules (variants)
  - Order of prototypes and, subsequently, production units. The earlier the manufacturer is notified about the order, the sooner prototypes will be delivered.
- We (ETH) wait for approval/disapproval of the concept and based on decision, PP1 PCB will be modified and produced.
Thank you for your attention

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  - Krzysztof.Stachon@cern.ch

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Institute for Particle Physics and Astrophysics
ipa.phys.ethz.ch
## BACKUP: BTL: Cooling capacity

*Table 2: 2PACL system planned for CMS, with details of the pump type and maximal power removal capacity*

<table>
<thead>
<tr>
<th>CMS</th>
<th>Heat per cooling unit</th>
<th>Cooling units</th>
<th>Plant type (Pump heads)</th>
<th>Max power/unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Outer Tracker (OT)</td>
<td>86</td>
<td>2</td>
<td>3</td>
<td>103</td>
</tr>
<tr>
<td>Inner Tracker (IT)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Barrel Timing Layer (BTL)</td>
<td>46</td>
<td>1</td>
<td>2</td>
<td>69</td>
</tr>
<tr>
<td>Calorimeter Endcap (CE) + z NEAR</td>
<td>62</td>
<td>1</td>
<td>2</td>
<td>87</td>
</tr>
<tr>
<td>Calorimeter Endcap (CE) + z FAR</td>
<td>62</td>
<td>1</td>
<td>2</td>
<td>87</td>
</tr>
<tr>
<td>Calorimeter Endcap (CE) - z NEAR</td>
<td>62</td>
<td>1</td>
<td>2</td>
<td>87</td>
</tr>
<tr>
<td>Calorimeter Endcap (CE) + z FAR</td>
<td>62</td>
<td>1</td>
<td>2</td>
<td>87</td>
</tr>
<tr>
<td>Endcap Timing Layer (ETL) +/ -z</td>
<td>85</td>
<td>1</td>
<td>3</td>
<td>103</td>
</tr>
<tr>
<td>Spare plant</td>
<td>1</td>
<td></td>
<td>3</td>
<td>103</td>
</tr>
</tbody>
</table>

Source: [https://edms.cern.ch/ui/file/2475066/1/LVUPS_Phase2_capacity_220228_docx_cpdf.pdf](https://edms.cern.ch/ui/file/2475066/1/LVUPS_Phase2_capacity_220228_docx_cpdf.pdf)

- $432 \times 120 \text{ W} + 432 \times 60\text{ W} = 77.7 \text{ kW}$
- $432 \times 60 \text{ W} + 432 \times 60\text{ W} = 51.8 \text{ kW}$
BACKUP: BV system – requirements summary

Number of SiPMs
- per readout unit: 768
- per SiPM array: 16

Number of SiPM arrays
- per readout unit: 48

SiPM bias voltage range
- Maximum bias voltage required: 43.96 V
- Minimum bias voltage required: 27.73 V

SiPM array:
- Maximum current required: 17 mA
- Maximum power required: 0.35 W

ALDO:
- Maximum voltage drop: 3.0 V

<table>
<thead>
<tr>
<th>SiPM array parameter</th>
<th>Requirement</th>
<th>Vendor 1</th>
<th>Vendor 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum BV required</td>
<td>43.96 V</td>
<td>43.96 V</td>
<td>38.76 V</td>
</tr>
<tr>
<td>Minimum BV required</td>
<td>27.73 V</td>
<td>32.55 V</td>
<td>27.73 V</td>
</tr>
<tr>
<td>Average operating BV</td>
<td>-</td>
<td>39.2 V</td>
<td>32.5 V</td>
</tr>
<tr>
<td>Maximum current</td>
<td>17 mA</td>
<td>12 mA</td>
<td>15 mA</td>
</tr>
<tr>
<td>Maximum total power SiPMs</td>
<td>0.35 W</td>
<td>0.35 W</td>
<td>0.35 W</td>
</tr>
<tr>
<td>Power for TECs (1 array)</td>
<td>0.58 W</td>
<td>0.58 W</td>
<td>0.58 W</td>
</tr>
<tr>
<td>Maximum total power per array</td>
<td>1.04 W</td>
<td>≤ 1.04 W</td>
<td>≤ 1.04 W</td>
</tr>
</tbody>
</table>

Table 1: SiPM array power requirements. [1]

Single BV channel (=768 SiPMs) requirements:
- Voltage range: 27.73 V – 43.96 V
- Maximum current required: 0.816 A
- Maximum power required: 16.8 W

Sources:
There are two limiting parameters that we consider:

**Scenario A:** max current requirement
\[ I = 48 \times 17 \text{ mA} = 0.816 \text{ A} \]

**Scenario W:** max power requirement
\[ P_S = 48 \times 0.35 \text{ W} = 16.8 \text{ W} \]

Additionally, we consider the following scenarios:

Bias voltage \( V_S \)
1) \( V_S = 27.73 \text{ V} \)
2) \( V_S = 43.96 \text{ V} \)

Cable resistance \( R_C \)
\( R_C = 1.234 \Omega \) (double wires power and return)
\( R_C = 2.468 \Omega \) (single wires power and return)
## BACKUP: BV system – solution

### Calculations:

<table>
<thead>
<tr>
<th>Scenario A (max current)</th>
<th>Present BVPS specs</th>
<th>Suggested BVPS specs</th>
</tr>
</thead>
<tbody>
<tr>
<td>current I</td>
<td>0,816</td>
<td>0,606</td>
</tr>
<tr>
<td>V_B</td>
<td>48,0</td>
<td>47,4</td>
</tr>
<tr>
<td>P_S</td>
<td>35,9</td>
<td>16,8</td>
</tr>
<tr>
<td>P_S per array</td>
<td>0,75</td>
<td>0,35</td>
</tr>
<tr>
<td>P_B</td>
<td>39,1</td>
<td>18,3</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Scenario W (max power)</th>
<th>Present BVPS specs</th>
<th>Suggested BVPS specs</th>
</tr>
</thead>
<tbody>
<tr>
<td>current I</td>
<td>0,382</td>
<td>0,606</td>
</tr>
<tr>
<td>V_B</td>
<td>47,4</td>
<td>47,9</td>
</tr>
<tr>
<td>P_S</td>
<td>16,8</td>
<td>16,8</td>
</tr>
<tr>
<td>P_S per array</td>
<td>0,35</td>
<td>0,35</td>
</tr>
<tr>
<td>P_B</td>
<td>18,1</td>
<td>19,1</td>
</tr>
</tbody>
</table>

Max BVCH needs (from calculations):
- \( V_B = 49.0 \text{ V} \)
- \( I = 0.816 \text{ A} \)
- \( P_B = 40 \text{ W} \)

Modification of the BVPS specs is recommended as present operating area is too large.

### Max BVCH needs (from calculations):
- \( V_B = 49.0 \text{ V} \)
- \( I = 0.816 \text{ A} \)
- \( P_B = 40 \text{ W} \)
BACKUP: TEC system – requirements summary

- Requested TEC module parameters:
  - $V_{PS_{\text{max}}}$ = 35 V
  - $I_{PS_{\text{max}}}$ = 2 A
  - $P_{PS_{\text{max}}}$ = 60 W

- Cables resistance for a single TEC channel:
  - $(40m \times (2 \times 0.75 \text{ mm}^2) + 7m \times 0.75 \text{ mm}^2)$
  - $R_{\text{cables}} = 1,403 \ \Omega$

- TEC array resistance range:
  - $R_{\text{TEC}\_\text{array}} = 13 \ \Omega @ T_{\text{hot}} = -35^\circ C$
  - $R_{\text{TEC}\_\text{array}} = 21.8 \ \Omega @ T_{\text{hot}} = 10^\circ C$
  - $R_{\text{TEC}\_\text{array}} = 24 \ \Omega @ T_{\text{hot}} = 25^\circ C$

**Power needs based on bench measurements***:

(*Arjan Heering email dated 06/12/2021)
- $P_{\text{TEC}\_\text{array}} = 700 \text{ mW}$ to achieve $\Delta T = -10^\circ C$ when $T_{\text{hot}} = -35^\circ C$ and $P_{\text{SiPM}\_\text{array}} = 420 \text{ mW}$
- $P_{\text{TEC}\_\text{array}} = -700 \text{ mW}$ to achieve $\Delta T = 25^\circ C$ when $T_{\text{hot}} = 25^\circ C$ and $P_{\text{SiPM}} = 0 \text{ mW}$ (turned off)
- $P_{\text{TEC}\_\text{array}} = -1008 \text{ mW}$ to achieve $\Delta T = 30^\circ C$ when $T_{\text{hot}} = 10^\circ C$ and $P_{\text{SiPM}} = 0 \text{ mW}$ (turned off)
BACKUP: TEC system – solution

Resistances calculations

<table>
<thead>
<tr>
<th>T_hot [°C]</th>
<th>R_TEC_array [Ω]</th>
<th>R_TEC_net [Ω]</th>
<th>R_total [Ω]</th>
</tr>
</thead>
<tbody>
<tr>
<td>-35</td>
<td>13</td>
<td>17,333</td>
<td>18,736</td>
</tr>
<tr>
<td>10</td>
<td>21.8</td>
<td>29,0667</td>
<td>30,46967</td>
</tr>
<tr>
<td>25</td>
<td>24</td>
<td>32</td>
<td>33,403</td>
</tr>
</tbody>
</table>

Conclusions:

Cooling operation:
- 700 mW / TEC_array easily achievable
- Sufficient margin: 1054 mW / TEC_array achievable

Heating operation:
- 700 mW / TEC_array achievable with present power supply requirements
- No margin for higher power needs.
- If there is a need for that, an increase of voltage limit of the power supply could be requested. Increase of voltage to 42 V results in 1053 mW / TEC_array.

Modification of the TEC PS specs may be considered to enlarge operating area for annealing operation mode.

**Present TEC PS specs:**
- V = 35 V
- I = 2 A
- P = 60 W

**Potential change:**
- V = 42 V
- I = 2 A
- P = 60 W