LHC BPM changes and status

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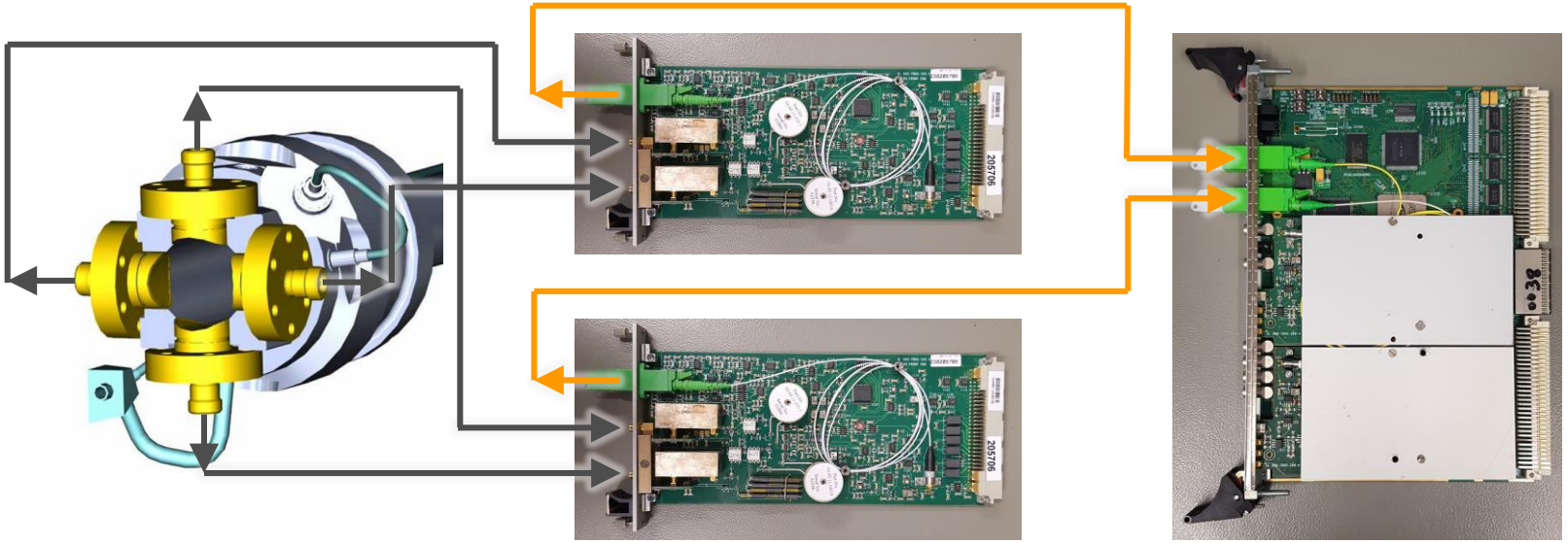
LHC BPM system architecture overview

Beam line <-- copper cables --> Tunnel / gallery <-- optical fibres --> Surface



1 x BPM pick-up

2 x WBTN

1 x DAB (carrier)
w/ 2 x integrator (mezzanine)

Summary of LS2 & YETS HW interventions

- Refurbishment of the laboratory calibration test bench & calibration procedures
- Replacement & recalibration of 221 WBTN cards
- Replacement & recalibration of 50 complete DAB cards (1 DAB + 2 integrators)
- Dis- and reconnection of 81 BPMs for vacuum interventions
- Installation of a new warm BPMWI.A5L8.B2 to functionally replace the non-conform cryogenic BPMR.5L8.B2
- Replacement / reconnection of cryogenic cables in 3 BPMs

Summary of LS2 & YETS SW interventions

- Real-time system upgrade to the version recommended for Run3 (CentOS7, Festa 8.3.1) & CCDE TL configuration clean-up
- Upgrade of Java expert applications – further work ongoing
- Change of the timestamp source - from BST to local
- New FESA – PM integration (to be validated with beam in 2022), PM did not work correctly in 2021
- BI / CEM / CSS agreement to delay Lumens deployment until EYETS 2022-23

System readiness for beam

- **LHC BPM system is fully operational and ready for beam with the same performance as in Run 2**
  - System validated during LS2 (RF ball, calibration) and 2021 beam tests (beam measurements)
- BPM activities during commissioning:
  - Validation of the new PM-FESA integration
  - Bunch phasing
  - Data taking with ABP

Feedback from OP and ABB

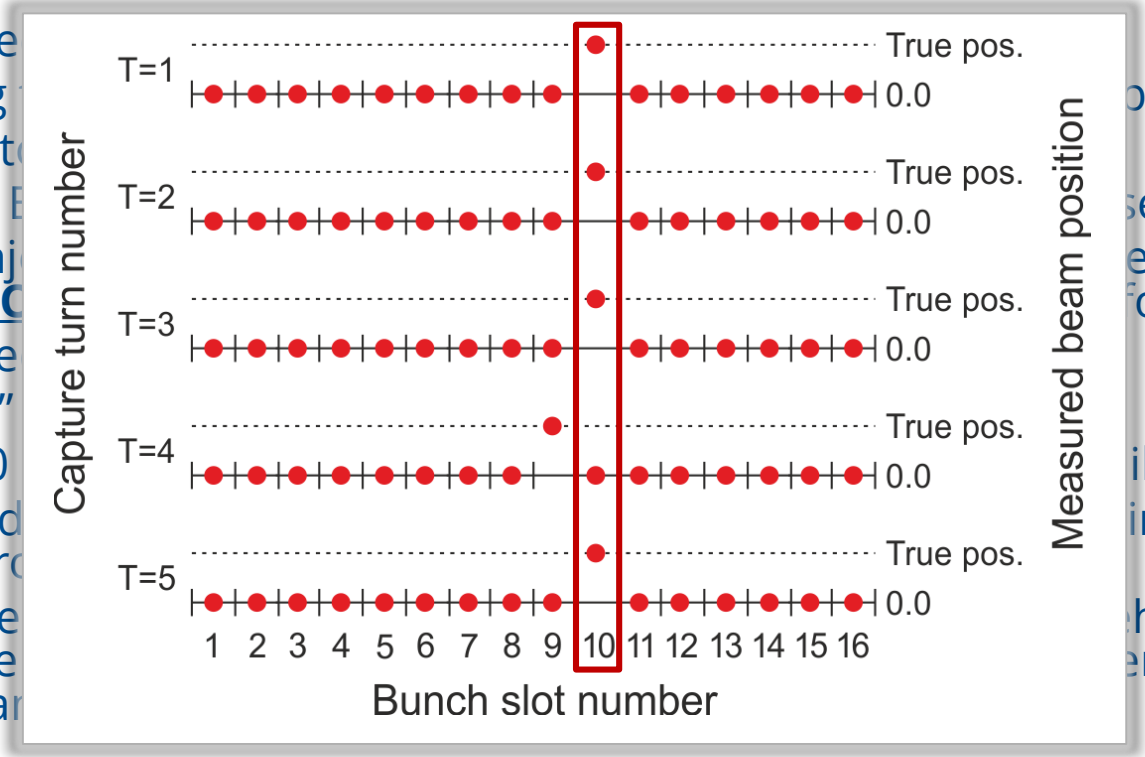
- List of 143 suspicious BPMs from OP (39) & ABP (116) complied at the start of LS2
  - Recalibration of the system and a massive WBTN replacement campaign in LS2
- List of 142 suspicious BPMs from OP (14) & ABP (132) compiled after the 2021 beam tests
  - ABP flags BPMs only after very heavy pre-processing
  - Detailed analysis of “raw” data by BI-BP, including historical data from 2015-18

Executive summary of BI analysis

- **50** BPMs likely experienced DAB HW problems (memory / bad connection)
  - Affecting only turn-by-turn capture (i.e. ABP) and **not** orbit (i.e. OP)
  - The same BPMs affected consistently since at least 2015
  - DABs replaced during YETS, new sequencer task to test all DABs
- **29** BPMs exhibit the “exact zero” problem
  - Affecting only turn-by-turn capture (i.e. ABP) and **not** orbit (i.e. OP)
  - Problem exists since at least 2015, affects the same BPMs on a short time-scale (~ hours) and different BPMs on a long time-scale (~ weeks)
  - Investigations will continue in Run 3 (more beam measurements needed)
  - Effective workaround proposed to ABP, will be implemented for Run 3
- **14** BPMs with other minor problems (e.g. disconnected cables) – all already fixed
- **39** BPMs look fine to BI

“Exact zero” problem

- BI performe
  - Ensuring
  - “Fully aut
- A few (~10) E
  - Bunch inj
    (only +1 C
  - Confirme
  - “Missing”
  - Exact 0.0
  - Proposed
    lack of cr
- A lot of time
  lab or in the
  to understar



by each BPM

se

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for both planes)

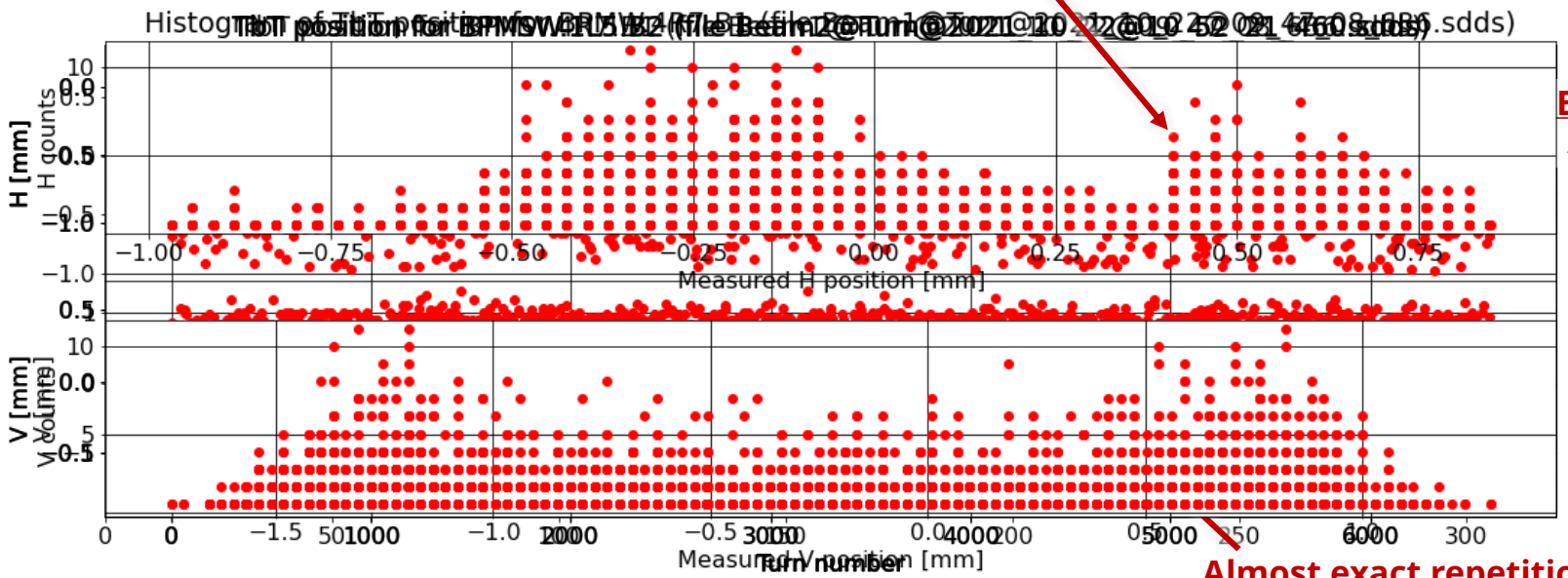
ibration method

inor error due to

haviour in the

ements needed

HW DAB problems



Step-like change in histogram

"Empty" band

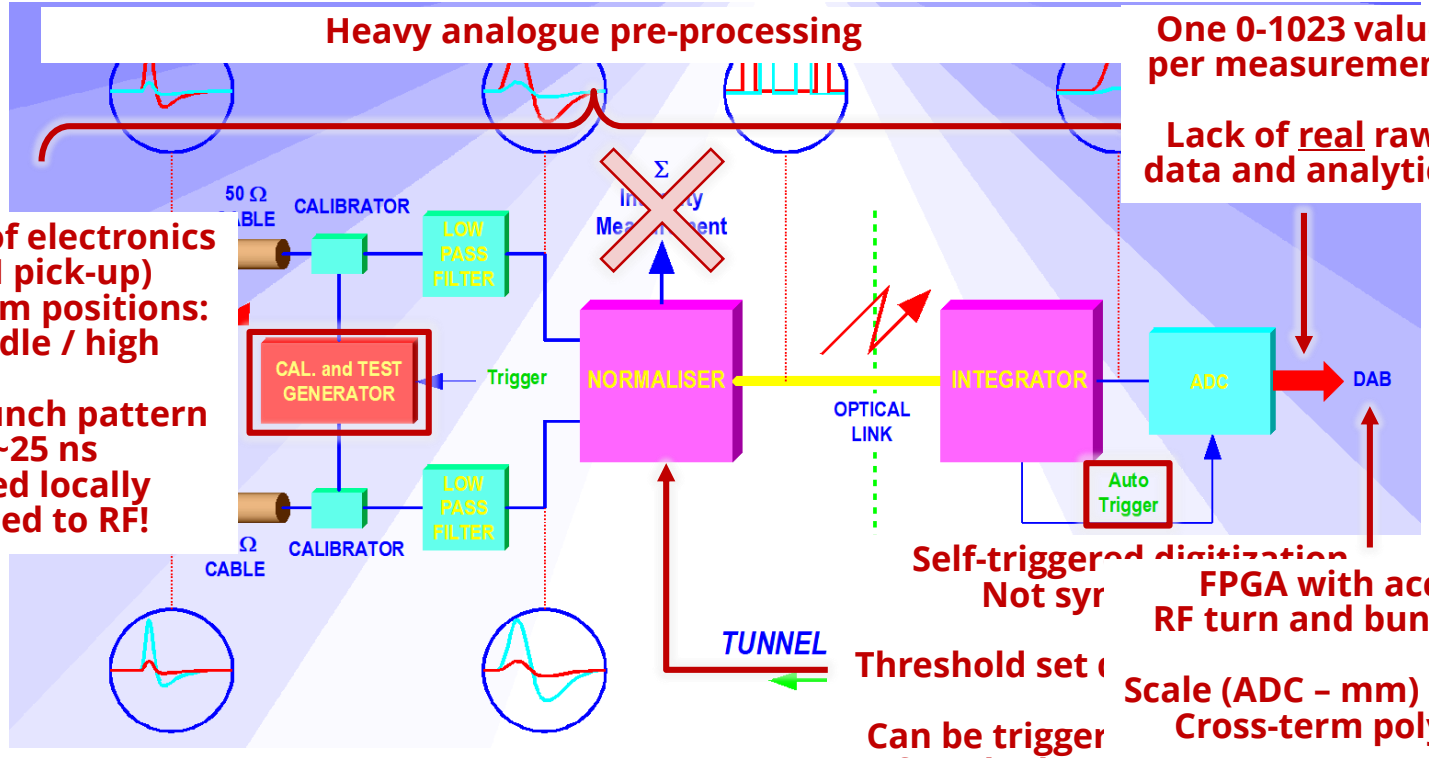
Almost exact repetition
64 turn - 64 turn
Small difference due to cross-term polynomial

Summary

- LHC BPM system is fully operational and ready for beam with at least the same performance as in Run 2
- Major tunnel and surface maintenance activities already completed
- Systematic analysis with beam needed to understand the origin of the old and non-blocking “exact zero” problem
- DAB HW problems will be detected by the sequencer
- Final validation of the new FESA-PM integration will be done with beam

Thank you for your attention

LHC BPM system architecture



Calibration of electronics (not BPM pick-up) in three beam positions: low / middle / high

For multi-bunch pattern
Tb = ~25 ns
Generated locally
Not synced to RF!

One 0-1023 value per measurement

Lack of real raw data and analytics

Self-triggered digitization
Not syn

FPGA with access to RF turn and bunch clocks

Threshold set

Scale (ADC – mm) calibration
Cross-term polynomial

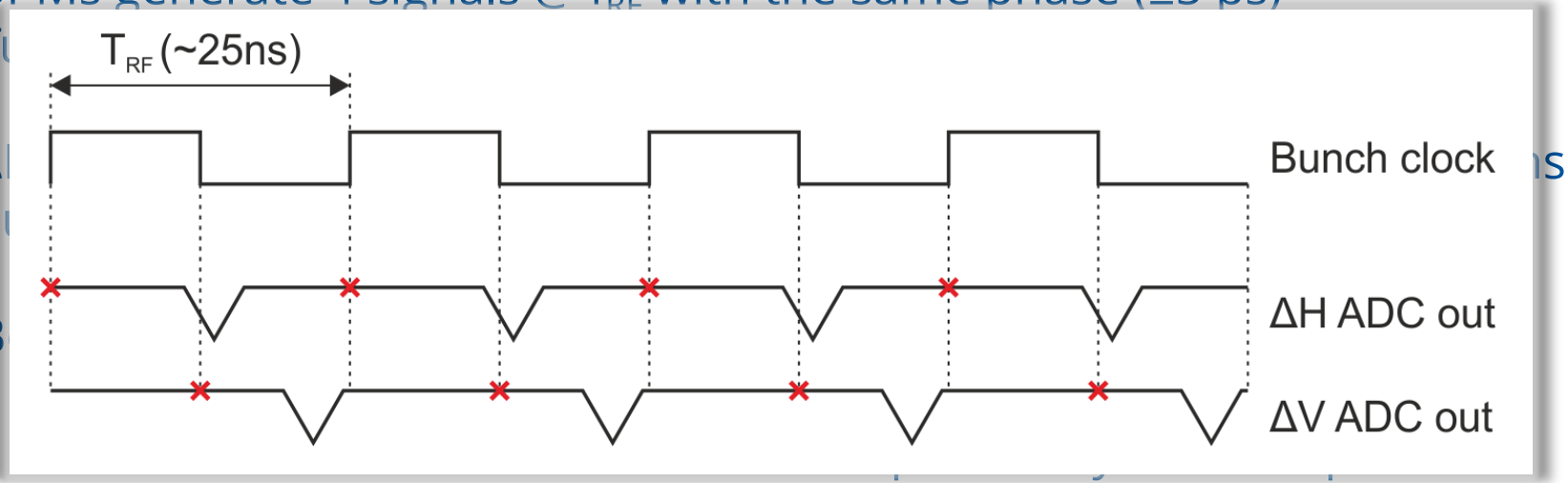
Can be trigger
for a bad sensitivity setting

“Exact zero” – analysis until now

- Recreating the problem without beam challenging / impossible
  - Our tunnel calibration signals are not synchronous with f_{RF}
  - No success with producing even a single exact 0 with synchronous beam-like signals generated on our laboratory test bench
    - Reference electronics and electronics removed from the LHC surface racks
- A hint from 2021– swapping two surface cards solved one instance of this problem
  - Very limited statistics, could have been coincidental
- More studies needed in Run 3 to understand the issue
  - Analysis of as many captures as possible
    - Logging and automatization would be beneficial
  - Commissioning time and hardware interventions must be anticipated
    - Measurements of raw analogue signals
    - Power-cycling electronics
    - Swapping cards
    - Other ideas will be surely developed as we improve our understanding of the problem

Bunch phase detection

- BPMs generate 4 signals @ f_{RF} with the same phase (±5 ps)
- Tu
  -
- Δ
- Su
  -
- B
  -
  -



  - Two possible values of phase shift: +0 T_{RF} / +0.5 T_{RF}
  - Phase shift selected and frozen automatically during phasing
  - Goal: ADC read-out far from transition states