Silicon pixel-detector R&D for future lepton colliders

VCI2022 – The 16th Vienna Conference on Instrumentation

February 24th, 2022

Dominik Dannheim (CERN)

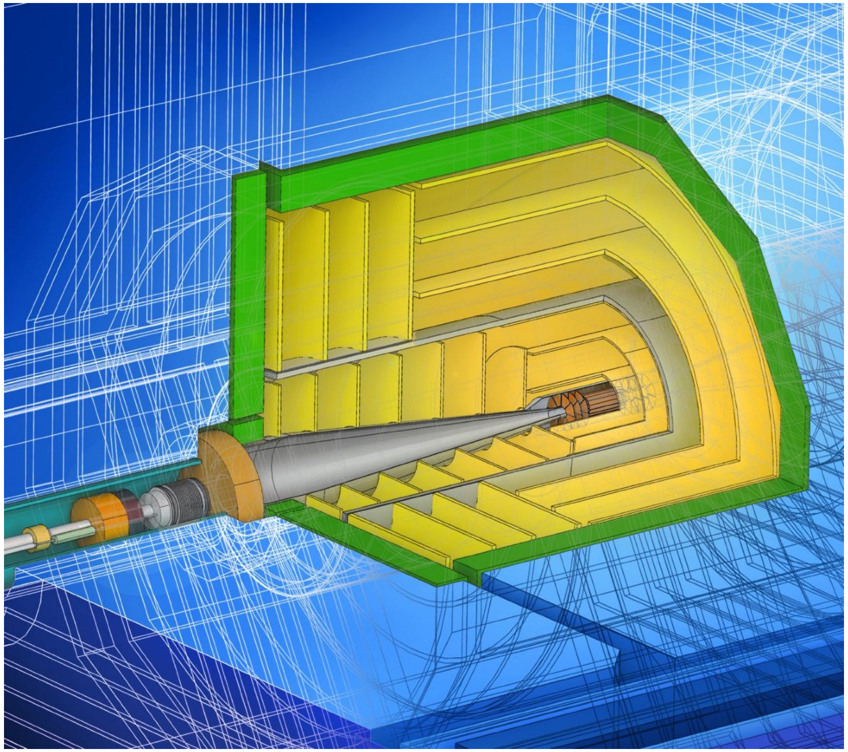
on behalf of the CLICdp collaboration

Outline

- Future Lepton Colliders and pixel-detector requirements

- Pixel-detector R&D examples:
  - Hybrid-detectors
    - CLICpix2 thin-sensor assemblies
    - ACF hybridisation
  - Monolithic sensors
    - CLICTD tracker-technology demonstrator
    - FASTPIX timing demonstrator

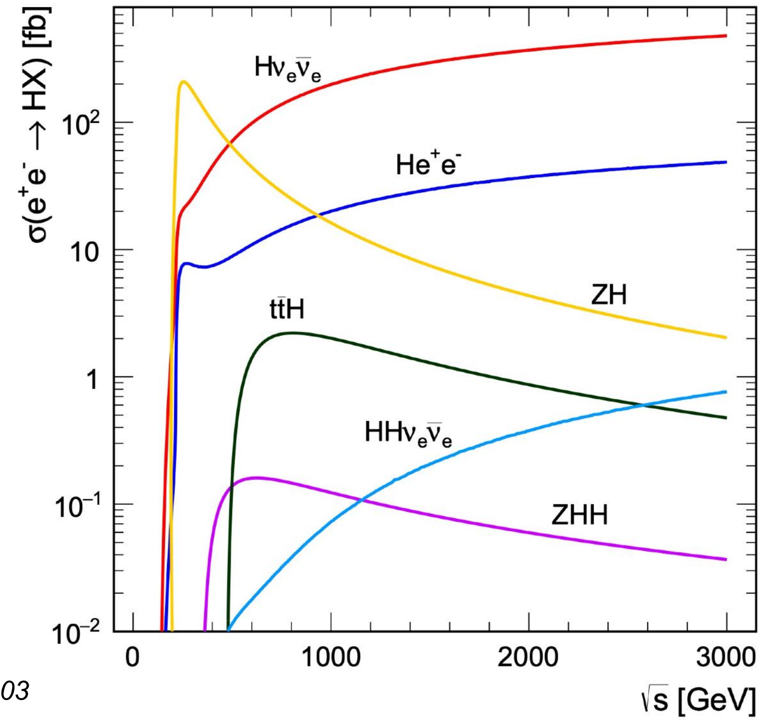
- Conclusions



Future Lepton Colliders

- Several proposals for post-LHC future Lepton Colliders:
  - $\sqrt{s}$ ~ 350 GeV - 3 TeV
  - Circular / linear collider designs
  - Physics goals:
    - Precision Higgs / top measurements
    - Measurement of electroweak precision observables
    - Direct/indirect Beyond-the-Standard-Model searches
- Vertex/tracking detector performance needs to match precision-physics goals:
  - Displaced vertices: $\sigma(d0) \sim 5 \oplus 15/(p[\mathrm{GeV}]\sin^{3/2}\theta)$ μm
  - Track-momentum: $\sigma(p_T) / p_T^2 \lesssim 2 \times 10^{-5}$ GeV^{-1}

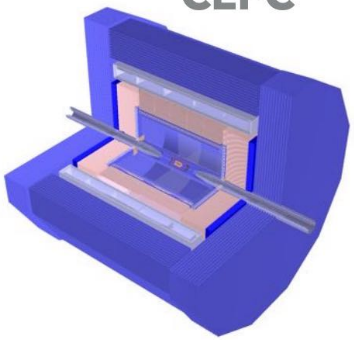
arXiv:1812.07986



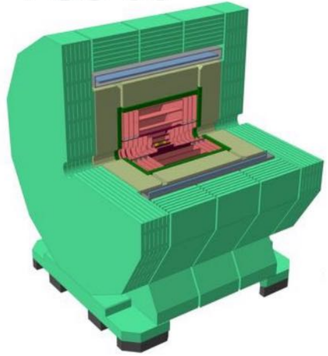
CERN-2012-003

ILC

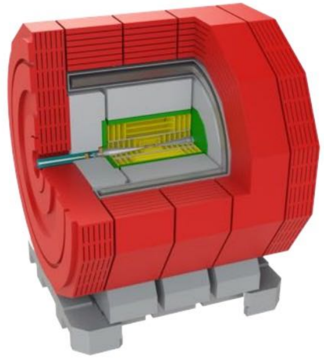
CEPC



FCC-ee



CLIC



Lepton Collider vertex/tracker requirements

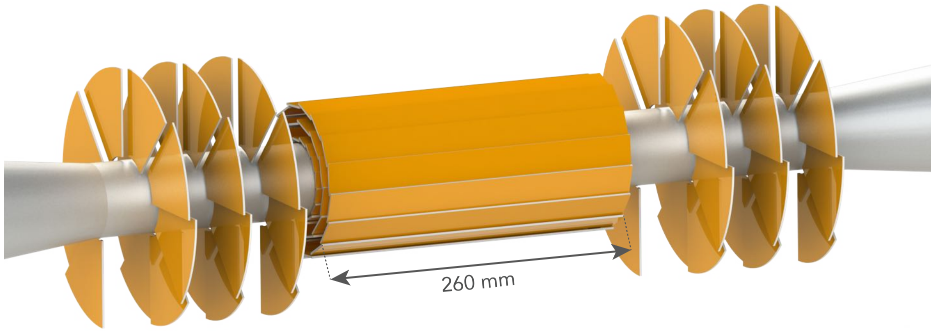
Vertex detector:

- good single point resolution: σ_{SP}~3 µm
- low material budget: $\lessapprox$ 0.2% X_0 / layer
  - → low-power ASICs for air cooling (~50 mW/cm²)

Large-area Tracker:

- 7 µm single-point resolution (~25-50 µm Rφ pitch)
  - → many layers, large outer radius
- ~1-2% X0 per layer
  - → low-mass supports + services, low power ~150 mW/cm²

CLIC vertex-detector simulation geometry



CLICdp-Note-2017-001

0.84 m²

Both:

- Moderate radiation exposure (>~10^4 below LHC!):
  - NIEL: < 10^{11} n_{eq}/cm²/y
  - TID: < 1 kGy / year
- few % max. occupancy from beam backgrounds

→ sets inner radius and limits cell sizes

→ time stamping down to ~5 ns accuracy (CLIC 3 TeV)

→ depleted sensors, fast frontend

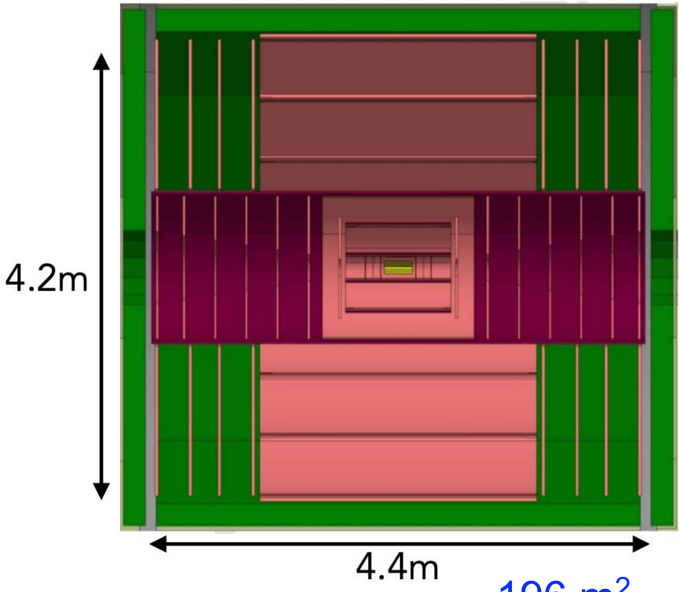
- Benefits of precision timing (<100 ps) for PID under study

Linear-Collider specific:

- Low duty cycle: ~20-200 ms gaps between bunch trains
  - → trigger-less readout, pulsed powering

→ Emphasis of this talk on technology R&D for 3-TeV CLIC (most challenging combination of requirements)

FCC-ee tracker simulation geometry (CLD)



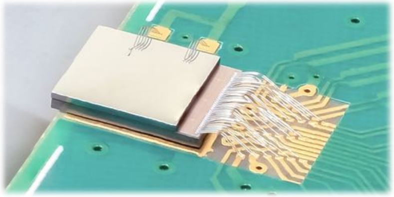
196 m²

http://arxiv.org/abs/arXiv:1911.12230

CLIC pixel-detector R&D

Hybrid Assemblies

CLICpix2 + planar sensor

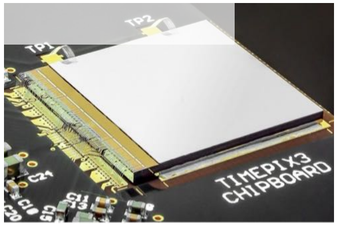


65 nm CMOS

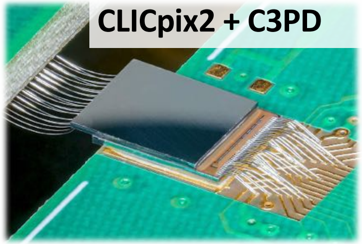
Cracow SOI

200 nm SOI

Timepix3 ACF-bonding



130 nm CMOS



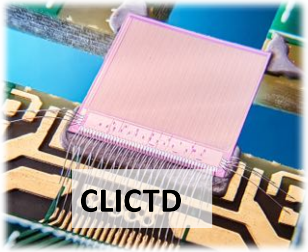
CLICpix2 + C3PD

65 nm CMOS
+ 180 nm HV-CMOS

Monolithic Sensors

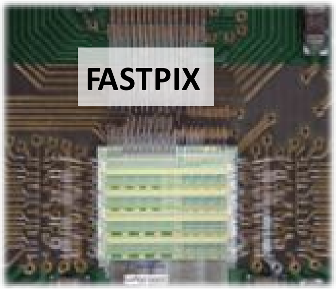
ATLASpix

180 nm HV-CMOS



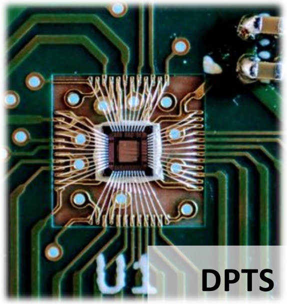
CLICTD

180 nm CMOS



FASTPIX

180 nm CMOS



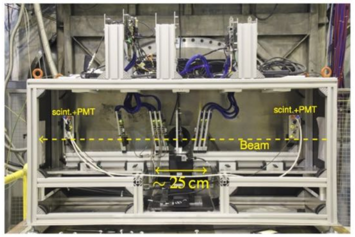
DPTS

65 nm CMOS

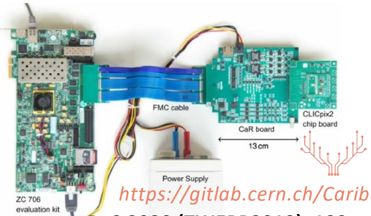
Tools

Detector technologies for CLIC, CERN-YR-2019-001

CLICdp beam telescope



Caribou readout system



https://gitlab.cern.ch/Caribou

PoS 2020 (TWEPP2019), 100

MC Simulation framework: Allpix Squared

https://gitlab.cern.ch/allpix-squared/allpix-squared

NIM A 901 (2018) 164-172

Analysis & reconstruction framework: Corryvreckan

https://gitlab.cern.ch/corryvreckan/corryvreckan

2021 JINST 16 P03008

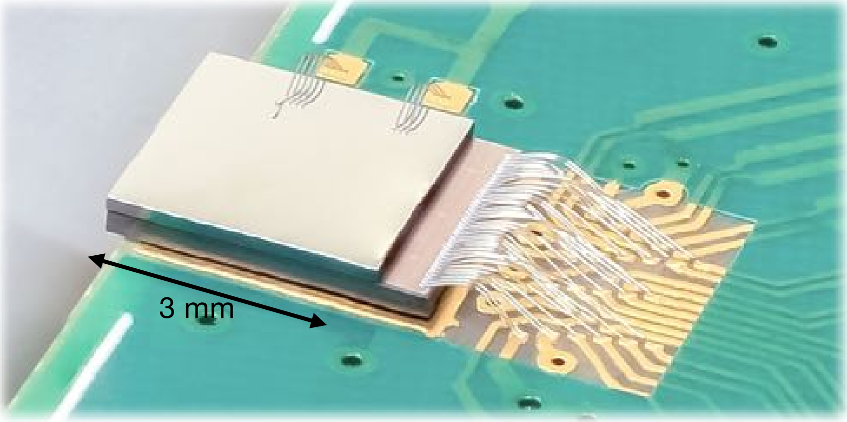
- Diverse R&D program, focusing on conceptual studies + small technology demonstrators
→ Flexible tools developed, to support the R&D and exploit synergies between the various R&D lines
- R&D performed within various collaborative frameworks (CLICdp collaboration, CERN EP R&D, AIDAinnova) and with strong links to HL-LHC developments

Fine-pitch hybrid planar pixel detectors

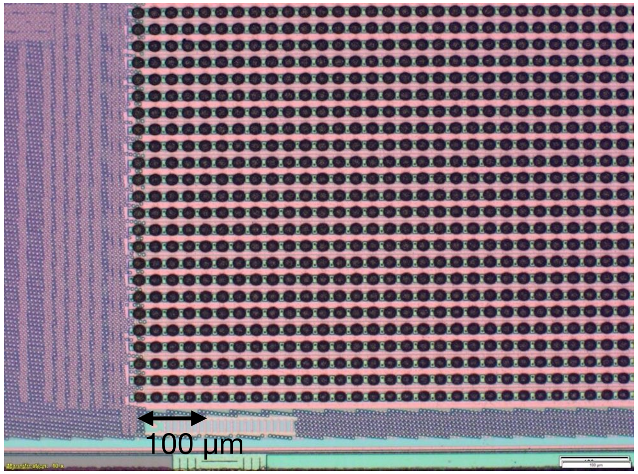
CLICpix2 readout ASIC:

- Targets CLIC vertex-detector requirements
- 65 nm CMOS process
- Pixel pitch 25 µm x 25 µm (128 x 128 pixels)
- Simultaneous 5-bit ToT + 8-bit ToA (10 ns bins) readout
- Used for development of 25 µm-pitch interconnect-process (IZM) and for testing innovative fine-pitch sensor designs (planar active edge, active HV-CMOS, enhanced-lateral-drift sensors)

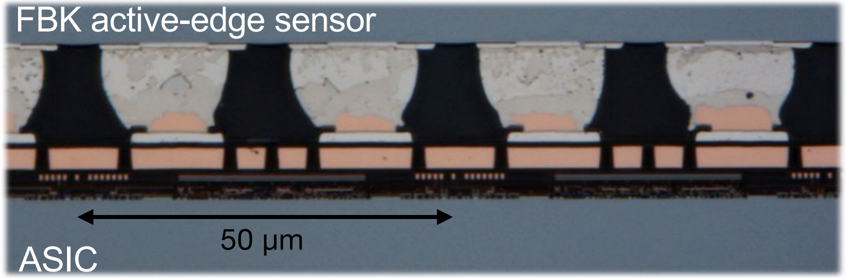
CLICpix2 planar-sensor assembly



SnAg bumps on CLICpix2 (IZM)



Cross section of bump bonds by IZM



- Single-die bump-bonding process with pixel pitch of 25 µm developed by IZM
- Interconnect yield of up to 99.6%

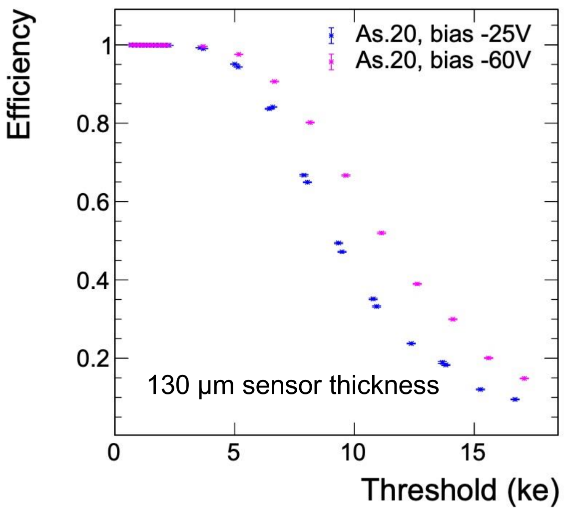
JINST, 15(03), C03045

CLICpix2 test-beam results

- Detailed test-beam studies for assemblies with high interconnect yield
- Excellent performance observed for 130 µm sensor thickness, meeting most CLIC requirements:
    - <3 µm intrinsic spatial resolution (mean cluster size ~2.6)
    - Hit-detection efficiency >99.7%
    - Hit-time resolution <5 ns
- However: sensor thickness well above target thickness of 50 µm

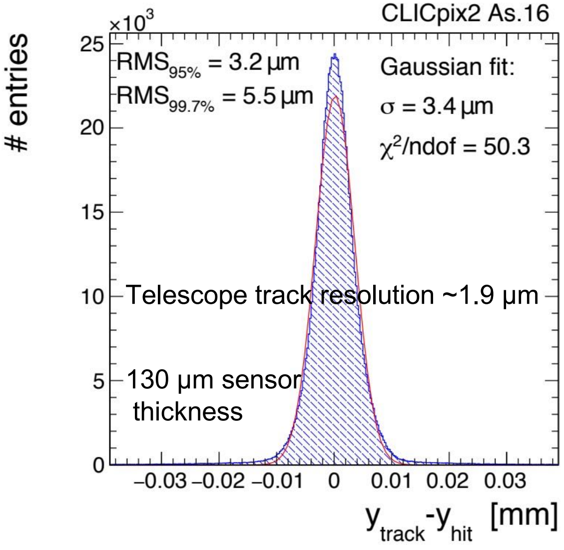
→ ~6.8 µm spatial resolution for 50 µm sensor thickness (mean cluster size ~1.3)

Efficiency

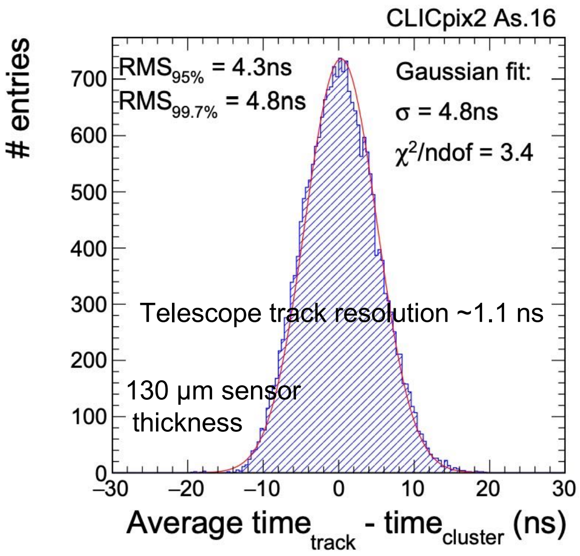


CERN-THESIS-2020-338

Spatial residuals



Timing residuals



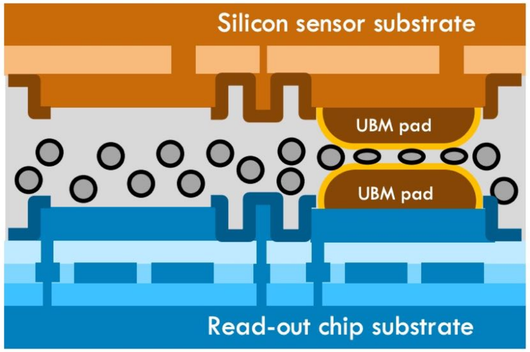
Anisotropic Conductive Film (ACF)

- Adhesive epoxy film with conductive micro particles
  - Compression of particles enables electrical connection between pads

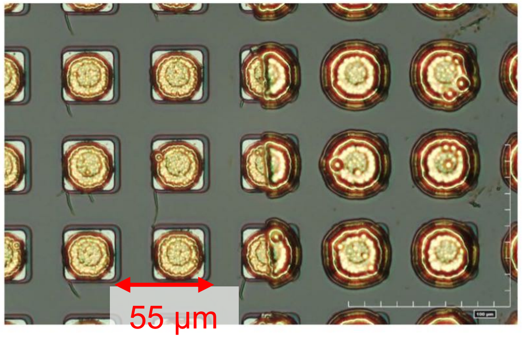
- New prospects for hybridisation and module integration

- Ongoing development / optimisation of two in-house processes:
  - Chemical Electroless Nickel Immersion Gold (ENIG) deposition for Under Bump Metallization (UBM)
    → uniformity, thickness
  - Semi-automatic flip-chip bonding with ACF layer
    → ACF material (particle diameter and density), epoxy thickness, lamination procedure, temperature/pressure profile for bonding

ACF bonding with conductive micro-particles

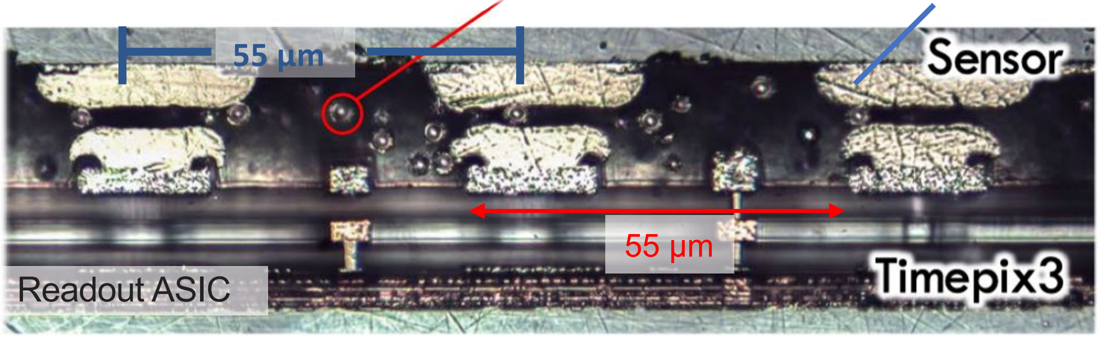


Timepix3 ENIG re-processing



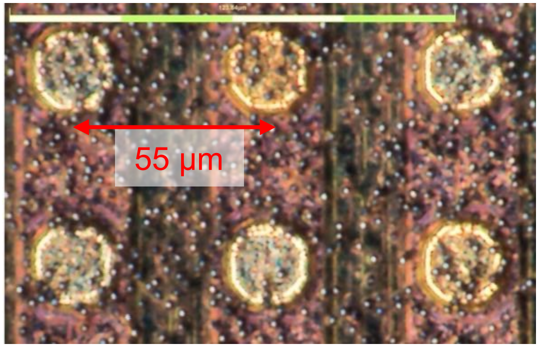
CERN-EP-RDET-2021-001

ACF-hybdridisation



https://agenda.linearcollider.org/event/9211/contributions/49469/attachments/37464/58685/ILCX_MVicente_ACF.pdf

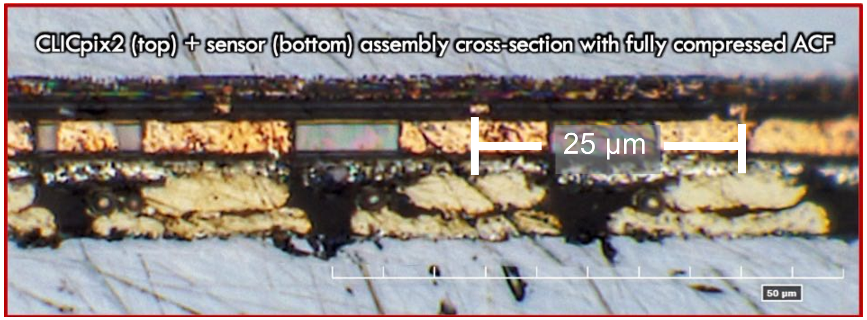
Timepix3 pixel matrix with ACF



ACF - Hybridisation Tests

- Bonding tests performed with Timepix3 and CLICpix2 ASICs
- 18 µm film with 3 µm micro particles, 100 kg bonding force
- Proof-of-concept for bonding areas up to 1 cm² and 55 µm pitch

Fine-pitch UBM plating with CLICpix2 ASICs

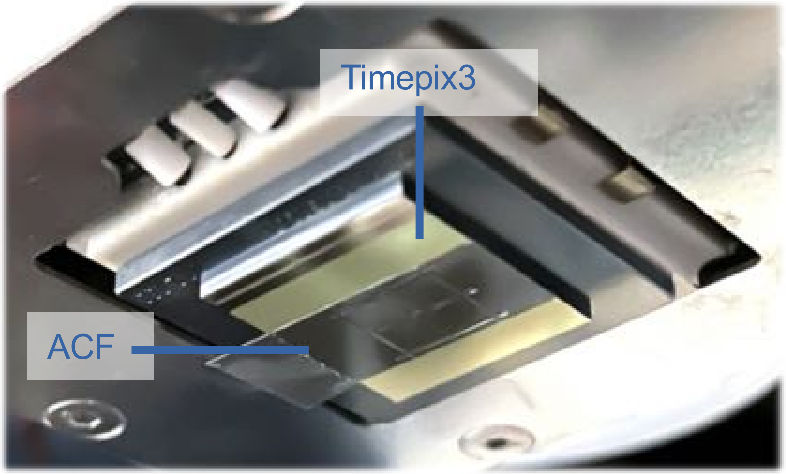


CLICpix2 (top) + sensor (bottom) assembly cross-section with fully compressed ACF

- Interconnection for larger areas / smaller pitch more challenging due to the required larger bonding force

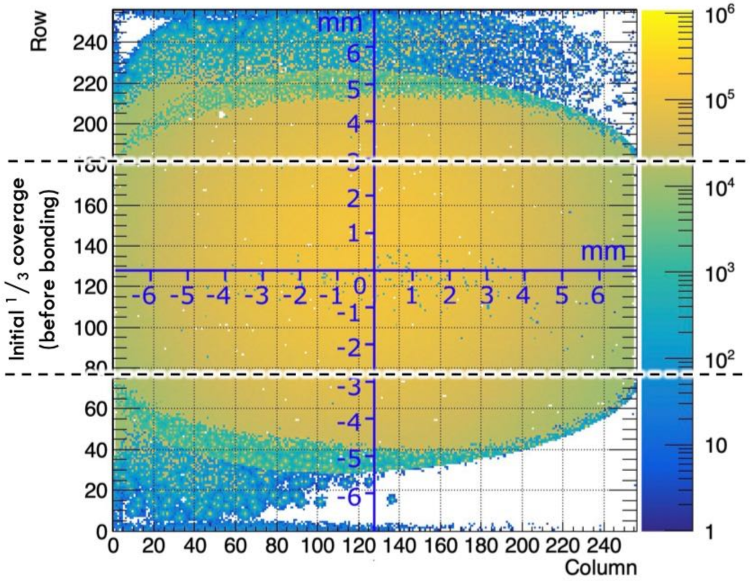
Bonding to Timepix3 sensor

Approx. 50% ACF coverage



Timepix3 hit map from Sr90 illumination

Approx. 30 % ACF coverage



ACF for module integration

ACF module integration

Larger bonding pads: 80 µm – few mm diam.

→ Similar to industrial ACF usage

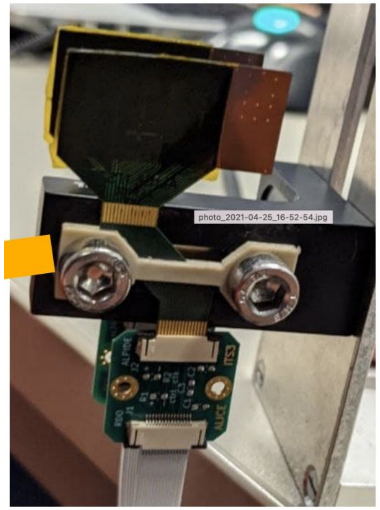
→ Good interconnect results

→ Topology / uniformity of UBM important

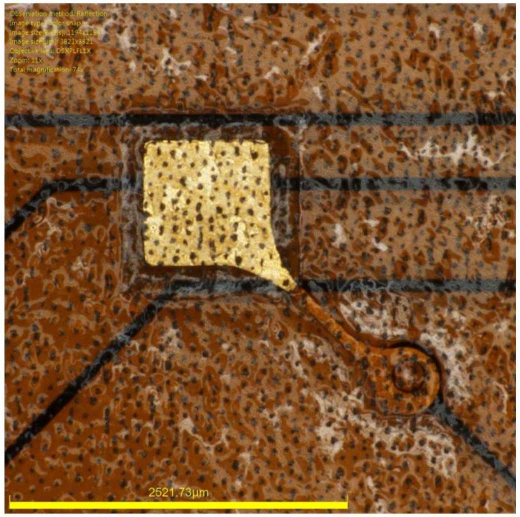
Various proof-of-concept projects:

- Beam tests of ALPIDE ACF modules
- Bonding tests with MALTA silicon bridges
- Tests with FCAL LUXE pad sensors

ALPIDE ACF module in DESY TB

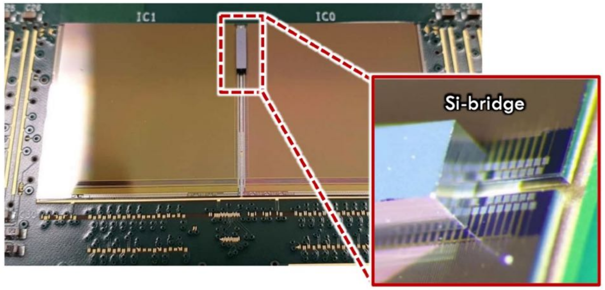


ACF on LUXE pad



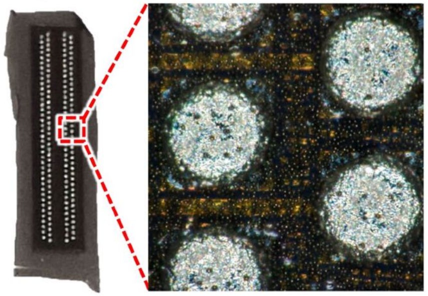
MALTA module building with silicon bridge and ACF bonding

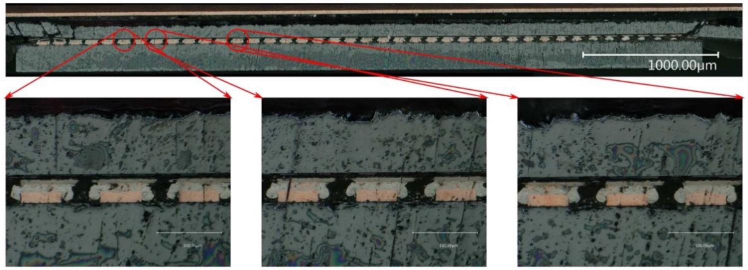
MALTA double module with Si-bridge chip (images credit: Florian Dachs)



Si-bridge with ACF

ACF over Si-bridge pads





Cross section for 5kg of pressure.

M. Mager, F. Dachs, Y. Benhammou

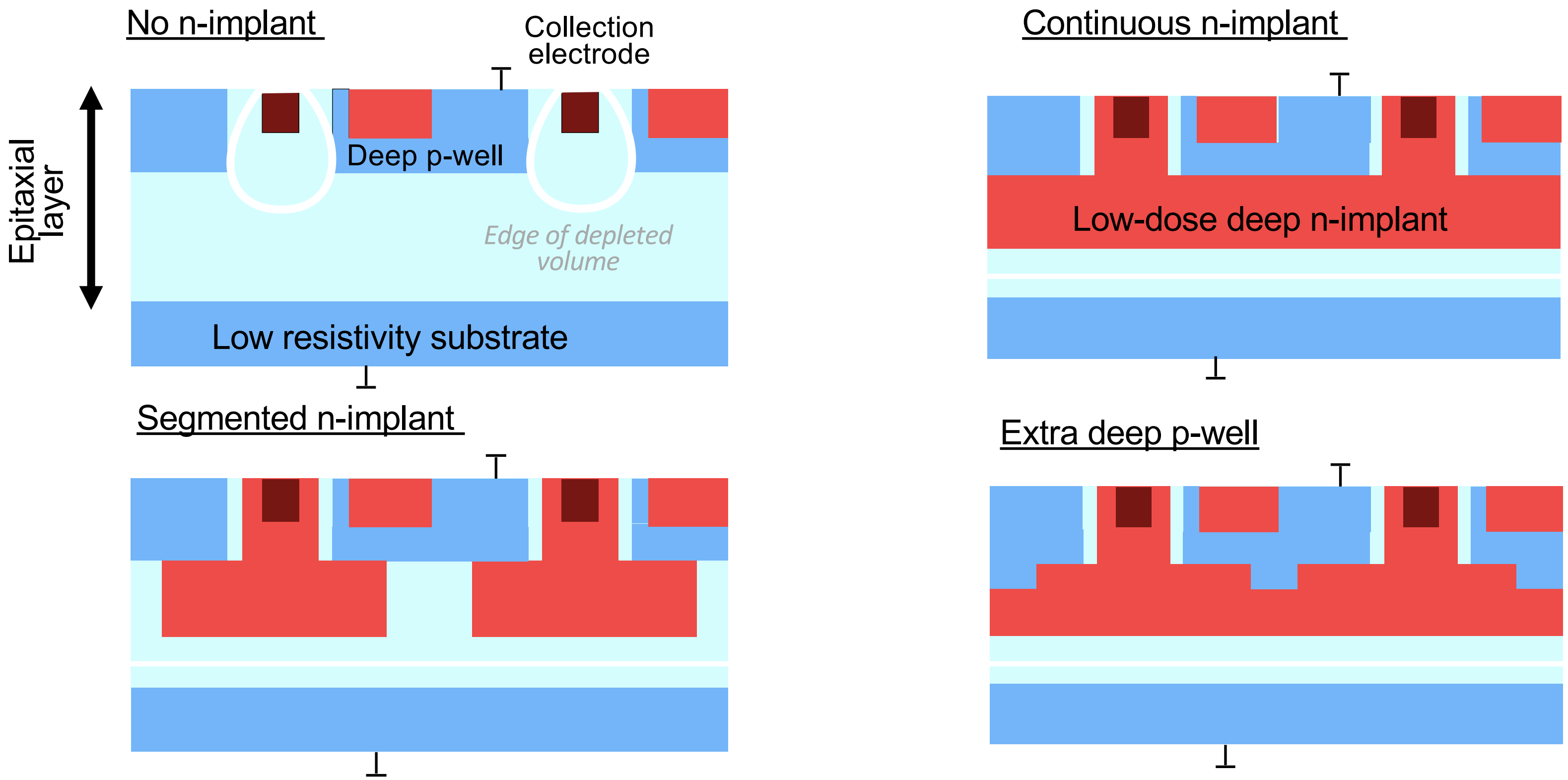
Small collection electrode monolithic CMOS

- Modified 180 nm CMOS imaging process with small collection electrode (O(fF) capacitance)

(e.g. ALPIDE, (Mini-)MALTA, CLICTD, FASTPIX …)

- Deep low-dose n-implant for full lateral depletion
- Introduction of lateral doping gradient leads to accelerated charge collection
  - Comparison of various design modification in terms of detector performance

JINST 14 (2019) C05013



Not to scale

Simulations

- Complex non-uniform field configurations in the small collection-electrode layout require sensor-design optimisations

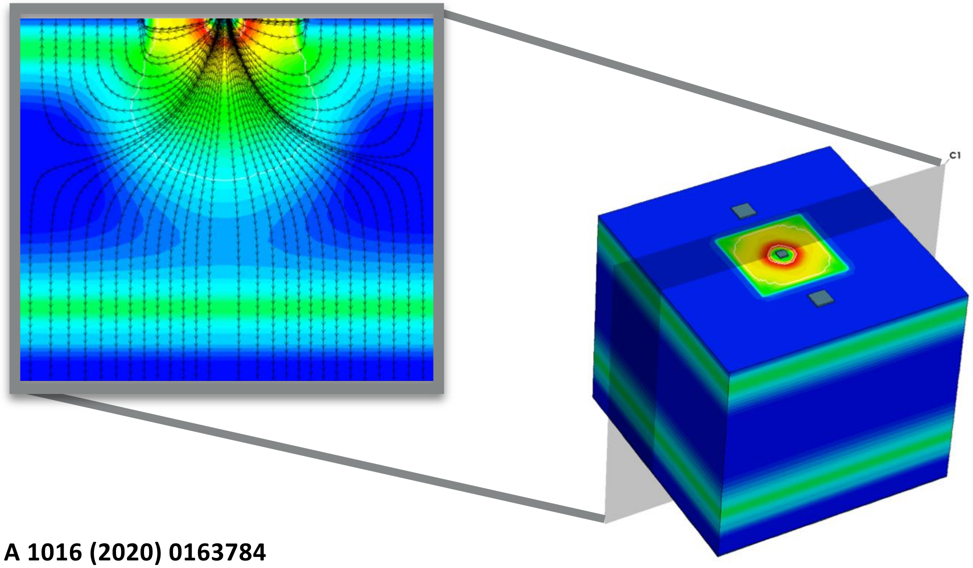
- Finite-element (3D TCAD) and Monte Carlo (Allpix Squared) simulation to combine accurate sensor modelling with high simulation rates

- Validated against transient 3D TCAD and data

https://gitlab.cern.ch/allpix-squared/allpix-squared

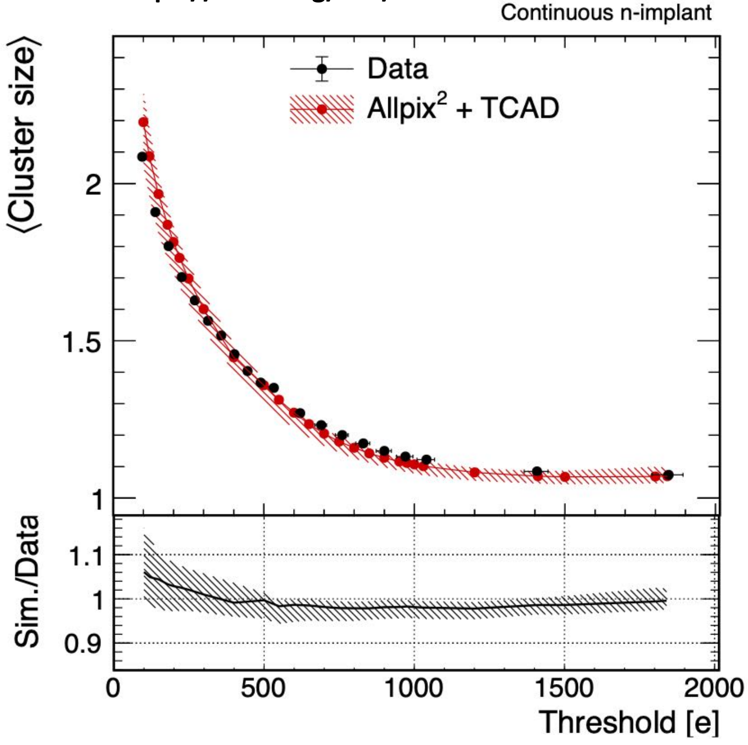
NIM A 901 (2018) 164172

Electrostatic potential + streamlines

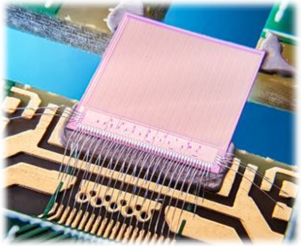


NIM A 1016 (2020) 0163784

CLICdp-Pub-2021-003
https://arxiv.org/abs/2202.03221



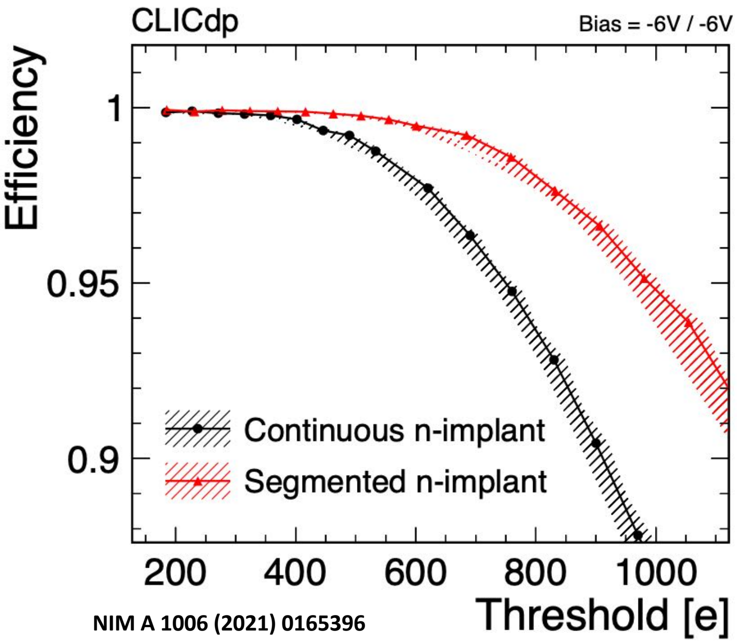
CLICTD Technology Demonstrator



CLICTD 180nm monolithic sensor

- Channel pitch: 300 µm x 30 µm (16x128 channels)
- Sub-pixel pitch: 37.5 µm x 30.0 µm
- Analogue front-end of 8 sub-pixels grouped in one digital front-end (= readout channel)
- 8-bit ToA (10 ns ToA bins) + 5-bit ToT (combined ToA/ToT for every 8 sub-pixels in 300µm dimension)
- Sensors produced with different substrate materials (epitaxial, high-resistivity Cz) and thicknesses (40-300 µm)

IEEE Trans Nucl. Science 67.10 (2020): 2263-2272.



NIM A 1006 (2021) 0165396

Excellent performance observed in test-beam measurements:

- Threshold: ~100 - 180 e (occupancy < 10^{-3} hits/sec)
- Single pixel noise : < 15 e
- Hit-detection efficiency : > 99.7 %
- Spatial resolution : 4.6 µm
- Time resolution : 5.2 ns (Limited by front-end time resolution)

- Reduced charge sharing for pixel flavour with segmented n-implant leads to higher concentration of charge in one pixel cell

→ Improved efficiency at high thresholds

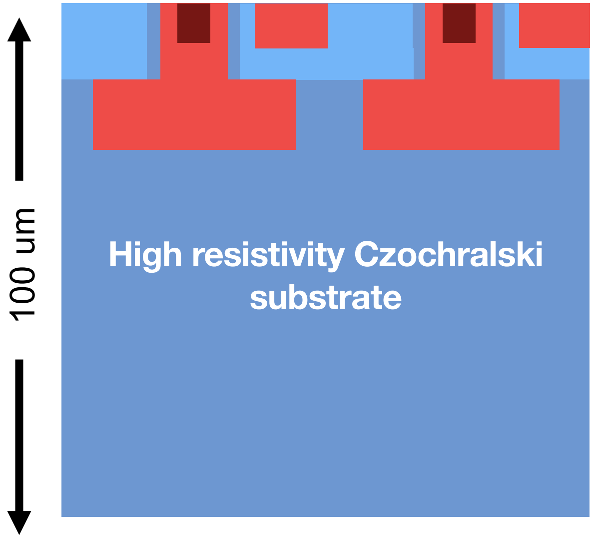
Advanced sensor materials

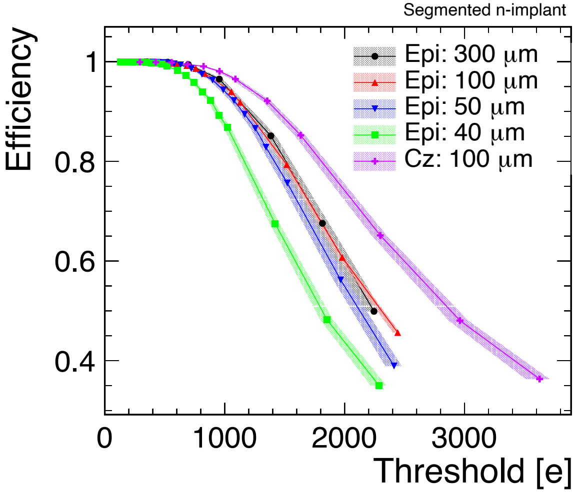
- Production using high-resistivity Czochralski (few kΩcm) wafers allowing for larger depleted volume
  → Larger active sensor volume

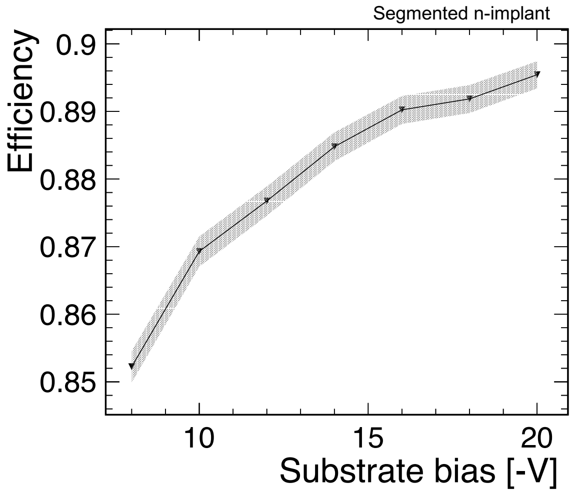
NIM A 986 (2021) 164381

- Improved efficiency at high thresholds due to higher signal
- High-resistivity Czochralski sample enables combination of small collection electrode with large depleted volume
  → Improvement for all performance parameters (though limited by front-end)

Not to scale







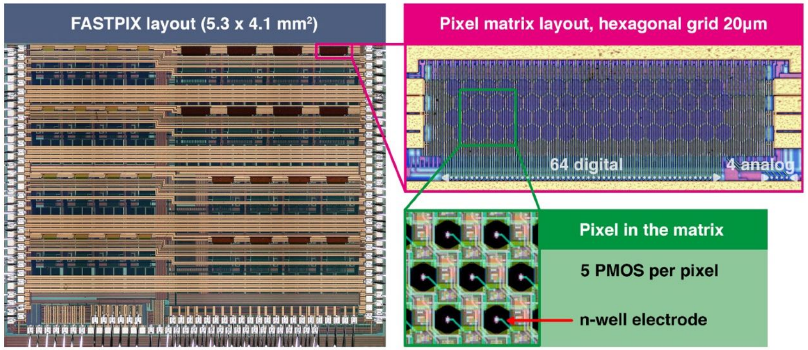
	Required (CLIC tracker)	Epi	Cz*
Spatial resolution (transv.)	< 7 µm	4.6 µm	4.3 µm
Time resolution*	~ 5 ns	5.2 ns*	4.4 ns*
Efficiency	> 99.7 %	> 99.7 %	> 99.7 %
Material content	< 200 µm	40 - 100 µm	100 µm

*limited by front-end

ATTRACT FASTPIX

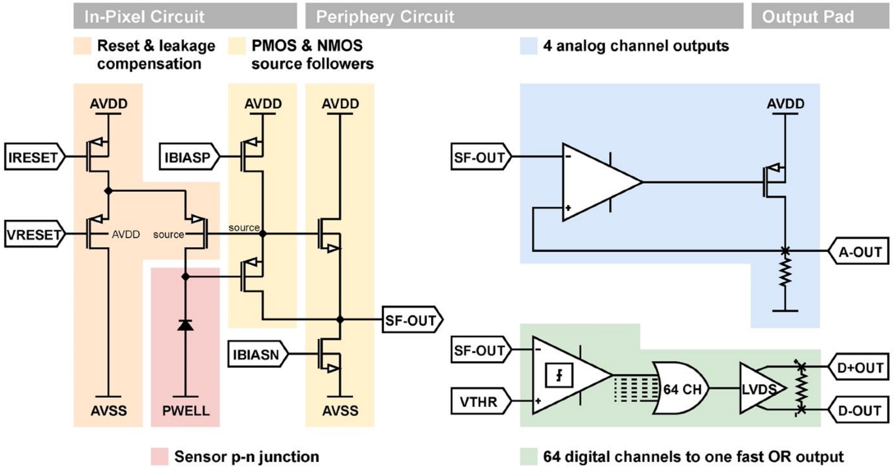
FASTPIX technology demonstrator for sub-ns timing

- Modified 180 nm CMOS imaging process
- 32 mini matrices of hexagonal pixels (8.66 to 20 µm pitch)
- 4 analogue outputs + 4x16 pixels with ToT/ToA
- Various sensor designs and process options
- Position and ToT encoding via delay lines (asynchr. r/o)



On-chip readout circuit

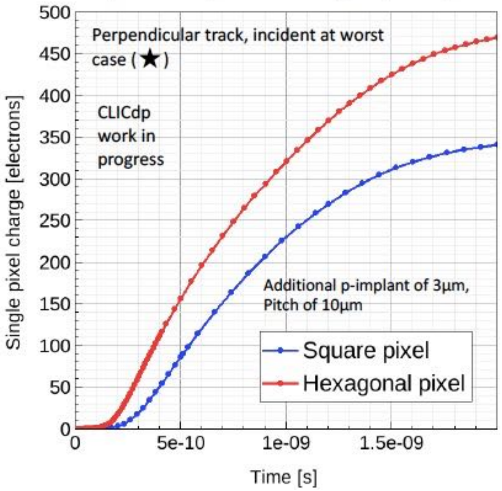
W. Snoeys, T. Kugathasan

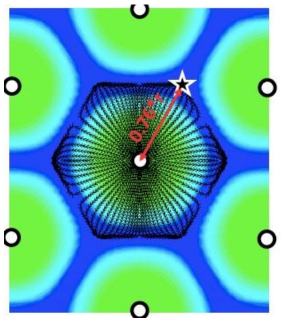


Simulated chip parameters:

Sensor capacitance		1 fF
Equivalent Noise Charge		11 e$^-$
Jitter (for Q_{in} = 1000 e$^-$)		20 ps
Power	In pixel source follower	18 µW
	Periphery discriminator	150 µW
	Analog monitoring buffer	20 mW

3D TCAD Simulation

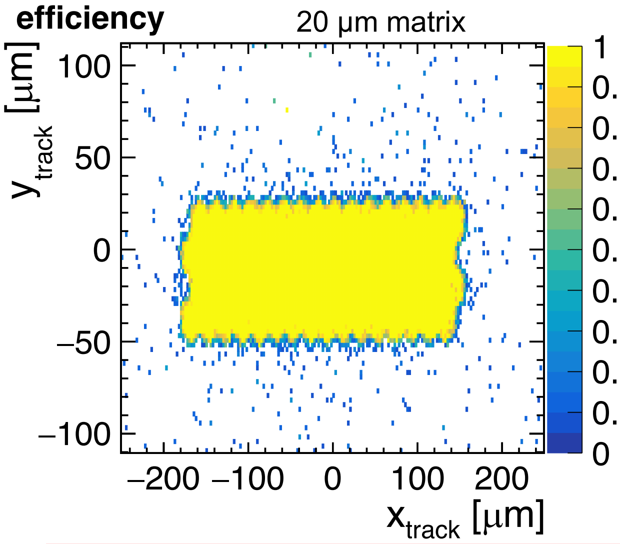


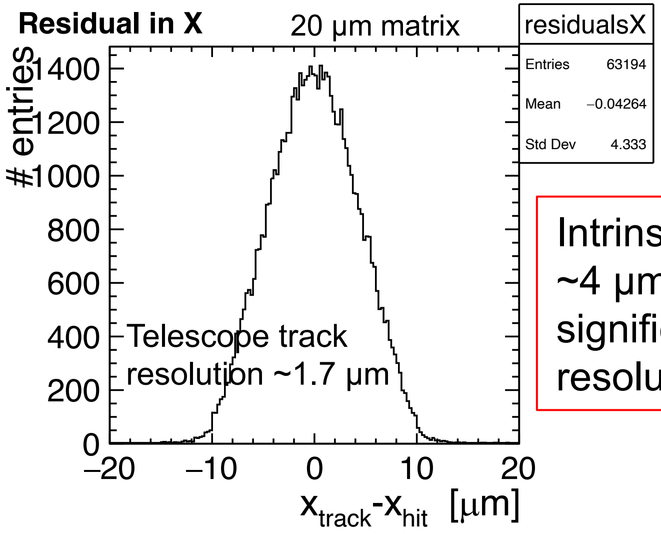


T. Kugathasan et al: Monolithic CMOS sensors for sub-nanosecond timing, Hiroshima 2019

- Optimised for precise sensor timing in 3D TCAD simulation studies
- Hexagonal pixel layout:
  - Improved charge collection at pixel edges
  - Reduced number of neighbouring pixels → Less charge sharing

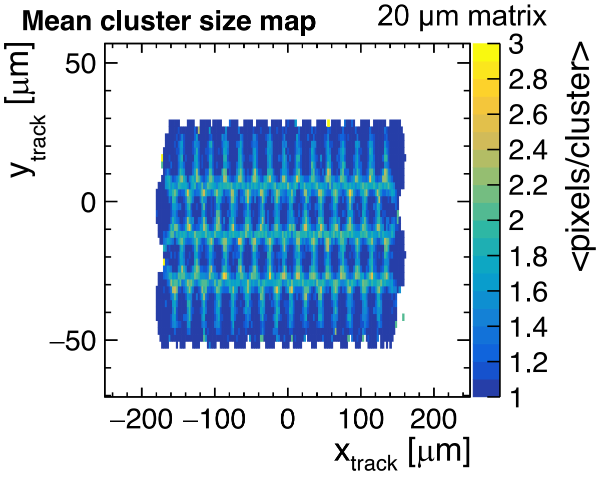
ATTRACT FASTPIX: Test-beam measurements (I)

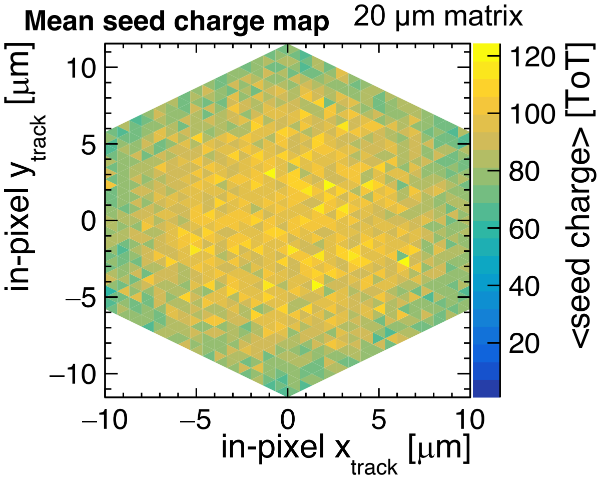




Intrinsic position resolution ~4 μm (for 20 μm pitch), significantly below binary resolution of 5.8 μm

→ Fully efficient operation
(for ~43 e threshold, ~5 e noise)

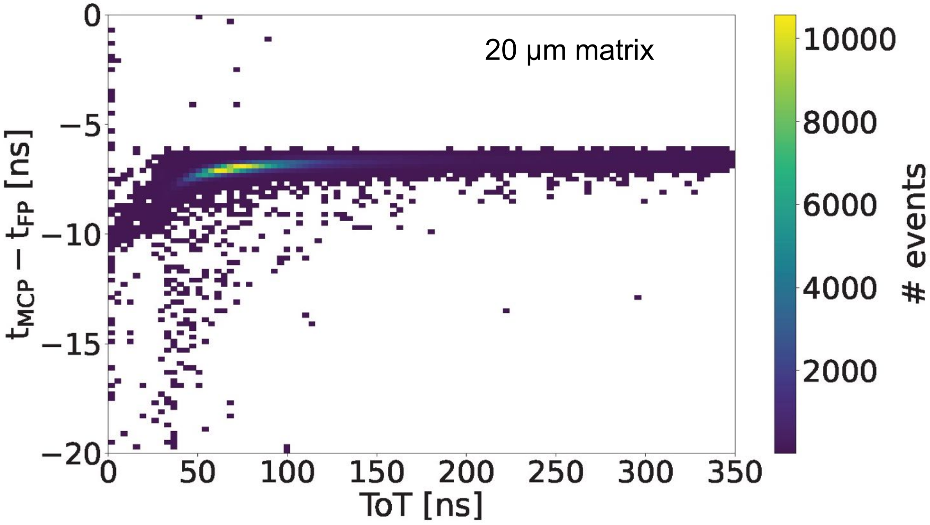




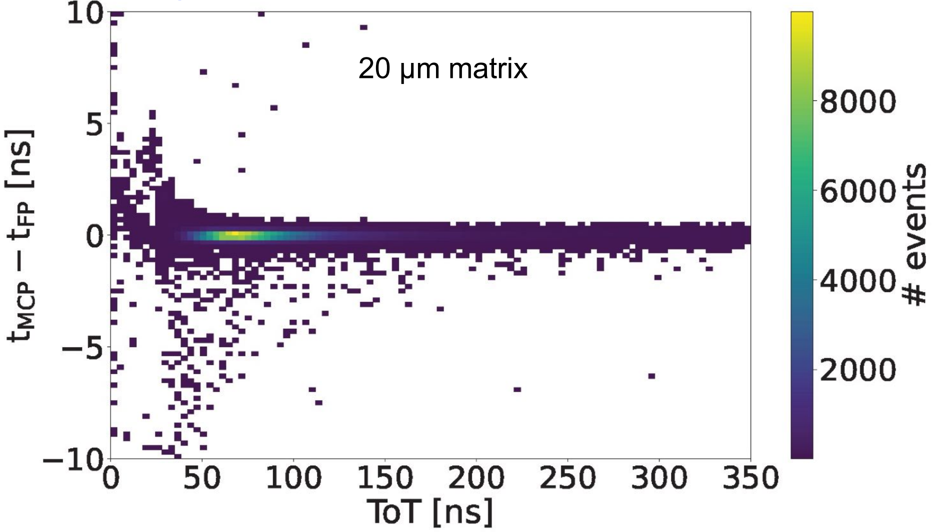
Charge sharing mostly at the pixel edges
→ increased cluster size
→ Reduced seed charge

ATTRACT FASTPIX: Test-beam measurements (II)

Seed-pixel time residuals vs. ToT before time-walk correction



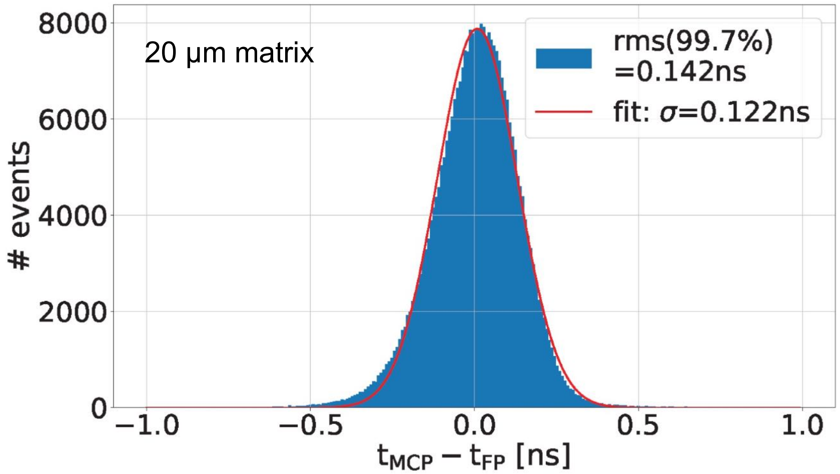
Seed-pixel time residuals vs. ToT after time-walk correction



Test-beam timing results:

- Strong time-walk effects in particular at matrix edge due to charge sharing
- Time resolution of ~500 ps w/o time-walk correction
- Time resolution of ~120 ps after offline time-walk correction

Seed-pixel time residuals after time-walk correction



Braach, J.; Buschmann, E.; Dannheim, D.; Dort, K.; Kugathasan, T.; Munker, M.; Snoeys, W.; Vicente, M. Performance of the FASTPIX Sub-Nanosecond CMOS Pixel Sensor Demonstrator. Instruments 2022, 6, 13. https://www.mdpi.com/2410-390X/6/1/13

Conclusions

- Stringent requirements for Lepton Collider vertex and tracking detectors have inspired broad and integrated technology R&D program

- Innovative sensor + readout technologies under study
  - Combination of vertex-detector requirements remains challenging (CLICpix2)
  - Tracker requirements met by monolithic technologies (CLICTD)
  - Sub-nanosecond sensor timing demonstrated in monolithic technology (FASTPIX)

- Innovative interconnect technology under development for hybridisation and module building (ACF)

- Advanced tools for characterization (Caribou), simulation (Allpix2) and analysis (Corryvreckan) support the detector R&D

Thanks to everyone who provided material for this talk!

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Part of the measurements leading to parts of these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF)

Additional Material

Caribou DAQ

Versatile data acquisition system based on programmable hardware

https://gitlab.cern.ch/Caribou

System-on-Chip (SoC) board

- Embedded CPU for DAQ, user interface, operating system (Linux)
- Field programmable gate array (FPGA) for detector control and data processing

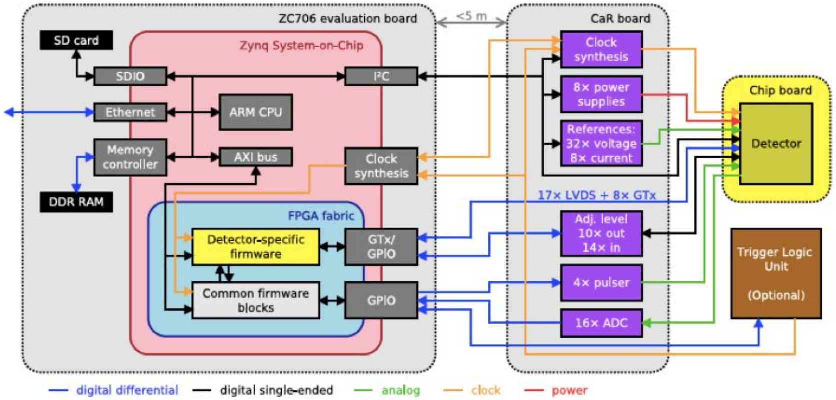
Control and Readout (CaR) interface board

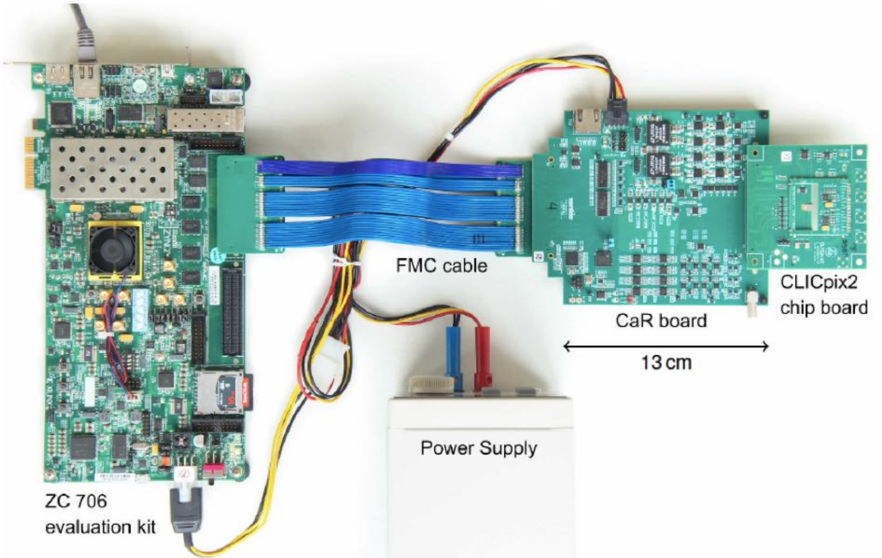
- Physical interface from SoC board to detector chip
- Voltage regulators, ADCs, pulse/clock generator

Application-specific detector carrier board

- Only detector chip and passiv components

- Successfully used for ATLASPix, ATLASPix2, ATLASPix3, CLICpix2/C3PD, H35Demo/FEI4, RD50-MPW1





https://iopscience.iop.org/article/10.1088/1748-0221/12/01/P01008

Allpix-Squared simulation toolkit

Selected Applications

- **Detectors for HEP**
    - MAPS (CLICTD, ALICE, ARCADIA,…), RD53, ATLAS ITk Strips, …
- **NASA / Space Radiation Analysis**
- **ISS radiation monitor simulations**
- **Germanium X-ray detector (Synchrotron SOLEIL)**
- **Education / Outreach activities**
    - EDIT Detector School, Beamline for Schools 2019,…

Publications

NIM A 901 (2018) 164-172

NIM A 964 (2020) 163784

Website

https://cern.ch/allpix-squared

Repository

https://gitlab.cern.ch/allpix-squared/allpix-squared

User Forum

https://cern.ch/allpix-squared-forum/

User Manual

https://cern.ch/allpix-squared/usermanual/allpix-manual.pdf

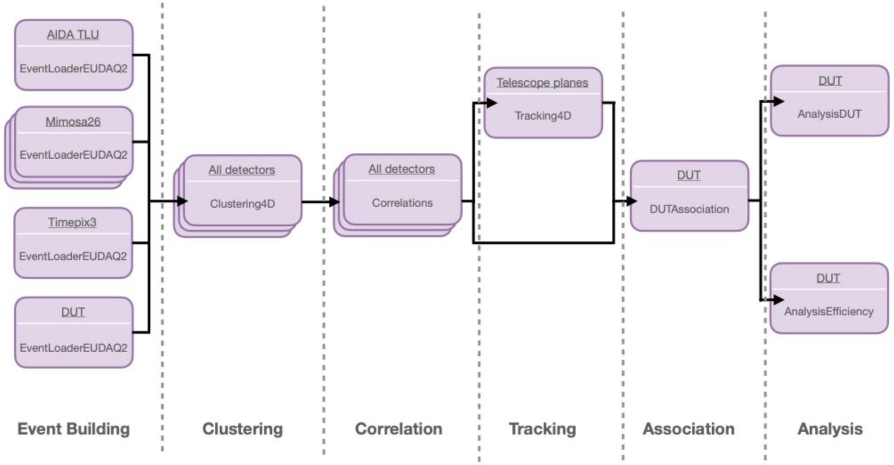
Mailing list

https://e-groups.cern.ch/e-groups/Egroup.do?egroupId=10262858

Corryvreckan test-beam analysis framework

Reconstruction and analysis software for test-beam data

- Highly flexible/configurable by using separate modules for each reconstruction/analysis step



- Wide user base e.g.

  CLICdp, ALICE ITS3, ATLAS ITk,
  LHCb Ib/II, Mu3e, etc.

Corryvreckan

2021 JINST 16 P03008

- Visit the website for the manual, tutorials and more

  https://cern.ch/corryvreckan

- Check out the repository

  https://gitlab.cern.ch/corryvreckan/corryvreckan

- Join the discussion in the forum

  https://corryvreckan-forum.web.cern.ch/

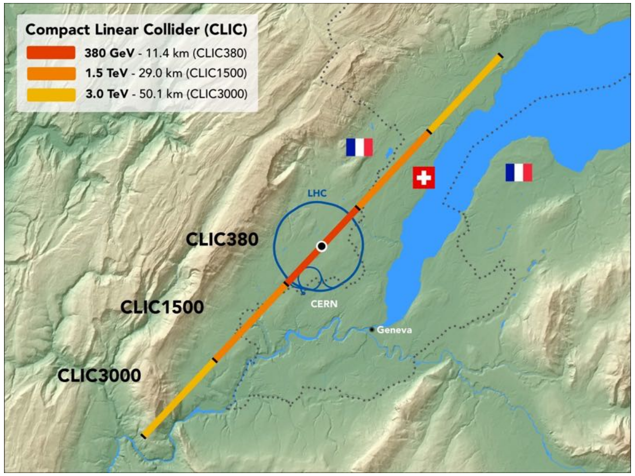
- Contact us

  corryvreckan.info@cern.ch

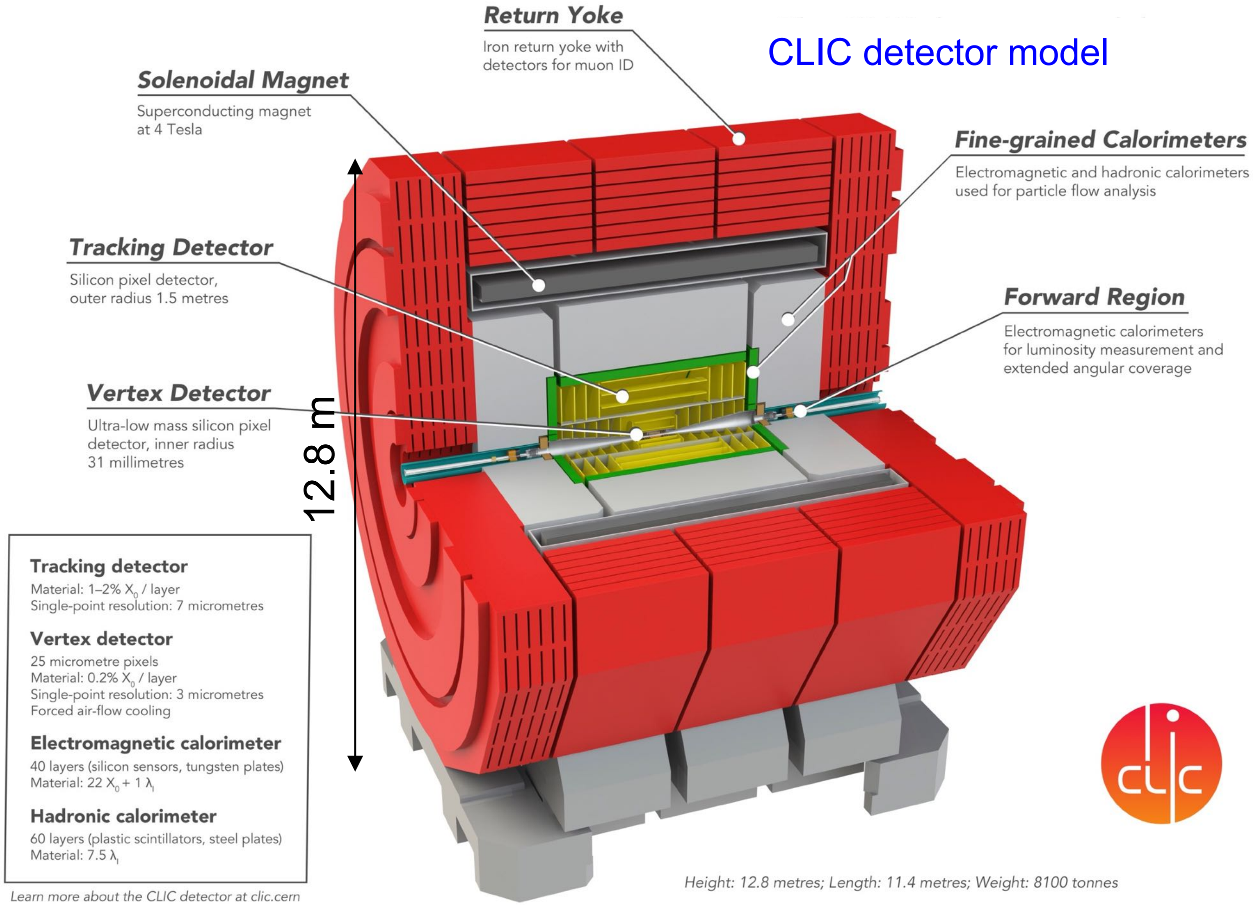
CLIC accelerator and detector

- CLIC (Compact LInear Collider):
  linear e^+e^- collider concept for post HL-LHC phase
- $\sqrt{s}$ from few hundred GeV up to 3 TeV
  (two-beam acceleration with ~100 MV/m)
- Precision and discovery physics at the TeV scale
- Detector and physics studies within the CLICdp collaboration of 30 institutes

Staged CLIC implementation



CLIC detector model



Tracking detector
Material: 1–2% X_0 / layer
Single-point resolution: 7 micrometres

Vertex detector
25 micrometre pixels
Material: 0.2% X_0 / layer
Single-point resolution: 3 micrometres
Forced air-flow cooling

Electromagnetic calorimeter
40 layers (silicon sensors, tungsten plates)
Material: 22 X_0 + 1 λ_I

Hadronic calorimeter
60 layers (plastic scintillators, steel plates)
Material: 7.5 λ_I

Learn more about the CLIC detector at clic.cern

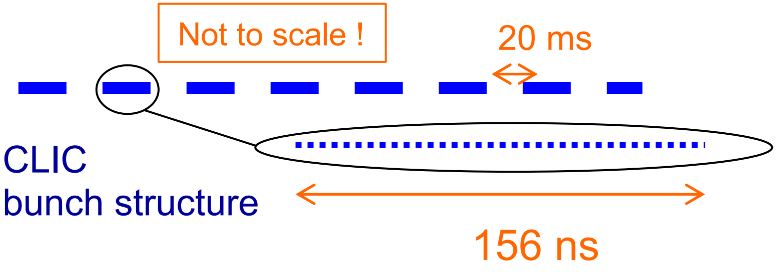
Height: 12.8 metres; Length: 11.4 metres; Weight: 8100 tonnes

CLICdp collaboration institutes

Experimental conditions at CLIC

- CLIC operates with bunch trains, 50 Hz repetition rate

→ Low duty cycle
→ Trigger-less readout between trains
→ Allows for power-pulsed operation of detector, to reduce average power consumption

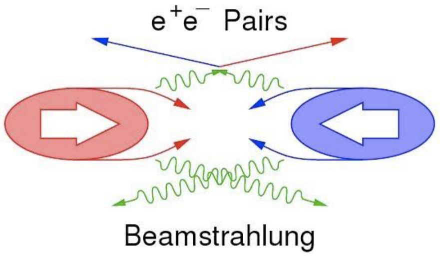


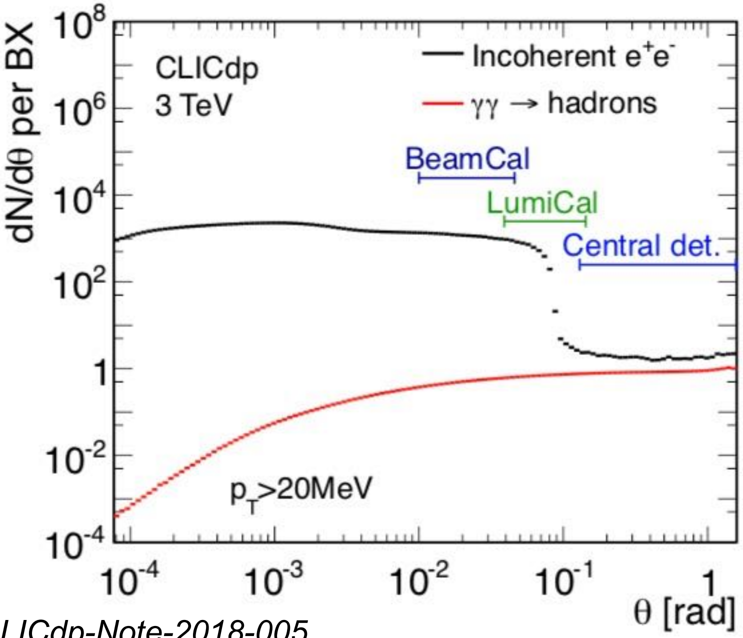
CLIC
bunch structure

- Collisions within 156 ns bunch trains
- High E-fields lead to Beamstrahlung

→ High rates of beam-induced background particles
→ Drives detector design (layout, granularity, timing)

Very small bunches:
40 nm (x) x 1 nm (y) x 44 µm (z)
(at 3 TeV)





CLICdp-Note-2018-005

Main backgrounds in detector

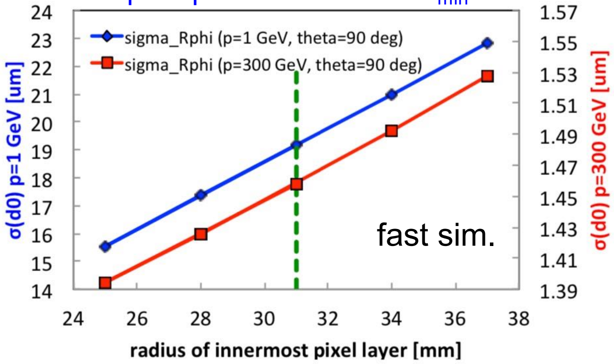
- **Incoherent e+e- pairs**
  - 19k particles / bunch train at 3 TeV
  - Constrains beam pipe radius, granularity
- γ γ →hadrons events
  - 17k particles / bunch train at 3 TeV
  - Constrains granularity, layout, impacts physics

High instantaneous hit rates (up to 6 GHz/cm²), however: very low readout rate (50 Hz)

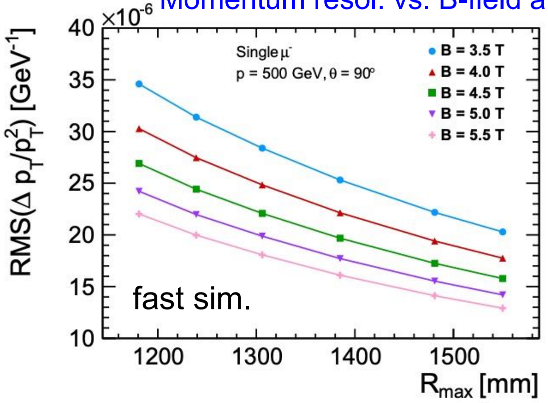
Detector design optimisation

- Study impact of technology parameters (pixel size, material budget) on detector performance
- Optimization of detector geometry (# layers, placement) for given technology assumptions
- Using fast simulations (LiC detector toy) and Geant-4 based full detector simulations including beam-induced backgrounds
- Main benchmark parameters: impact-parameter and momentum resolution, flavor-tagging performance, reconstruction efficiency

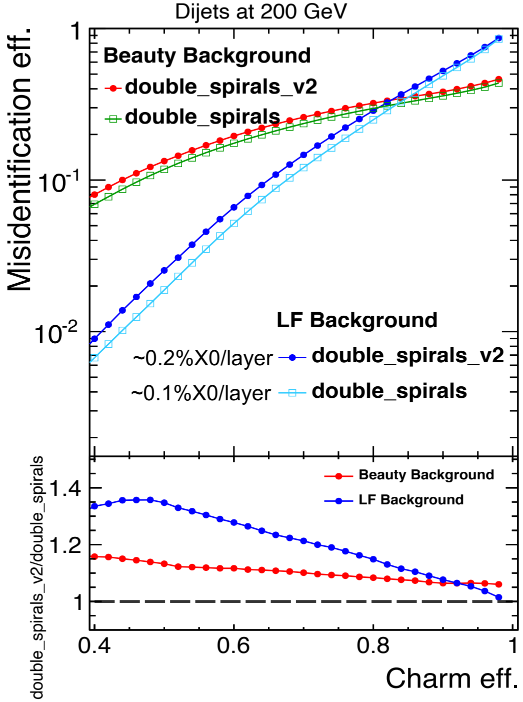
Impact-param. resol. vs. R_{min}



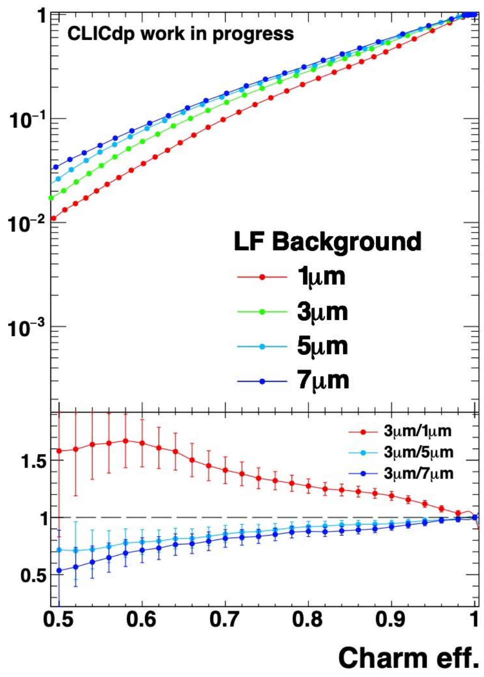
Momentum resol. vs. B-field and R_{max}



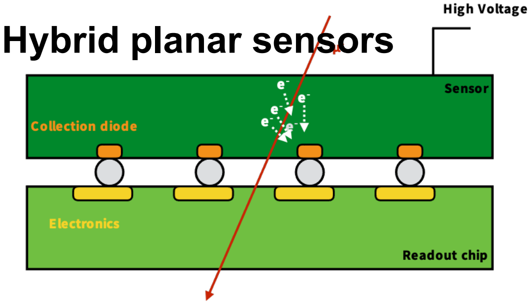
Flavor tagging vs. material budget

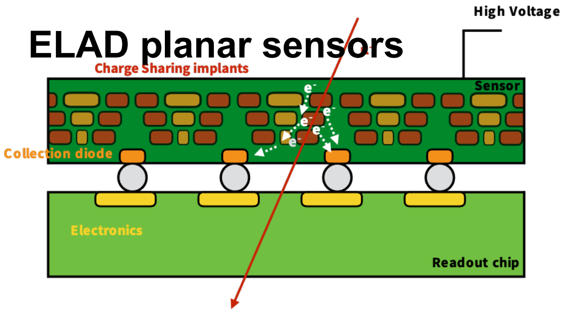


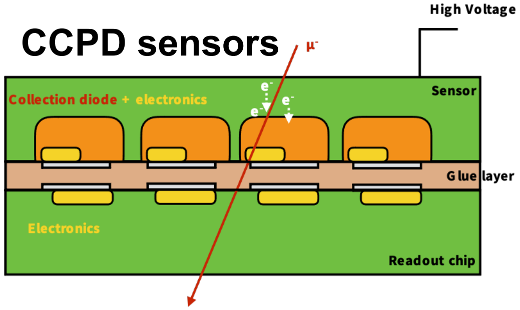
Flavor tagging vs. resolution



Sensor and readout R&D

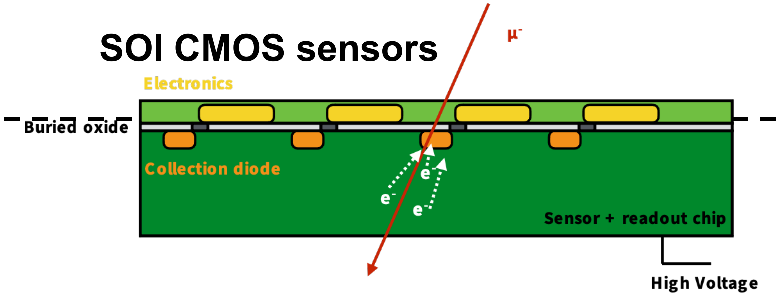

Hybrid planar sensors


ELAD planar sensors


CCPD sensors

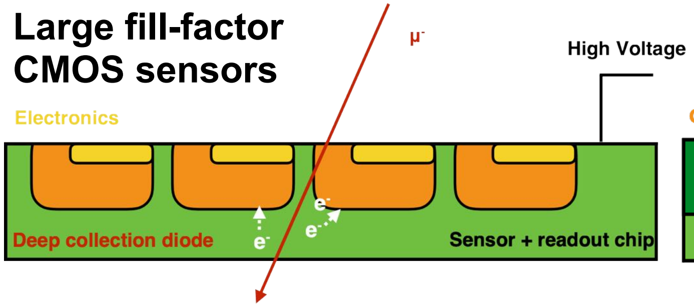
Hybrid detectors:

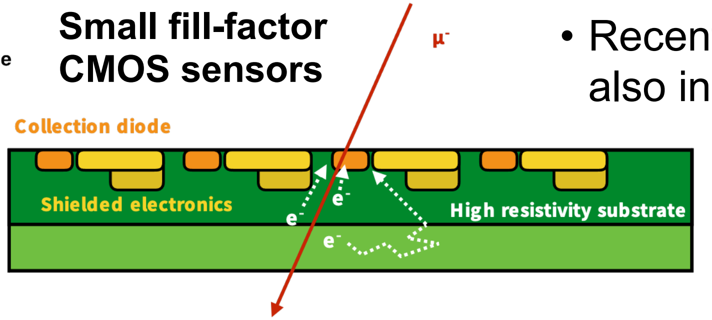
- Factorise r/o and sensor R&D
- Smallest feature-size ASICs
- Advanced sensor concepts
- Small pixels, highest performance → for inner layers


SOI CMOS sensors

Monolithic CMOS sensors:

- Lowest material budget
- Medium feature-size
- Simplified construction
  → for large-area tracker
- Recent developments target also inner layers

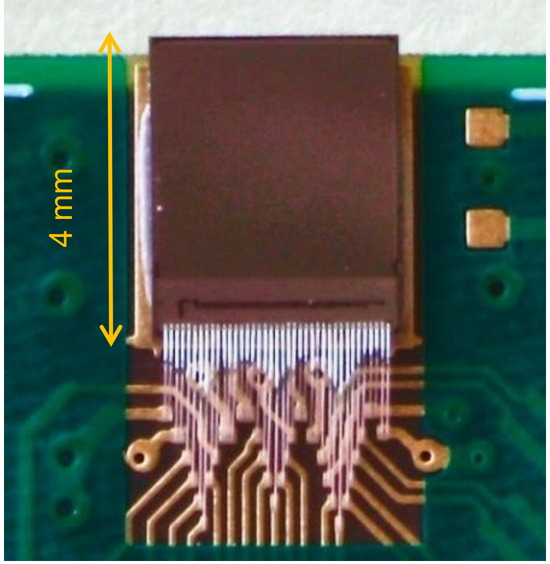

Large fill-factor CMOS sensors


Small fill-factor CMOS sensors

CLICpix2 r/o ASIC

- CLICpix2 in same 65 nm process as CLICpix:
  - Increased matrix size to 128 × 128 pixels
  - Longer counters for charge (5-bit) and timing (8-bit) measurements
  - Improved noise isolation and removal of cross-talk issue observed in first CLICpix
  - More sophisticated I/O with parallel column readout and 8/10 bit encoding
  - Integrated test pulse DACs and band gap

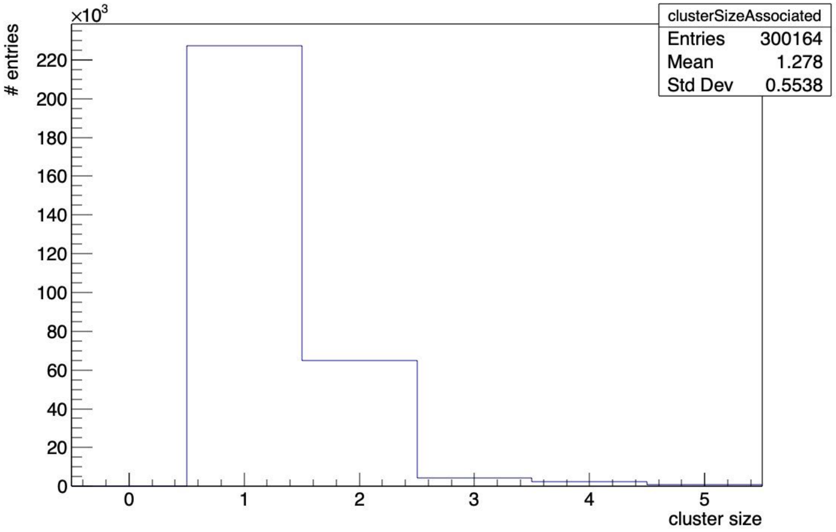
CLICpix2

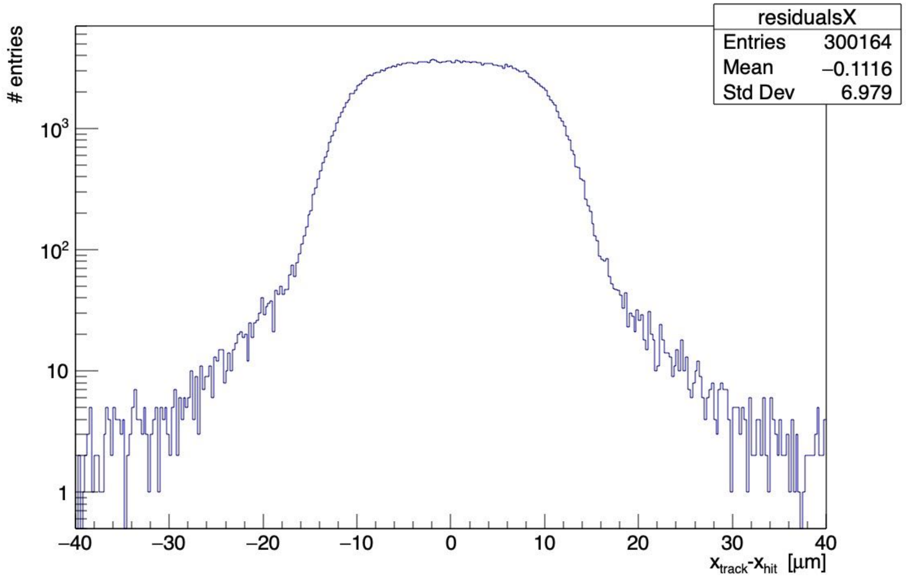


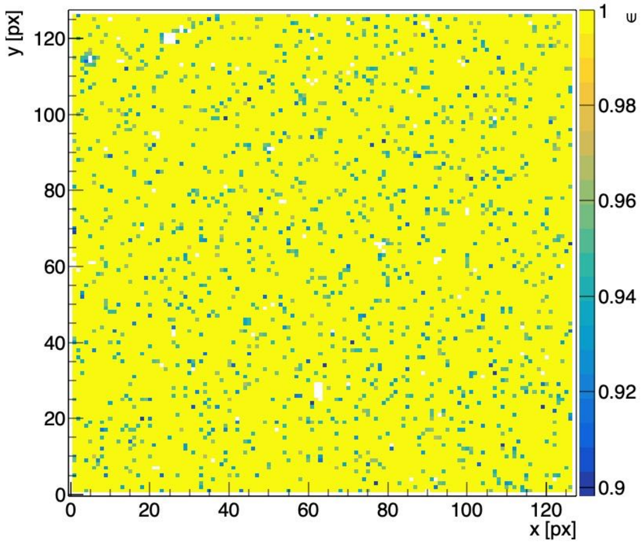
CLICpix2 analog F/E specifications

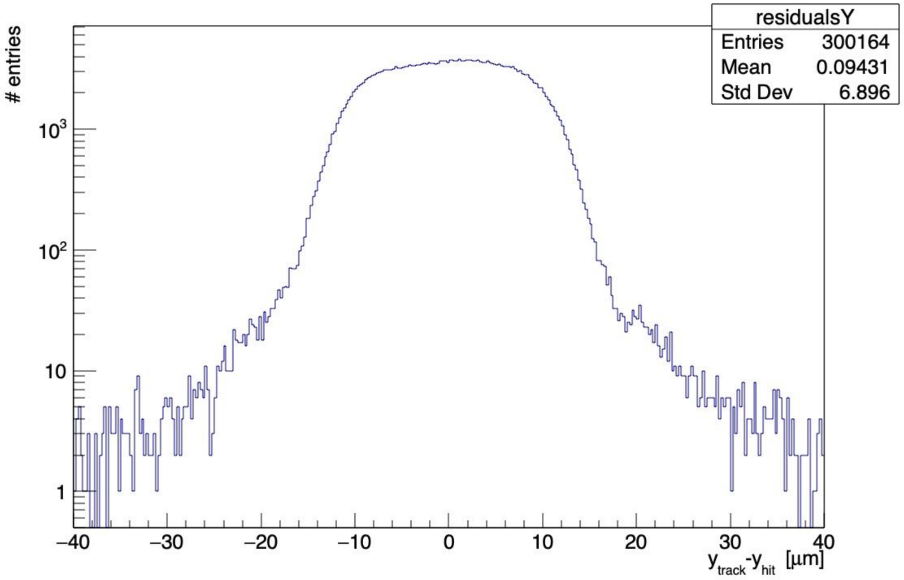
Parameter	Value
Power dissipation	≤ 12 μW
Area	≤ 12.5x25 μm^2
Input charge, Q_{in}	nominal 4 ke-, max. 40 ke-
Minimum threshold, $Q_{th,min}$	≤ 600 e-
Equivalent input-referred noise, $Q_{n,in}$	≤ 70 e-
ToT dynamic range	≥ 40 ke-
ToA accuracy	≤ 10 ns
Total ionizing dose (for 10 yr)	1 Mrad
Input charge types	e-, h+
Testability	in-pixel test pulse (i.e. Q_{test}) injection

CLICpix2 50-um test-beam results


Size distribution of associated clusters


Residual in X


CLICpix2_973_1_E1 Chip efficiency map


Residual in Y

Sensor bias voltage -60V, device without guard ring

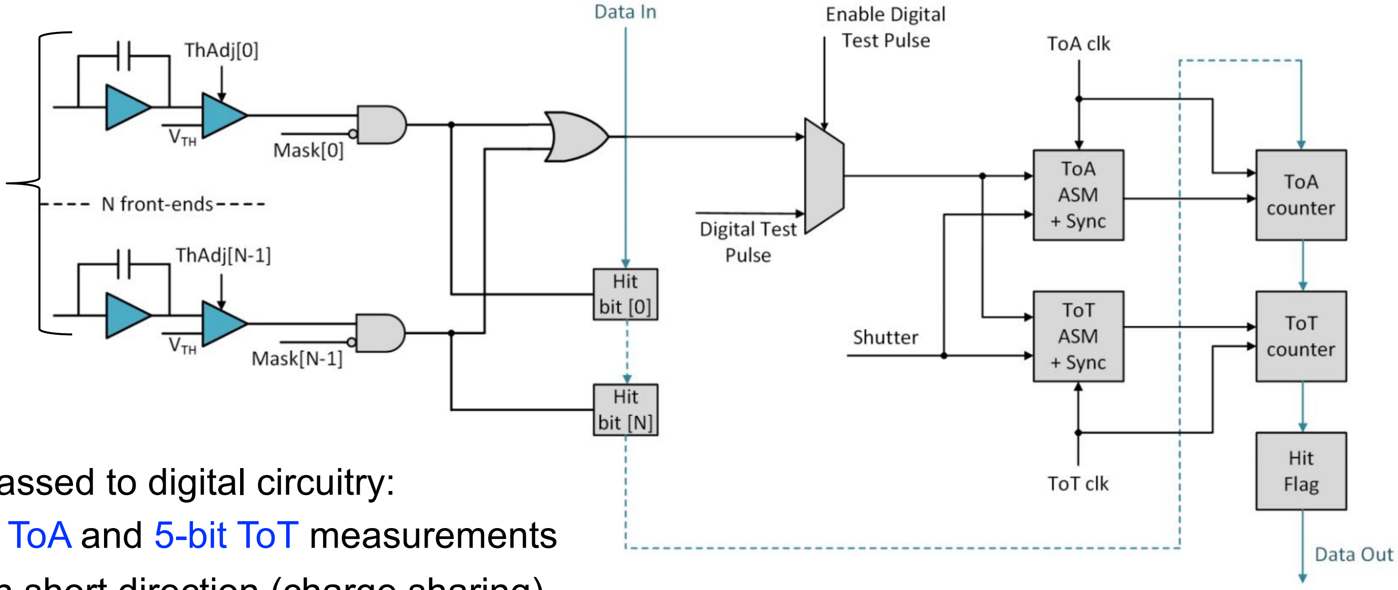
CLICTD monolithic HR-CMOS tracker chip

Good performance of studied 180 nm HR-CMOS technology with respect to requirements of CLIC tracker
→ Technology used for ongoing design of a fully integrated chip for the CLIC tracker

CLIC Tracker Detector (CLICTD) – monolithic HR-CMOS sensor with 30 μm x 300 μm pixels

Segmented macro-pixel structures to maintain advantages of small collection diode (prompt and fully efficient charge collection) while reducing digital logic:

Discriminator output of
8 collection diodes
combined in logical OR



Output of logical OR passed to digital circuitry:

- Simultaneous 8-bit ToA and 5-bit ToT measurements
- Expect σ_{SP}~7 μm in short direction (charge sharing)
- Hit bit pattern → maintain good resolution also in long direction
- 100 MHz clock to achieve 10 ns time binning