ATLAS L1Calo Phase2 Upgrade

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(on behalf of ATLAS/TDAQ/L1Calo)
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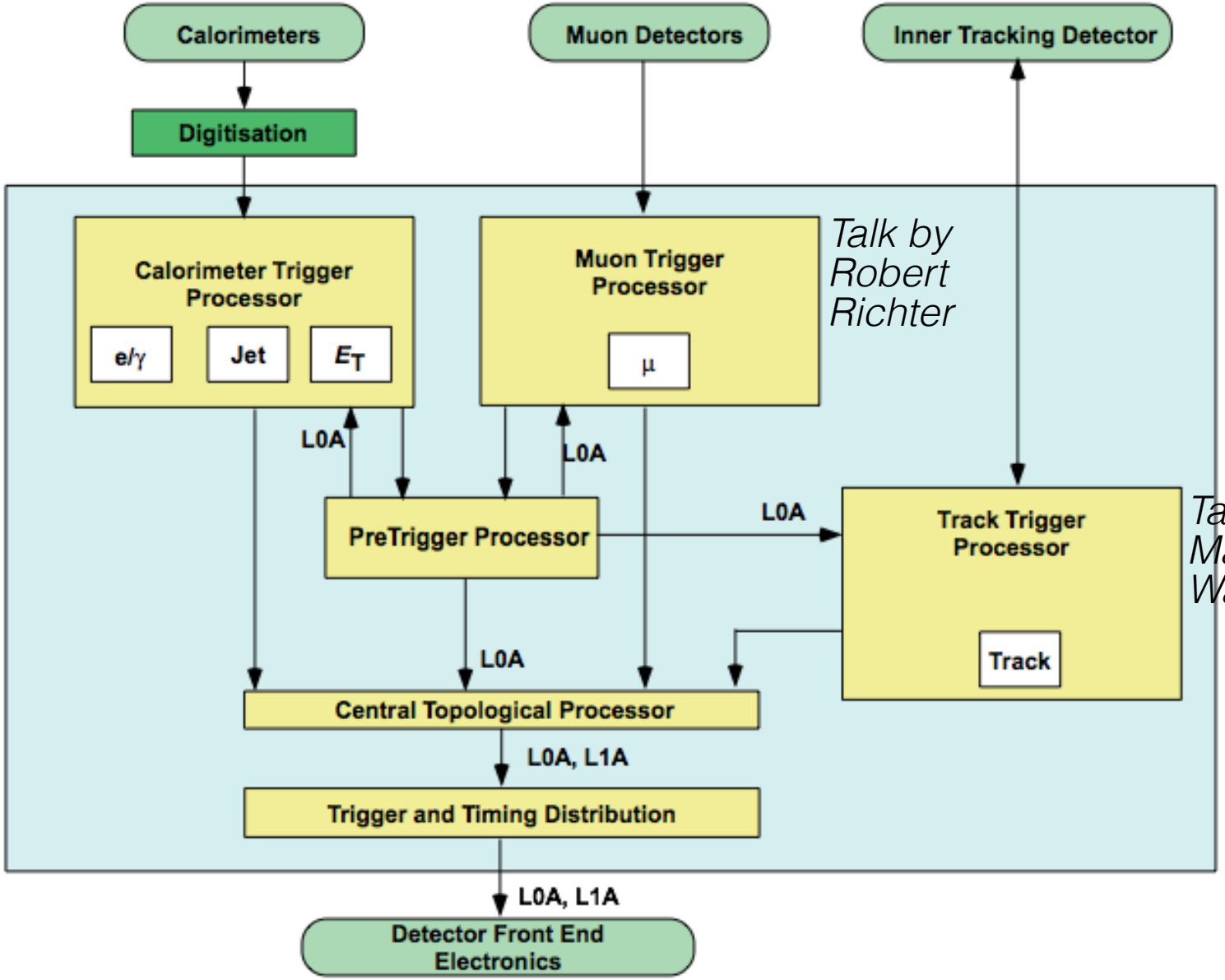
- Phase 2 Overview: L0 and L1
- Possible L0/L1Calo architecture
  - Links, algorithms, hardware, R&D

Scenarios for Level-1 in Phase 2

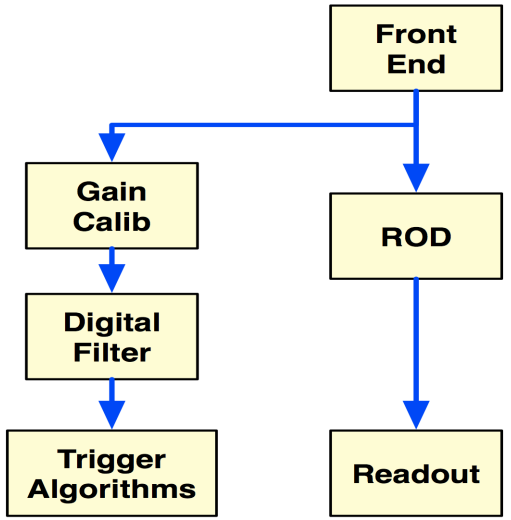
- ATLAS constraints
  - Hard to access some muon chambers even in a long shutdown
    - Some front end electronics may be impossible to replace
    - May have to live with maximum latency of 3.2μs
- Low latency scenario
  - Level-1 upgrade limited to 3.2μs
  - Not enough for level-1 track trigger
- Two stage L0/L1 scenario (preferred)
  - Level-0 stage for calo/muon triggers within 3.2μs
    - Send regions of interest to seed readout of regional track trigger
    - Ideally run at up to 500 kHz (though legacy systems may limit this)
  - Second stage level-1 trigger including calo/muon/track
    - Asynchronous, latency up to 9.6μs or possibly much longer

Overview of Phase 2 (L0/L1 scenario)

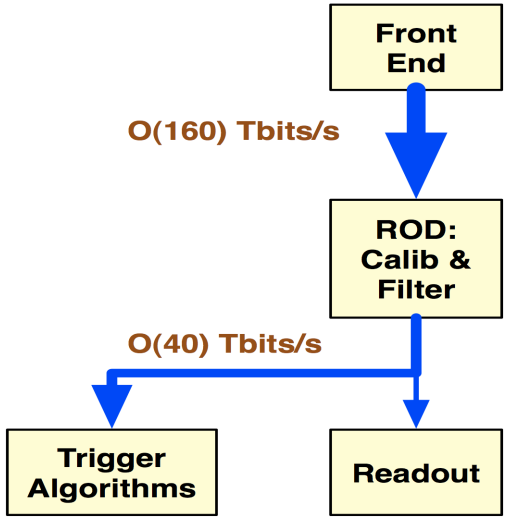


L1Calo Changes for Phase 2

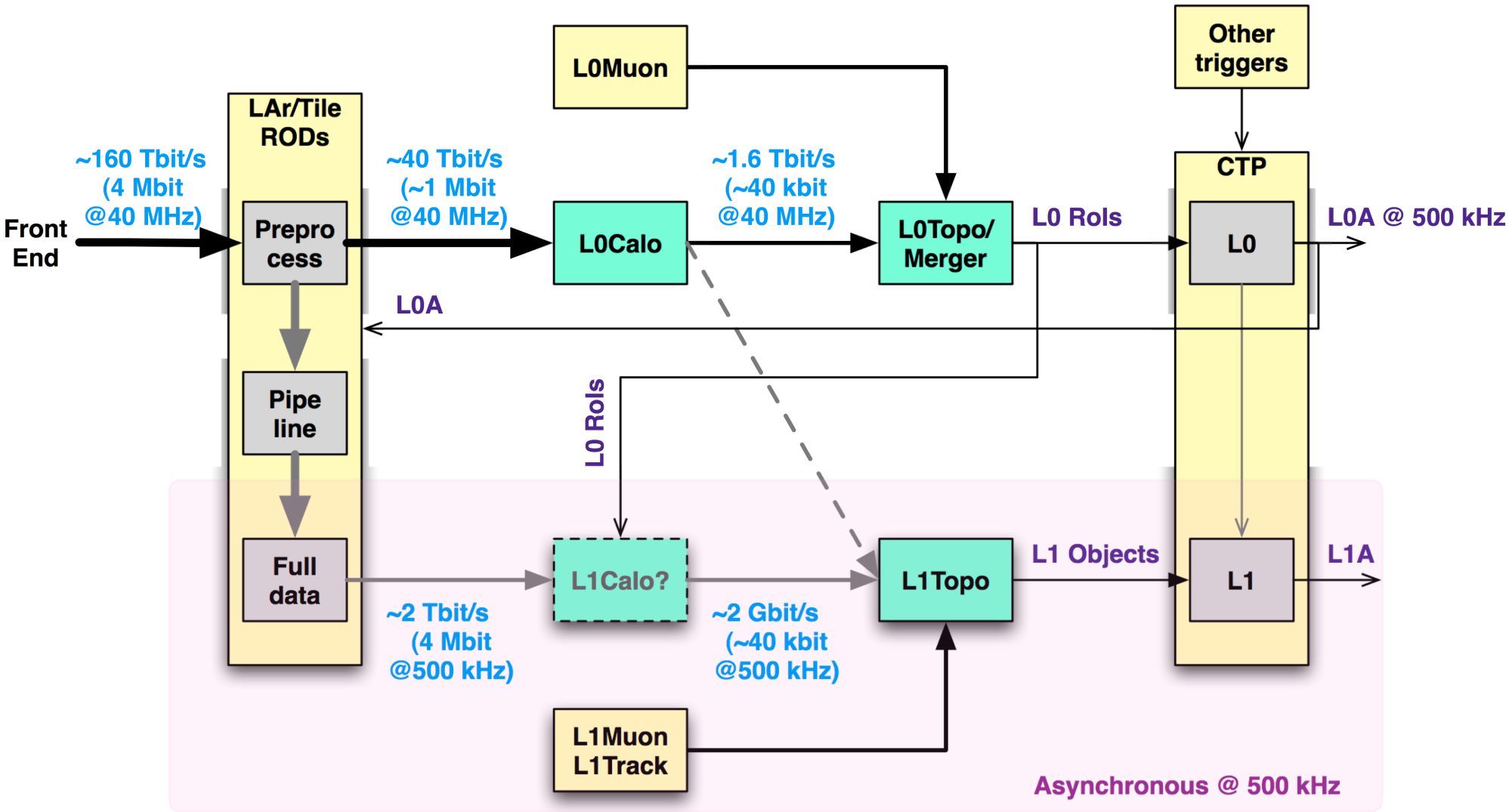
- Existing L1Calo system
  - Separate trigger & readout paths
  - 7k analogue trigger towers per BC
  - Analogue gain calibration per tower
  - Digital BCID filter per trigger tower
  - Digital trigger algorithms



- Phase 2 proposal
  - Digitise all calo cells every BC: 160 Tbits/s
  - Single readout+trigger path off detector
  - Single calibration & BCID filter per cell
  - Trigger sums formed off detector
  - Fine granularity trigger algorithms



Baseline Phase 2 L1Calo Architecture



In the low latency scenario, only the L0 blocks are possible

Phase 2 L1Calo Components

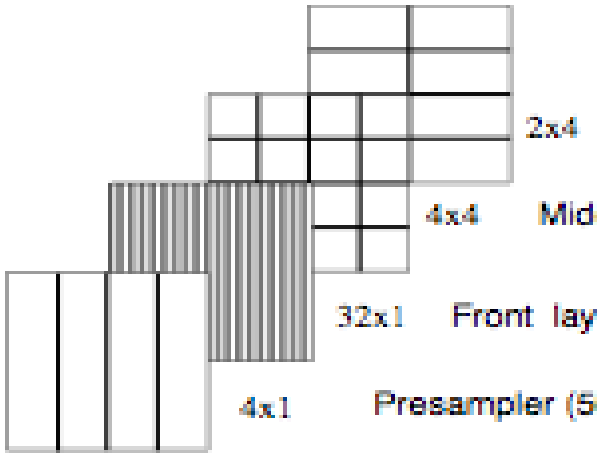
- L0Calo:
  - Find EM, Tau, Jet objects and Et sums every BC
- L0Topo:
  - Topological processor: merge L0Calo & L0Muon results
- L1Calo:
  - Asynchronous refinement of L0Calo using full calo data
    - Likely to be driven by L0 RoIs
- L1Topo:
  - Final topological processor for L1Calo, L1Muon & L1Track
- L0 & L1 CTP:
  - Final trigger decisions, interface with detectors
    - Interface with topological processors to be defined

Calo ROD – L0Calo Interface

- Calo Readout Driver (ROD) functions for L0Calo:
  - Derive calibrated Et from digitised pulses
    - No issues with analogue saturation
  - Assign Et to correct bunch crossing
  - Provide quality flags from optimal filter (pile up, etc)
  - Form sums of calorimeters cells into "mini towers"
    - Definition of mini towers (or "L0 primitives") to be defined
    - EM layer: both fine and coarse sums (for EM & Jet triggers)
  - Possibly run algorithms on cells within one ROD FPGA
    - Eg pi0 rejection using LAr EM strips
  - Transmit mini towers to L0Calo
  - Pipeline full data (for every cell) for use by L1 stage (& DAQ)

Calo ROD – L0Calo Links

- Baseline: 10 Gb/s links => 200 bits per bunch crossing
- Hadronic layer (and coarse EM sums for jet trigger):
  - One 10 Gb/s fibre link per 0.4*0.2 (or 0.2*0.4) in eta*phi
    - Can have finer eta*phi and depth granularity than now for jets
- EM layer fine granularity for EM/Tau algorithms:
  - One 10 Gb/s fibre link per 0.1*0.1 tower
    - 200 bits: more detail on eta, phi and depth
    - Concentrate bandwidth on middle layer?
      - Contains most of the energy
      - Heavily sum the strips layer

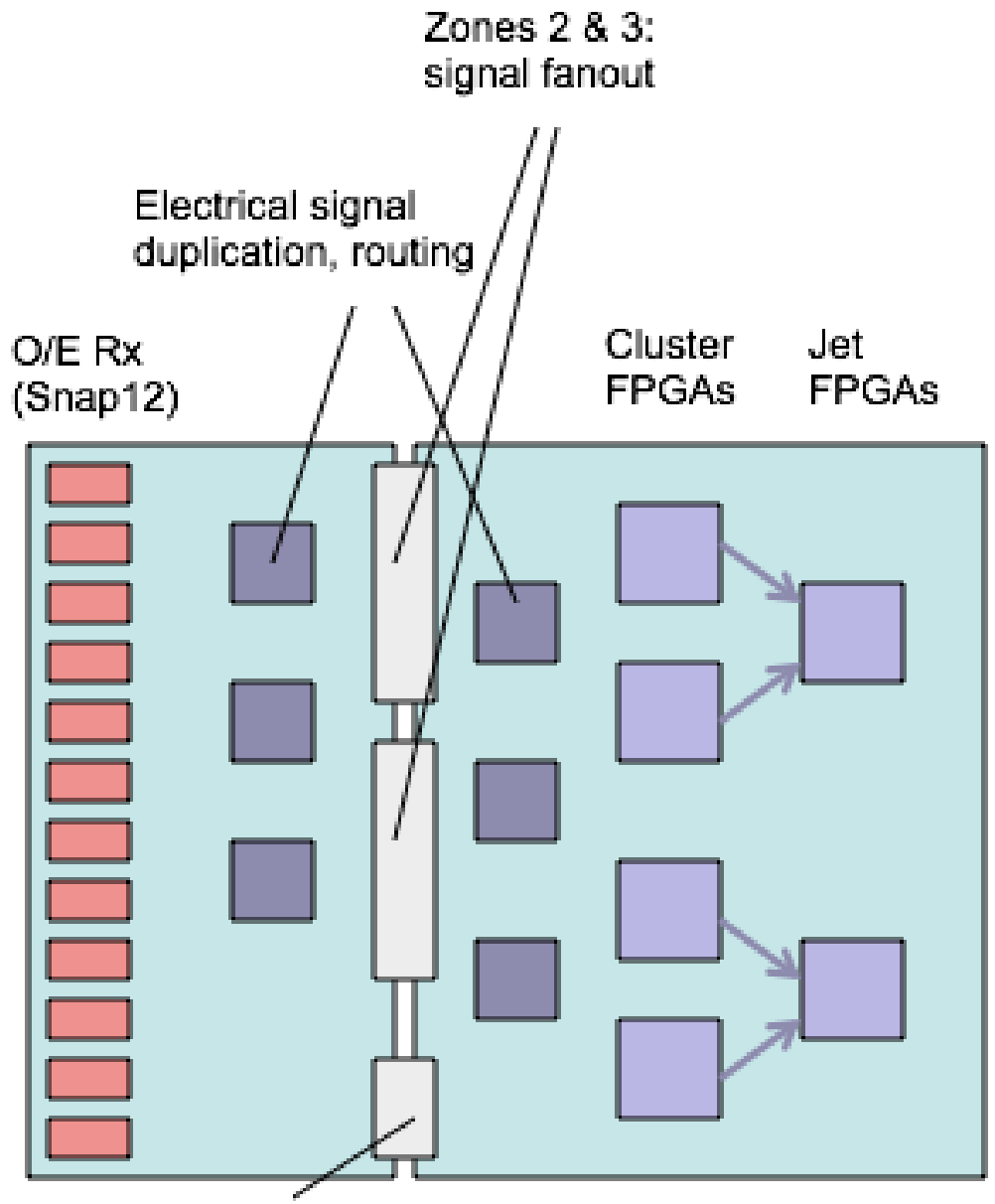


Phase 2 LOCalo Algorithms

- Sliding windows, now with finer granularity
  - Limitations will be fanout and number of inputs per FPGA
    - Expect O(50) 10 Gb/s links into Virtex 7
- Adopt L2 EM/Tau ideas
  - L2 "R core": ratio of 3*7 to 7*7 LAr middle layer cells
    - LOCalo bandwidth might require middle layer cells summed in pairs
- Investigating benefits of larger jet environment...
  - Present 0.8*0.8 eta*phi jets use 0.4*0.4 RoI maximum
    - Better to know if 0.8*0.8 area is a maximum within its environment
    - Problem: much larger fanout and more fibres per FPGA
    - Larger environment with 0.1 granularity may need separate jet system
    - Needs some simulation work...

Possible LOCalo Implementation

- "Strawman" module
  - Covers 0.4*1.6 eta*phi
  - Both EM/Tau and Jet
    - Resolve overlaps locally
  - Fully custom backplane
    - Fanout to adjacent slots
    - Passive optical fanout for adjacent crates in phi
  - Four full ATCA crates
    - ETSI 16 slot 23" crates?



Level-1 Calo Processor

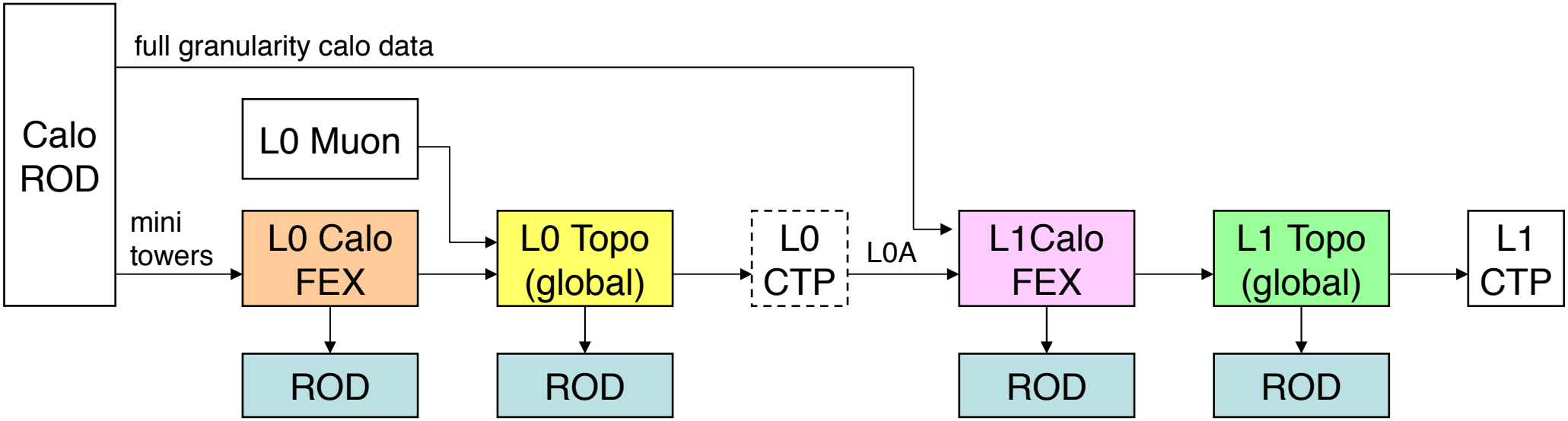
- Refinement of level-0 calo possible at the level-1 stage
  - Can be seeded by level-0 regions of interest
  - Gets full granularity calorimeter data for L0 events
- Long latency and asynchronous processing
  - Can consider using CPUs or graphics processors
  - Could use event based multiplexing (CMS style)
  - Variable processing time per event (similar to present L2)
  - But need to output events in the correct order
    - This is probably a detector requirement
    - It may also be required between each L1 functional block

Topological Processors: L0 and L1

- Level-0 topological processor
  - Evolution of phase 1 topological processor: see phase 1 talk
  - Similar set of algorithms as phase 1
    - But benefitting from greater precision in eta, phi and Et
    - Scope for additional algorithms…
- Level-1 topological processor
  - Combine calo, muon and track objects found at L1
    - Track/shower matching, combined muon tracks
  - Long latency and asynchronous processing: could use CPUs?
  - Design to use either L0 or L1 calo and muon inputs?

R&D Work

- Already designing ATCA demonstrators for phase 1
- More demonstrators being planned
  - Study PCB simulation: really understand high speed links
  - Optical fanout and patching
- Medium term: build up "slice" of full phase 2 system



Summary

- "Straw man" design emerging - at least for L0, but...
  - Needs more work on the details and input from simulation
  - Need to define algorithms
  - Need to estimate latency of L0Calo+L0Topo
- Evolutionary approach
  - Use phase 1 topo processor as L0Topo prototype
- Started thinking about asynchronous L1 stage
- ATLAS L1 Technical Proposal now being written
- R&D program emerging for phase 2
  - Technical demonstrators followed by prototype "slice"
  - LAr & Tile planning phase 2 prototypes to be used in ATLAS
    - Hope to feed outputs from these into L0Calo prototypes...