ACES 2011

MicroTCA in CMS

E. Hazen, *Boston University*
for the CMS collaboration

MicroTCA in CMS

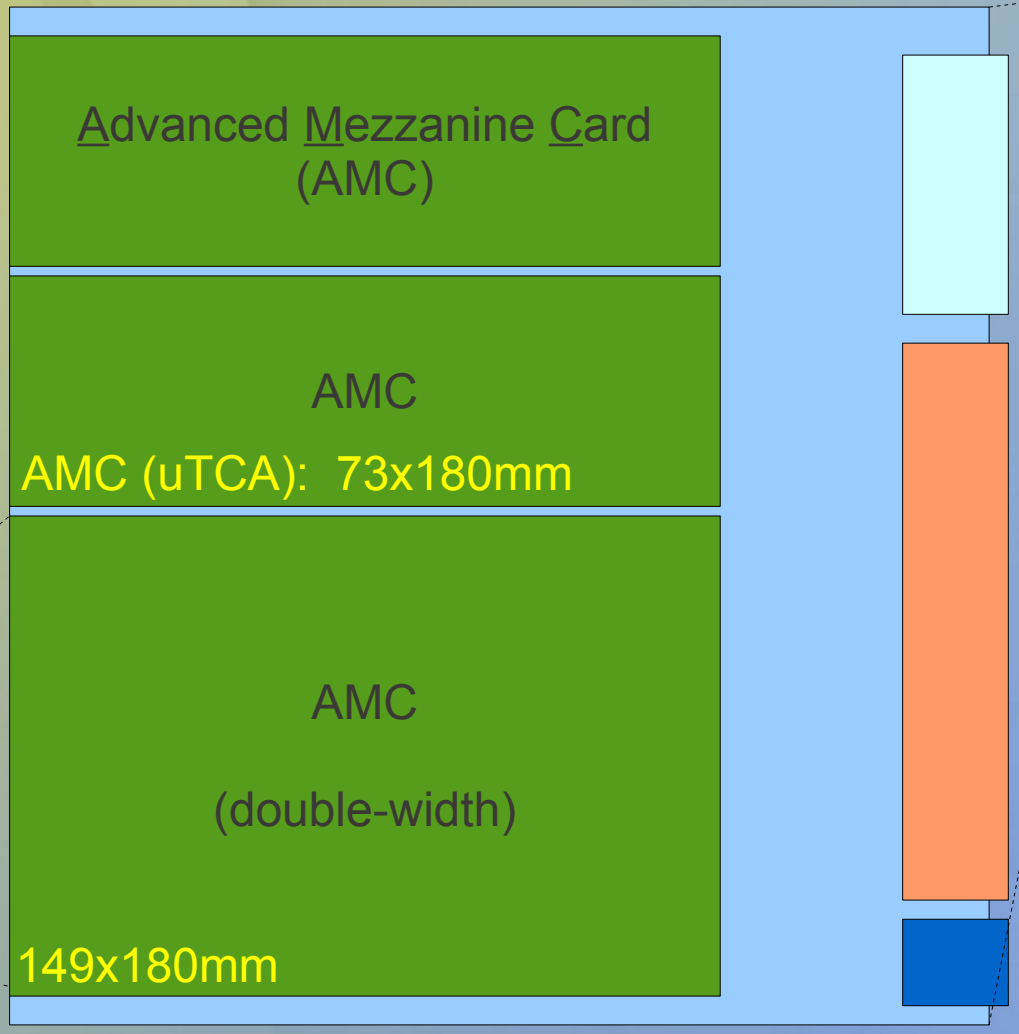
- What is MicroTCA?
- Common MicroTCA platform for CMS
- Hardware aspects
- Software aspects
- Summary and plans

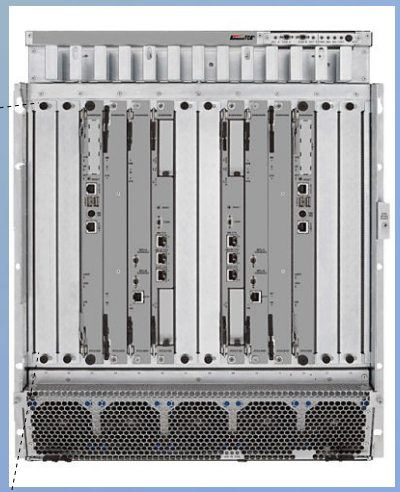
AdvancedTCA and MicroTCA

ATCA
- 8U Carrier
- AMC mezzanines

uTCA
- Small crate
- AMC mezzanines
  (plug to backplane)

ATCA Module: 8U x 280mm





Zone 2
- Clocks
- Fabric
  - up to 10 Gb/s
  - serial links

Zone 1
- Power
- Management

ATCA and uTCA Features

- Card management functions using IPMB (I2C) bus
- Management power (always on) and payload power (switched)
- High-speed (up to 10Gb/s) backplane “fabric” ports (up to 21 per module)
- Flexible (i.e. unspecified) backplane topology
- Wide industry support (should evolve to low cost)

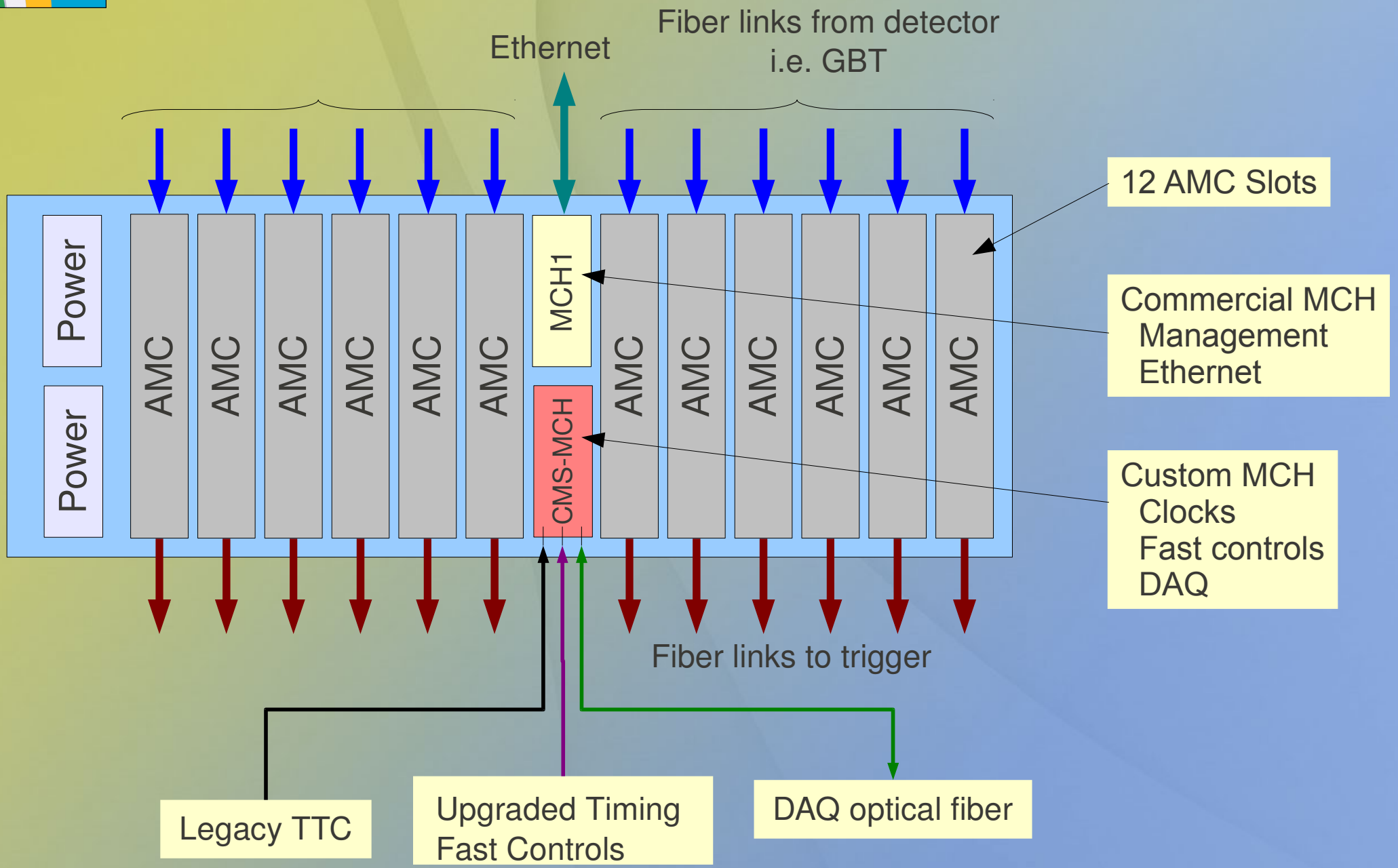
CMS MicroTCA Common Platform

in principle all CMS MicroTCA crates will use common...

- Hardware:
  - 12 Slot redundant crate with dual-star backplane
  - 12 AMC modules (double-width, full height)
  - 1 Commercial MCH for Management / Ethernet
  - 1 Custom MCH for Clock/Timing/DAQ
- Firmware / Software:
  - IPMI use for configuration control / monitoring
  - Ethernet protocol for control / local DAQ
    - Replacement for CMS “HAL” VME library
    - UDP / TCP yet to be decided

Hardware Aspects

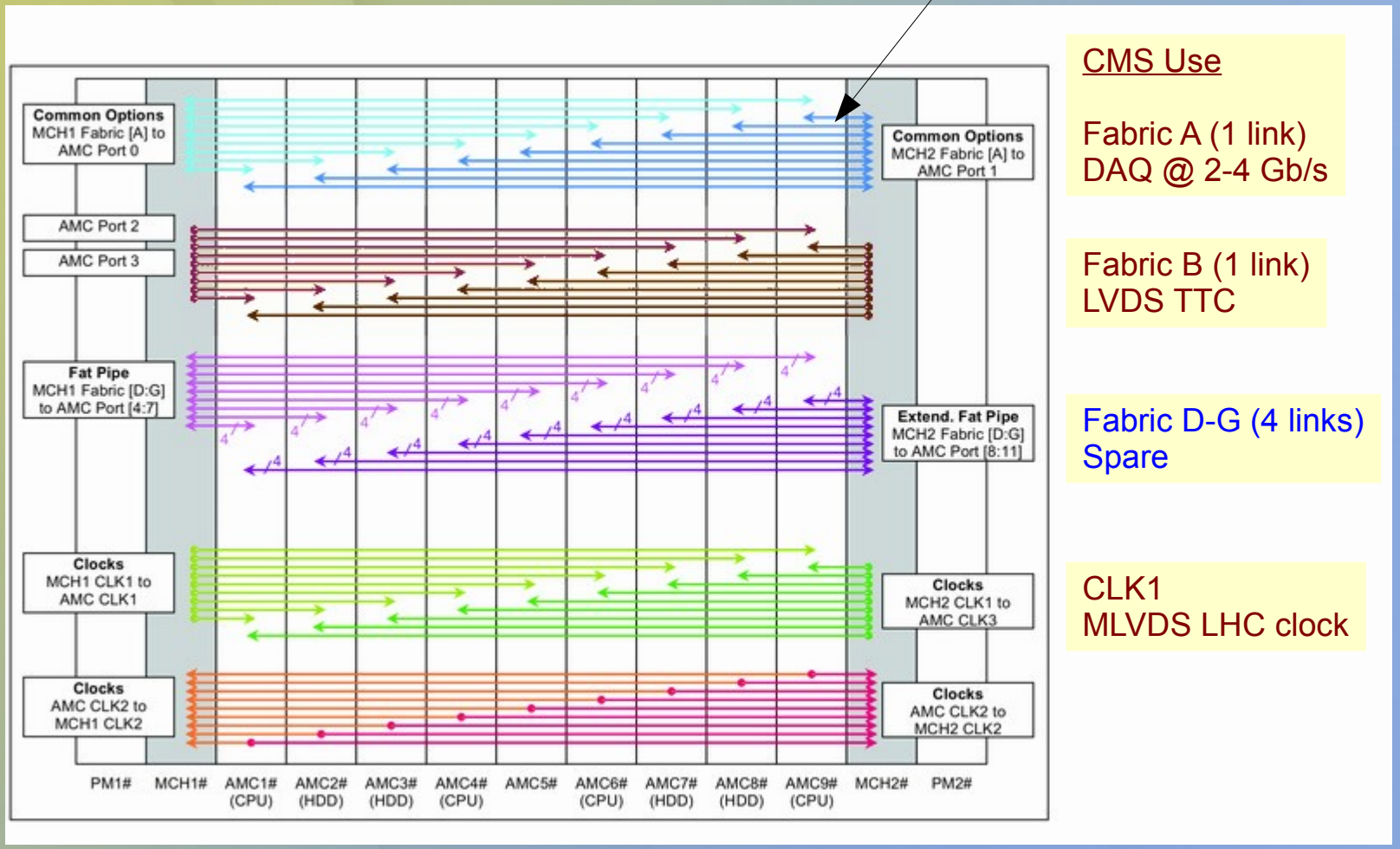
CMS uTCA Readout Crate (i.e. HCAL)



µTCA Dual-Star Backplane

Note: Interconnections can be customized by the backplane manufacturer inexpensively.

Bi-directional serial (up to 10Gb/sec) point-to-point links from each AMC to MCH (redundant links to each MCH)



Fabric A (1 link)
Gigabit Ethernet

Fabric B (1 link)
Spare

Fabric D-G
Spare

CLK1
Spare

CMS Use

Fabric A (1 link)
DAQ @ 2-4 Gb/s

Fabric B (1 link)
LVDS TTC

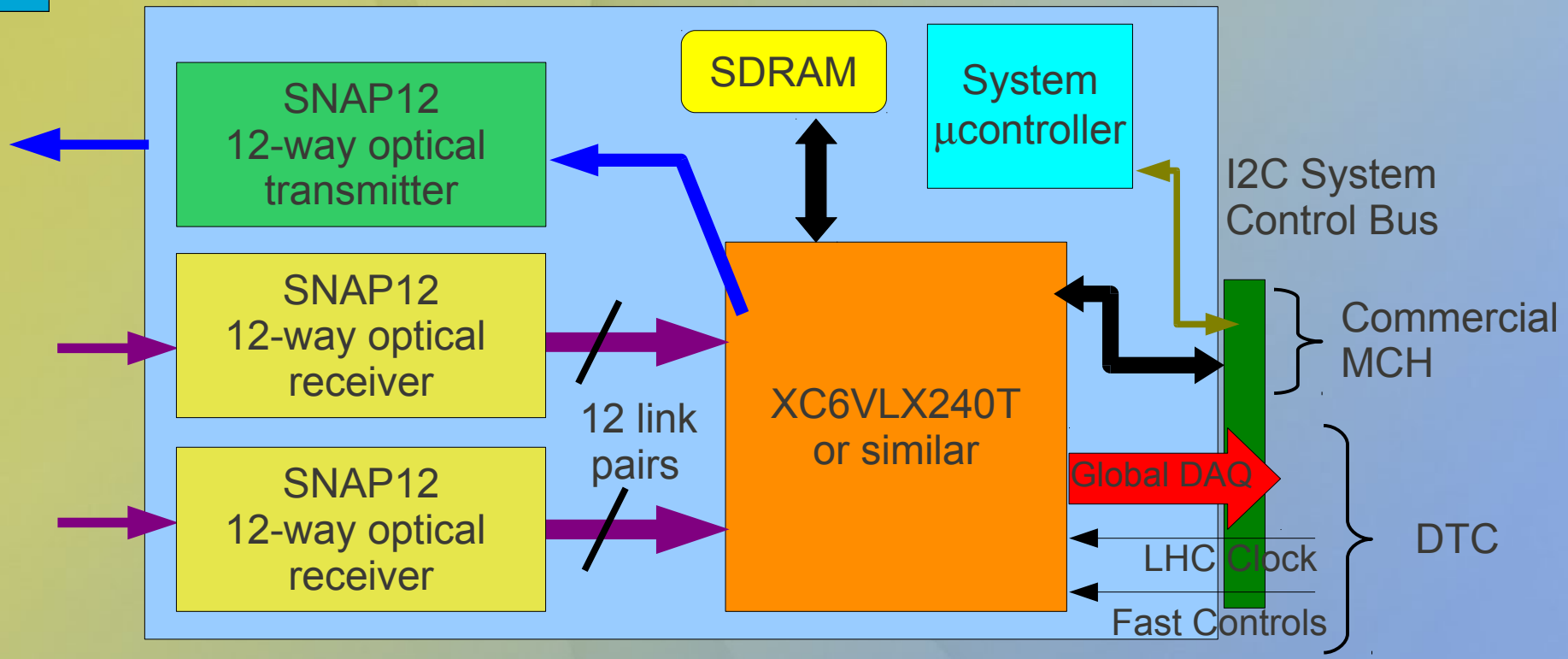
Fabric D-G (4 links)
Spare

CLK1
MLVDS LHC clock

MCH 1
Commercial /Std

MCH 2 aka “AMC13”
Custom design for CMS

Example AMC -- HCAL uHTR



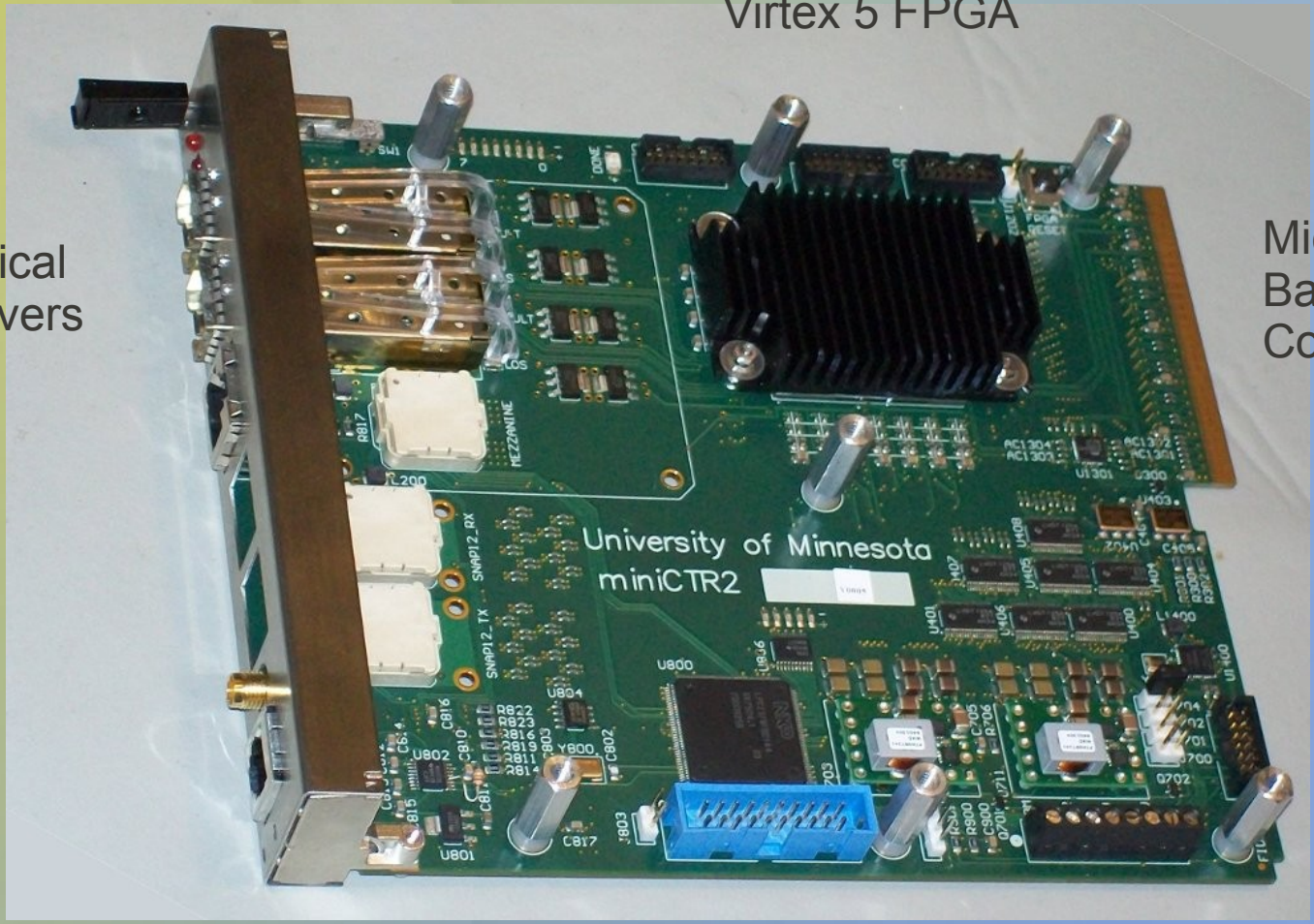
- Main features:
  - Single Virtex 6 supports 36 optical and 24 backplane SERDES
  - (DDR3) SDRAM for extended L1 pipeline storage (selective readout delay)

Prototype AMC (HCAL miniCTR2)

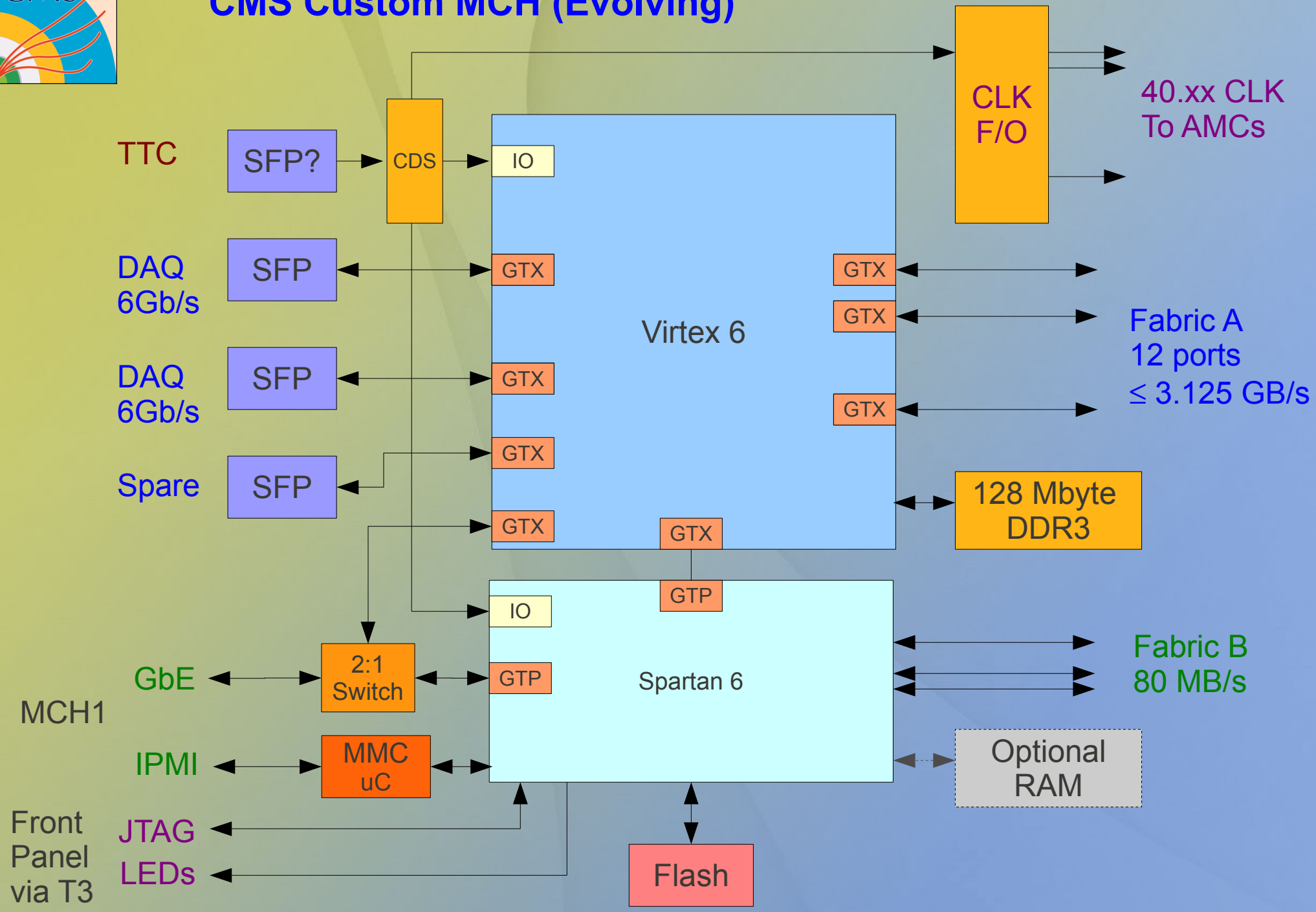
Virtex 5 FPGA

SFP Optical Transceivers

MicroTCA Backplane Connector

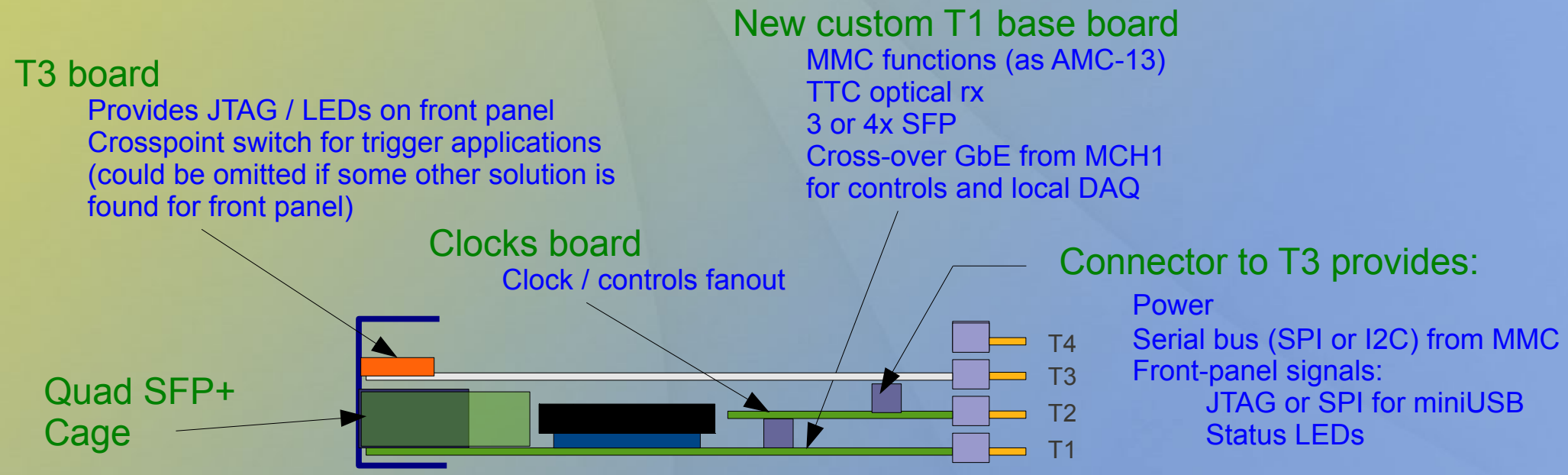


CMS Custom MCH (Evolving)



Custom MCH Board Stack

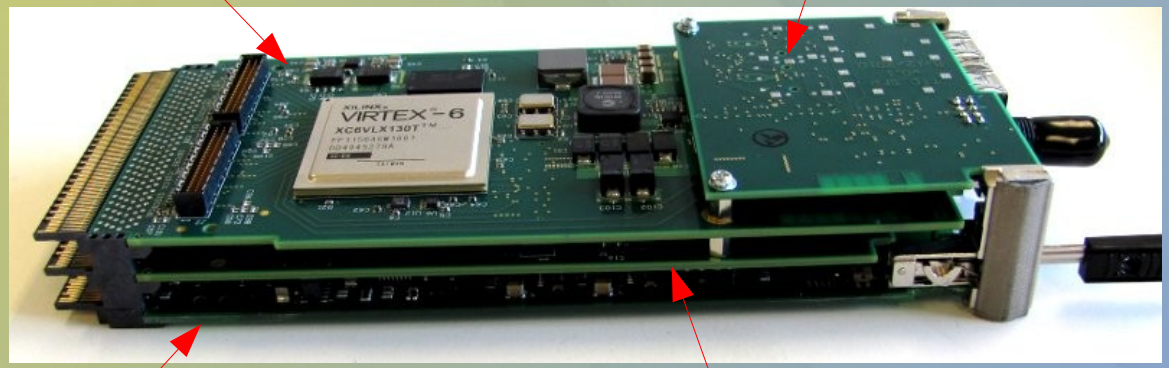
- Base configuration has only tongues 1, 2
- Base board - With optics and HS links (Fabric A)
- Clocks board - distributes LHC clock and controls
- Mezzanine connector for T3 with I2C
  - T3 has JTAG and LEDs



Initial Custom MCH Prototype

Fabric Board (DAQ)
(move from T3 to T1 in final design)

Optics Connector Board
(move to T1 in final design)



NAT-MCH Base Board
(will not be used in final design)

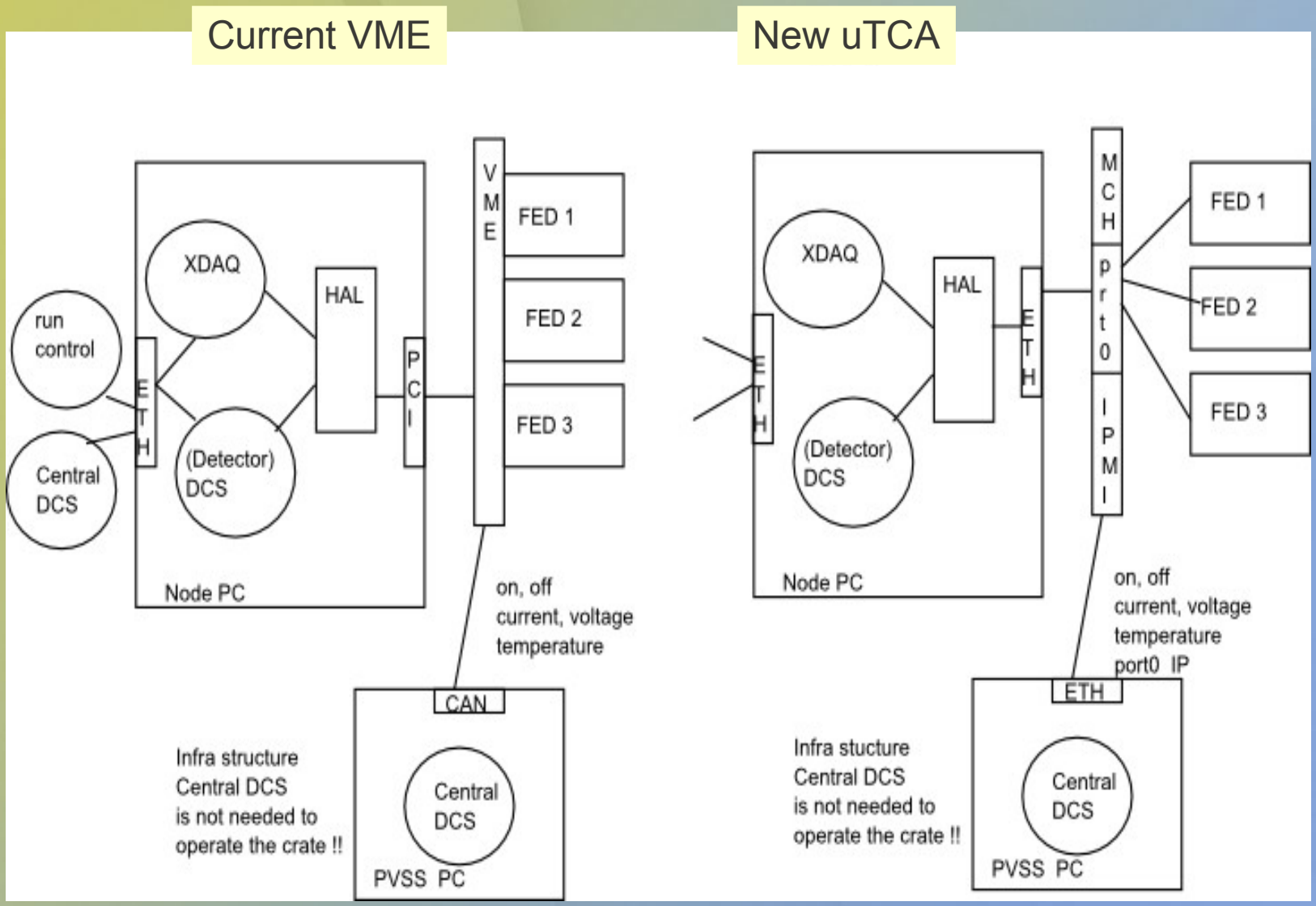
Clock / Controls Board
(smaller in final design)

Prototyped in 2010

- TTC receiver tested
- Fiber optics tested
- Backplane links tested
- Integrated in system for HCAL test beam

Software Aspects

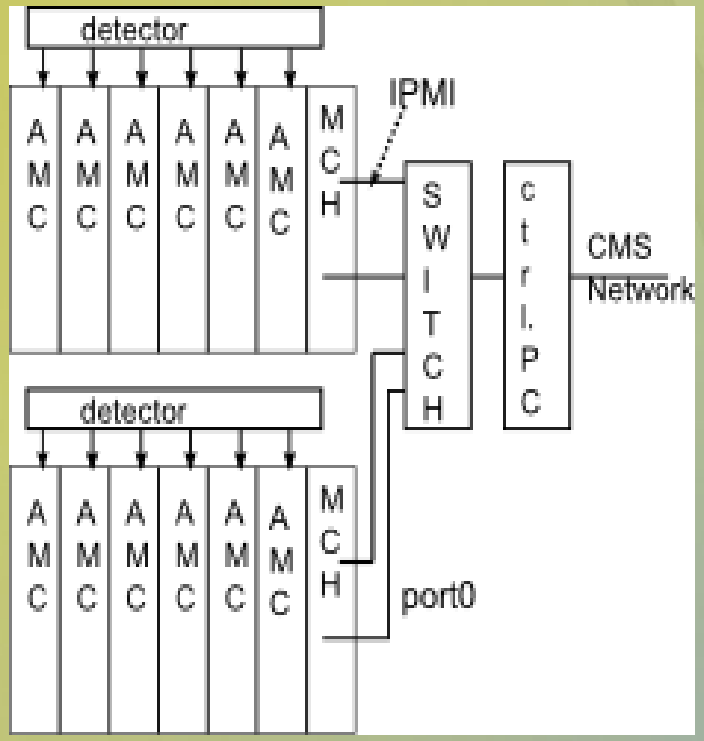
Evolution, not Revolution



Initialization Concerns

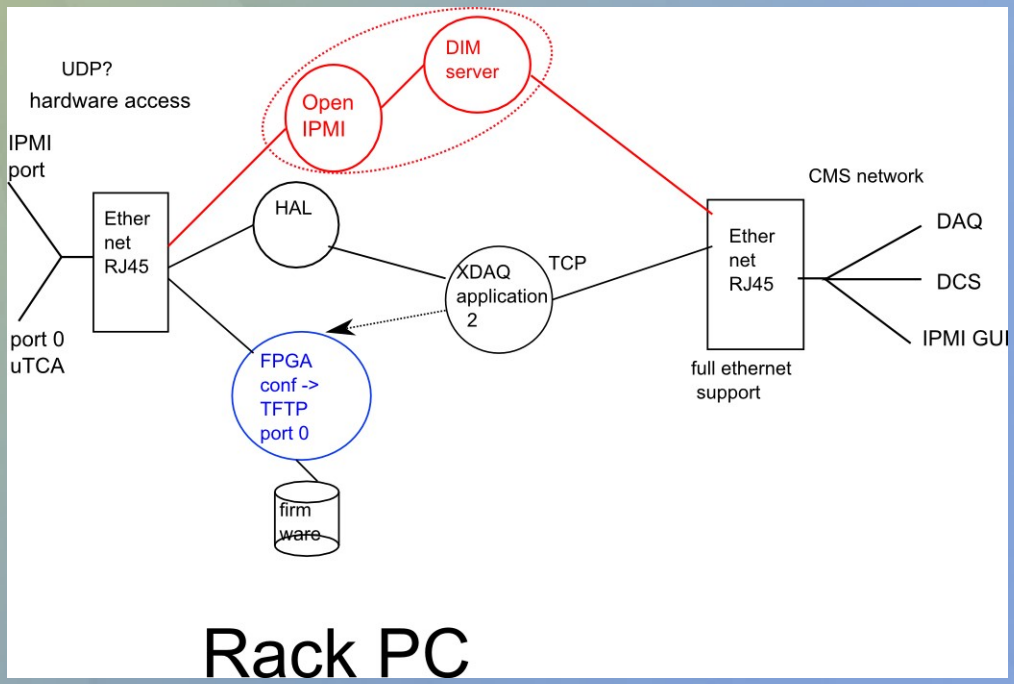
- Goal:
  - uTCA crates with AMCs should power up into an operational status without “software intervention”.
- Two regimes
  1) Commissioning, debugging:
     PVSS is not the environment for debugging.
     - Commissioning / configuration / debugging via IPMI GUI programs (provided by crate / AMC manufacturer)
     - Bulk (re) configuration : to be defined
       - Most likely scripts
  2) Operation: fully integrated into the experiment operations
     => SCADA interface
     (PVSS for logging and transfer to offline data base)
     - GUI and API should be common for all uTCA crates

One Rack PC controls a few uTCA crates



On the rack PC several processes can run (tbd) :

- DAQ application
- openIPMI to DIM server
- FPGA configuration
- Access control
  (simplify the IP interface on the AMC)



Processes and hierarchy TBD

IPMI ↔DCS, DAQ

- Minimize the DCS (PVSS) complexity
  - Monitor temperatures, voltages, currents
  - Switch on/off crates
  - Switch on/off AMC payload power
  - Alerts (set Alerts levels)
  - For test stands PVSS is not require (use IPMI GUI)
- Interface (i.e.) LHCb computer farm control
  uTCA ↔ RCMP ↔ (openIPMI)+DIM ↔ (DIM+PVSS)
  - Long term we want to remove DIM
- No direct communication between IPMI and DAQ

Common FPGA configuration scheme

- For operations only one path for : **port 0** (Ethernet)
  - No direct configuration of the FPGA. Is not needed for operations.
- Use multi configuration images in flash, with boot image that is able to program the FLASH(es)
  - Use hard coded boot logic of Xilinx and Altera.
- FLASH should be programmable by the MMC (IPMI compatible)
  - In case of corrupted image 0.
- Common development of image 0 and FLASH configuration software

Status and Plans

- Current Status
  - Crate / interconnect spec document in draft
  - Initial prototypes of MCH and AMC built (HCAL)
  - Design of full prototype MCH underway
- Plans
  - Install test crate for parasitic running in Dec 2011
  - Install “vertical slice” test system in HCAL in 2013 shutdown
  - Support other subsystems upgrade efforts