A Front End chip development for triggering with Silicon Strip Pt-modules

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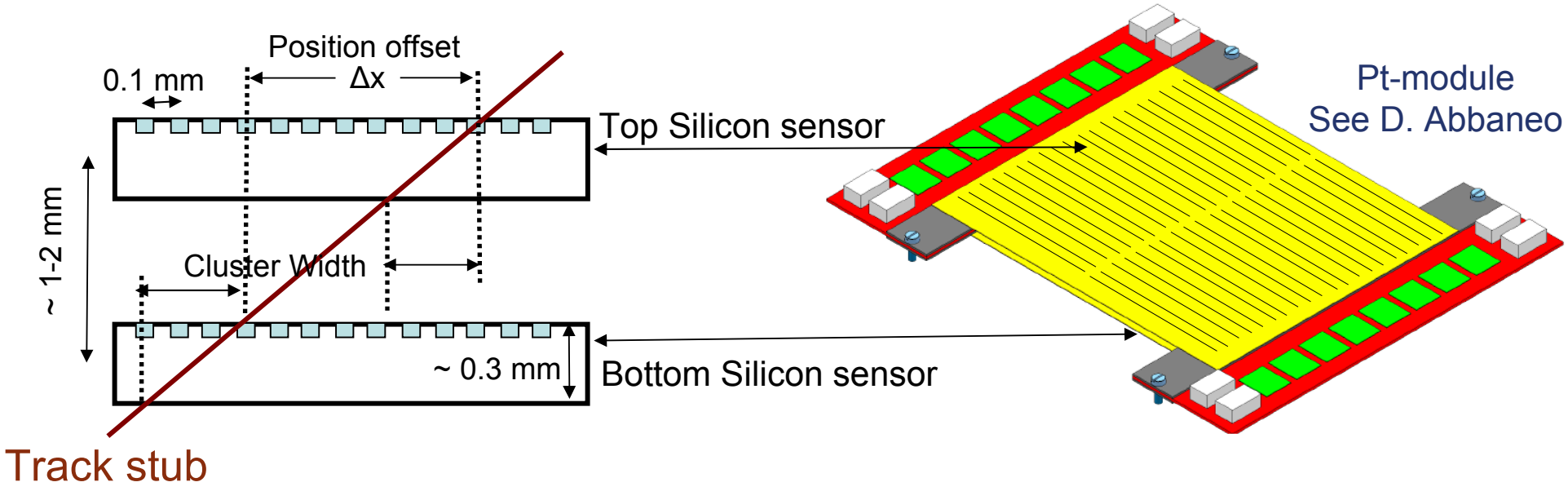
Outline

1. Introduction
2. Cluster and Stub finding
3. Data Link
4. Simulations
5. Conclusion

Silicon Strip Pt-module for Trigger purpose



Track bending in the B-field is inversely proportional to transverse momentum
Cluster Width and Offset selection in 2 sensors connected to same Front End ASICs (Pt-module) allows to reject low Pt tracks, reducing band width for read-out of proper trigger information at the LHC clock frequency

Front End ASIC architecture

Pre-amplifier and comparator stage
not included in current chip version

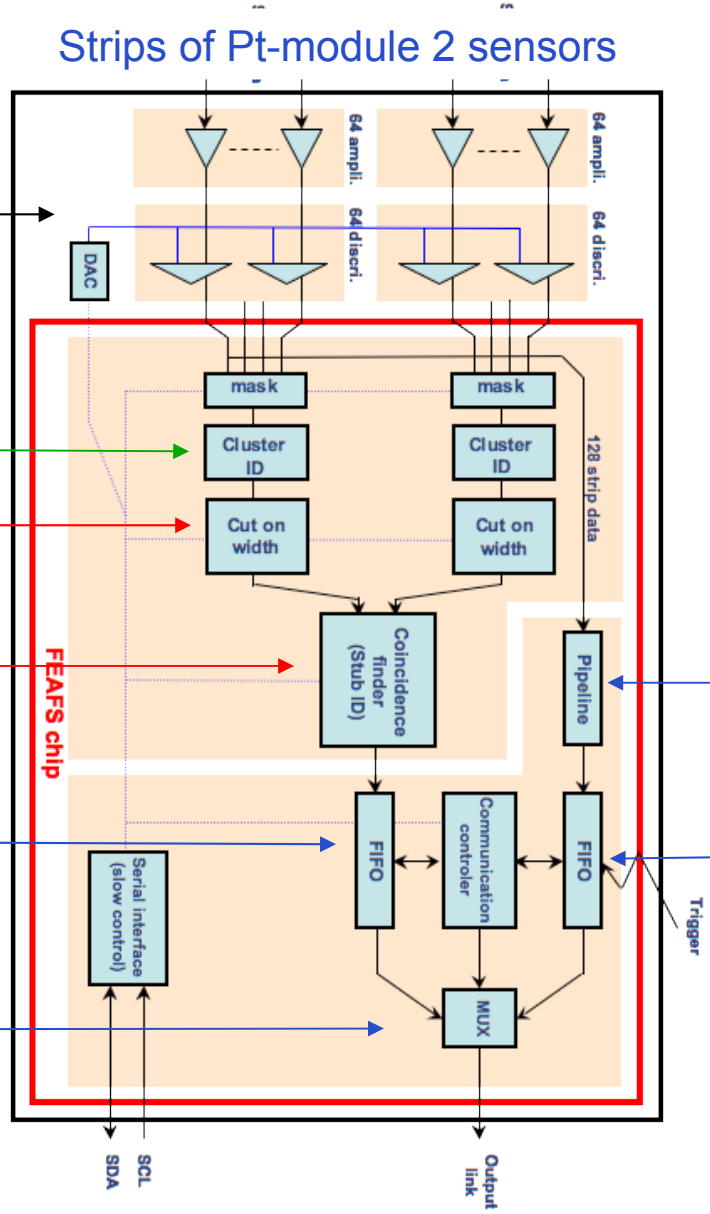
Find all clusters of strips
compute address on
5 bits, 360 µm precision

Select clusters
#strips < programmable threshold

Find cluster overlap
programmable window with offset
$|C1 - C2 + offset| \leq t_w$

Clusters address after selection
20/40 MHz LHC clock

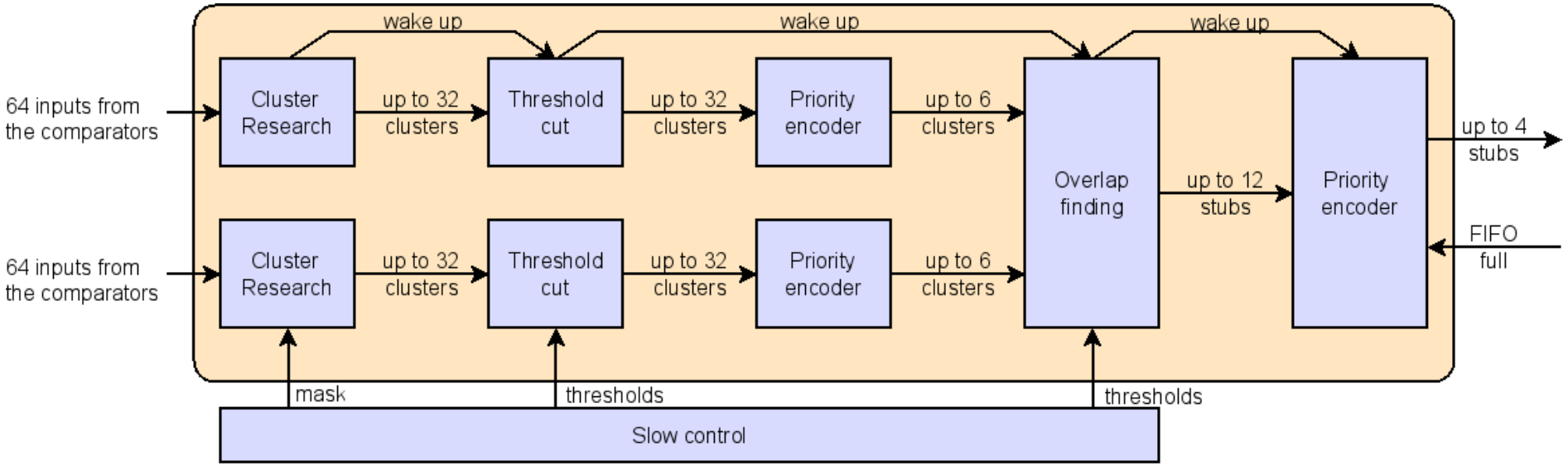
Asynchronous readout on
one data link for trigger
stubs and full read-out data



All strips
1 bit hit information

L1 Trigger 100 kHz

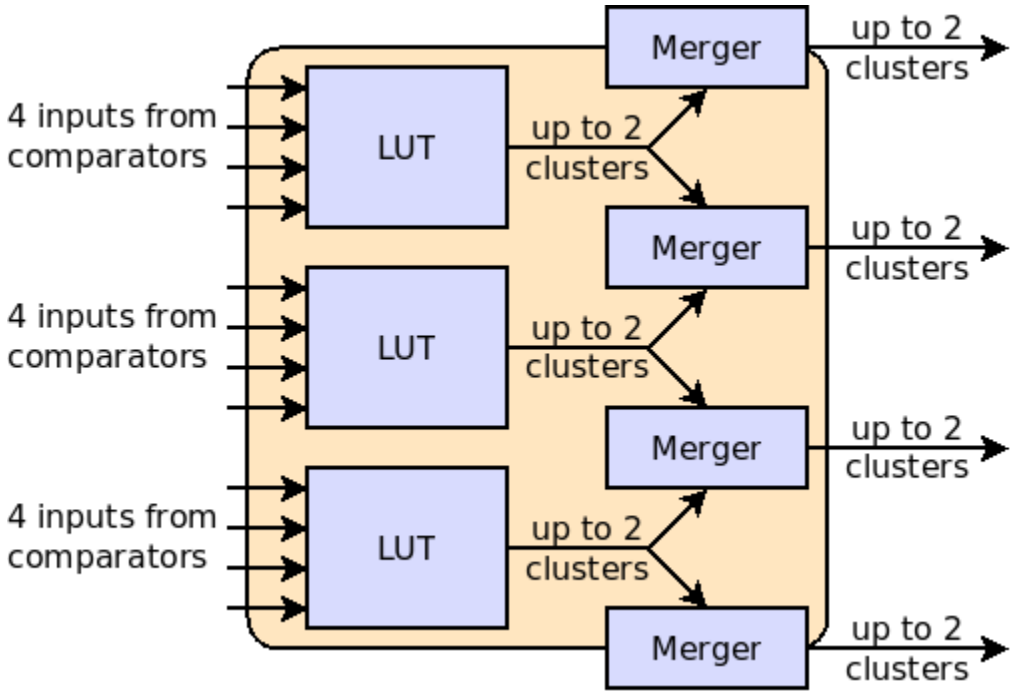
Cluster and Stub finding : Architecture



- Two flows up to the overlap finding
  - Masking of noisy channels
- The bus size is reduced at each step by priority encoders
  - Up to 6 clusters per 64 strips per sensor after CW selection
  - Up to 4 clusters per 2x64 strips (2 sensors) after overlap selection
- Wake up on the internal registers to reduce the consumption
- Overlap finding can be switched off (sensor edges or dead channels)

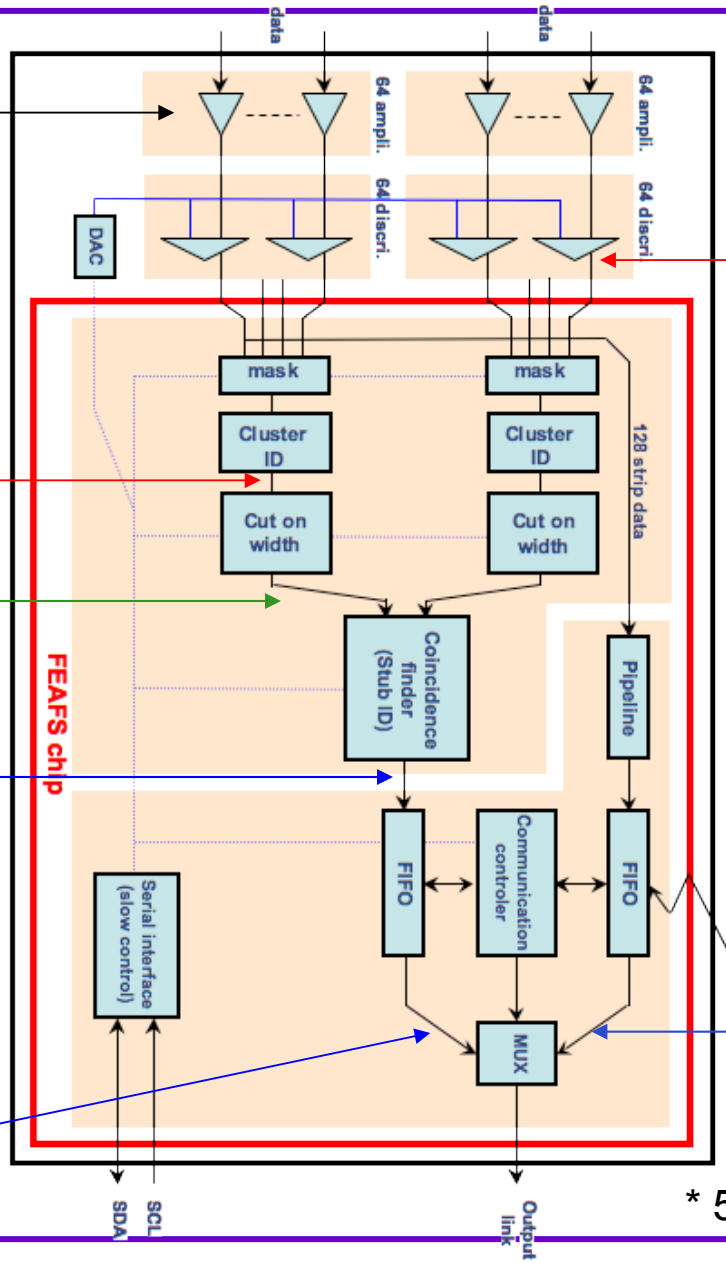
Cluster Finding : Algorithm

- 2x64 strips ⇒ 2x16 blocks of 4 strips
  - Same granularity as the degraded address (5 bits ⇒ 128 blocks)
  - Need for boundary block to merge clusters
- 32 LUT of 16x16 bits used to find clusters in each block (up to 2 clusters/block)
- Address of a cluster =
  - Address of its block
  - Arbiter when a cluster cross a boundary
- Only 1 clock cycle



Data flow

90 µm pitch 4.76 cm strips
2 x 128 channels Pt sensors



Full CMSSW simulation
x 200 pile-up* at R = 50 cm
1.6 % Strip Occupancy

<Cluster Width> ~ 4
0.4 % Cluster Occupancy

~ 100% efficiency at 2 GeV
2.5 reduction factor

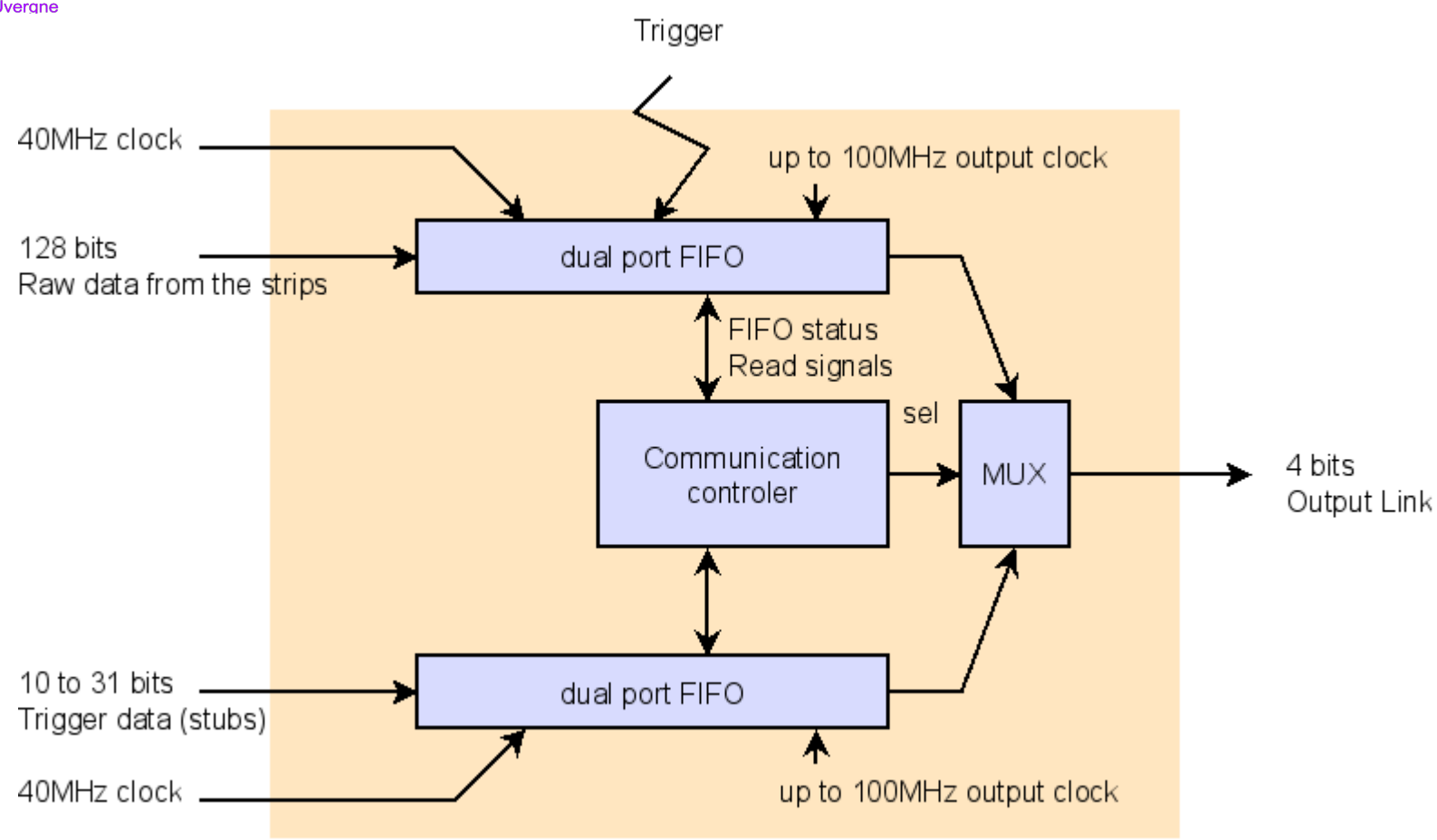
~ 100% efficiency at 4 GeV
6 reduction factor
0.7 MHz stub rate

Trigger data
2 bits header
2 bits #stub
5 bits address/stub
2 bits Pt/stub
Trigger flow
45/8 Mbps
(CW only/CW + coincidence)

Read-Out Data
no zero suppression
1 bit /strip at 100kHz L1 trigger rate
25.6 Mbps

* 5 x 10^{34} $cm^{-2}s^{-1}$ at 20 MHz LHC clock

Data flow



2 FIFO of 16 words depth for stubs and readout data
→ Used to safely pass from LHC clock domain (40MHz or 20MHz) to output link clock domain (up to 100MHz).

Output Frame

- **Trigger Frame:**

From 3 to 8 words of 4 bits, depending on the number of stubs.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id		Nb cl		Stub 1							Stub 2							Stub 3							Stub 4						
0	1	0	0	Add 1					Size 1																						
0	1	0	1	Add 1					Size 1			Add 2					Size 2														
0	1	1	0	Add 1					Size 1			Add 2					Size 2		Add 3				Size 3								
0	1	1	1	Add 1					Size 1			Add 2					Size 2		Add 3				Size 3		Add 4					Size 4
Word 1				Word 2				Word 3			Word 4					Word 5			Word 6				Word 7				Word 8			

- **Readout Frame:**

The 128 strips are split in 8 frame of 20 bits.

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id	word			N° Strip															
1	0	0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Word 1				Word 2				Word 3				Word 4				Word 5			

Trigger frames can be inserted between two readout frame

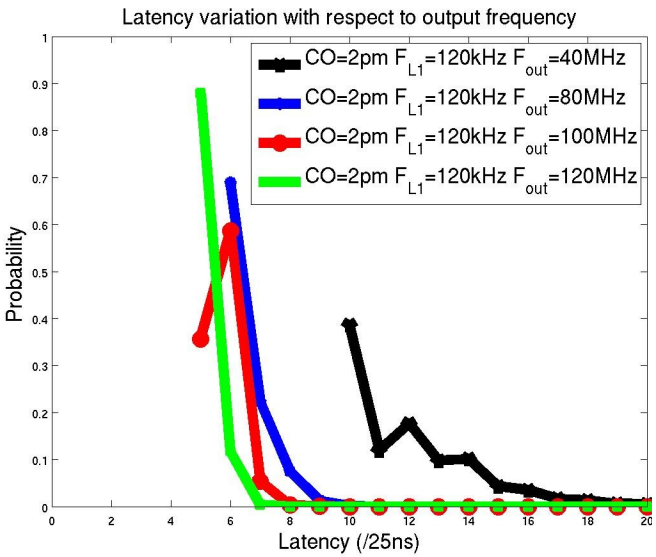
Communication controller

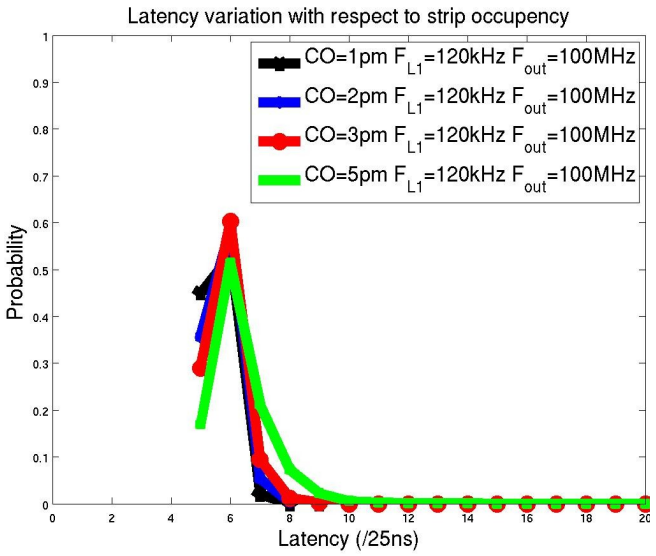
Performs the output bus arbitration with 4 running modes as a function of the FIFO states.

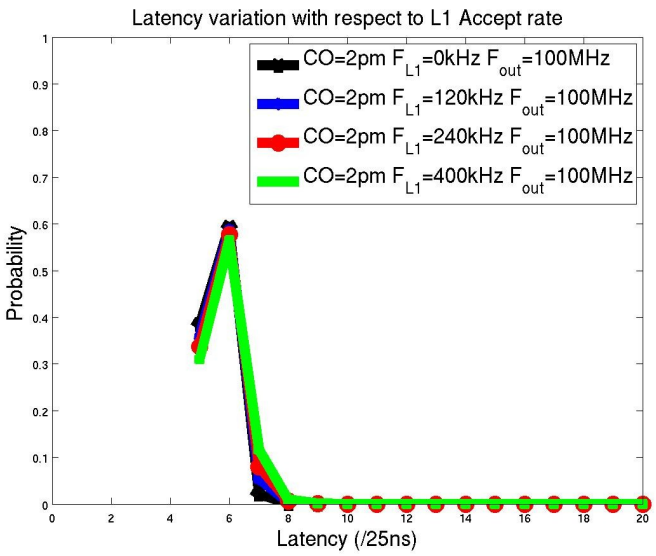
Communication Mode	Priority 1	Priority 2	Special
Normal	Trigger Data	Readout Data	
Derated (Trigger FIFO full)	Trigger Data	Ignored	Signal « trigger off » activated
Busy (Readout FIFO full)	Readout Data	Ignored	Signal « Busy » activated
Survival (Readout and trigger FIFO full)	Trigger Data	Readout Data	Signal « trigger off » and « busy » activated

Latency

- Study the latency of the full chip with respect to the L1 rate, the Cluster Occupancy (CO) and the output stage frequency







The trigger frame latency is bellow 10 clocks cycles for an output stage frequency above 80MHz

Even at twice the expected Cluster Occupancy, the trigger frame latency is bellow 10 clocks cycles

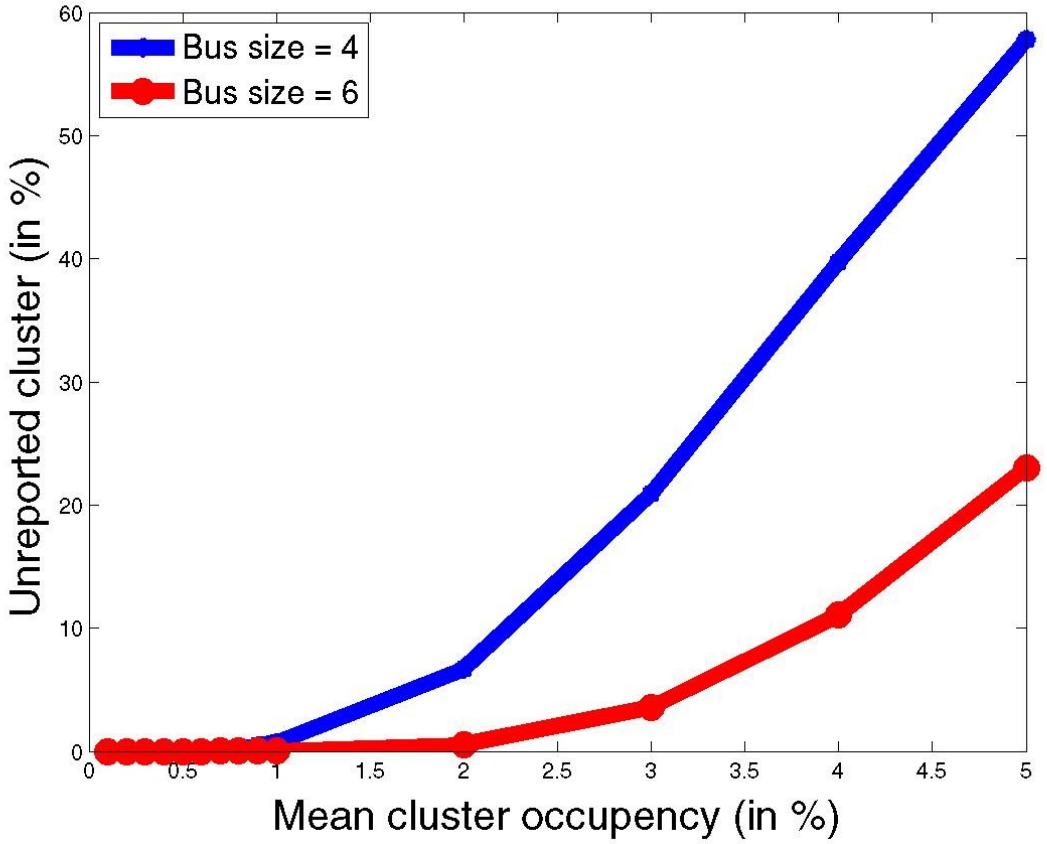
The trigger frame latency is not too dependent of the trigger rate

Unreported clusters

Simulation of the effect of the bus cut at the level of the priority encoder

→ No loss before 1% of mean cluster occupancy

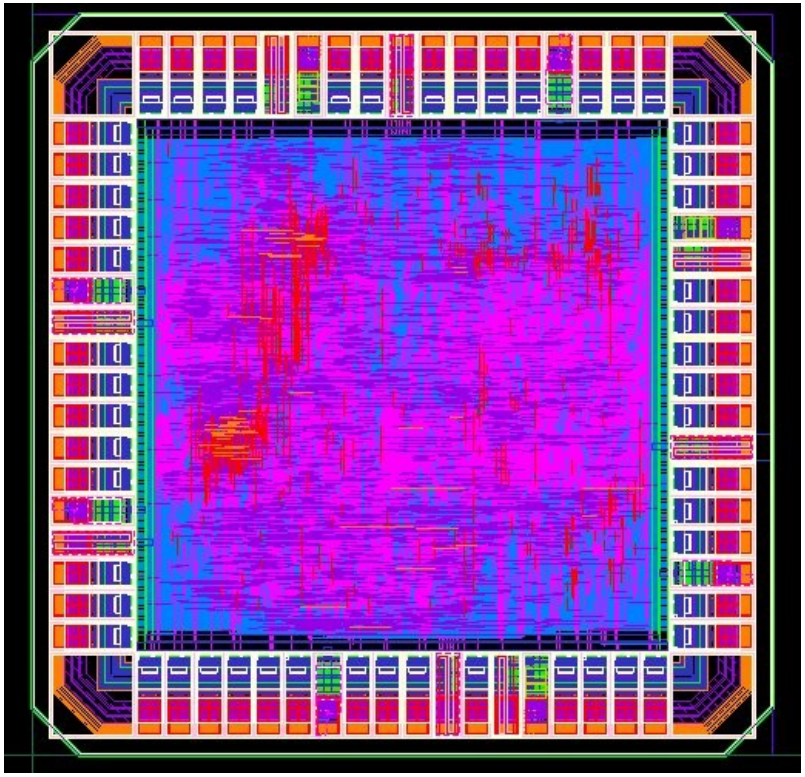
→ Final choice of the bus size to be decided with full realistic occupancy simulation



Chip status

- First prototype developed in 130nm from IBM with VCAD Standard cells
- 42300 cells (17300 for readout pipeline)
- Estimated power 60mW (with 20% activity on input)
- Only 32 inputs : internal mutiplexer
- Size: 4mm²

→ Chip received 15/02/2011 at packaging level



Conclusion and prospect

- Qualify the current chips
- Correct design according to qualification results
- Review specifications
  - Coupling to overall read-out architecture
    → Data format adapted to GBT
  - Minimize the number of GBT
    → Define concentrator ASIC
    → Zero suppression for full readout
    (as for trigger flow)
- Proceed towards 256 channels ASIC
  - Including preamplifier and comparator stage
  (Input compatible with Pt-module geometry)