

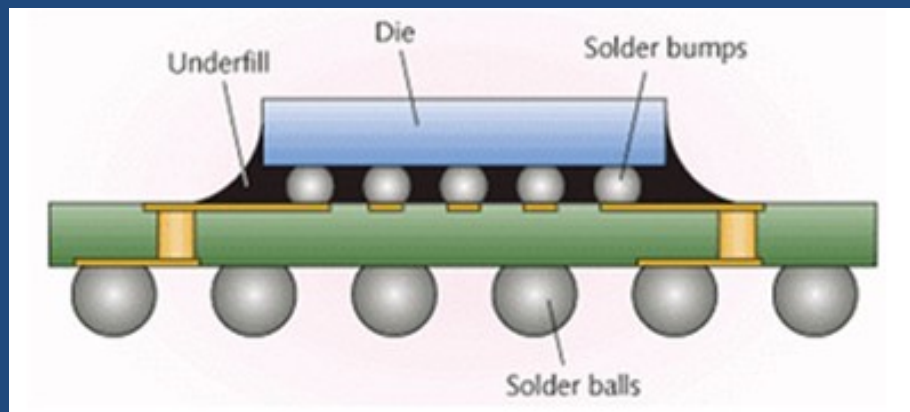


Experience with C4 flip-chip

....from the point of view of chip design & testing and on behalf of the GBT project

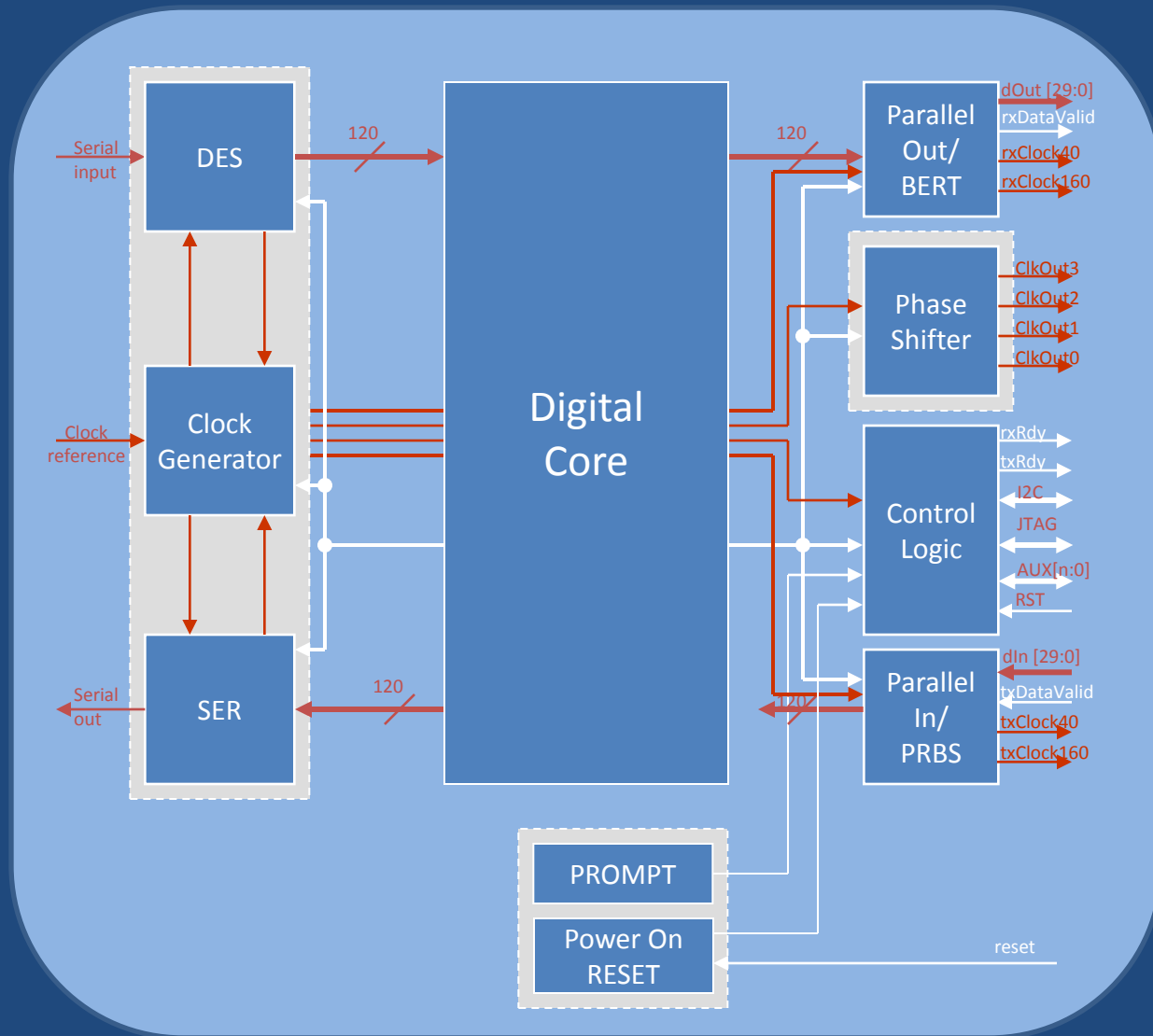
- Motivation
- Implications for design & testing

Controlled Collapse Chip Connection





Motivation: GBT-SERDES (prototype GBTX)



**4.8 Gbit/s
serial
data**

**More
details
from
Paulo
Moreira
today**

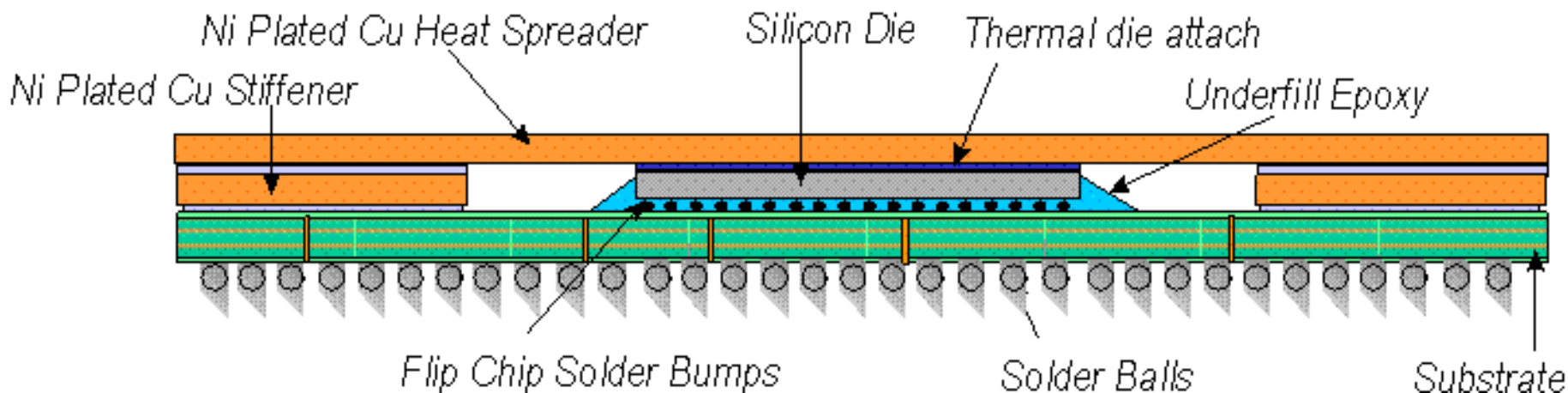
**60-bit I/O
bus at
160 MHz**

**.....
169 pads
(but
many
more for
GBTX)**



Motivation: GBT-SERDES (prototype GBTX)

- High speed lines: minimise inductance
- Direct powering to blocks
- Direct cooling on back-side (although coverplate is material eg Cu)
- Die size is pad-limited; extra silicon (400 I/Os in GBTX)
- Mount on BGA package





Technical Information

IBM 130nm library

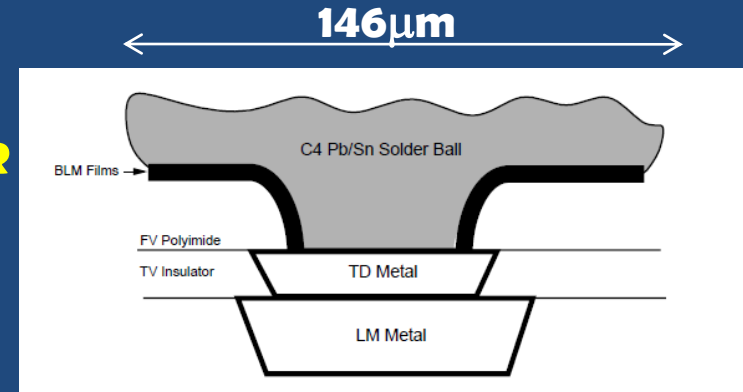
- **C4 pad only in LM metal stack**
- **pad & drivers separate blocks**

IBM deposit bumps on wafers;

- **more masks => extra cost**
- **MPWs: split between C4 & wirebond**

Size/pitch = “5 on 10” IBM standard (recommended for yield)
= **125/250 μ m**

Package vendor recommended **High-Temperature Solder**
(97Pb3Sn) for reliability





Design Implications

Floorplan at start of design

Communicate early with package/hybrid designers

-> we iterated a few times

-> placement of signal/power pads

Routing by hand is difficult

-> we used the CERN-VCAD

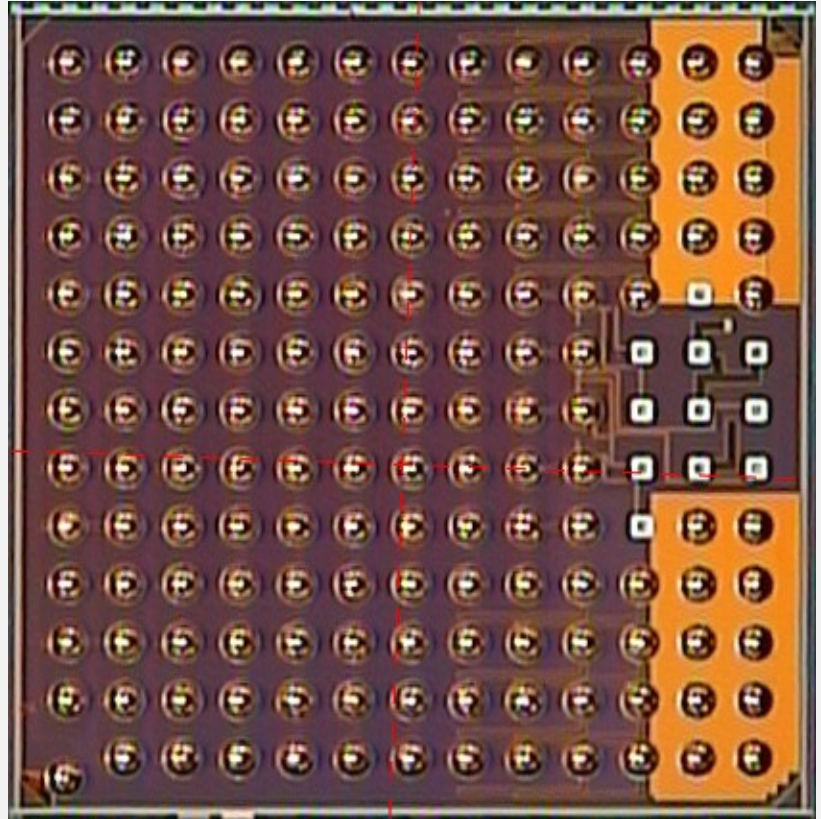
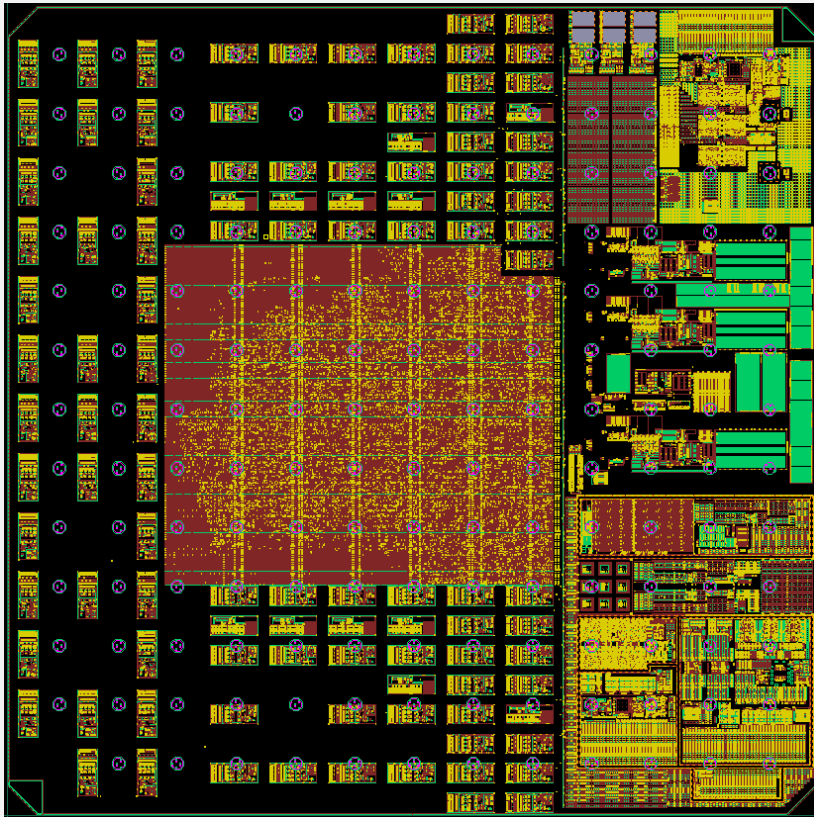
'digital design flow'

(analog blocks incorporated as black-box abstracts)

Solve ALL DRCs (even if not physical!)

157	158	159	160	161	162	163	164	165	166	167	168	169
dIn<22>	dIn<23>	dIn<24>	dIn<25>	dIn<26>	dIn<27>	dIn<28>	dIn<29>	txDataValid	a<0>	resetb	vddTxA	gndTxA
144	145	146	147	148	149	150	151	152	153	154	155	156
dIn<20>	dIn<21>	aux3	aux4	GND	aux5	sda	scl	GND	a<1>	tck	gndTxA	txOutputN
131	132	133	134	135	136	137	138	139	140	141	142	143
dIn<19>	GND	dOut<23>	dOut<24>	dOut<25>	dOut<26>	dOut<27>	dOut<28>	dOut<29>	a<2>	tdi	vddTxA	txOutputP
118	119	120	121	122	123	124	125	126	127	128	129	130
dIn<18>	dOut<22>	dOut<21>	rxClock160	rxClock40	tdo	txRdy	ClkOut2	ClkOut3	a<3>	2cAddress<1>	gndTxA	vddTxA
105	106	107	108	109	110	111	112	113	114	115	116	117
dIn<17>	GND	dOut<20>	VDD150	GND	VDD	GND	VDD150	GND	VDD	2cAddress<0>	vddTxA	gndTxA
92	93	94	95	96	97	98	99	100	101	102	103	104
dIn<16>	dOut<19>	dOut<18>	VDD150	GND	VDD	GND	VDD150	GND	VDD	ClkOutN0	vddCkA	gndCkA
79	80	81	82	83	84	85	86	87	88	89	90	91
dIn<15>	dOut<17>	dOut<16>	VDD150	GND	VDD	GND	VDD150	GND	VDD	ClkOutP0	gndCkA	DiffRefClkN
66	67	68	69	70	71	72	73	74	75	76	77	78
dIn<14>	dOut<15>	dOut<14>	VDD150	GND	VDD	GND	VDD150	GND	VDD	ClkOutN1	vddCkA	DiffRefClkP
53	54	55	56	57	58	59	60	61	62	63	64	65
dIn<13>	GND	dOut<13>	VDD150	GND	VDD	GND	VDD150	GND	VDD	ClkOutP1	gndRxA	vddRxA
40	41	42	43	44	45	46	47	48	49	50	51	52
dIn<12>	dOut<12>	dOut<11>	txClock160	txClock40	rxDataValid	rxRdy	ClkOut0	ClkOut1	a<4>	mode<1>	vddRxA	gndRxA
27	28	29	30	31	32	33	34	35	36	37	38	39
dIn<11>	GND	dOut<10>	dOut<9>	dOut<8>	dOut<7>	dOut<6>	dOut<5>	dOut<4>	aux2	mode<0>	gndRxA	rxInputN
14	15	16	17	18	19	20	21	22	23	24	25	26
dIn<10>	dIn<9>	dOut<3>	dOut<2>	GND	dOut<1>	dOut<0>	dIn<8>	GND	aux1	trms	vddRxA	rxInputP
2	3	4	5	6	7	8	9	10	11	12	13	
dIn<7>	dIn<6>	dIn<5>	dIn<4>	dIn<3>	dIn<2>	dIn<1>	dIn<0>	aux0	reset	gndRxA	vddRxA	

Layout & Bumped Die





Testing Results

Package designed by Endicott Interconnect

Assembly by Endicott

No cover-plate mounted

No C4 problems found on chips tested so far

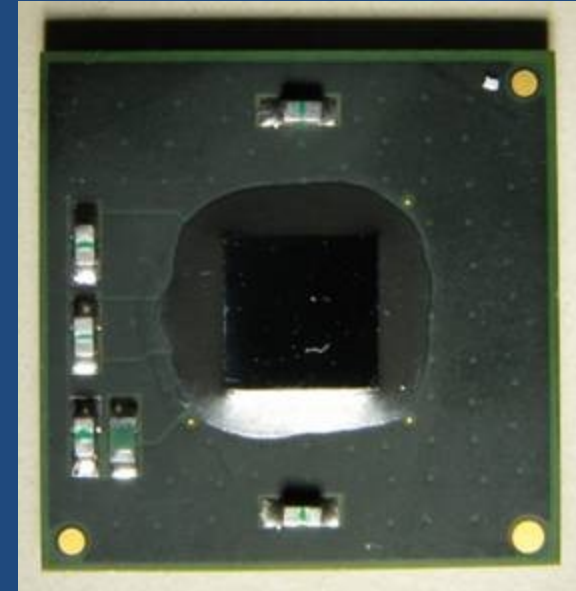
Chip testing issues:

Need complex package/hybrid immediately

Package design was significant part of project cost

Chip orientation is bad for radiation testing

**attenuation of 10keV X-rays in CERN facility
back-grinding needed for heavy ion tests**





Summary

C4 has many performance advantages

Standard industrial process

Requires careful planning: floorplan, package/hybrid

Implies extra financial cost upfront

Extra cost may be offset by savings elsewhere