ATLAS LAr Calorimeter Electronics Upgrade

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on behalf of the ATLAS LAr Calorimeter Upgrade Group

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Outline

- Motivation and plans for ATLAS LAr electronics upgrade - a reminder
- Radiation tolerant front-end electronics
  - pre-amplifiers, shapers, summing amplifiers
  - ADC
  - Link-on-Chip
  - powering
- Back-end electronics
  - high bandwidth, low latency read-out driver
- Electronics for new detectors
  - MiniFCal readout

ATLAS LAr Electronics

- 4 high granularity LAr calorimeters
- 182486 readout channels

- pre-amplifiers and summing amplifiers (PAS chip) for Hadronic Endcap Calorimeters (HEC)
  → on-detector, inside LAr cryostat
  → qualified for 1000 fb^{-1}

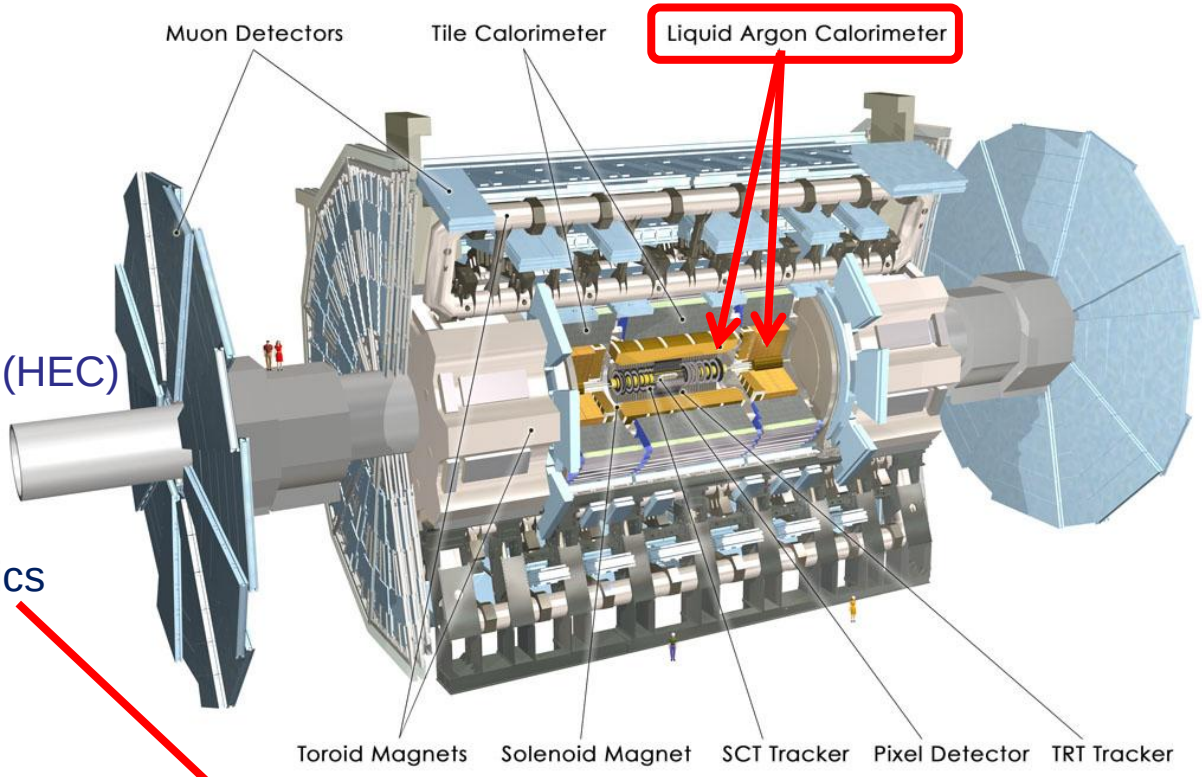
- front-end and trigger-sum electronics
  - 1524 front-end boards (FEB)

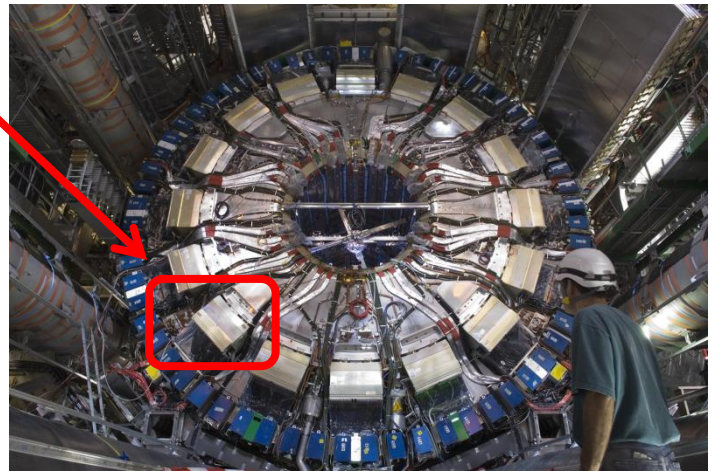
  → on-detector
  → qualified for 700 fb^{-1}

- back-end electronics and more trigger logic
  - 192 read-out driver boards (ROD)

  → off-detector

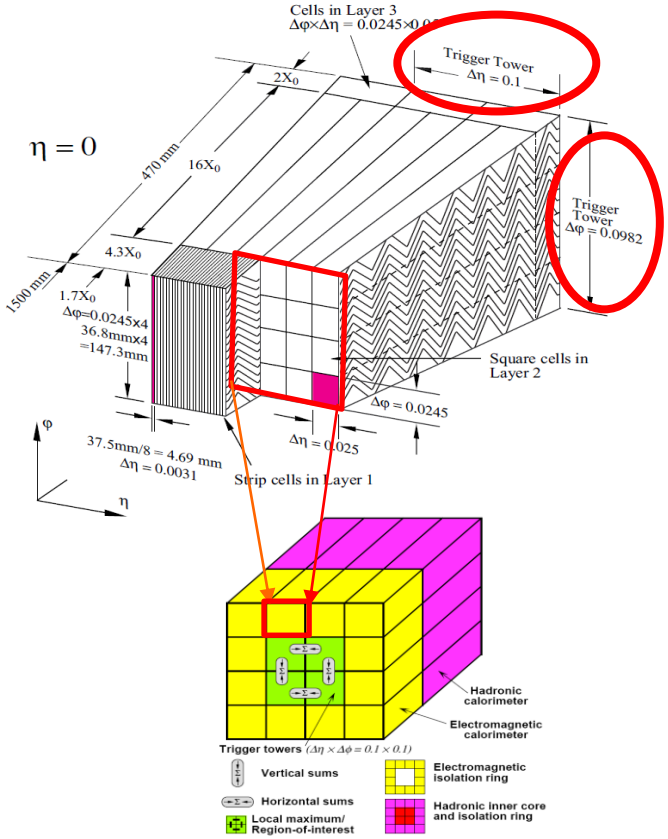
- all electronics components
  → exceed 10 yrs operational time in ~2016

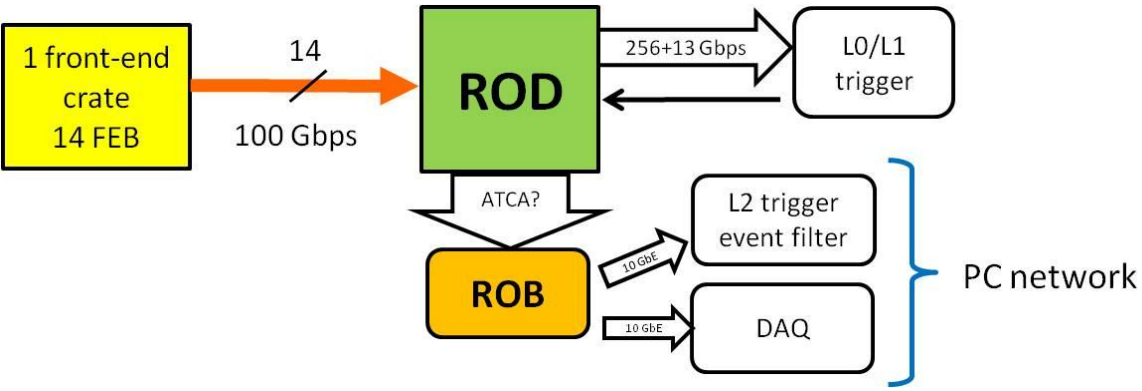




Motivation for Upgrade of Read-out Electronics

- improve radiation tolerance
  - safety factors for electronic components are included (x 2-5), but are not sufficient to safely cover high-luminosity phase
- improve reliability:
  - replace ageing electronics (less severe for electronics immersed in LAr)
- exploit high detector granularity also as input to trigger electronics
  - reduce pile-up background by taking all detector layers into account
  - better isolation of leptons/photons from hadrons (π^0)
  - sharper trigger threshold for hadronic jets





- go for free-running read-out scheme

→ no trigger logic on front-end

→ data buffer moved to back-end

→ larger trigger buffers and more latency budget for improved ATLAS trigger logic

HEC PAS development

- prepare HEC readout for 10 yrs HL-LHC
  - 5-10 x 10^{34} $cm^{-2}s^{-1}$ x safety factor 10
- design goals for pre-amplifiers (inside LAr cryostat):

	Specification of one preamplifier	Specification of 1 PAS chip (8 pre- & 2 summing amplifiers)
Noise	50 nA with 0 pF Input load (100 nA with 200 pF)	
Max. input current	250 µA	1000 µA
Dynamic Range	10^4 (13 bits)	
Nonlinearity	1,4% (measurement old chip)	
	2% (Specification)	
Power	15 mW	250 mW
Gain variation	< 2%	
Peaking time for 220pF (5 to 95%)**		50 ns after RC^2-CR shaper with RC=CD=15ns
Xtalk	< 1%	
Uniformity for 8 channels		<2% (measurement 1%)
Input impedance	50Ω +/-2 Ω	
Temperature dependence	Gain, noise, power consumption : change between room and LAr temperature ≤ factor of 2-3 for the whole chip	

HEC preamp @ HL-LHC	
TID	5 MRad
NIEL	2 x 10^{15} cm^{-2}
SEE	1.2 x 10^{12} cm^{-2}

→ LAr heating & boiling

→ LAr cooldown

HEC PAS development

- different technologies tested: IHP CMOS, IHP SiGe, IBM SiGe
- status:

Foundry / Type	Size : w/l (μm^{2})	Equivalent Input Noise (nA) at room temperature
IHP nmos	750*0,24	116
IHP nmos	1500*0,9	82,5
IBM npn HB	0.12*20*2	204
BB96 / Triquint	4 Preamp + Summing stage	497

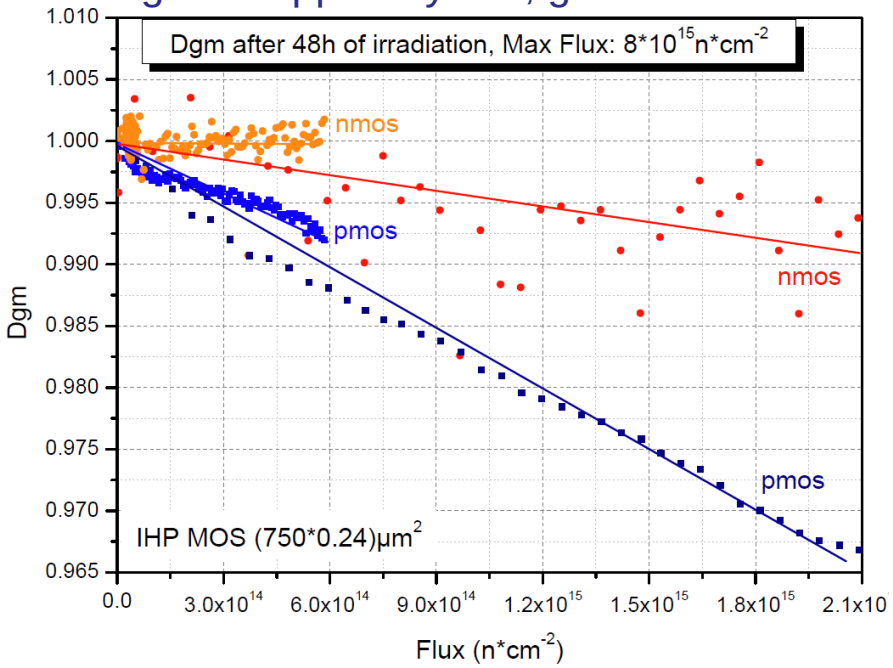
Material	**SiGe**			**Si**			**GaAs**	
Transistor	**Bipolar HBT**			**CMOS FET**			**FET**	
Foundry	**IHP**	**IBM MB HB**	**AMS**	**IHP**		**AMS**	**Triquint**	**Sirenza**
Type	**npn**	**npn**	**npn**	**nmos**	**pmos**	**nmos**	**pHEMT**	
Gain change@ $2*10^{15} n*cm^{-2}$	**3%**	**2% 2%**	**5%**	**2%**	**3%**	**3%**	**2% $1.2*10^{15}$**	**2%**
Gain change@ Max.rad.($n*cm^{-2}$)	**75% $2.2*10^{16}$**	**11% 20% (3.6 7.8)*10^{15}**	**55% $2.3*10^{16}$**	**8% $8*10^{15}$**	**11% $8*10^{15}$**	**22% $2.3*10^{16}$**	**2% $1.2*10^{15}$**	**2% $2*10^{15}$**

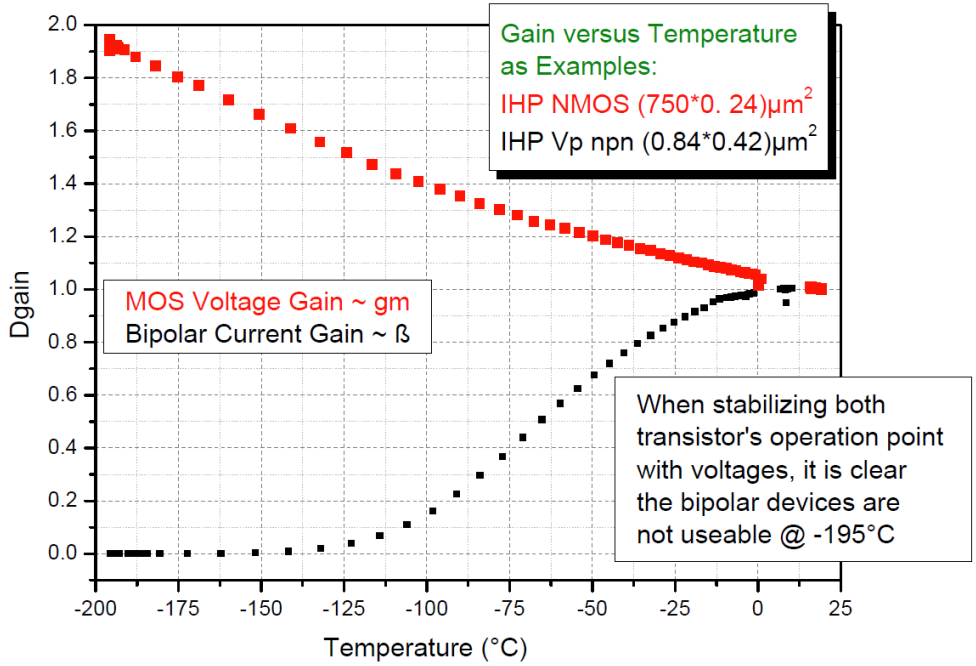
- @ 40 MHz

- IHP nmos technology chosen for further prototyping

HEC PAS more details

- IHP nmos currently pursued as most attractive technology
  - neutron radiation criteria (most critical) passed (p and γ in preparation)
  - reasonably stable hi→low temperature behavior
  - good support by IHP, good models





- next steps:
  - include temperature and radiation into models (from S-parameter measurements)
  - choose adequate preamp circuits and prepare circuit test chip (2011)
  - design+produce a HEC-II preamp prototype chip (2012)

- if IHP CMOS not fully satisfying (due to noise, dynamic range):
  - backup solutions: IHP or IBM SiGe bipolar

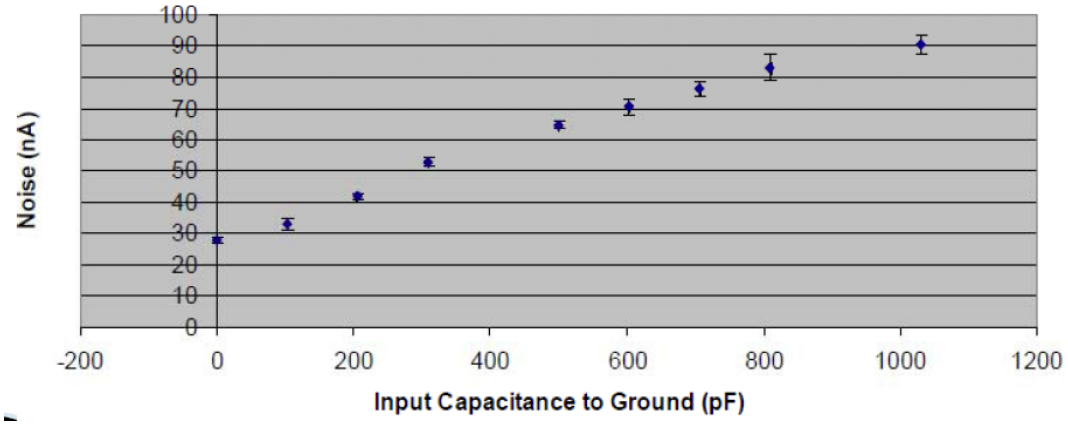
LAr pre-amplifier and shaper development

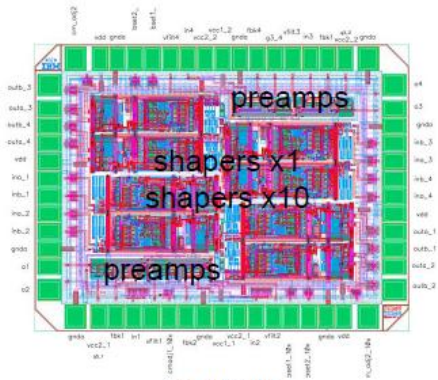
- LAPAS chip in SiGe IBM 8WL BiCMOS process (0.13 µm)

- Status: progress in measurements with prototype board
  - two x 1 preamp and shaper channels
  - two x 10 preamp and shaper channels
  - ready for tests with ADC blocks
- example:

Dynamic Range	16 bits in 2 ranges
INL	0.1% within each range
ENI	75nA
Max Signal Current	5mA
Shaping Time Const. (RC)	15ns
Shaping Function	$(RC)^2$-CR
Ionizing Radiation Tol.	30kRad
Neutron Equivalent Dose	10^{13} n/cm^2

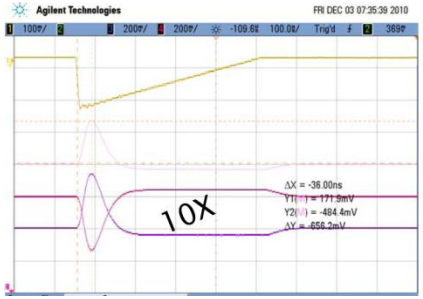
Equivalent Noise Input vs. Input Capacitance to Ground

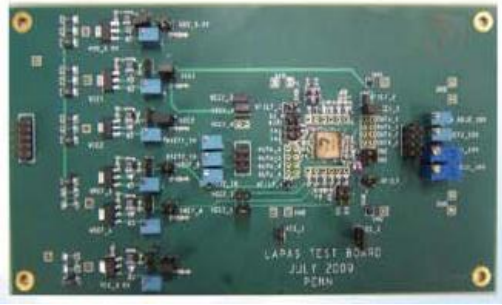




LAr Chiplet
2mm X 2mm

- noise at 1 nF slightly larger than 75 nA due to additional feedback resistor to reduce input impedance to 25 Ω

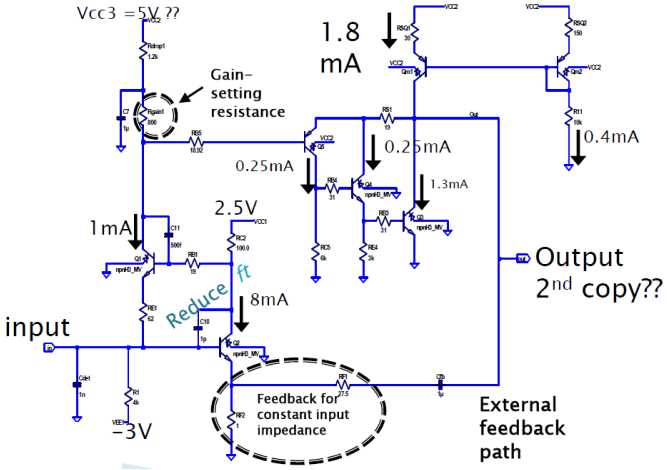




- future plans with LAPAS ASIC:
  - daughter board design for upgrade prototype foreseen in spring 2011

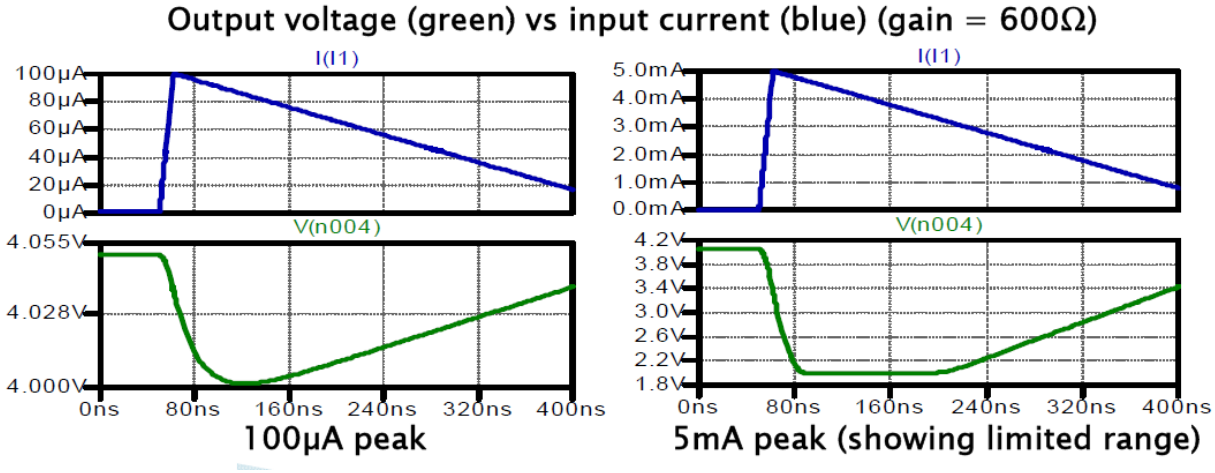
LAr pre-amplifier and shaper development

- IHP SiGe 0.25 µm BiCMOS prototype development
- program:
  - optimize layout for preamp and differential shaper
  - submit first IHP prototype by spring/summer 2011



preliminary IHP pre-amp design

- example of ongoing work:

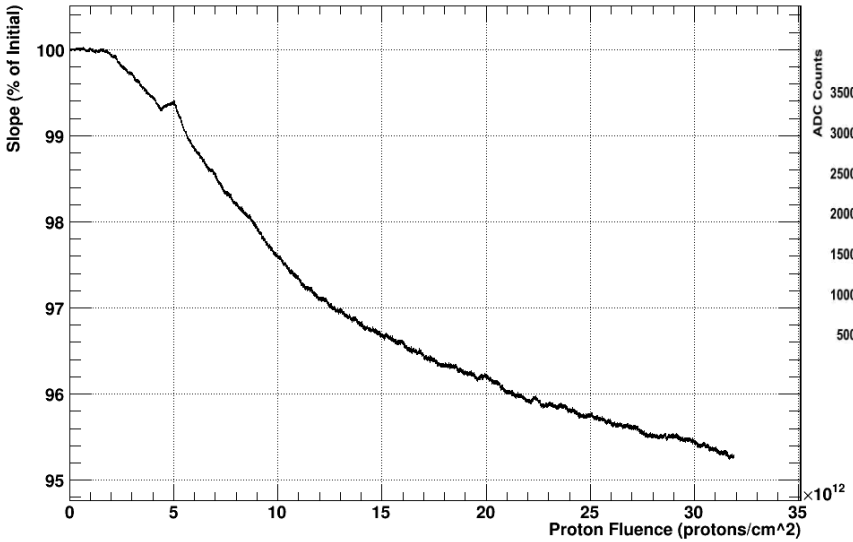


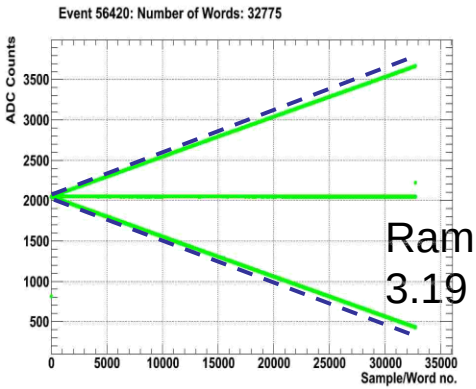
- to prevent clipping at 5 mA peak input, either:
  - increase VCC2 → best if process allows
  - decrease R_{gain} → lower gain, increased power in shaper to meet noise requirement

Radiation tolerant commercial ADC

- test results from COTS products:
  - ST RHF1201 12-bit ADC, very expensive
  - works stably up to 2 x 10^{12} p/cm^2, 106 kRad (Si)
  - 5% change in ramp slope at 1.6 MRad

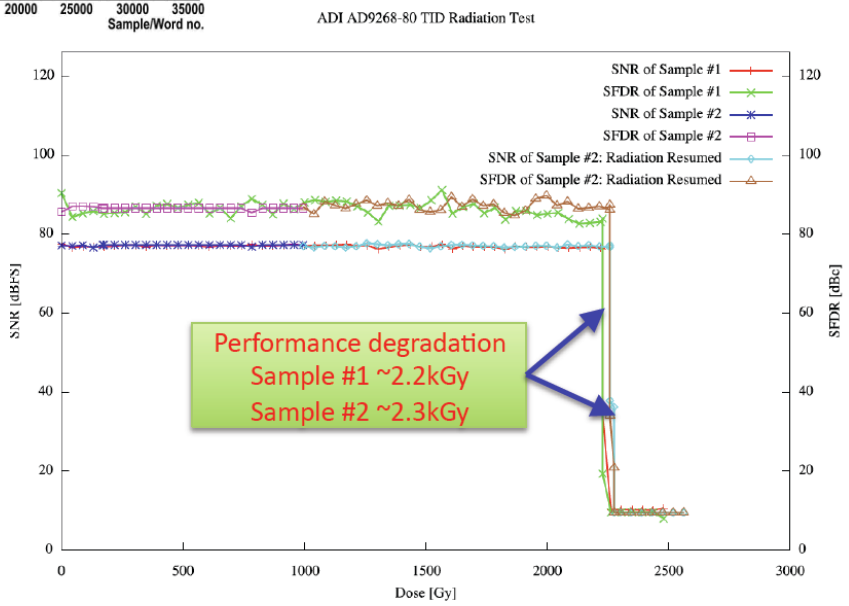
COTS FEB ADC @ HL-LHC	
TID	7.8 MRad
NIEL	6.6 x 10^{14} cm^{-2}
SEE	1.3 x 10^{14} cm^{-2}





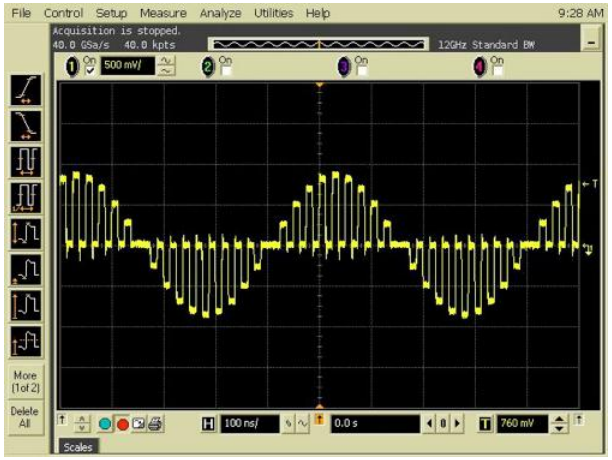
Ramps after
3.19 x 10^{13} p/cm^2

- AD9265-80, AD9268-80, AD9269-40, AD9650-65, LTC2204, ADS6445 fail at 120-230 kRad

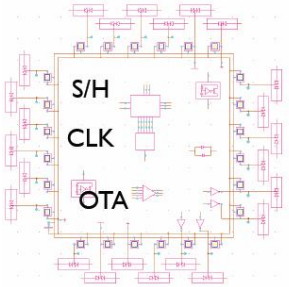


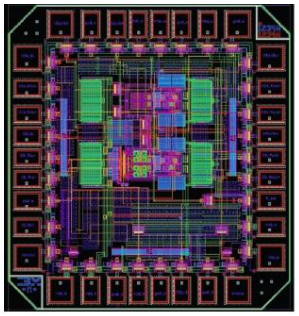
Radiation tolerant custom ADC

- NEVIS09 chip with OTA, S/H, CLK test structures
- IBM 8RF, 130nm CMOS technology
- inject sinusodial signal, check S/H rise/fall time and amplitude
- irradiation up to 2 x 10^{14} p cm^{-2} , 10 MRad (Si)
- no degradation visible



custom FEB ADC @ HL-LHC	
TID	0.6 MRad
NIEL	1.7 x 10^{14} cm^{-2}
SEE	3.2 x 10^{13} cm^{-2}

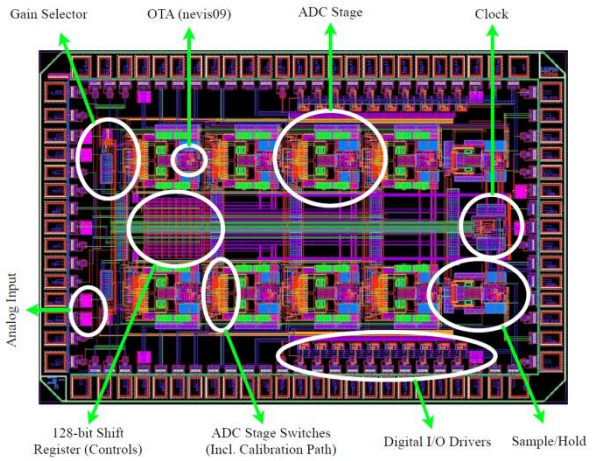




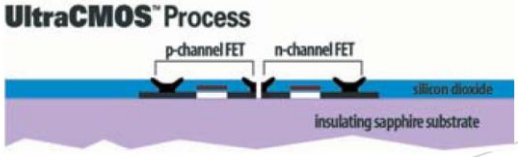
- NEVIS10 chip with two 4-stage ADC pipelines, 1.5 bits/stage, gain selector structures for each pipeline → true ADC

- test programme ongoing: verify12-bit precision, power consumption, calibration strategy, sensitivity to bias voltage, cross-talk, radiation tolerance, analog and digitial gain selection

- go for full prototype chip in 2013

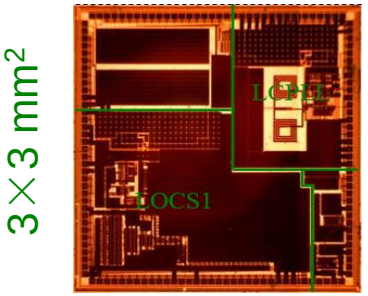


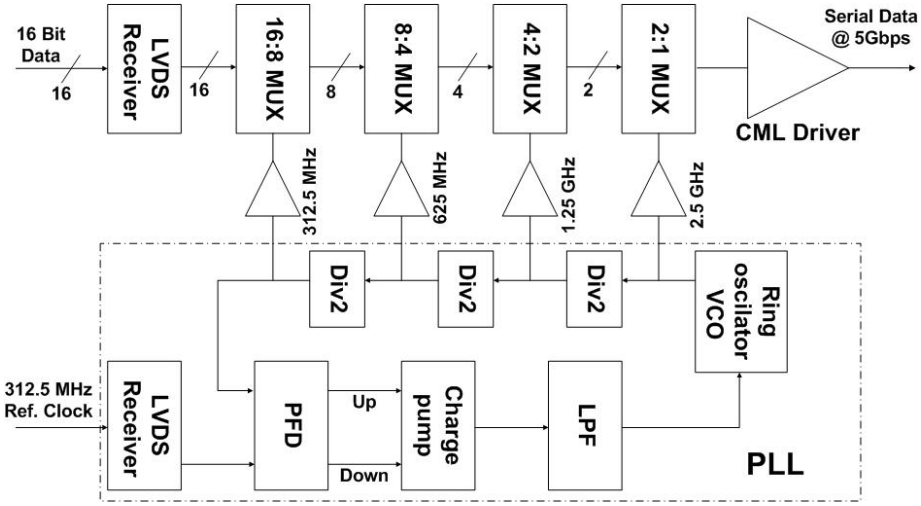
Link-on-Chip (LOC)



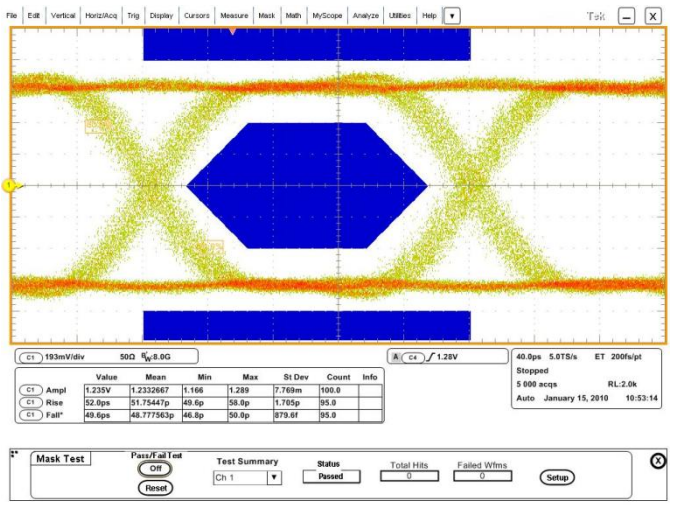
- 0.25 µm thin-film Silicon-on-Sapphire (SoS) CMOS technology:
  - low power, low cross talk → good for mixed-signal ASIC designs.
  - economical for small to medium scale ASIC development.

- The first generation LOC prototype succeeded in:
  - the LOCs1, a 5 Gbps 16:1 serializer
  - 2.5 GHz ring oscillator VCO
  - 4 stage 2:1 multiplexing with the last stage specially designed for high speed.
  - input data and ref. clock in LVDS
  - output in CML at 5 Gbps
  - the 5 GHz LCPLL, a crucial step toward 10 Gbps speed.





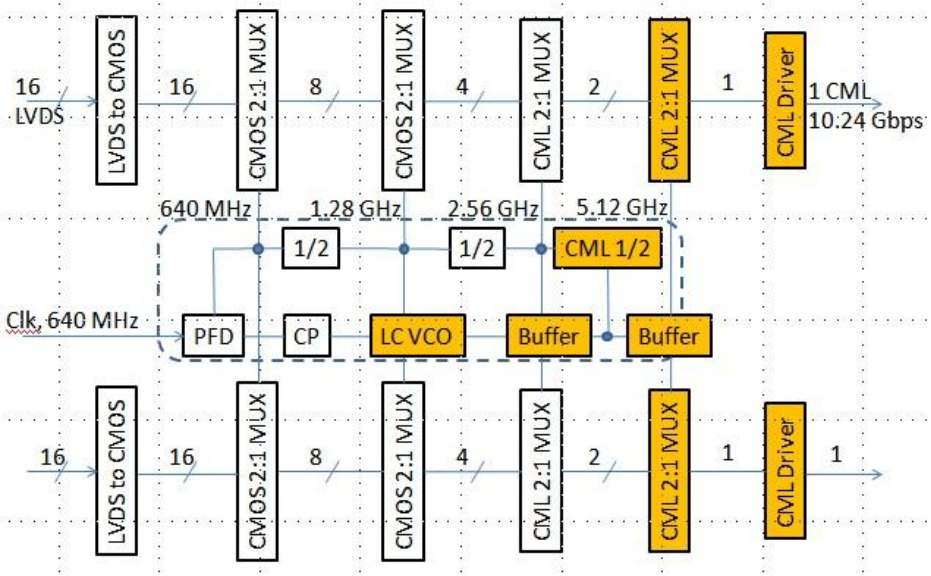
LOCs1



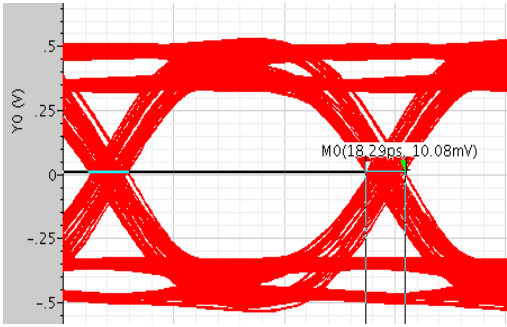
Eye diagram at 5 Gbps

Link-on Chip (LOC)

- The second generation LOC design status:
  - Initial thought was LOCs6 but
  - difficulties found in the 5 GHz clock fanout over the whole chip.
  - limitation in the GC process (evaluated to be rad-tol).
- a faster PC process (still 0.25 µm) will come out June 2011 that provides ~15% speed increase and 30 – 50% area reduction.
- a 180 nm will follow the PC process (announced by foundry)
- with the PC and the 180 nm feature size, the LOCs6 concept will be re-visited.
- now we step back to LOCs2: a 2-lane shared PLL serializer array.
  - LOCs2 design status on fast units:



- Buffer: Above 4.6 GHz, 200 mV swing, post layout and worst case (ss, 85 C)
- CML 1/2: Above 4.3 GHz, schematics with extra trace capacitance (ss, 85 C).
- CML Driver:
  Eye diagram of 7-bit PRBS at 8 Gbps, with inductance peaking (7.4 nH), (ss, 85 C)



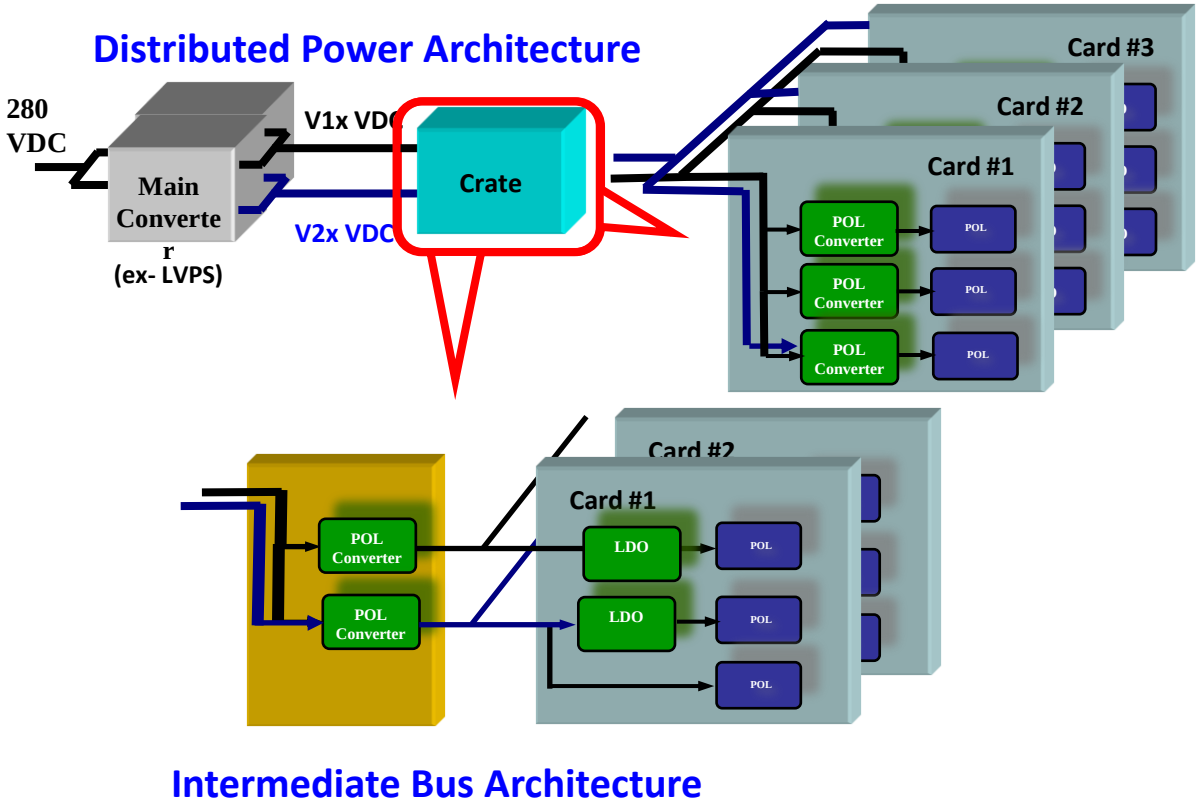
- CML 2:1 MUX:
  this is the next step
- LC VCO: Successfully prototyped at 5 GHz

DC Front-End Powering

- total power consumption per Front-End Crate remains the same (goal)
  - about 80 W per Front-End Board, 3 kW per power supply
- fewer voltage levels on FEB (goal)

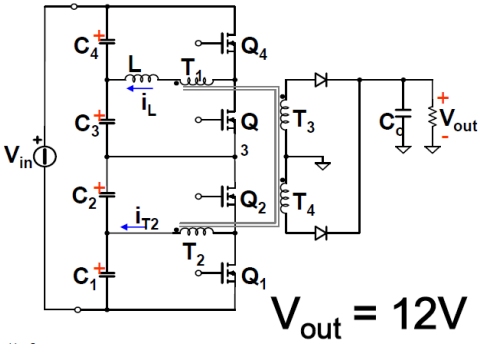
- power architectures:
  - Distributed Power Architecture with main converter and point-of-load converters (POL)
  - Intermediate Bus Architecture, additional set of bus voltages

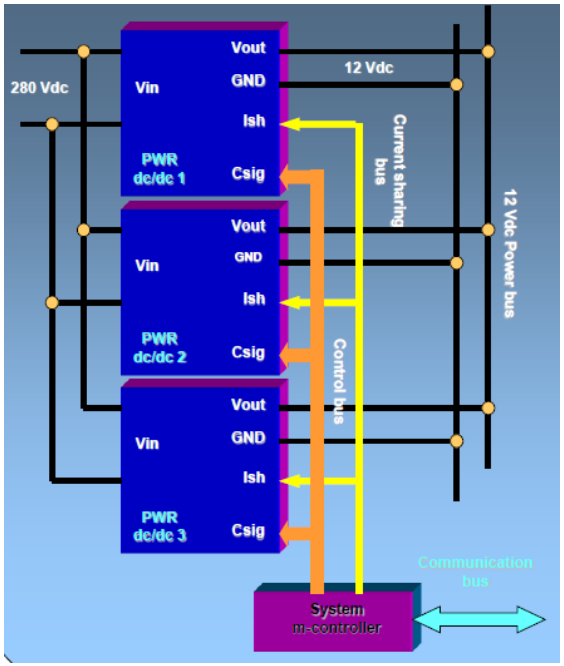
FEB POL @ HL-LHC	
TID	0.3 - 4.7 MRad
NIEL	0.3 - 4 x 10^{14} cm^{-2}
SEE	5 - 8 x 10^{13} cm^{-2}

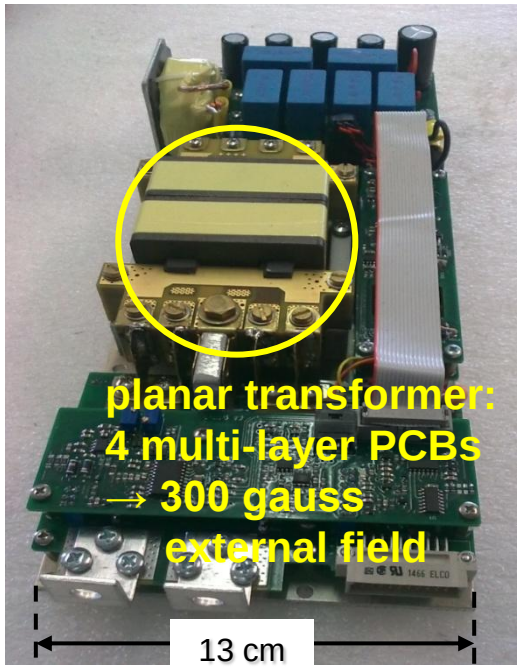


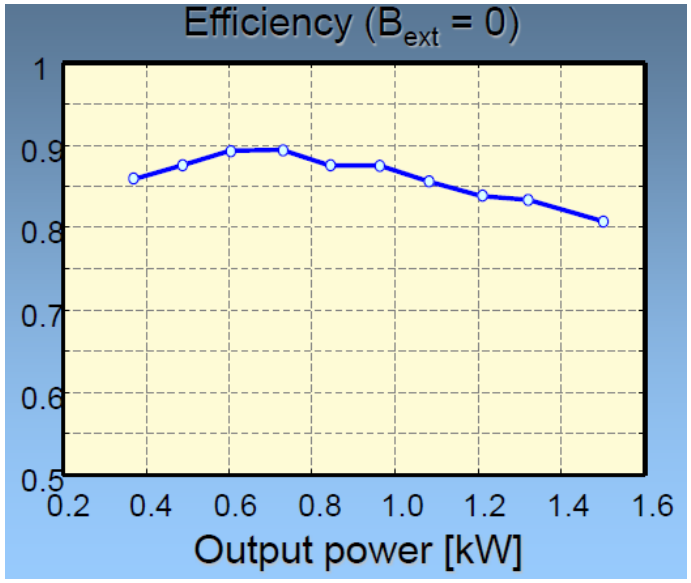
Main Converter Development

- 3 modules, 1.5 kW each
- n+1 redundancy, current sharing
- power cell topology: switch in-line converter
- voltage on switches reduced by factor 4

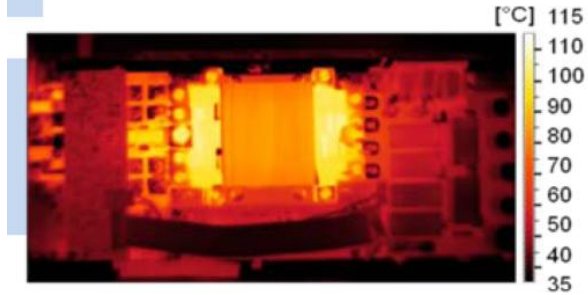






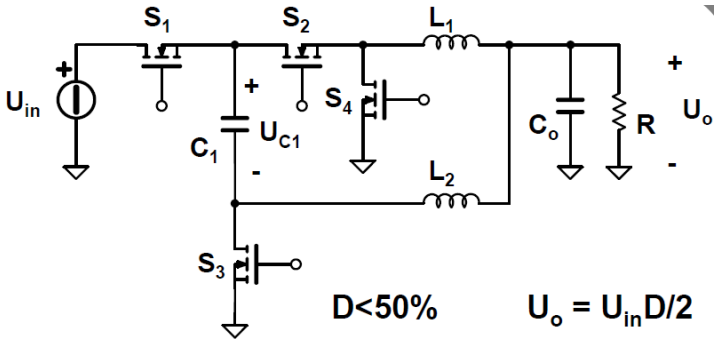


- thermal management and cooling is being simulated and measured



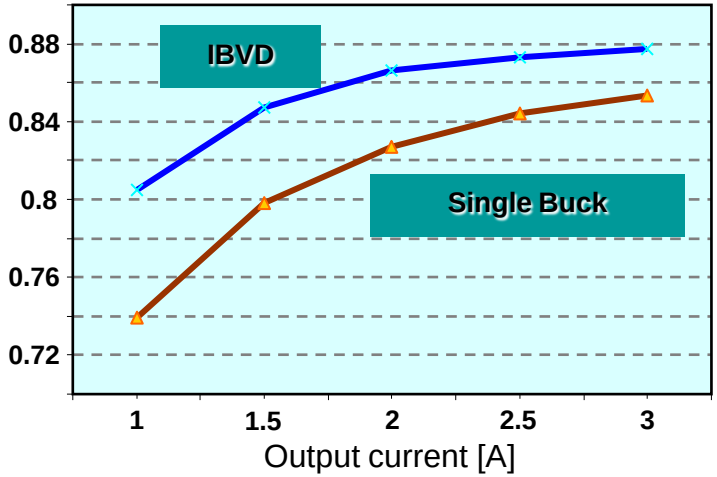
POL Converter

- non-isolated POL converter
- Interleaved Buck Converter with Voltage Divider – IBVD
  - high step-down ratio (12-48 V to 3-5 V)
  - reduced switch voltage stress ($U_{in}/2$)
  - interleaved operation with automatic current sharing and ripple cancellation

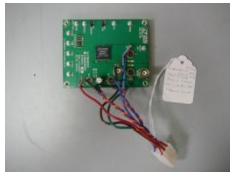


- prototype specs:
  - Input voltage: U_g = 12 V
  - Output voltage: U_o = 2.5 V
  - Output current: I_o = 3 A
  - Operating frequency: f_s = 1 MHz
  - 350 nH air core inductors
  - Dimensions: 6 x 4.2 cm^2

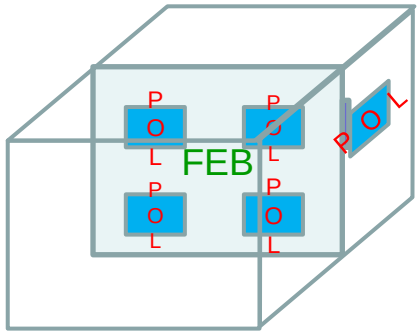
Efficiency comparison (B_{ext} = 0)



- also tested:

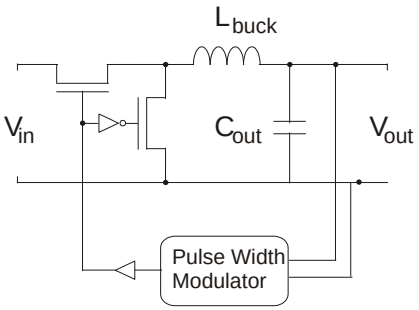


- 2 Si based POL tested in different positions inside front-end crate:
  - LTM4602 – 6A High Efficiency DC/DC µModule
  - IR3841 – Integrated 8A Synchronous Buck Regulator
- noise shielding necessary if inside Front End Crate

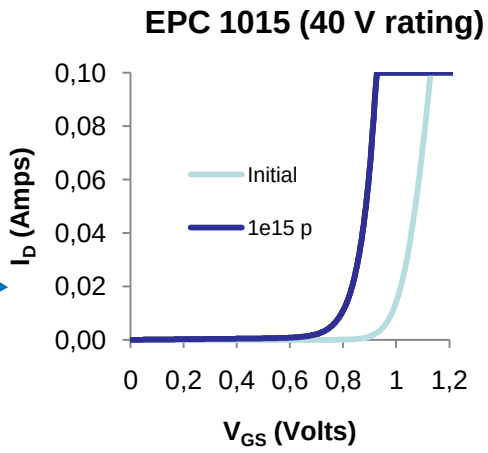


Buck converter – Component Irradiation Tests

Company	Device	Technology	Dose before damage seen	Observation Damage Mode	Potential Use
IHP	ASIC custom LDMOS V_{DS} = 12-15 V rating	0.25 µm CMOS	53 Mrad	Slight Damage (Threshold Voltage Shift)	Voltage Rating too low for switch
XYSemi	MOSFET (2 amps) LDMOS V_{DS} =15-20 V rating	0.25 µm CMOS	52 Mrad	Minimal Damage	Voltage Rating too low for switch
Enpirion	EN5360 #2	0.25 µm CMOS	100 Mrads	Minimal Damage	DC-DC Buck Converter (Clue for PWM)
Enpirion	EN5360 #3	0.25 µm CMOS	48 Mrads	Minimal Damage	DC-DC Buck Converter (Clue for PWM)
EPC	EPC 1014 (40 Volt)	GaN	64 Mrad	Minimal Damage	Upper and Lower Switches
EPC	EPC 1015 (40 Volt)	GaN	10^{15} protons	Slight Damage 300 mV Threshold Voltage Shift	Switches
EPC	EPC 1001 (100 V) 1012 (200 V)	GaN	In test 10^{15} protons	NA	Switches



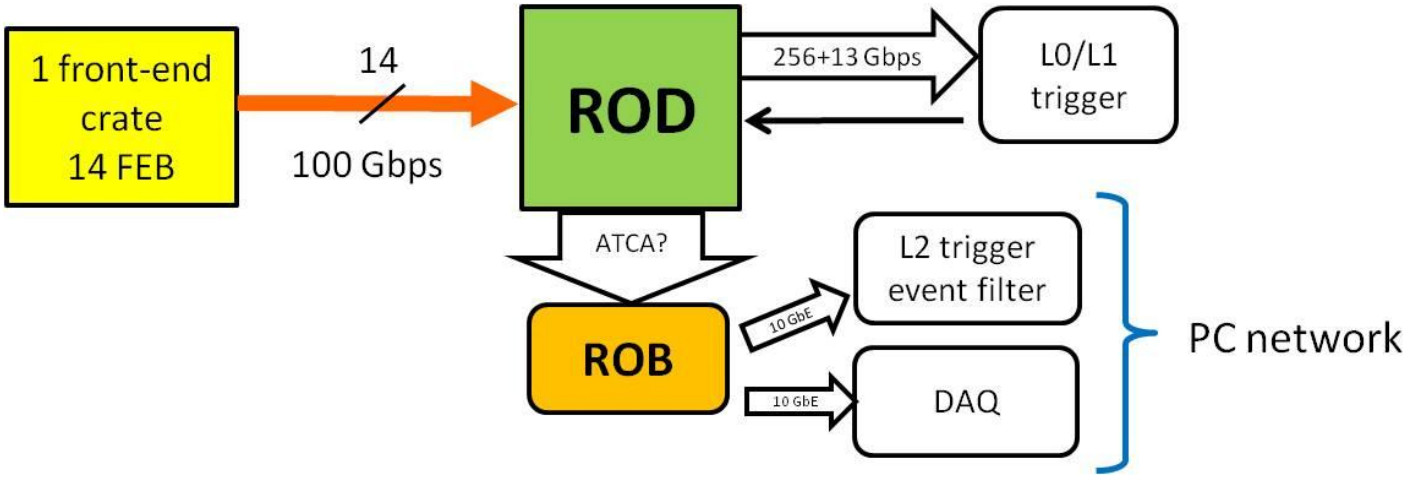
Synchronous Buck Converter



- GaN devices meet the radiation qualification as converter switches.
- A suitable rad tolerant CMOS process can be used to produce a Pulse Width Modulator (PWM)
- Ideally a p-channel FET would be used for upper switch/drive for the upper switch.

- development ongoing

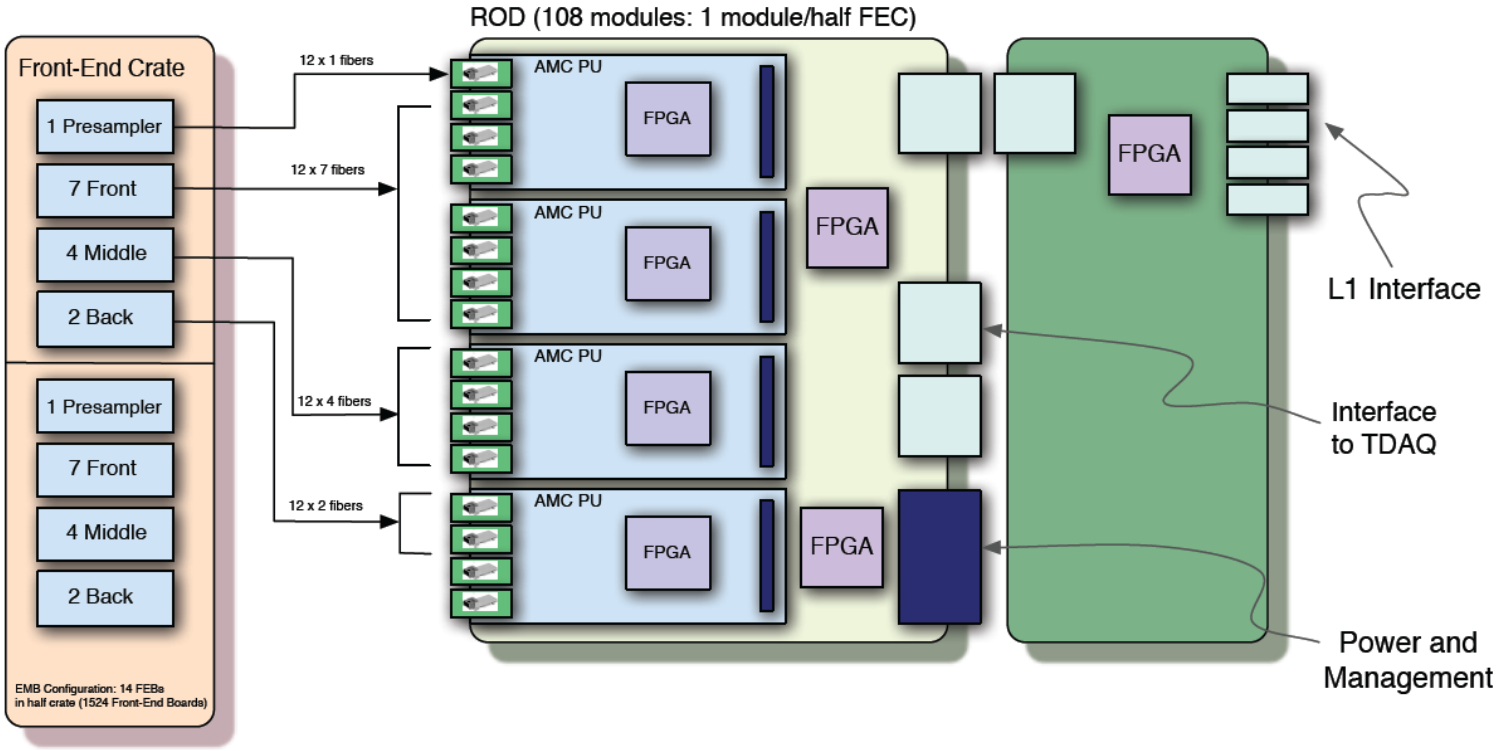
New Prototype Design of the Back-End



- R&D baseline:
  - shaping and digitization at high rate on front-end board → 128 channels at 40 MHz
  - transfer rate to off-detector electronics → 100 Gb/s per front-end board → total 150 Tb/s
  - radiation tolerant multi-fiber optical links at ~ 12 x 10 Gb/s
  - fully digital off-detector trigger
    → digital pipeline on Read-Out Driver (ROD) → long latency buffer up to ms
    → fast trigger sums on ROD → calorimeter trigger
    → more flexible and higher trigger granularity

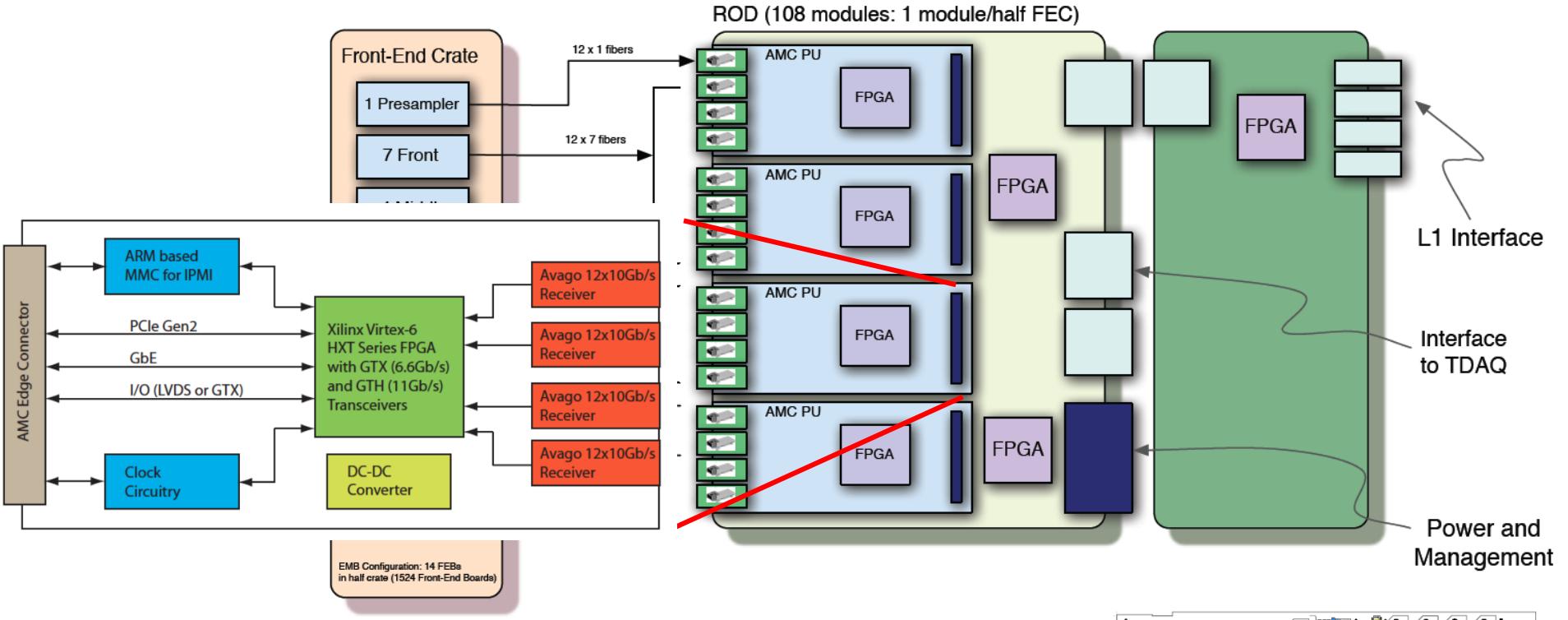
Read-out Driver Development

- ATCA/AMC prototypes with FPGA+SERDES >= 6Gbps

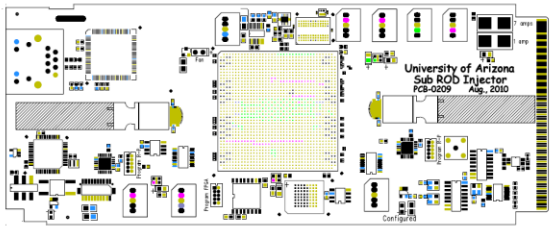


Read-out Driver Development

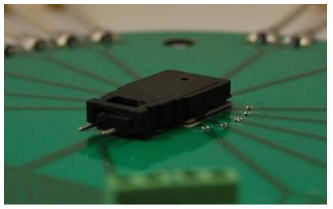
- ATCA/AMC prototypes with FPGA+SERDES >= 6Gbps



- sub-ROD module in production, based on Virtex 6
- Optical Link: Avago 12x10Gbps SNAP-12 transmitter/receiver



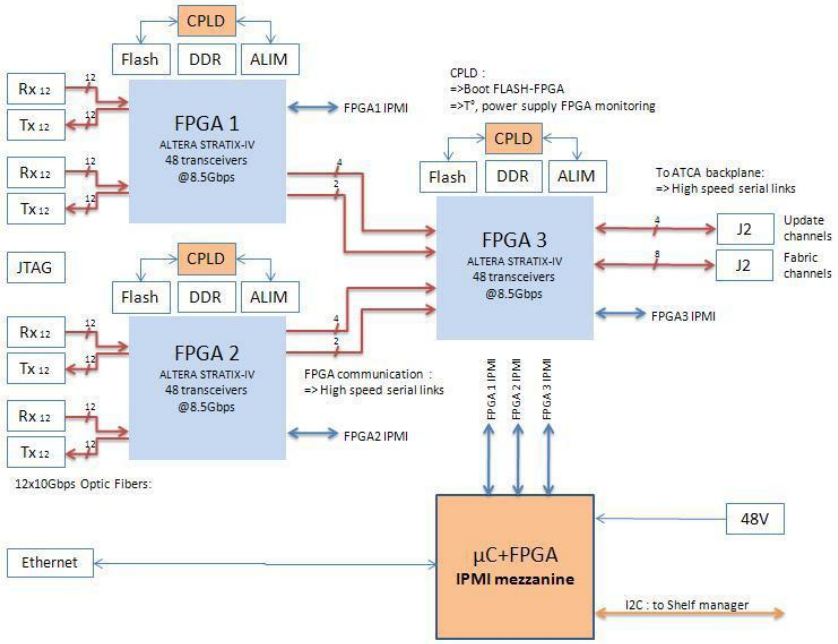
- sub-ROD injector module in production, based on Stratix IV
- delays in SNAP12 from Reflex Photonix
- plan to use LightABLE optical engine from Reflex Photonics (12 x 11.2 Gbps max.)



120 Gbps LightABLE™ Surface Mount Parallel Fiber Optic Engine

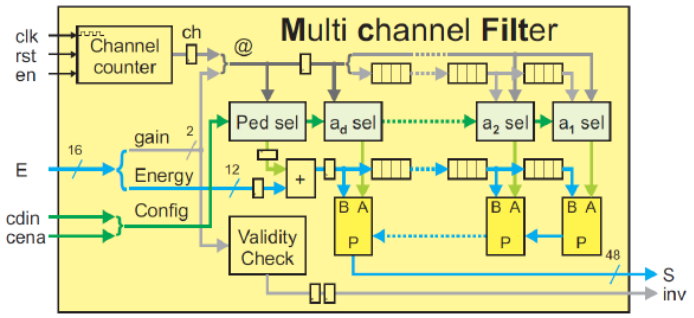
Development around Read-Out Driver

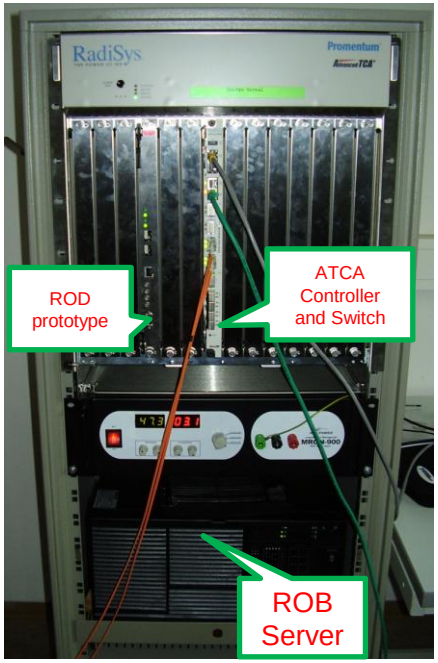
- high bandwidth ATCA demonstrator development



- ongoing FPGA development work:
  - interface for L0/L1 trigger
  - pre-processing of data for L0/L1 input
  - long-latency data buffering
  - interface to DAQ based on standard protocol, e.g. FPGA sending data to server CPU memory via 10 Gb/s Ethernet
- simulation of free-running read-out

- proof-of-principle for high bandwidth readout:
  - digital signal filter designed with minimal latency (3+2 FPGA clock cycles)
  - suppress electronic and pile-up noise @ 40 MHz





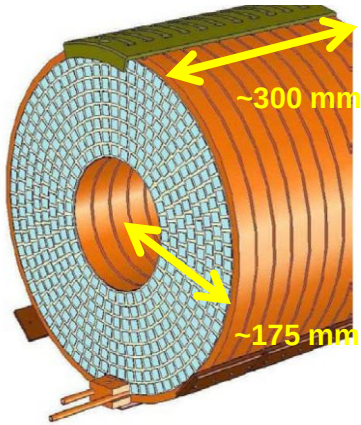
Electronics for MiniFCal

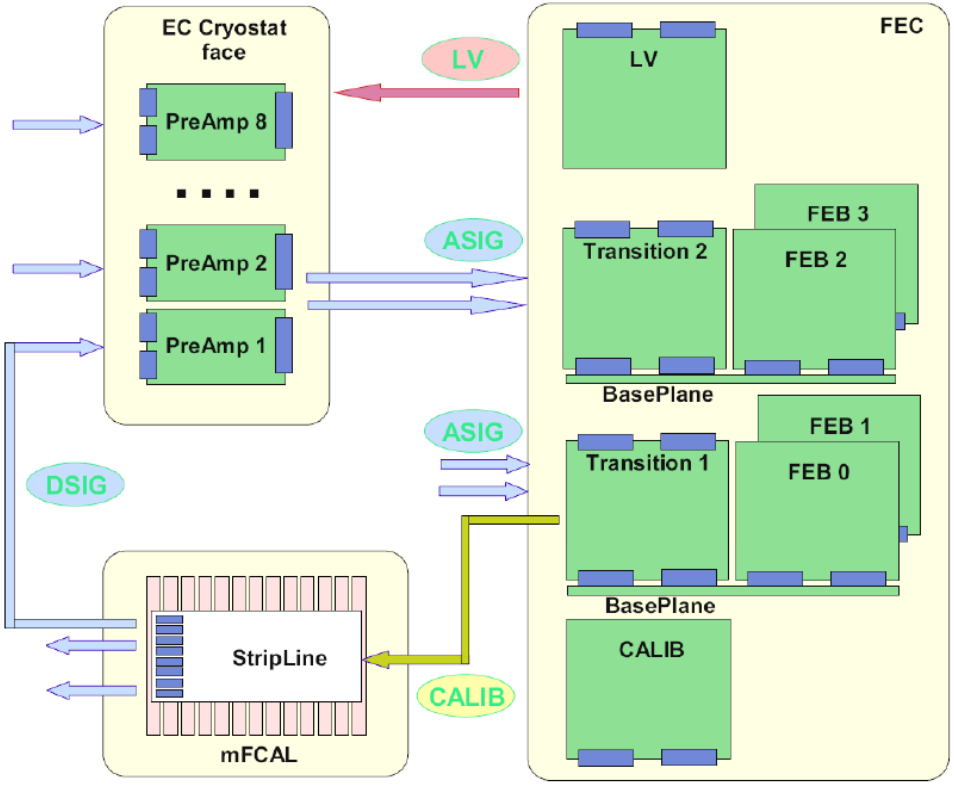
- concept for readout of diamond/Cu sampling calorimeter

- preamplifiers: fast, low noise, rad-hard
- located outside MiniFCal
- preamps power from Front End Crates
- transition board as interface to FEB

- radiation levels (neutrons, all energies)
  LAr end-cap face 5000 kHz/cm^2
  Front-End Crate 100 kHz/cm^2
- expected S/N~440 for summed signal

- identified technology for further prototyping: SiGe





Summary

- progress in development and radiation testing of individual components needed for LAr electronics upgrade at HL-LHC
- many details need dedicated and further effort to be fully solved or optimized
- next logical step in 2011/12 is to combine the components to more complete prototype setups of the readout chain
- system and integration aspects are being worked out
- currently also working on a staged upgrade scenario of the LAr readout
  - better understanding of possible complications at an early stage
  - less dramatic change when complete readout is going digital

More Information