ATLAS calorimeter and topological trigger upgrades for Phase 1

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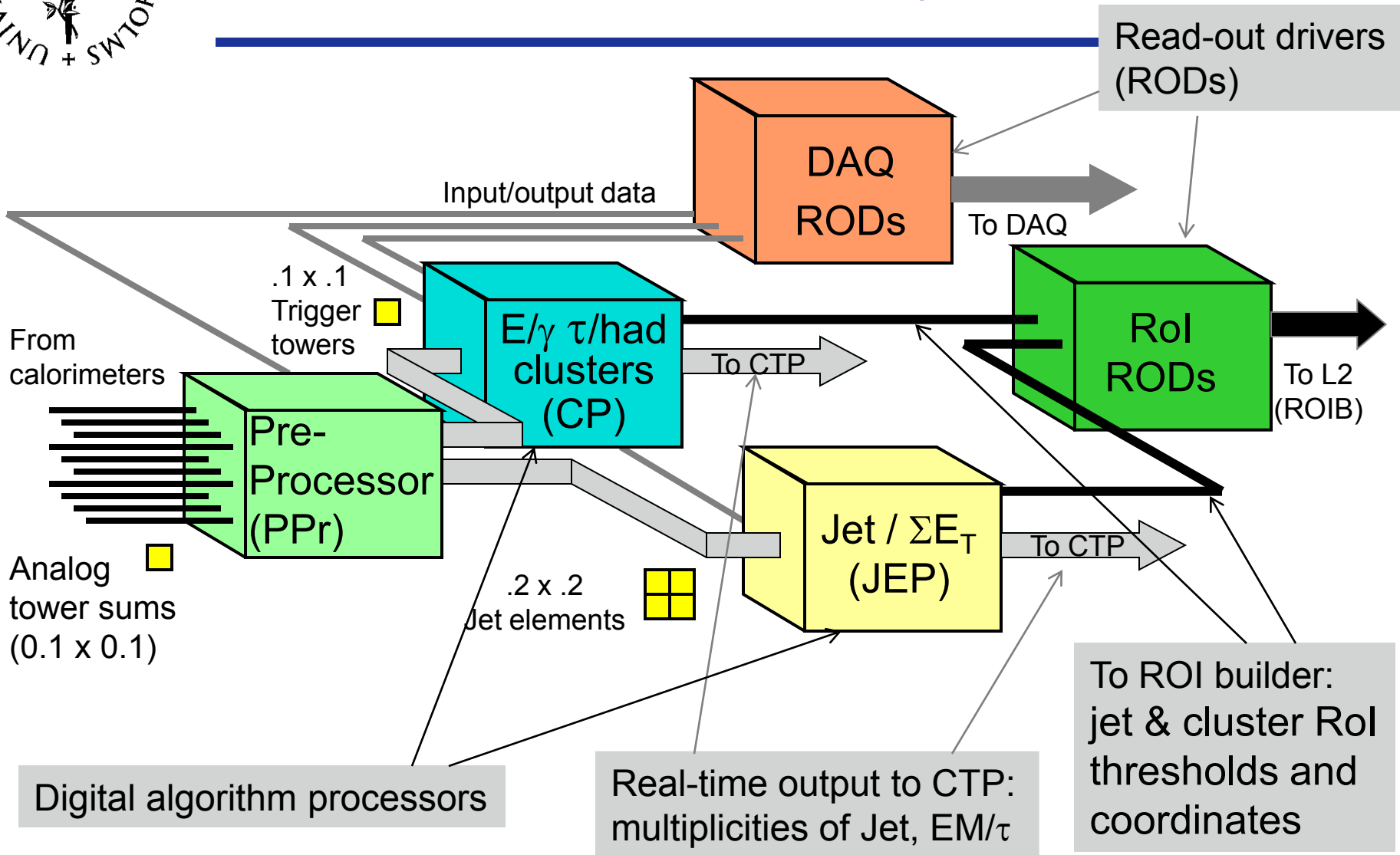
For ATLAS TDAQ/L1Calo

+ Overview
+ Upgrade to PreProcessor MCM
+ Topological trigger

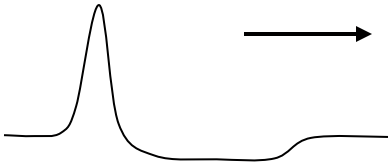
Current L1Calo system



Phase I upgrades to L1Calo

- PreProcessor:
  - New mixed-signal MCM with FPGA
- Topological processing
  - Add RoI coordinates and additional information to the real-time data path
  - Topology-based algorithm processor for L1Calo (plus Muon) RoIs

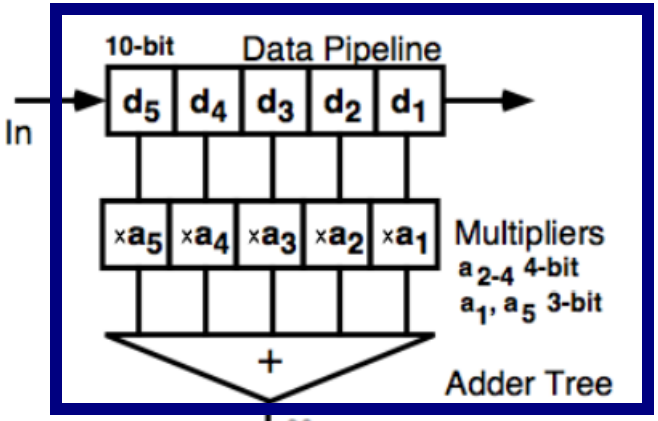
PreProcessor MCM functionality



Analog trigger tower sum
0.1 × 0.1

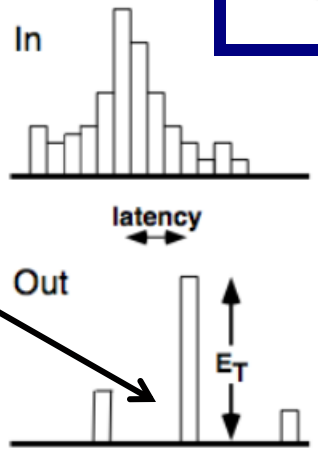
ADC

(1/4)

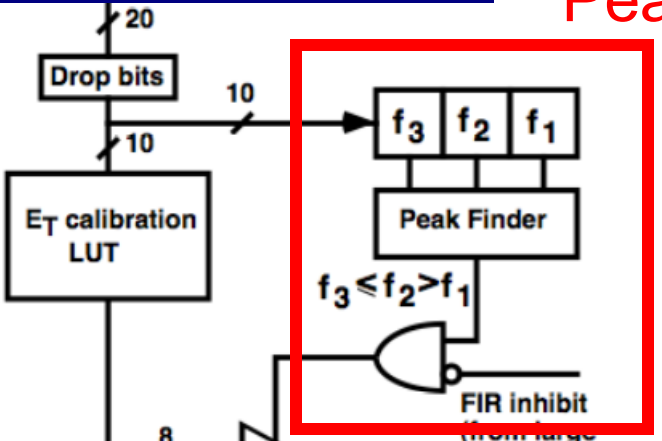


FIR filter
(5 samples)

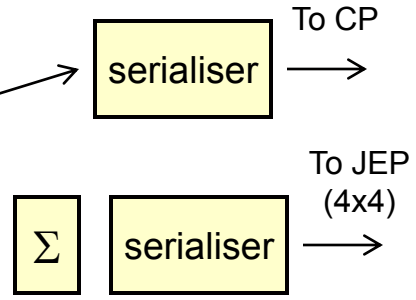
Peak finder



No consecutive non-zero values



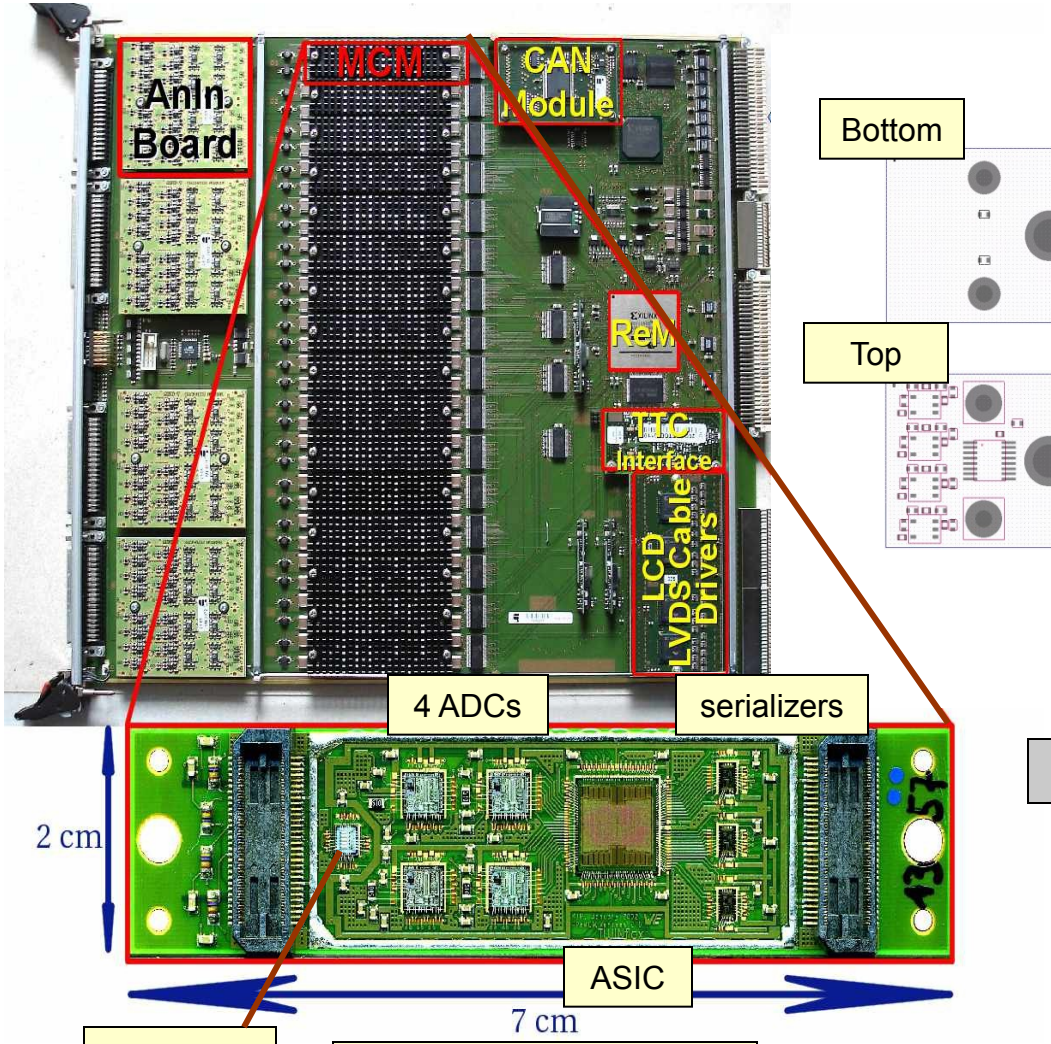
Used to identify bunch crossing



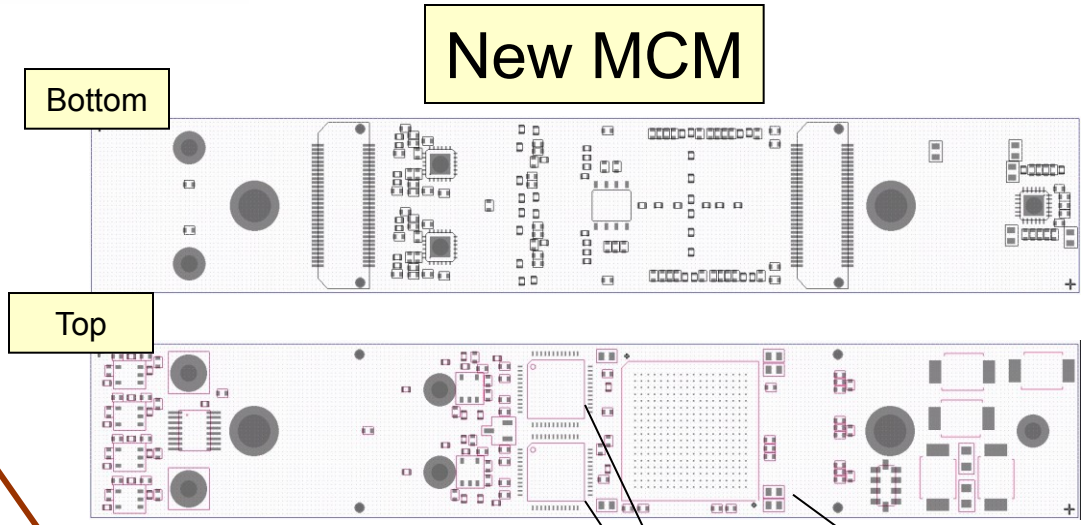
New PreProcessor MCM

- FPGA-based replacement for existing mixed-signal MCM
- Motivations
  - Drop-in replacement if failure rate higher than expected
  - Possible to upgrade digital processing algorithms, e.g.
    - Improve BCID algorithms
    - Compensate for baseline shifting at high luminosity
- Features
  - Two dual-channel FADCs (AD9218)
    - Lower power consumption/channel
    - Run at 80 MHz clock rate (latency reduction)
  - Replace several digital chips with single FPGA (Spartan 6):
    - Adjustable fine delay for ADC clocks
    - PreProcessor ASIC
    - 480 Mbit/s LVDS serialisers to CP and JEP

PreProcessor MCM upgrade



Current MCM

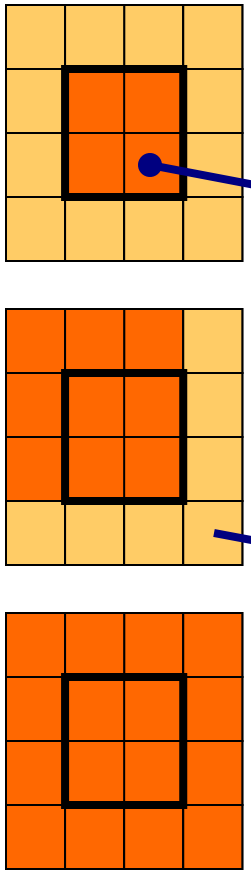


Topological processing

- Motivations
  - Reduce rates while saving physics efficiency
    - Current triggers are multiplicity based
    - Higher thresholds lose physics, less effective with pileup
  - Minimum changes to L1Calo system, rest of experiment
- Adding topology to L1Calo:
  - Keep present data granularity, Jet and EM/τ cluster algorithms
  - Add RoI coordinates and information to real time data path
    - New firmware in existing processor modules
    - Higher backplane speed to increase RTDP bandwidth
    - Replace data merging modules in crates with new boards
      - Receive and process high-speed backplane data
      - Send RoIs to topological processor (TP) over high-speed links
  - Topological processor (TP)
    - New subsystem (preferred solution)
    - Pipelined, fixed-latency processing of all RoIs (L1Calo + Muon)

Jet and cluster algorithms

Jet algorithm:



0.4 x 0.4

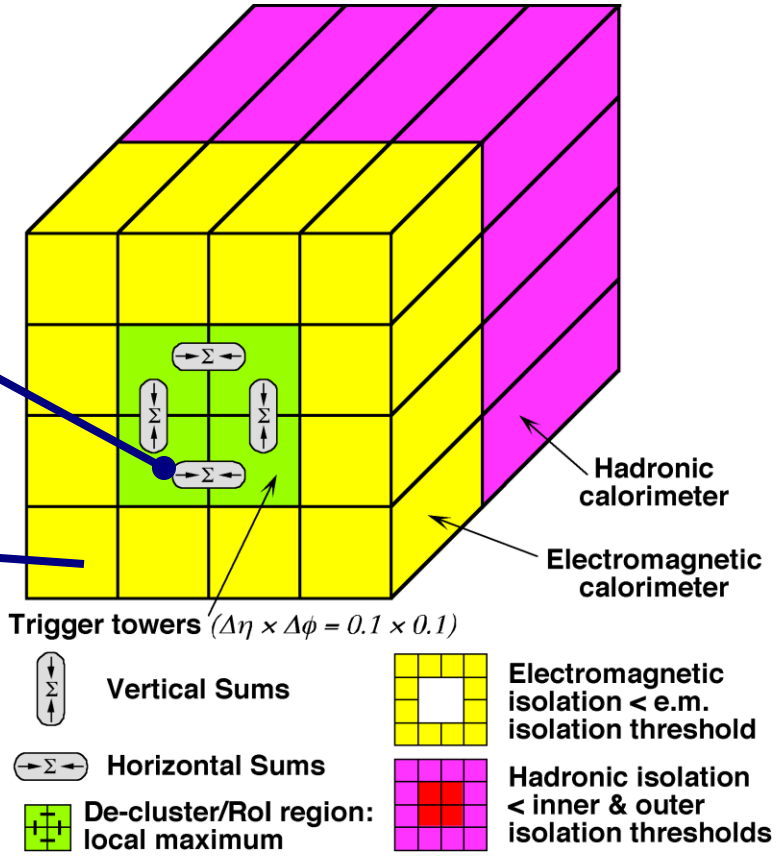
0.6 x 0.6

0.8 x 0.8

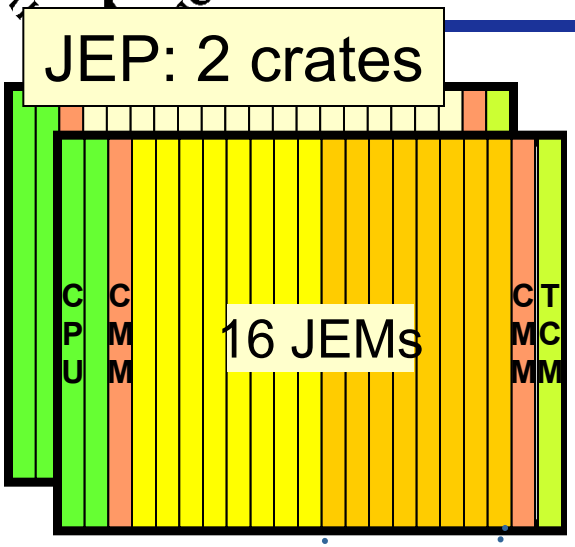
Local maximum

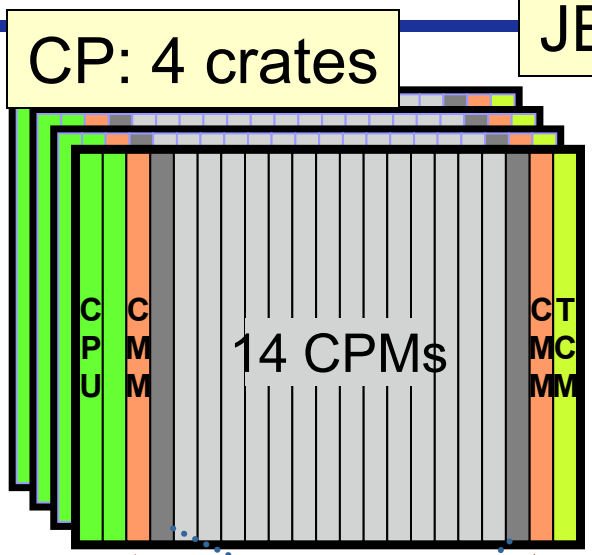
"Environment"

EM cluster algorithm (τ/had similar):



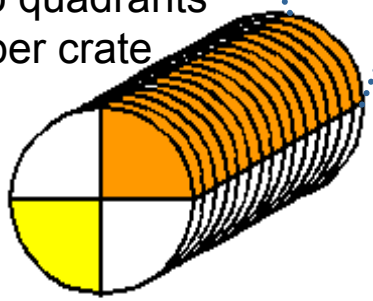
Digital algorithm processors



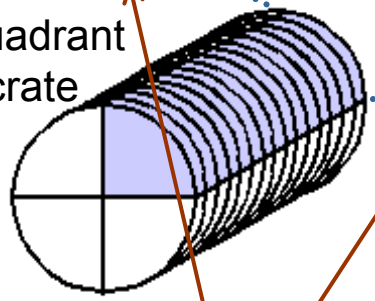


JEM

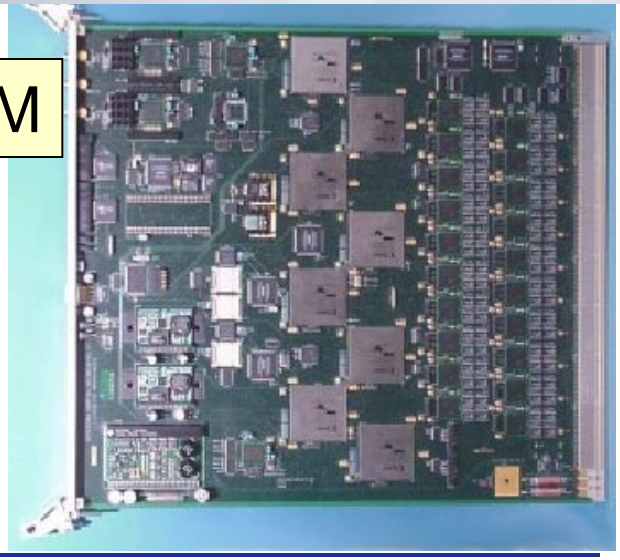
Two quadrants per crate



One quadrant per crate



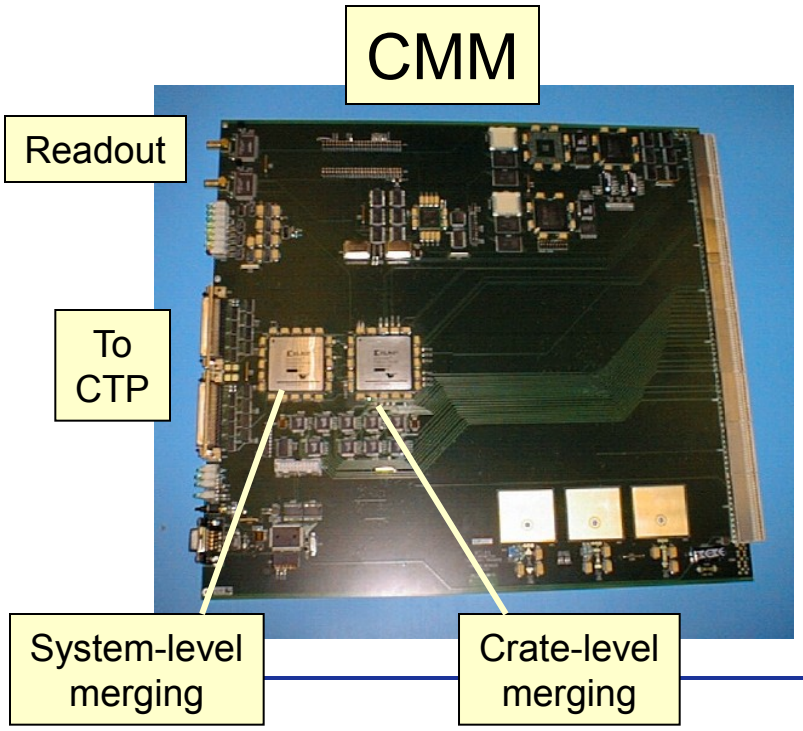
CPM

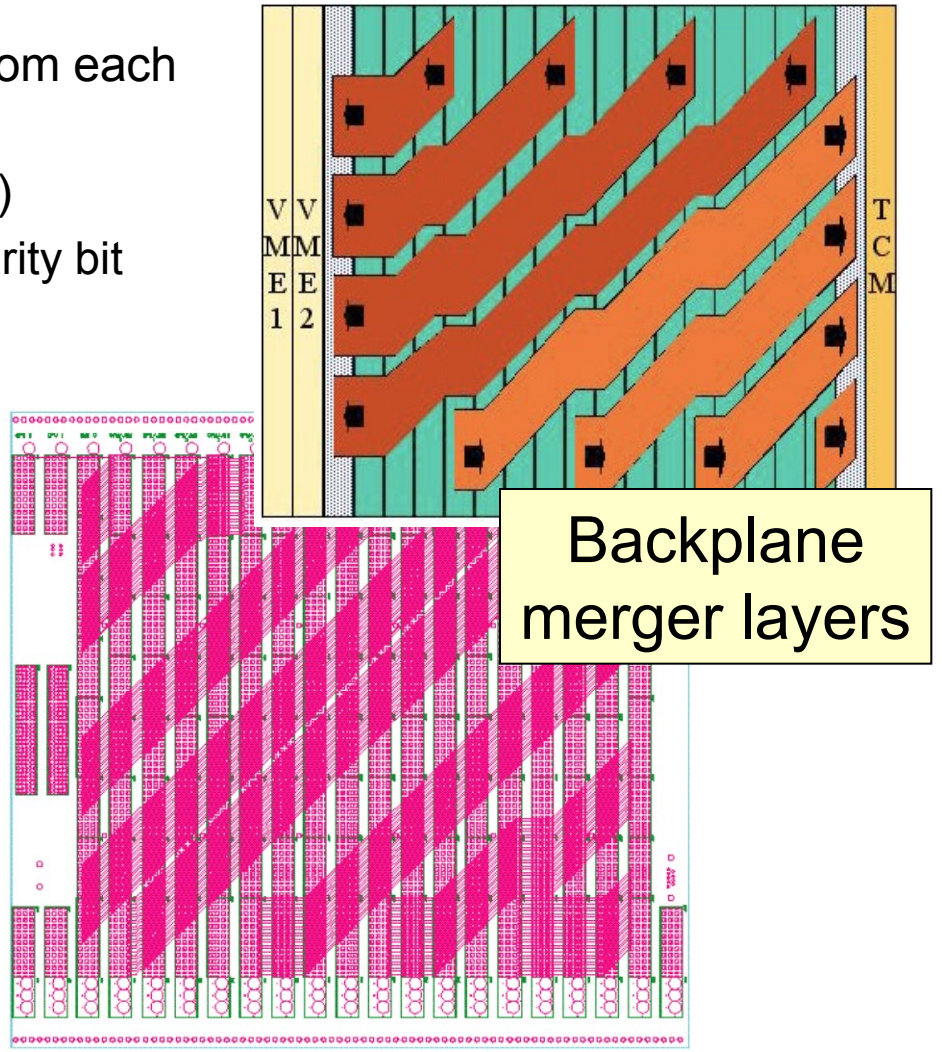


2 merger modules (CMM) collect real-time results from all CPMs/JEMs in the crate

Data merger module: CMM

- 25 point-to-point backplane links from each JEM/CPM to each CMM
- Current speed 40 MHz (25 bits/BC)
  - e.g. 8 × 3-bit multiplicities + 1 Parity bit

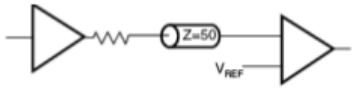


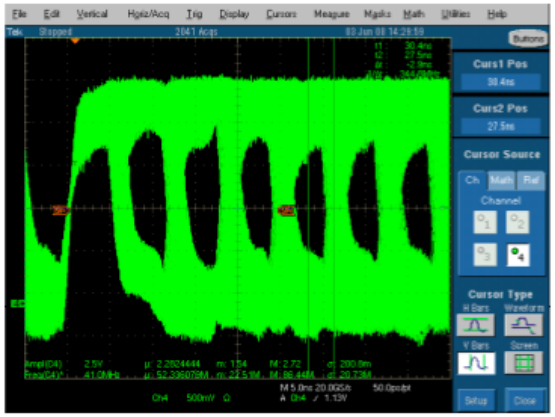


Higher backplane bandwidth

- Backplane can run at >320 Mbit/s (8 × current)
  - (given fast transmitter, optimum termination)
- Actual limit: FPGA outputs on CPM and JEM
  - Both work well at 160 Mbit/s (4 × current)

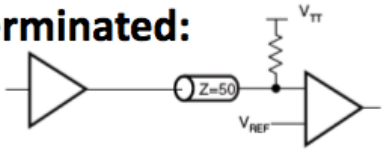
Series terminated:

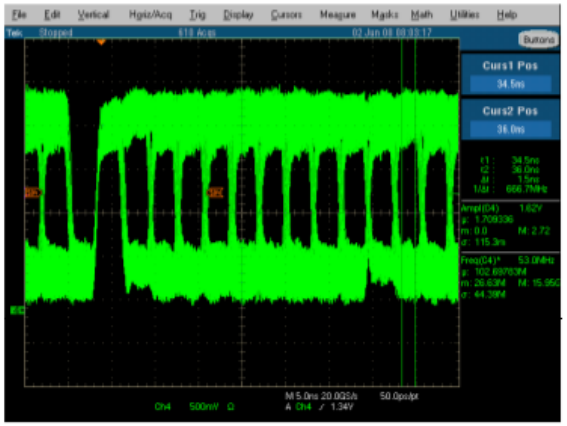




160 Mbits, CMOS 2.5V

Parallel terminated:

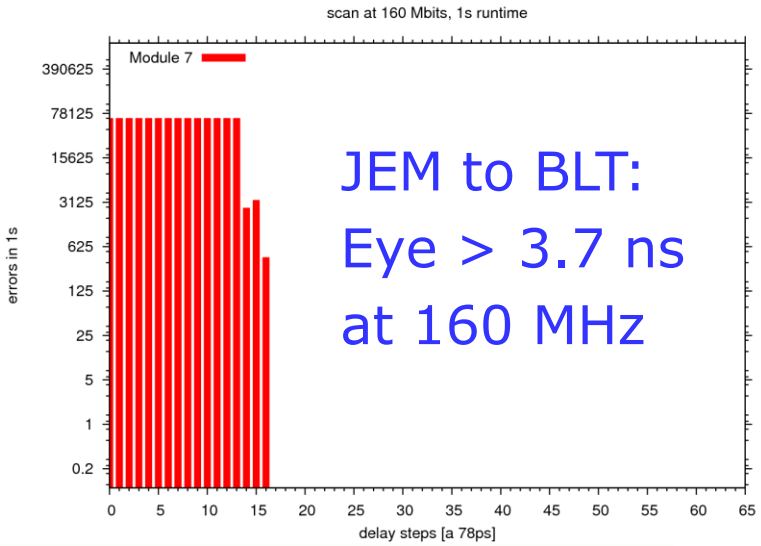




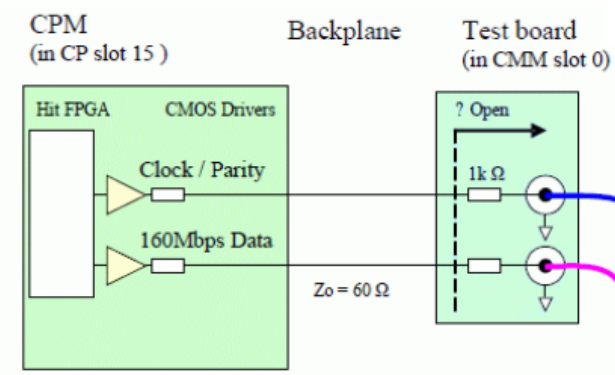
320 Mbits, CMOS 2.5V

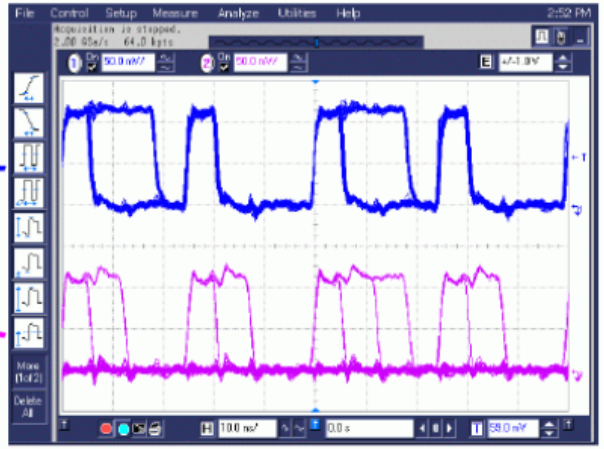
Transmission tests

Backplane link tester (BLT)

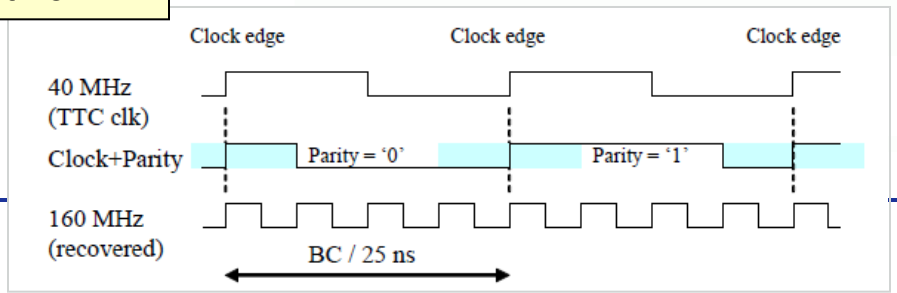


JEM to BLT:
Eye > 3.7 ns
at 160 MHz





Clock and parity encoded together on bit 25:



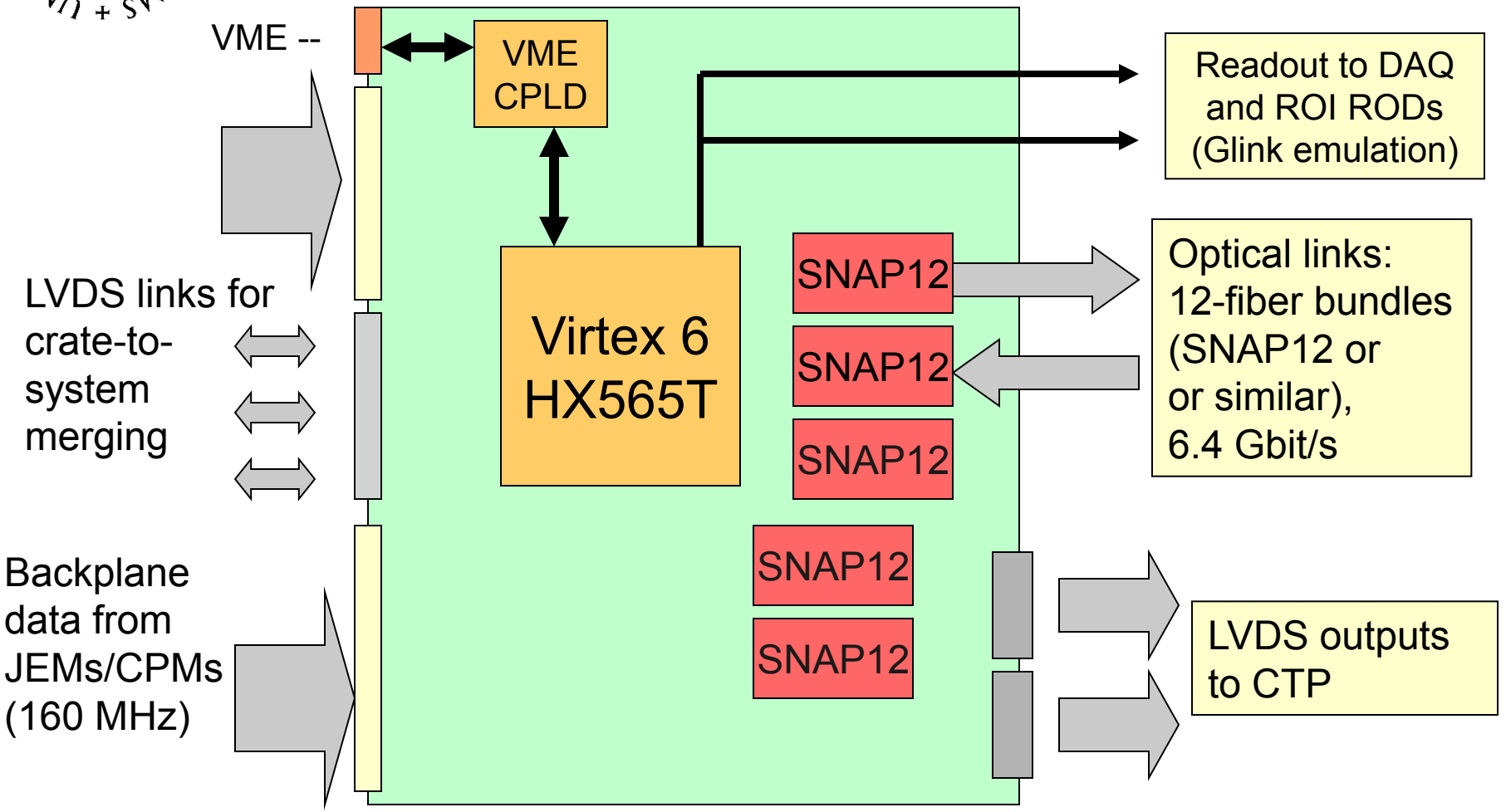
160 MHz transmission from CPM

Adding RoIs to backplane data

- Example: proposed 96-bit jet output
  - 4 × 24 bits at 160 MHz (25th bit used for clock + parity)
  - 8 "presence bits" (Which of the 8 subregions had an RoI?)
  - Report up to 4 RoIs (expect < 2 per JEM)
    - 2 fine position bits (localize jet to 0.2 × 0.2 coordinates)
    - 8 threshold bits
    - Up to 12 additional bits per RoI
      - For example, jet E_T

<table>
<tr><td>P1</td><td>P2</td><td>P3</td><td>P4</td><td>P5</td><td>P6</td><td>P7</td><td>P8</td><td colspan="4">Threshold bits RoI 1 (8b)</td><td colspan="4">Threshold bits RoI 2 (8b)</td></tr>
<tr><td colspan="2">Fine Pos RoI 1</td><td colspan="2">Fine Pos RoI 2</td><td colspan="2">Fine pos RoI 3</td><td colspan="2">Fine Pos RoI 4</td><td colspan="4">Threshold bits RoI 3 (8b)</td><td colspan="4">Threshold bits RoI 4 (8b)</td></tr>
<tr><td colspan="8">Jet RoI 1 E_T (12b)</td><td colspan="8">Jet RoI 2 E_T (12b)</td></tr>
<tr><td colspan="8">Jet RoI 3 E_T (12b)</td><td colspan="8">Jet RoI 4 E_T (12b)</td></tr>
</table>

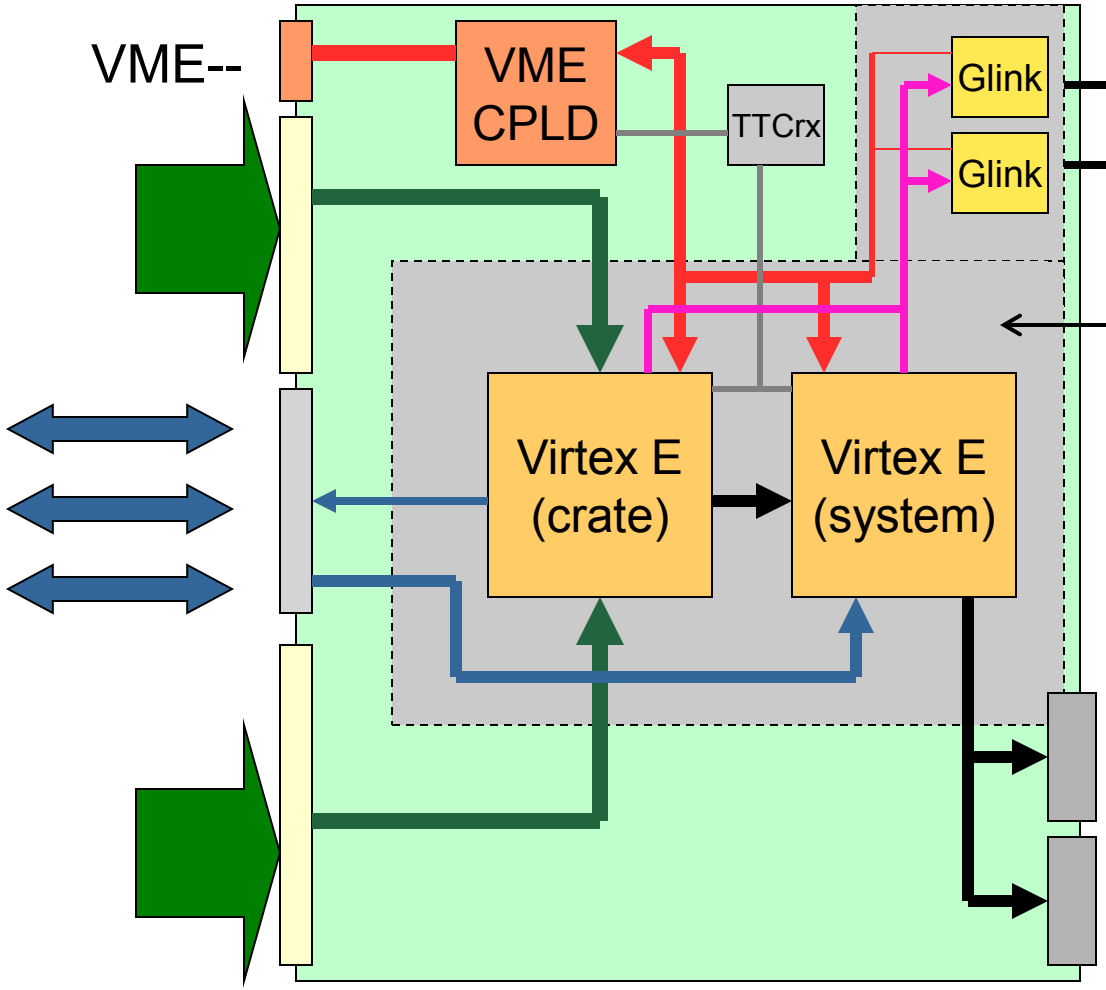
CMM replacement: CMM++



Must be backward-compatible with existing CMM

CMM++ firmware studies

Device: Virtex 6
(XC6VHX565T-2FF1924)



Backward-compatible Jet firmware, including jet and system FPGAs, emulated Glinks

(based on production CMM VHDL code)

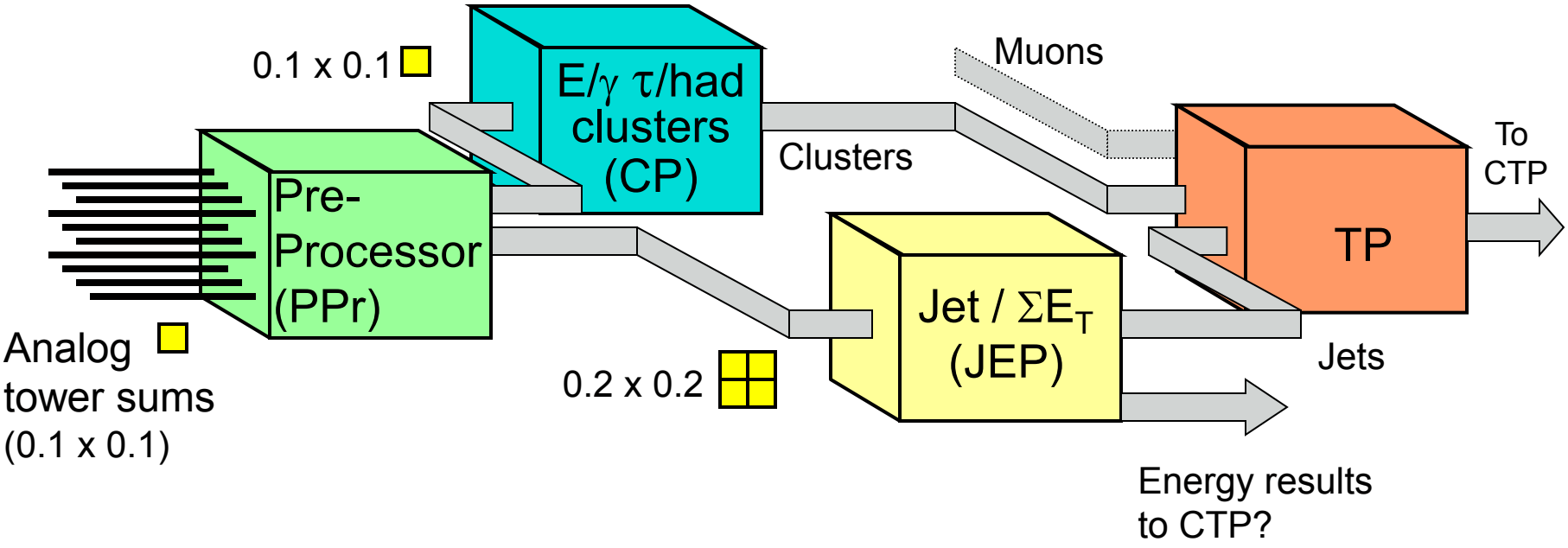
"Legacy" design uses
~ 2% of internal resources;
Plenty of room left....

2-3x faster than Virtex E

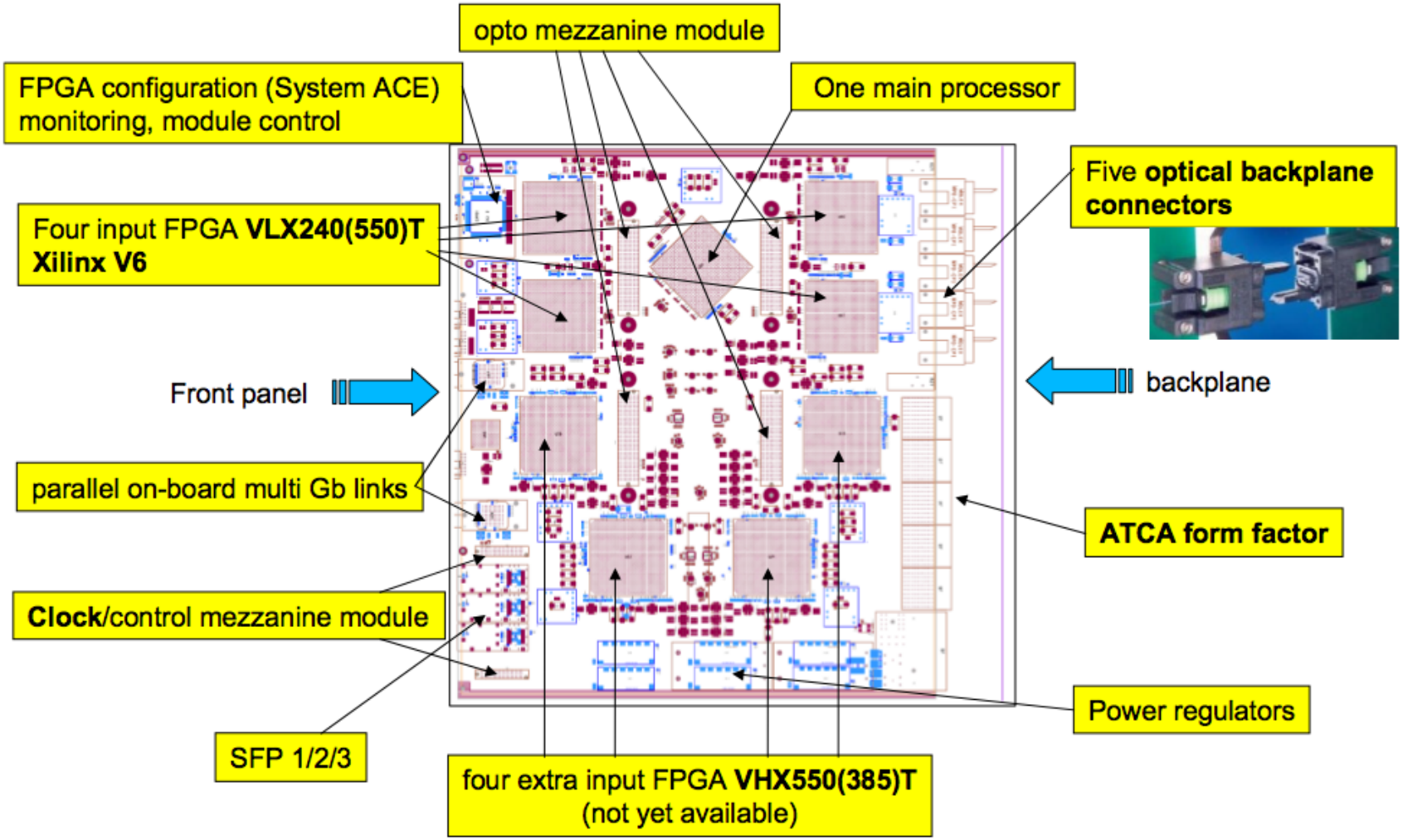
Topological processor (TP)

- Two options being considered:
  - Preferred: New topological processor (TP) subsystem
    - Modern technology / form factor (Virtex 6/ATCA)
    - Receive and process all L1Calo RoIs
    - Able to include Muon RoIs
  - Backup: Topological algorithms in CMM++
    - Connect fiber links in a star configuration, with one CMM++ as the TP
    - Process all jet, CP RoIs
    - No room for muon RoIs
    - More limited algorithm processing (less scalable)

TP subsystem (preferred)

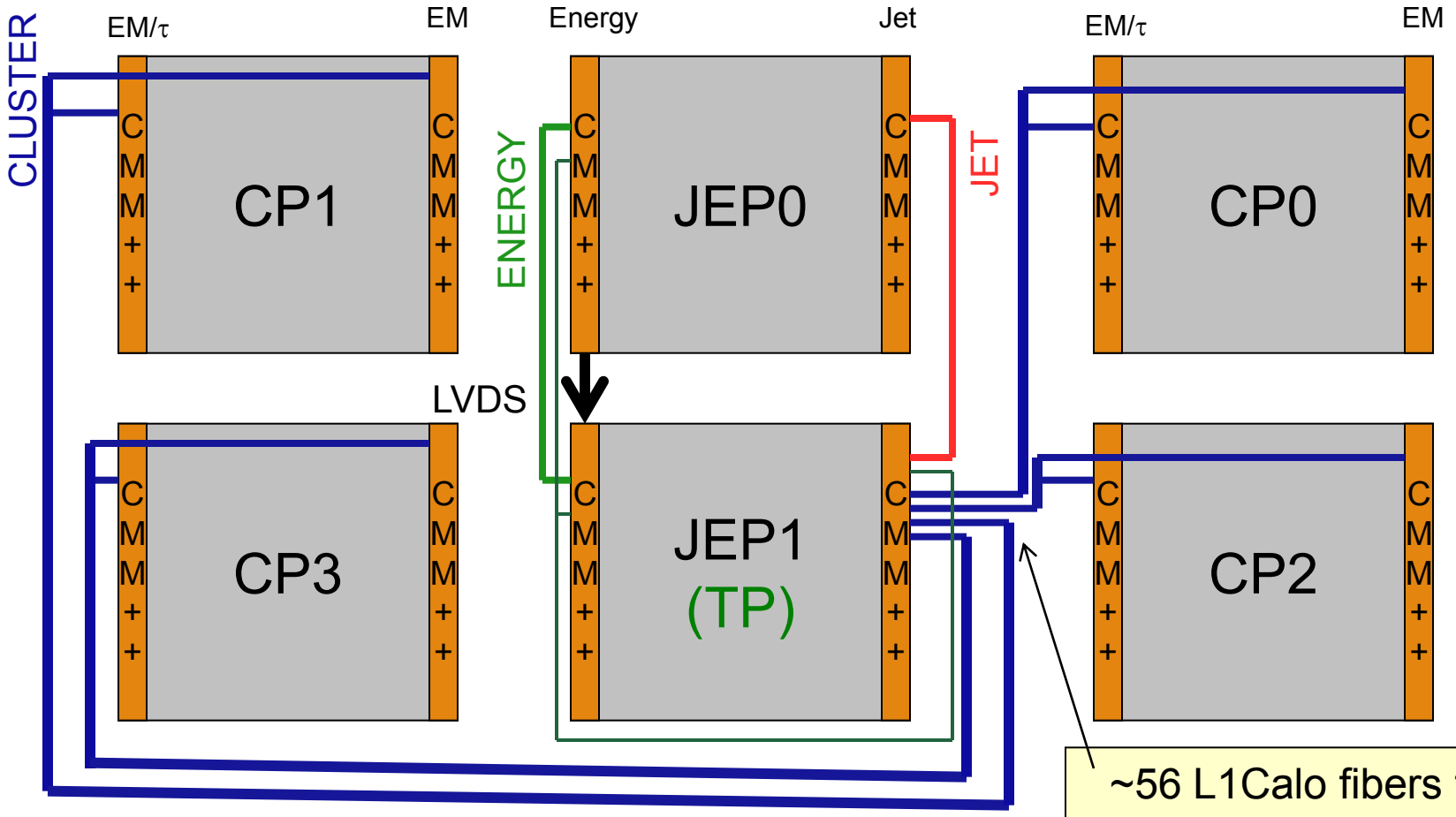


TP technology demonstrator



TP will almost certainly be simpler. Goal of demonstrator is to encounter and learn from problems with high density, high-power ATCA boards

Backup: TP in designated CMM++



Note: Not enough room for muon ROIs

Summary and status

- PreProcessor MCM replacement
  - ASIC code ported to Spartan 6 FPGA, plus serialiser and clock manager functionality
  - PCB layout complete and sent out, expect boards back soon
- CP/JEP crates
  - Backplane transmission tests at 160 MHz look good
  - Studies indicate upgraded firmware in CPMs and JEMs will easily fit and run at full speed
  - CMM++ specifications in early stage, studies of prototype firmware look promising
- Topological Processor (TP)
  - Two options (CMM++ or new TP crate)
  - Technology demonstrator layout nearly complete, soon available for testing