

CMS Detector

Pixels
Tracker
ECAL
HCAL
Solenoid
Steel Yoke
Muons

SILICON TRACKER
Pixels (100 x 150 μm^2)
~1m² ~66M channels
Microstrips (80-180 μm)
~200m² ~9.6M channels

CRYSTAL ELECTROMAGNETIC CALORIMETER (ECAL)
~76k scintillating PbWO₄ crystals

PRESHOWER
Silicon strips
~16m² ~137k channels

STEEL RETURN YOKE
~13000 tonnes

CMS Phase I Muon Trigger Upgrades

Ivan K. Furić
for the CMS collaboration

SUPERCONDUCTING SOLENOID
Niobium-titanium coil
carrying ~18000 A

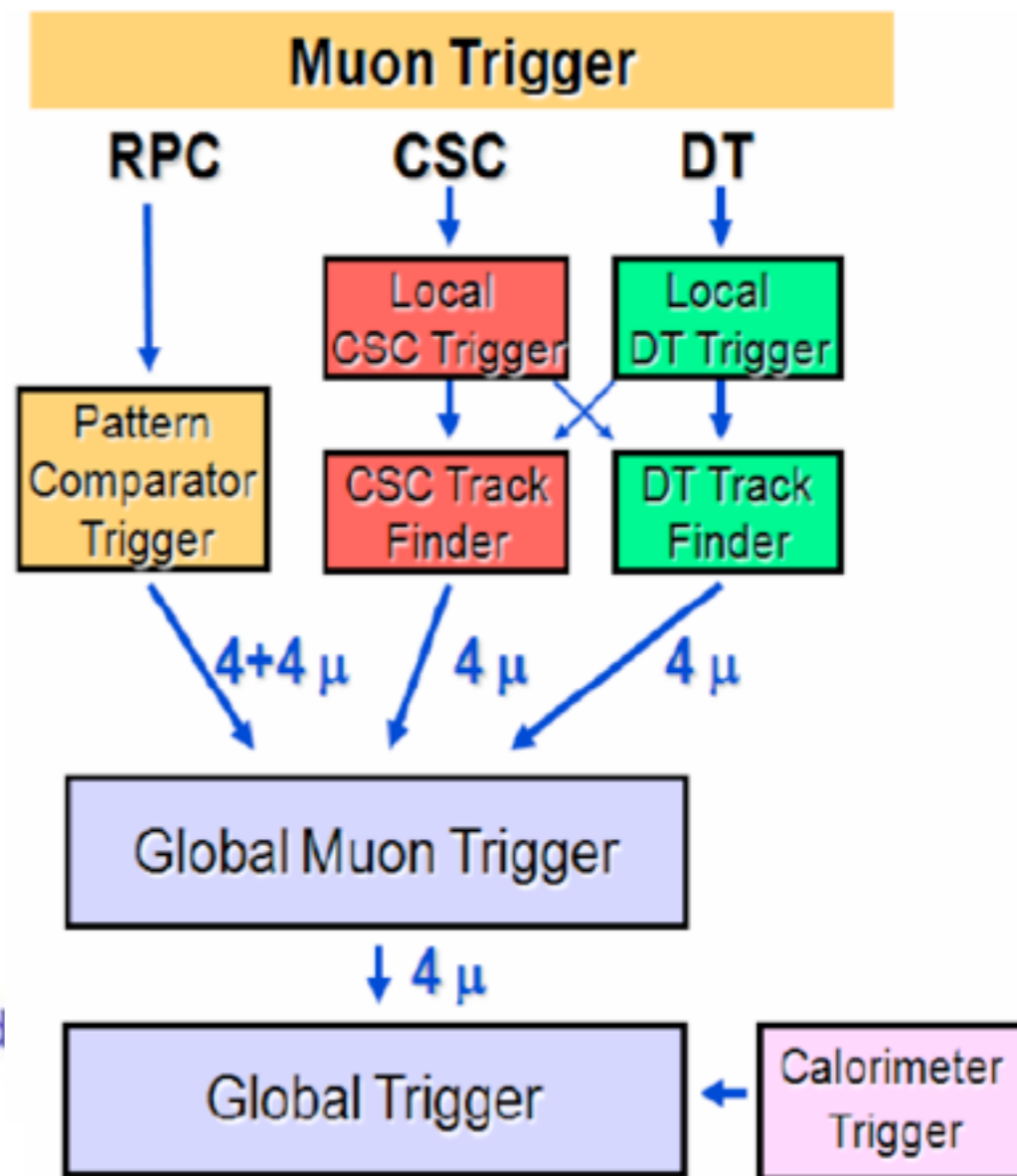
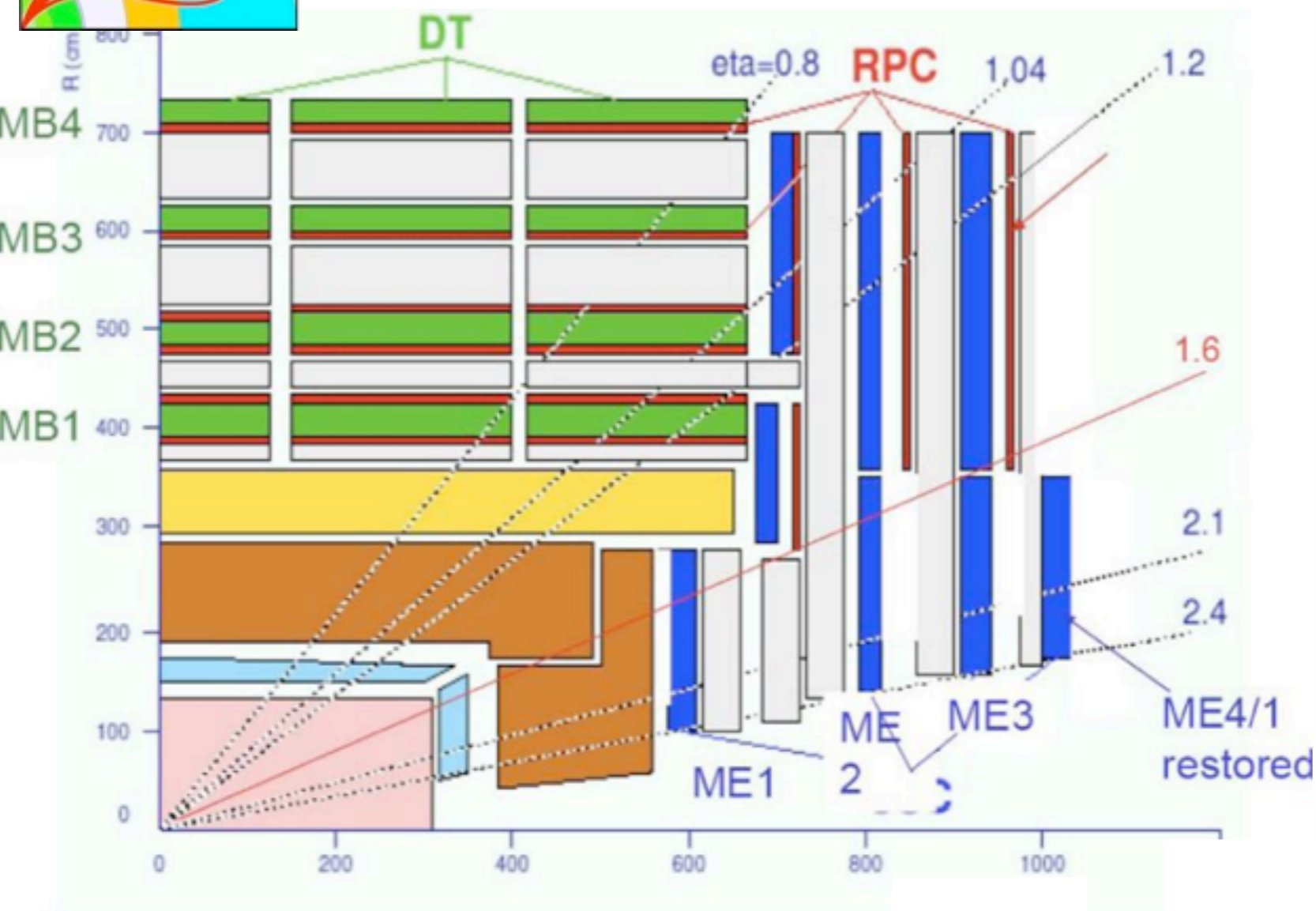
HADRON CALORIMETER (HCAL)
Brass + plastic scintillator
~7k channels

FORWARD CALORIMETER
Steel + quartz fibres
~2k channels

MUON CHAMBERS
Barrel: 250 Drift Tube & 480 Resistive Plate Chambers
Endcaps: 468 Cathode Strip & 432 Resistive Plate Chambers

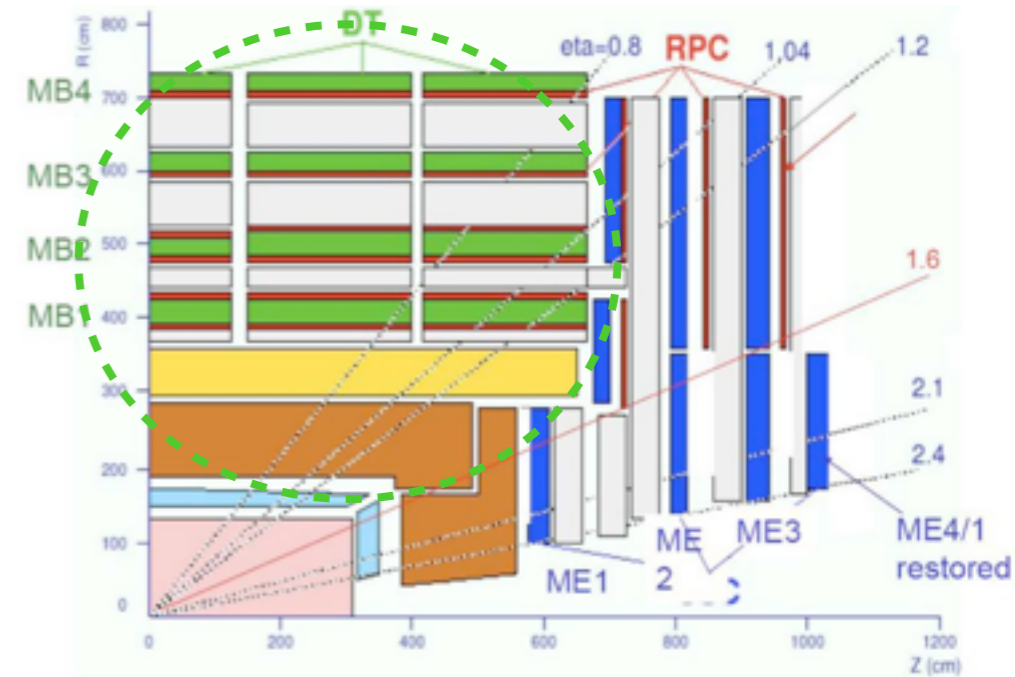
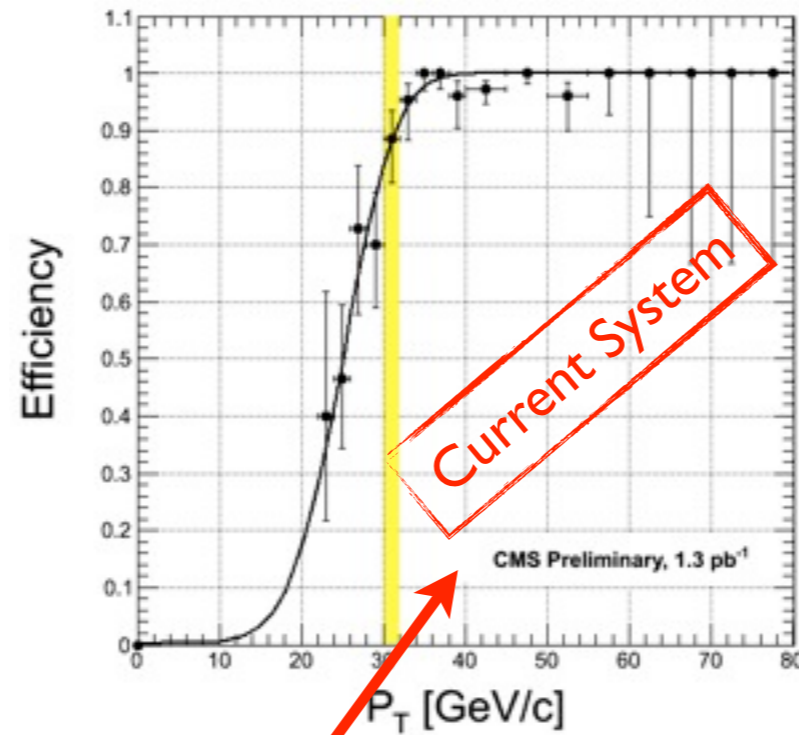
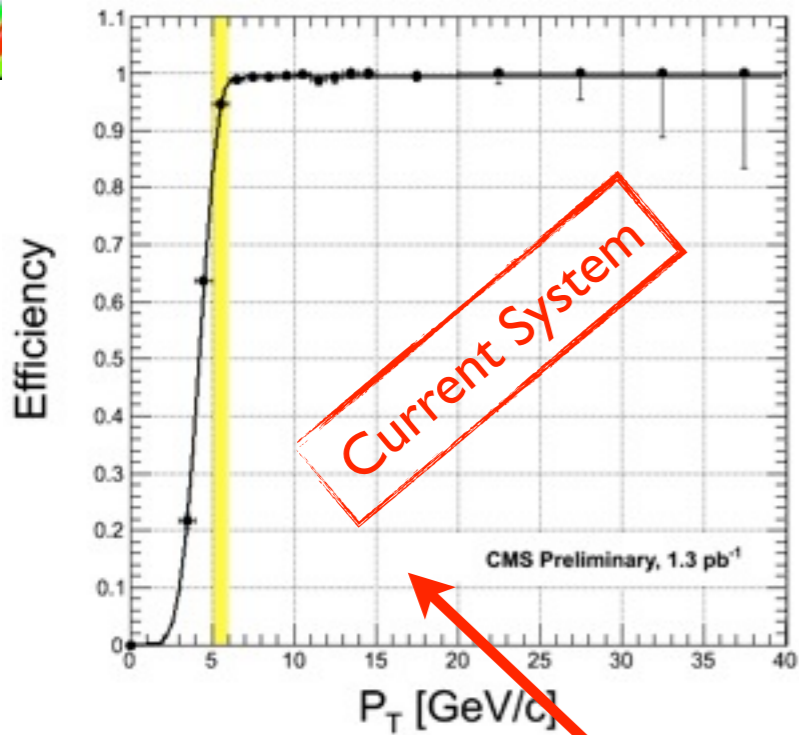
Total weight : 14000 tonnes
Overall diameter : 15.0 m
Overall length : 28.7 m
Magnetic field : 3.8 T

CMS Muon Trigger

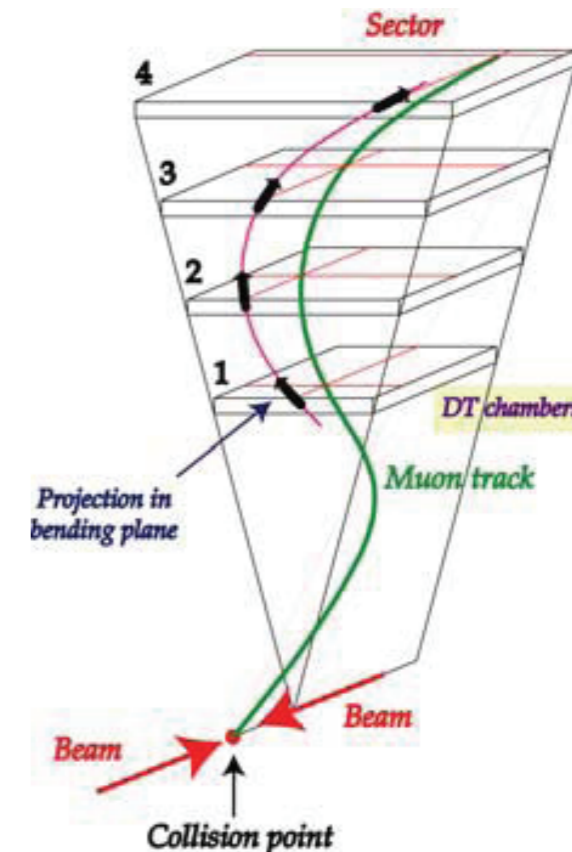


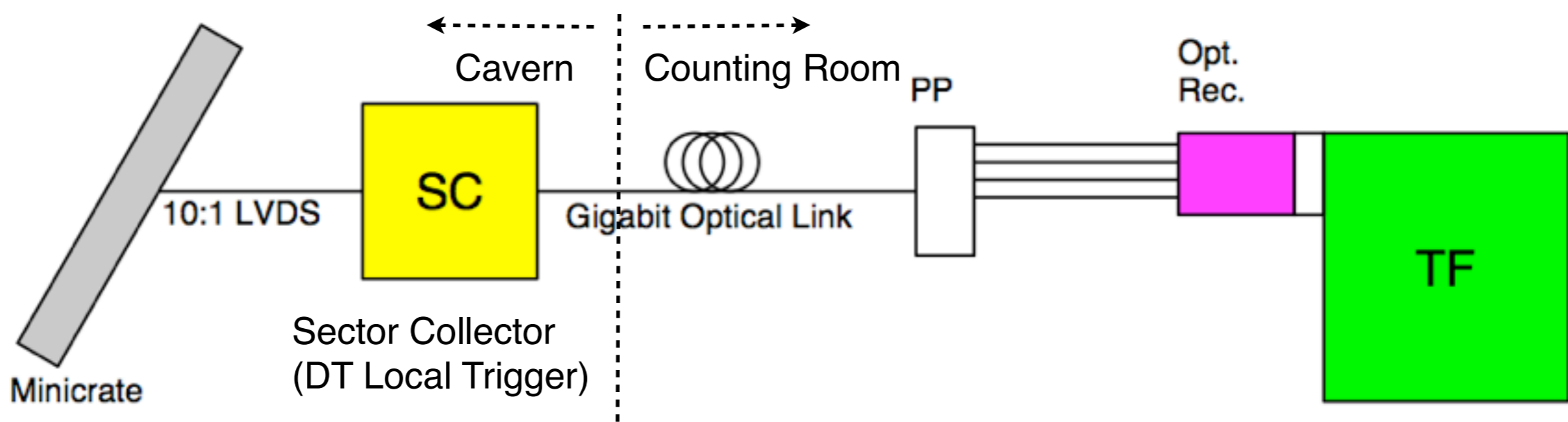
- in this talk: data flow, algorithms, architecture of trigger system (mostly off detector electronics)
- muon electronics upgrade - see talk by M. Matveev at 18:35

DTTF Upgrade Motivation



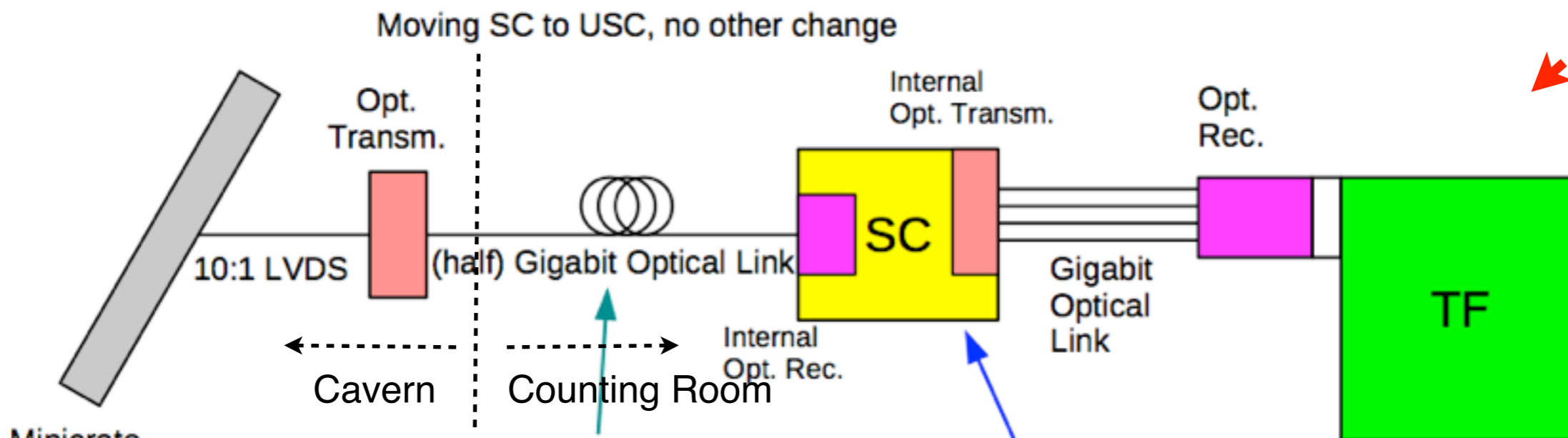
- p_T assignment very close to optimal
- present design based on requirement for low latency
- highly interconnected, high speed parallel links $\sim 35k$ pins input + out
- take advantage of high speed serial links, new FPGAs \rightarrow more flexibility





Moving SC to counting room ...

Track Finder Board
Pattern Recognition
 p_T Assignment

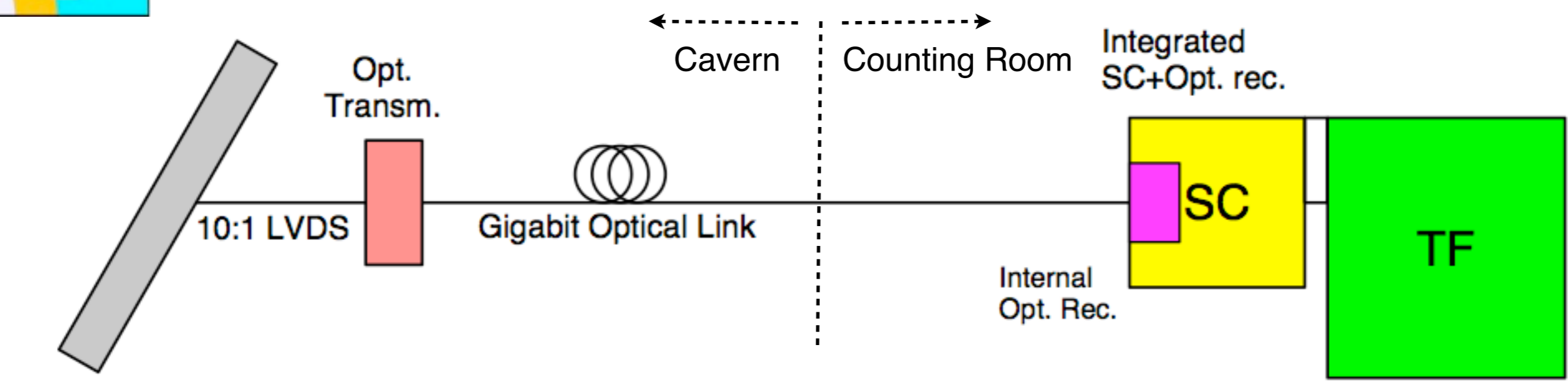


needs to insert a lot of new Optical Cables
(already agreed by the CMS management)

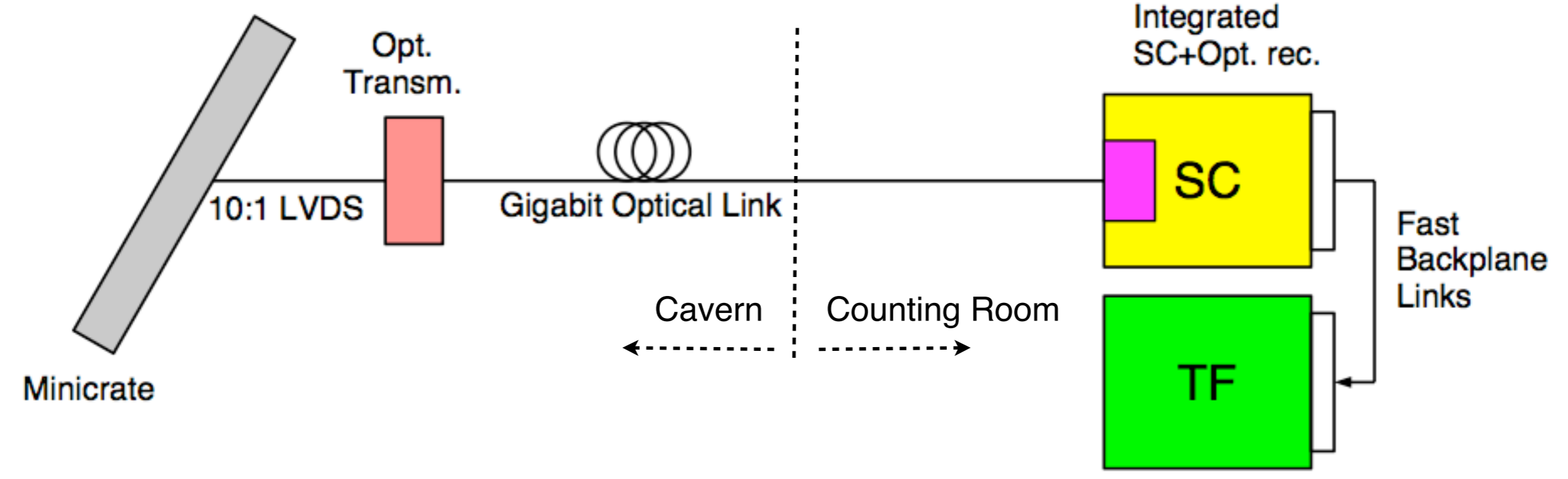
transform data Optical to Electric,
back from Electric to Optical



.. allows design flexibility



SC – Optical Receiver Integration



Trigger Object distribution through fast serial Links (μ TCA)



Drift Tube Track Finder Upgrade Considerations

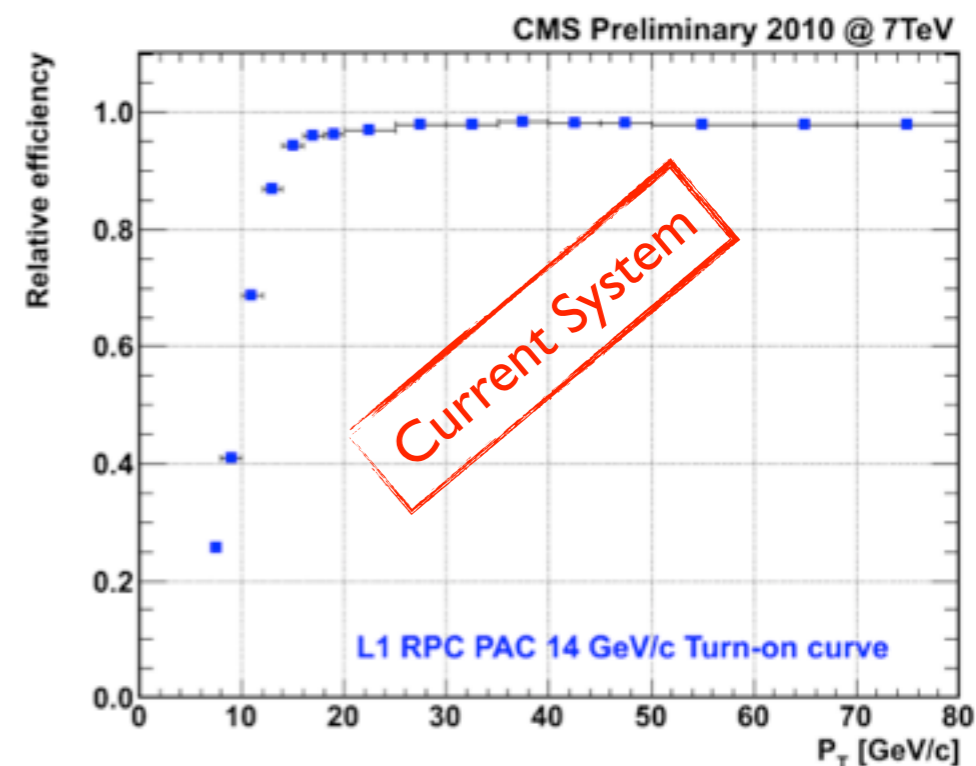
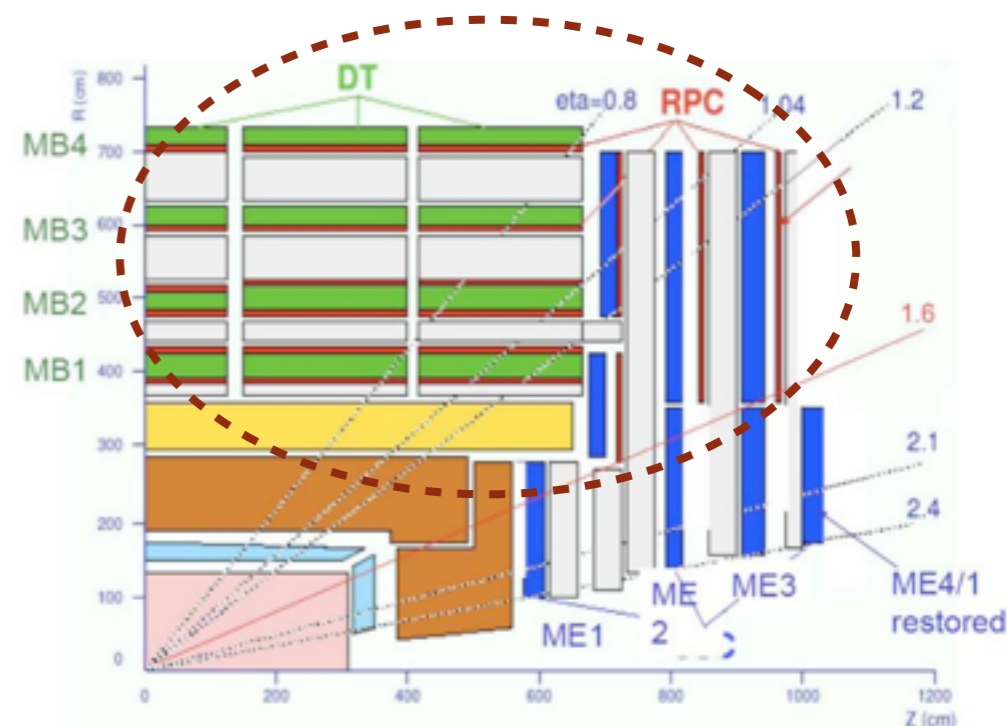
- avoid crate to crate cabling as much as possible
- Currently considering platforms:
 - μ TCA: card size might be too small to fit needed I/O
 - ATCA: more surface per card
 - enough rack space in USC?
 - if possible avoid custom backplanes in design
 - use common CERN design units as much as possible





RPC Trigger Upgrade

- current coverage $|\eta| \leq 1.6$
- p_T assignment performing well
- plan: complete coverage to $|\eta| \leq 2.1$
- current trigger electronics well suited
- working on pattern optimization for high occupancy environment
- high $|\eta|$ triggering difficult due to high occupancy
- $|\eta| \sim 1.6$ difficult for both CSC and RPC triggers in 2/3 configuration - can we add an extra hit in this region?

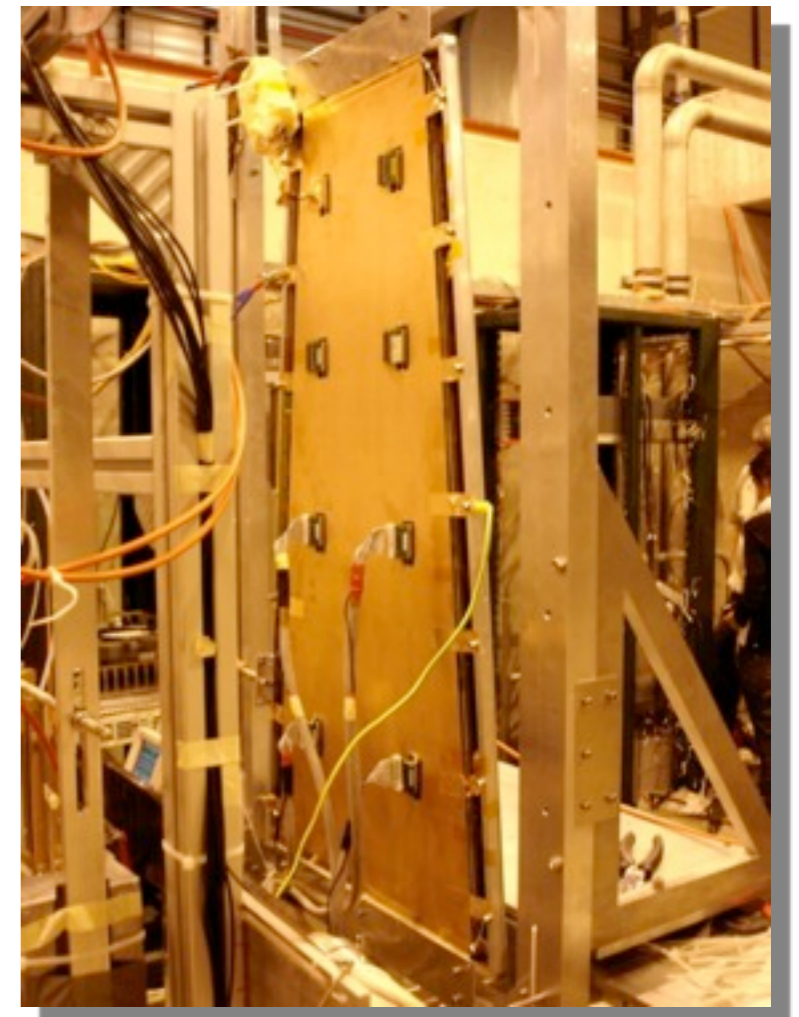




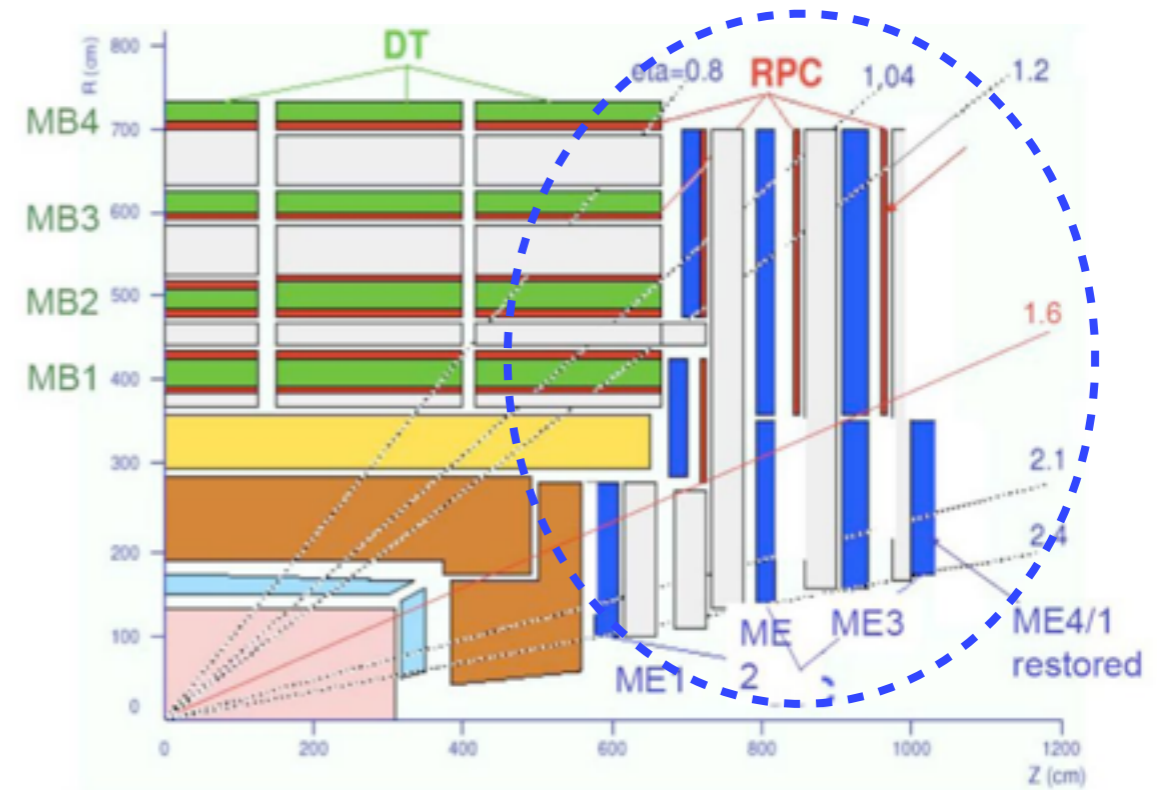
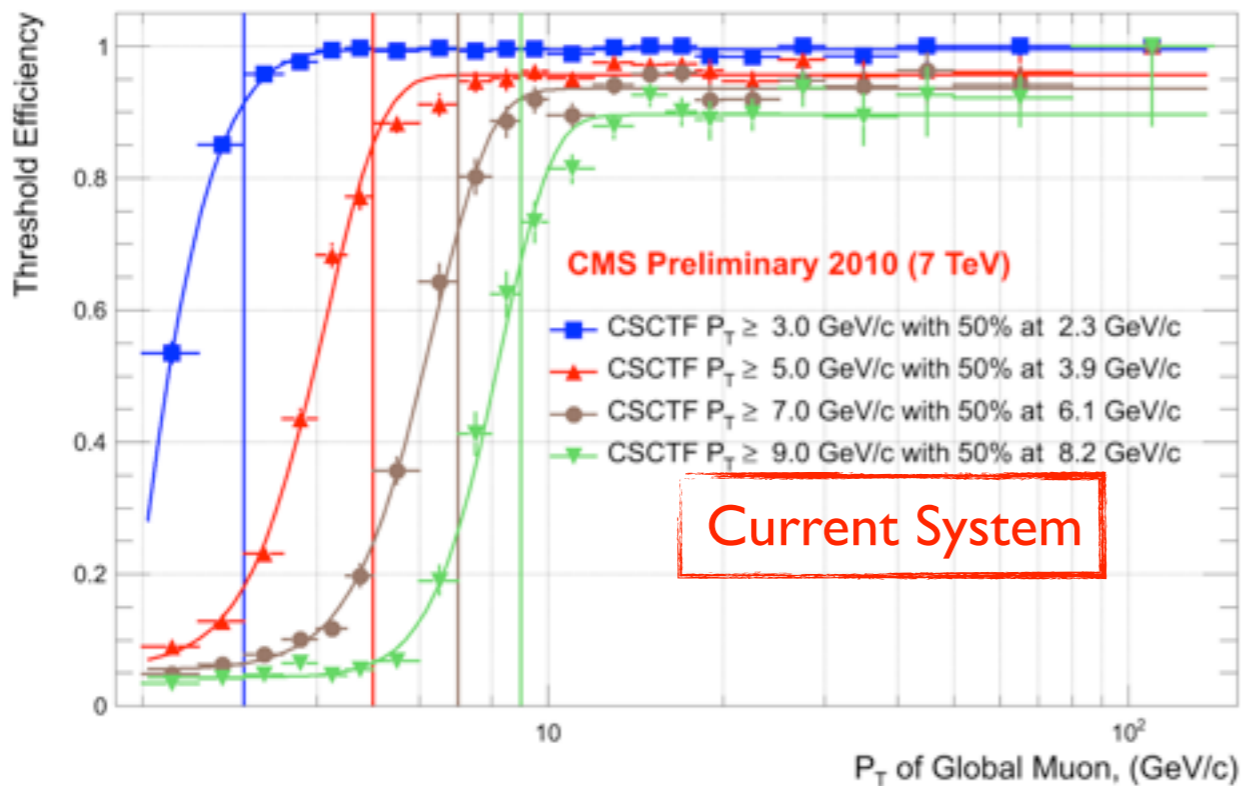
Possible new technology: MPGD Chambers

- rate capability : $10^4/\text{mm}^2$
- space/time resol: $\sim 100 \mu\text{m} / \sim 4\text{-}5 \text{ ns}$
- ideal for high $|\eta|$ + high occupancy
- efficiency $> 98\%$;
excellent long term operation
- gas mixture: Argon - CO₂
(non flammable mixture)
- large area: $\sim 1\text{ m} \times 2\text{ m}$ with industrial processes
- multiple scattering, geometry, offline momentum resolution studies underway
- trigger enhancement with MPGD chamber studies underway in parallel

Large Prototype: GE1/1
BeamTest @ RD51 setup
October 2010



CSCTF Upgrade Motivation

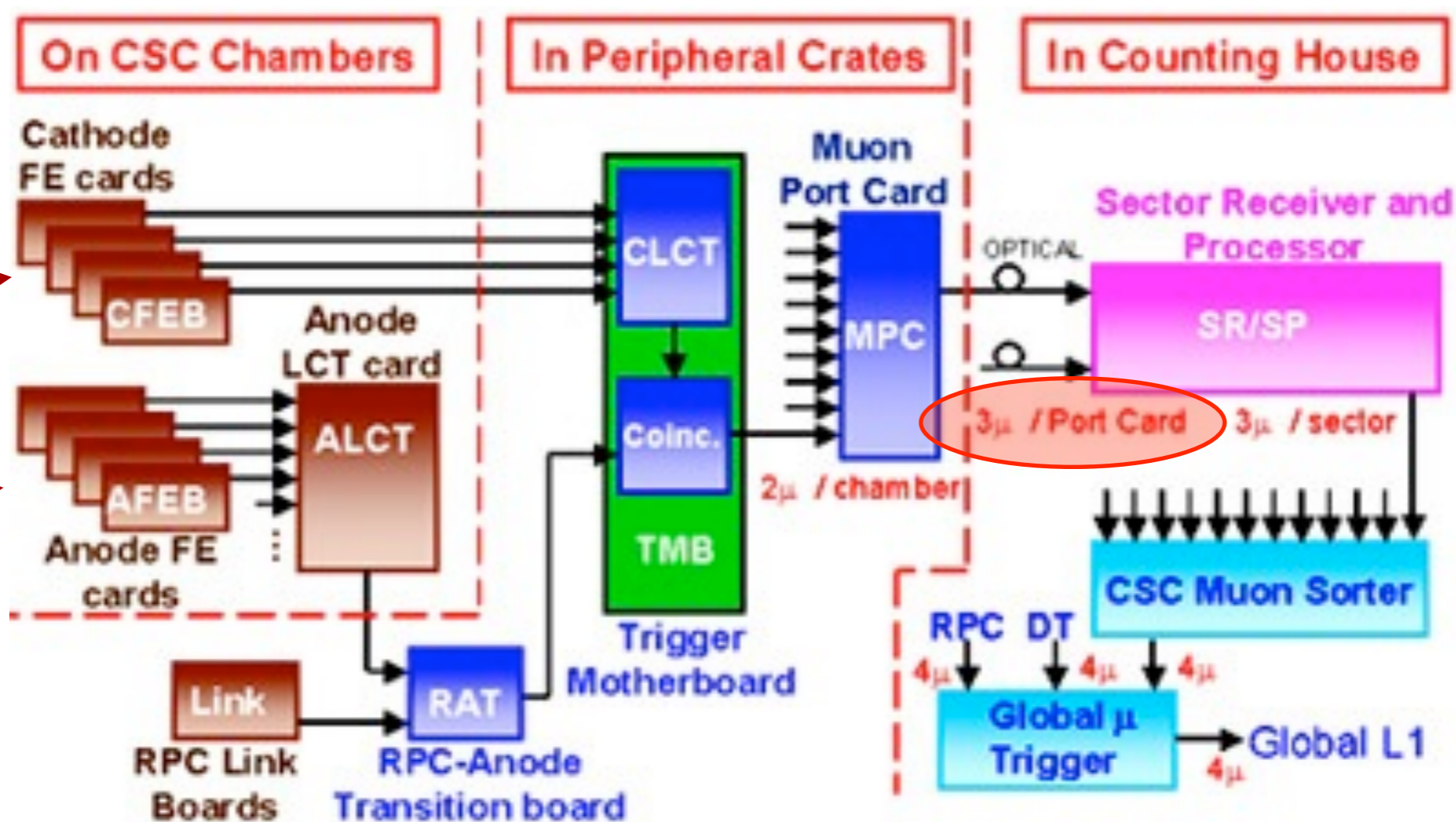


- momentum assignment pretty good, possibly limited by LUT address space
- concern - possible high occupancy in forward region
- improve p_T assignment if possible
- recover efficiency at 30° trigger sector borders



CSCTF Current Data Flow

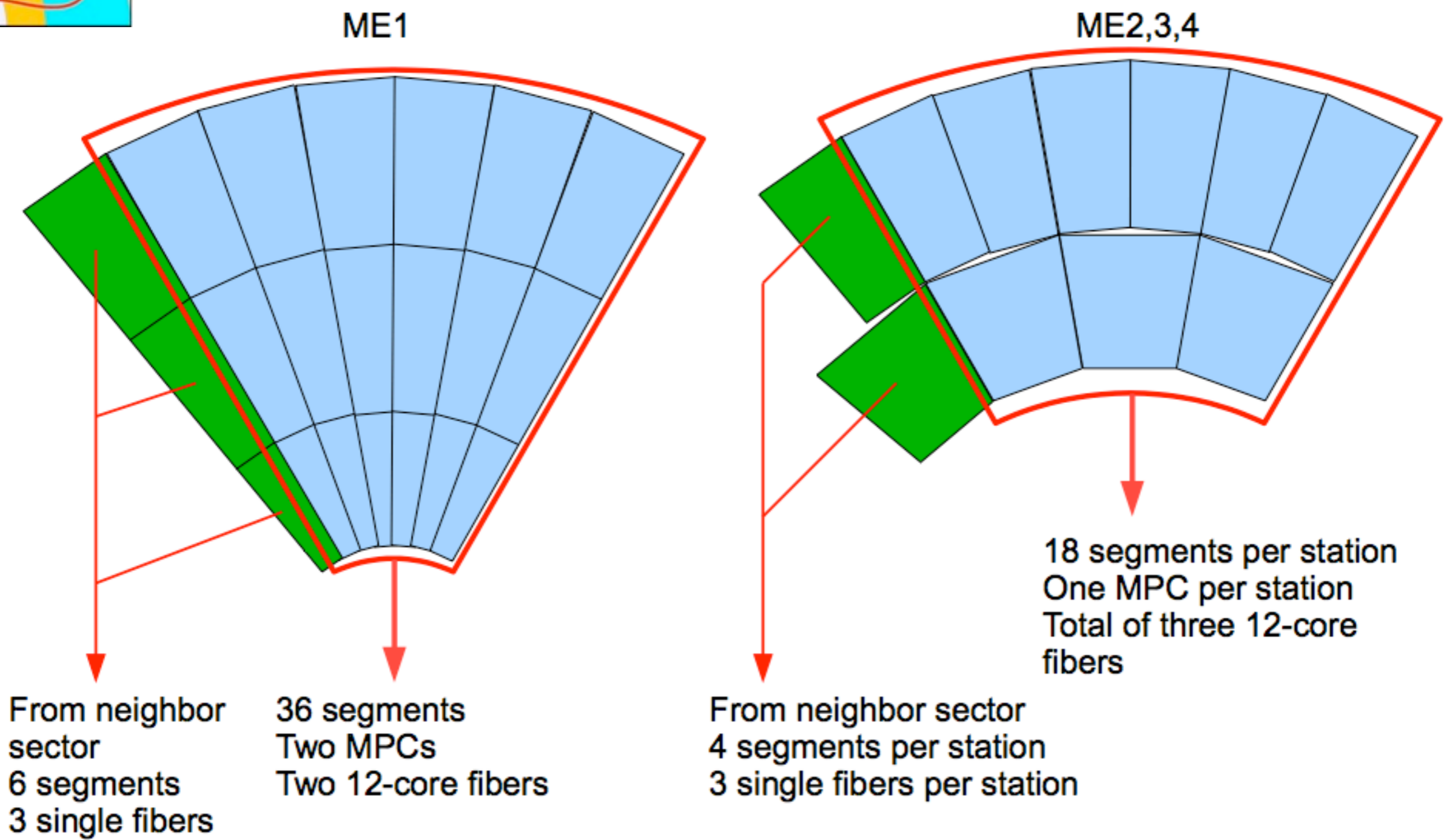
~ hit φ positions
~ hit r positions



- multi-step analysis and reduction designed for “low” occupancy
- in high occupancy environment, 3 primitives per station per 30° sector may become a bottleneck
- pull all stops - allow all L1 primitives into Sector Processor



CSCTF Data Flow Upgrade

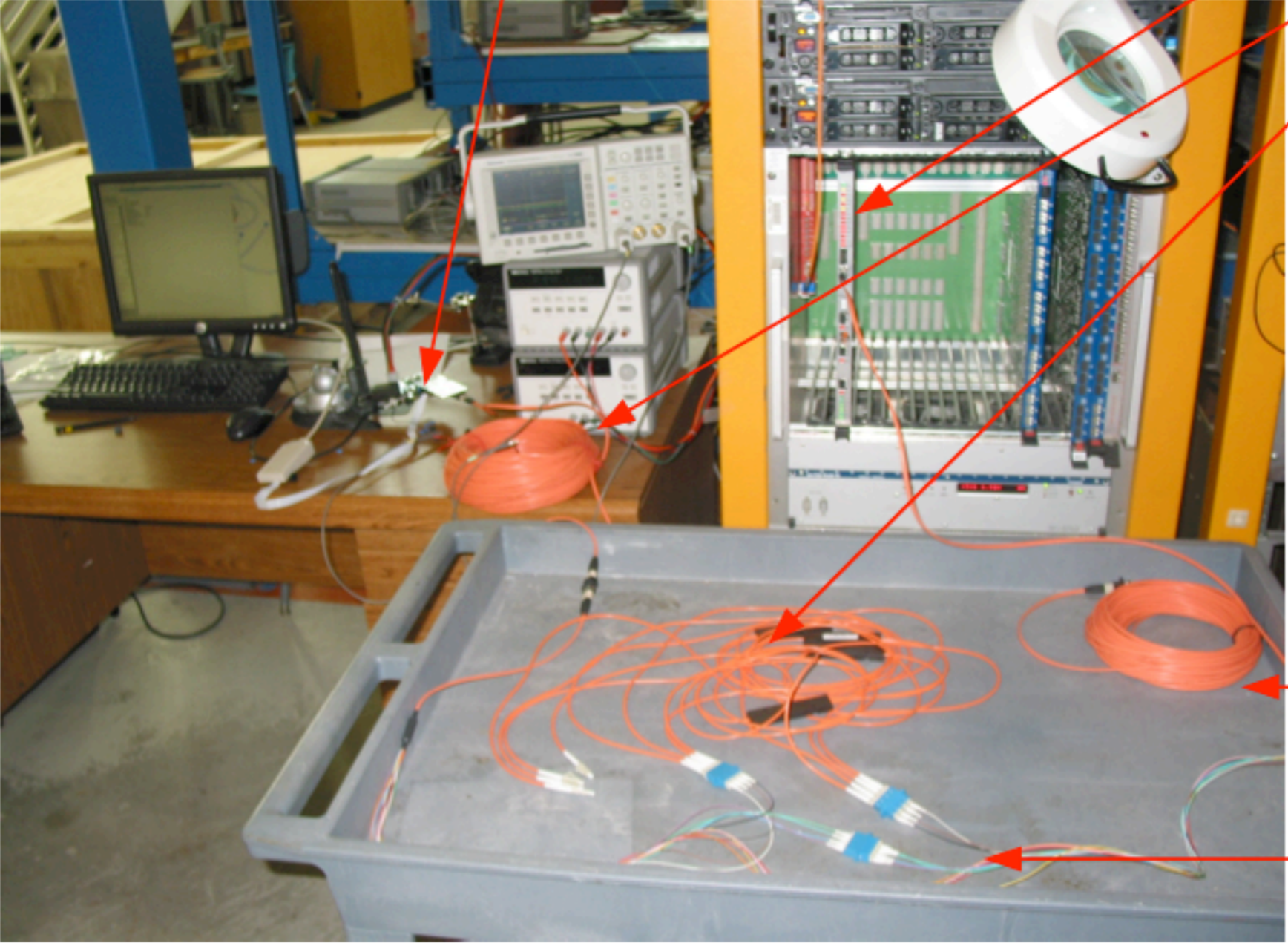




CSCTF Data Flow Demonstrators

Upgrade CSCTF
Sector Processor RX Prototype

Upgrade Muon Port Card
TX Prototype



100-meter 12-core fiber

4 optical splitters
50/50 %

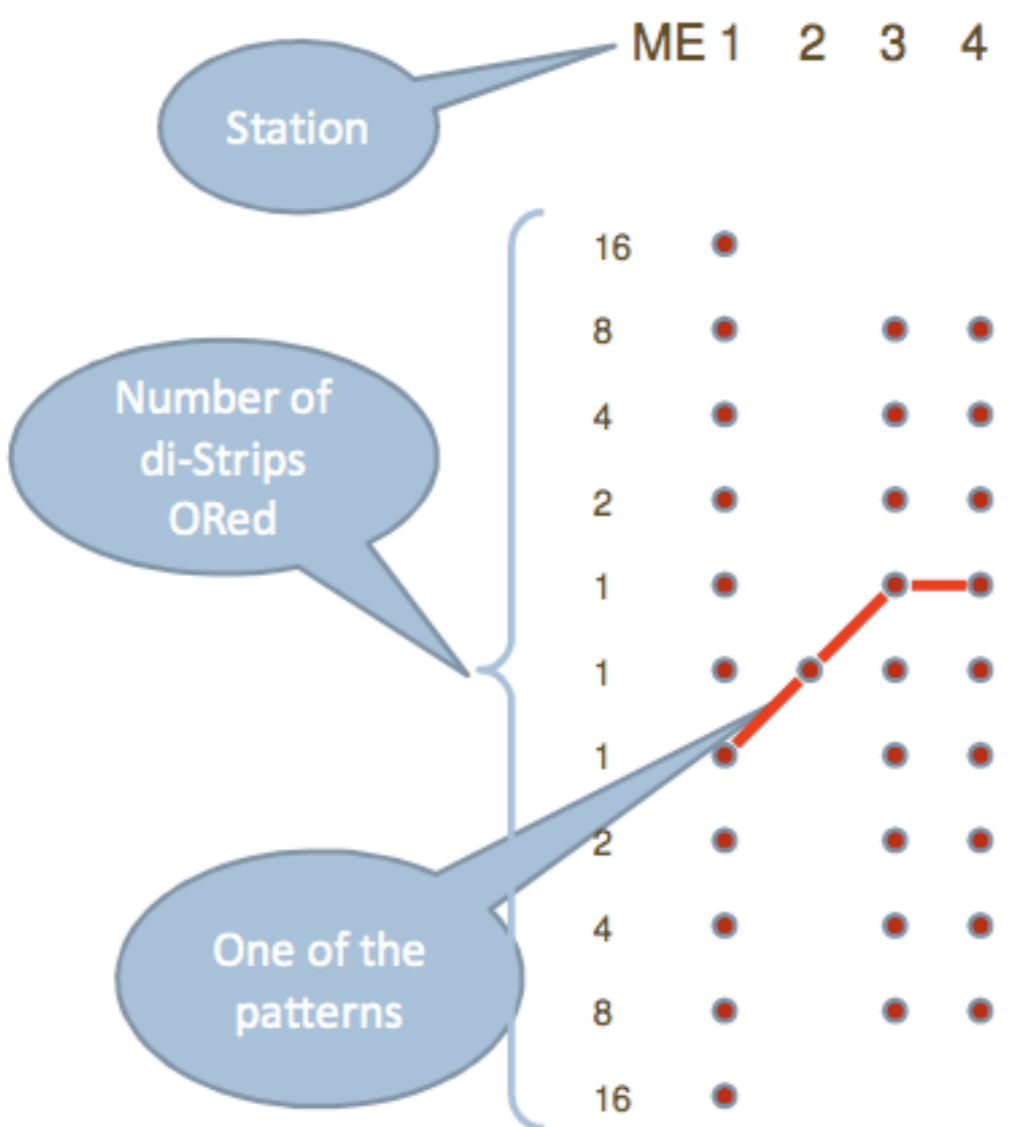
25-meter 12-core fiber

12-core fanout

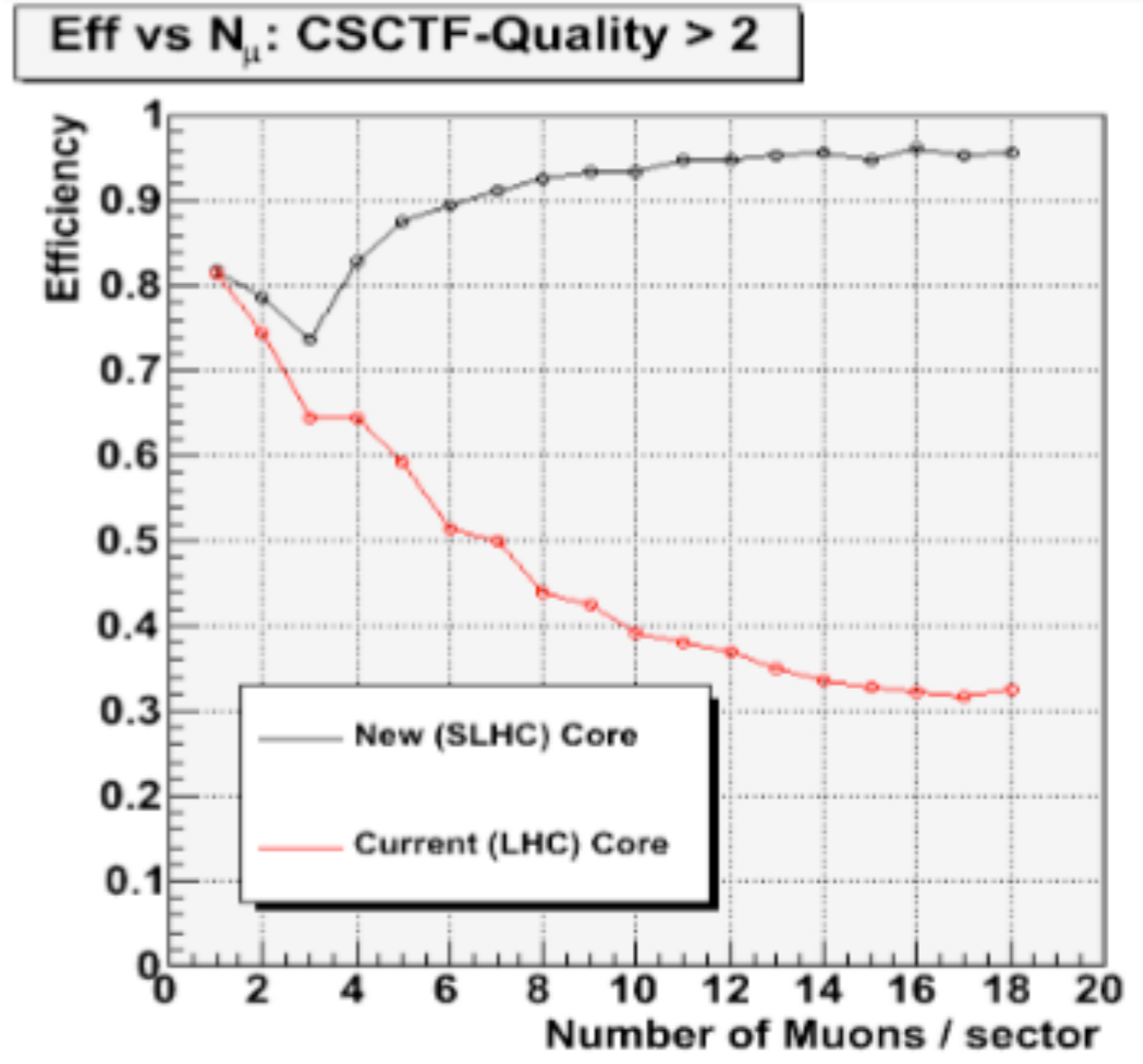


Track finding algorithm

- current design - ϕ comparisons, does not scale well
- switch to pattern matching system for upgrade

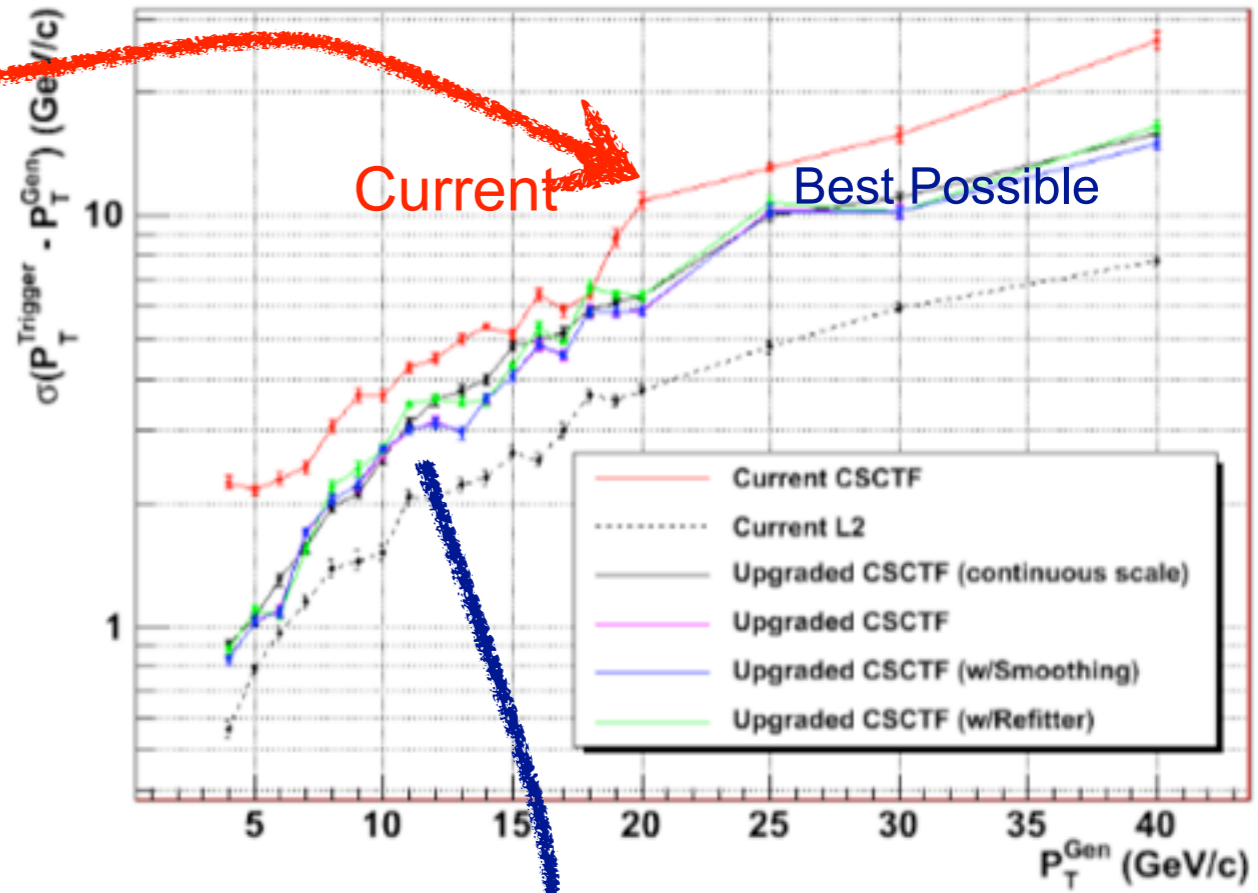
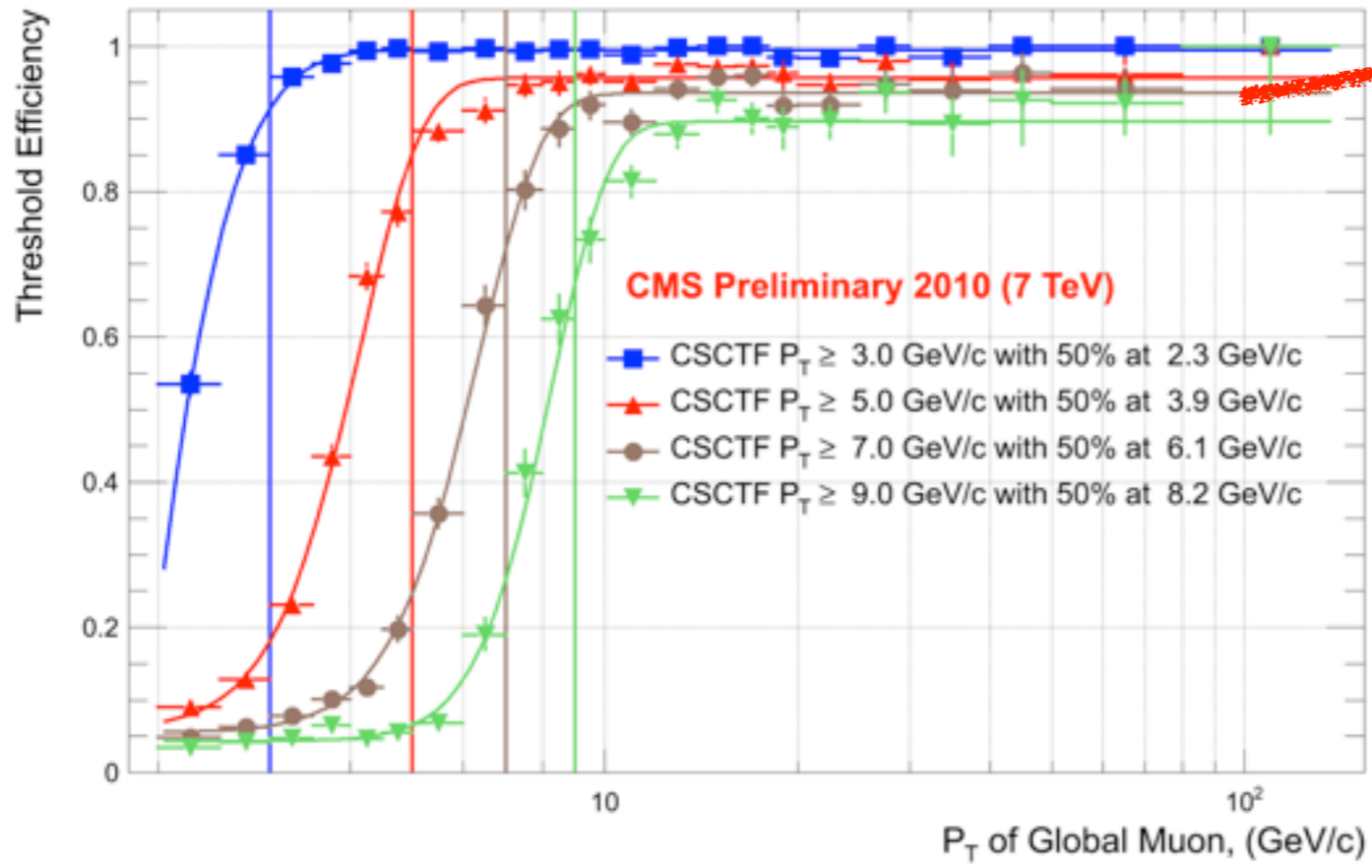


Possible ϕ pattern envelope structure

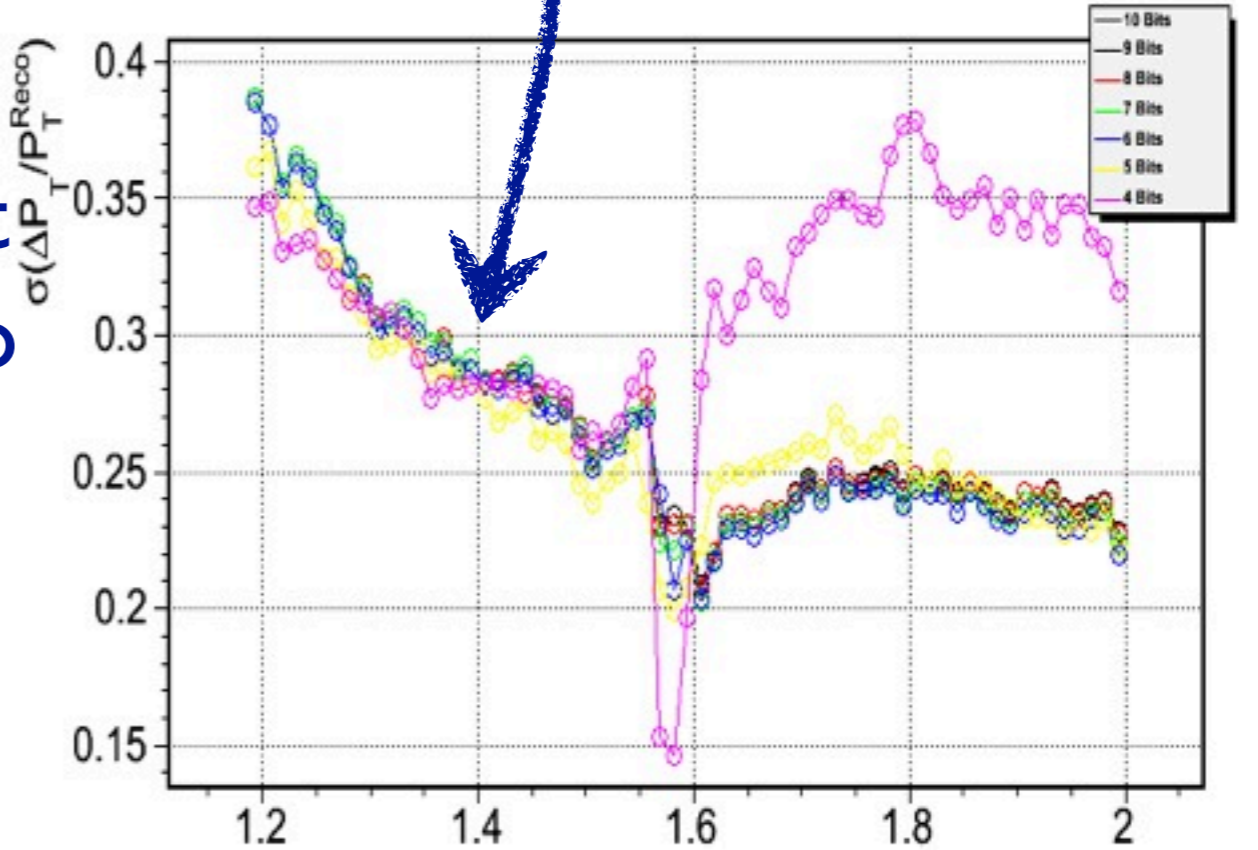




p_T Assignment



- best possible - load L1 trigger primitives into offline Kalman fit
- testing nonlinear $\Delta\phi$ binning to optimize information content
- determines LUT address space, further correction algorithms



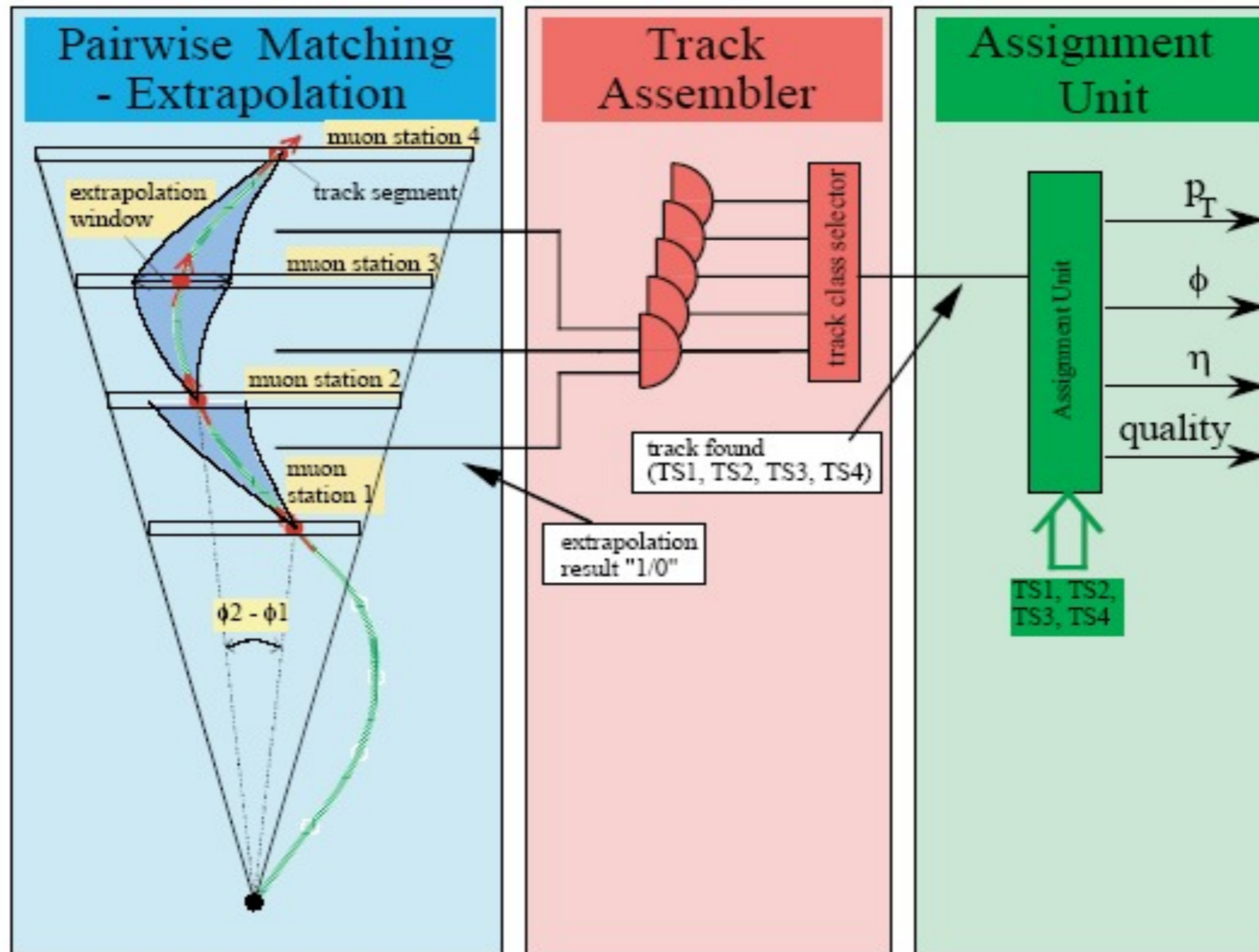


Conclusions

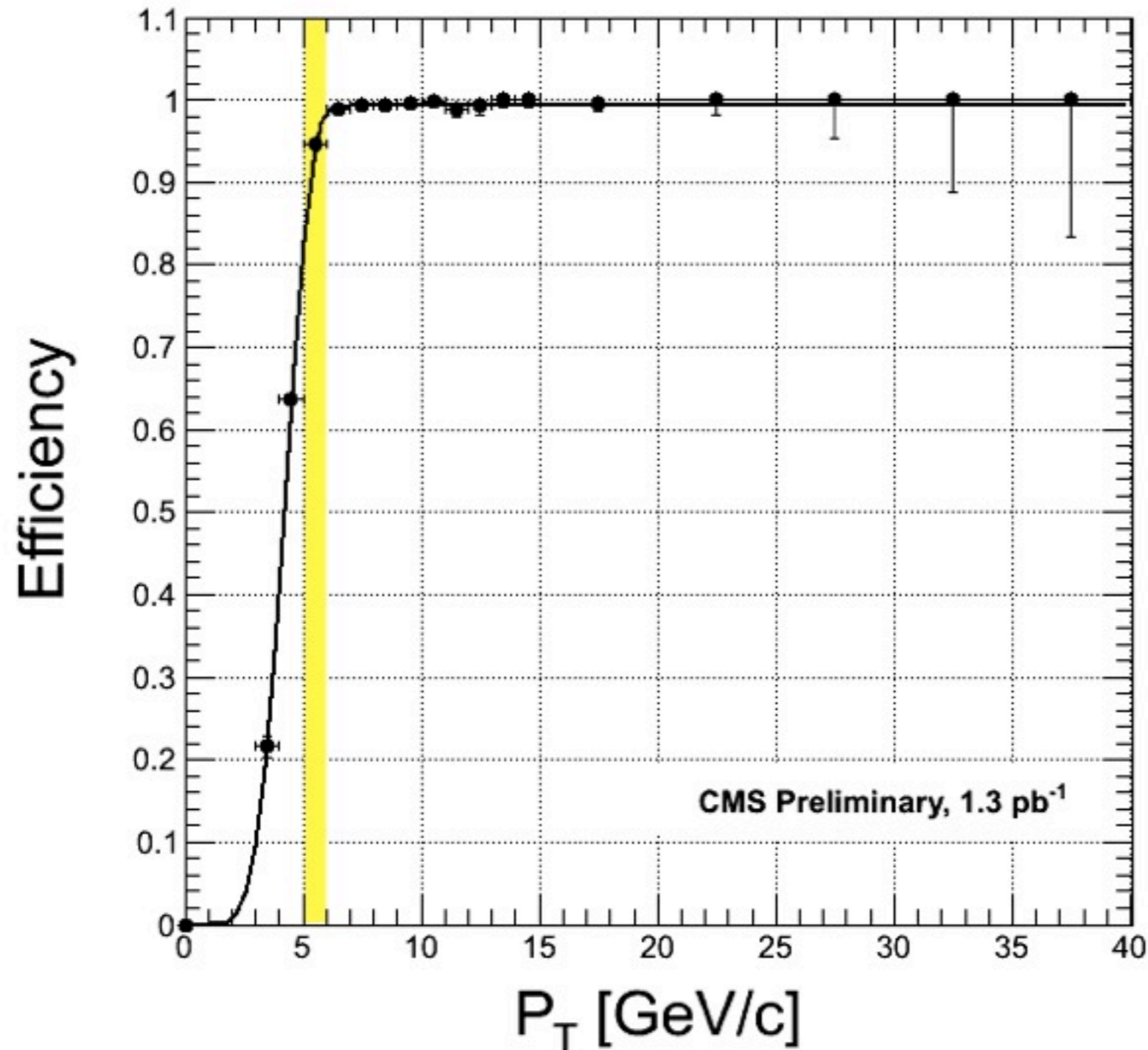
- DT
 - algorithms in great shape, upgrade architecture will take advantage of fast serial links and new FPGAs
 - new design will allow for more flexibility (for the future)
- RPC (+ MPGD)
 - increase coverage: $|\eta| > 1.6$ - possibly use MPGD
 - plan to build more copies of current boards to cover
 - optimizing patterns for high occupancy and high $|\eta|$
- CSC
 - robustness: fully open internal data throughput to SP
 - sector crosstalk - recover inefficiency at boundaries
 - improve p_T assignment: studies in progress
- Phase II: see talk by A. Montanari tomorrow at 9:30 am

Supporting Slides

DT Track Finder Algorithm



DTTF 5 GeV/c P_T Turn-on from J/ψ

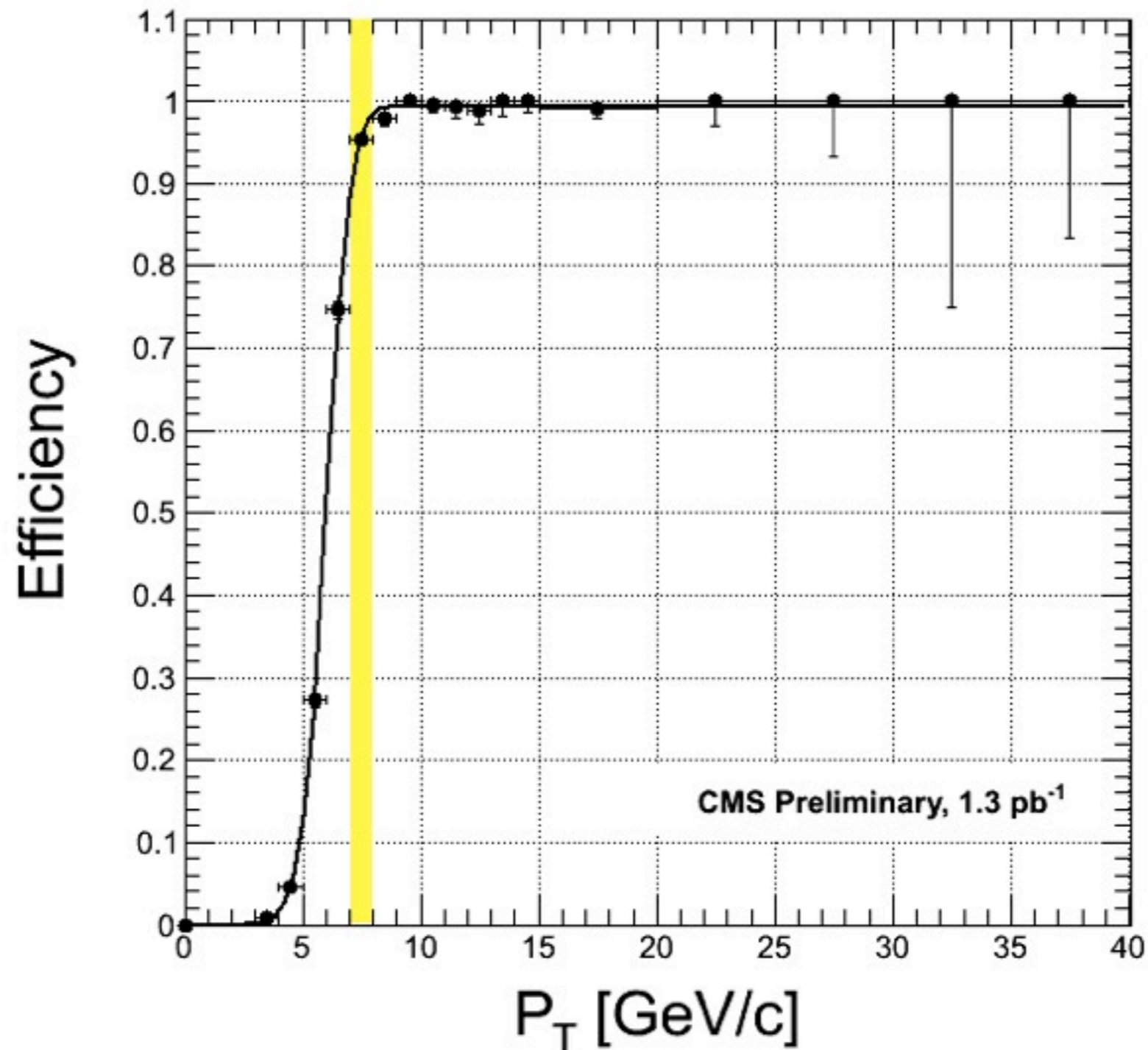


$$|\eta| < 1.1$$

N.B. In this plot, three known PHTFs, where DT trigger segments at MB2 have bad slope are not considered.

Turn-on expected to reach $\geq 90\%$ efficiency at the nominal cut.

DTTF 7 GeV/c P_T Turn-on from J/ψ

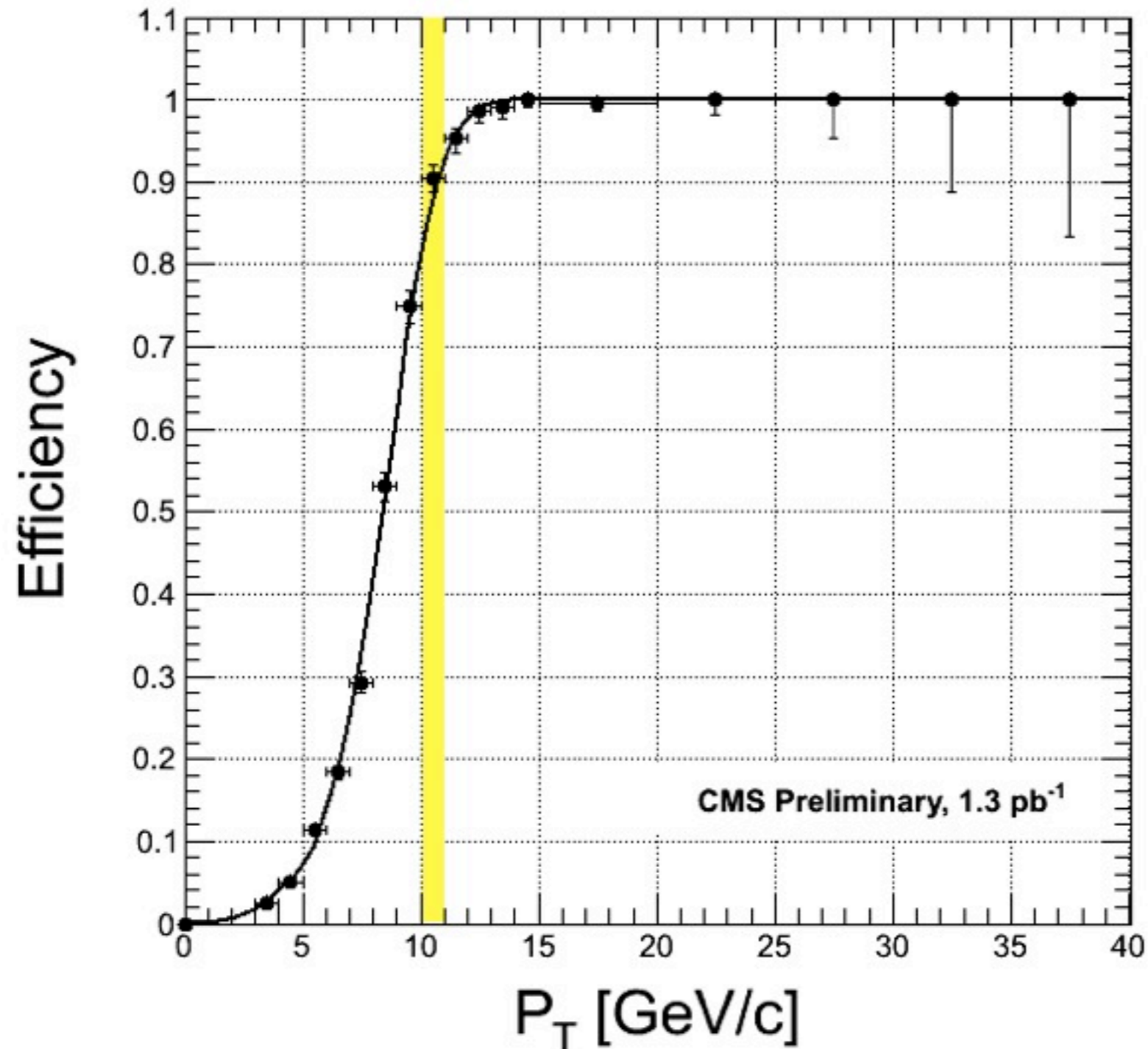


$$|\eta| < 1.1$$

N.B. In this plot, three known PHTFs, where DT trigger segments at MB2 have bad slope are not considered.

Turn-on expected to reach $\geq 90\%$ efficiency at the nominal cut.

DTTF 10 GeV/c P_T Turn-on from J/ψ



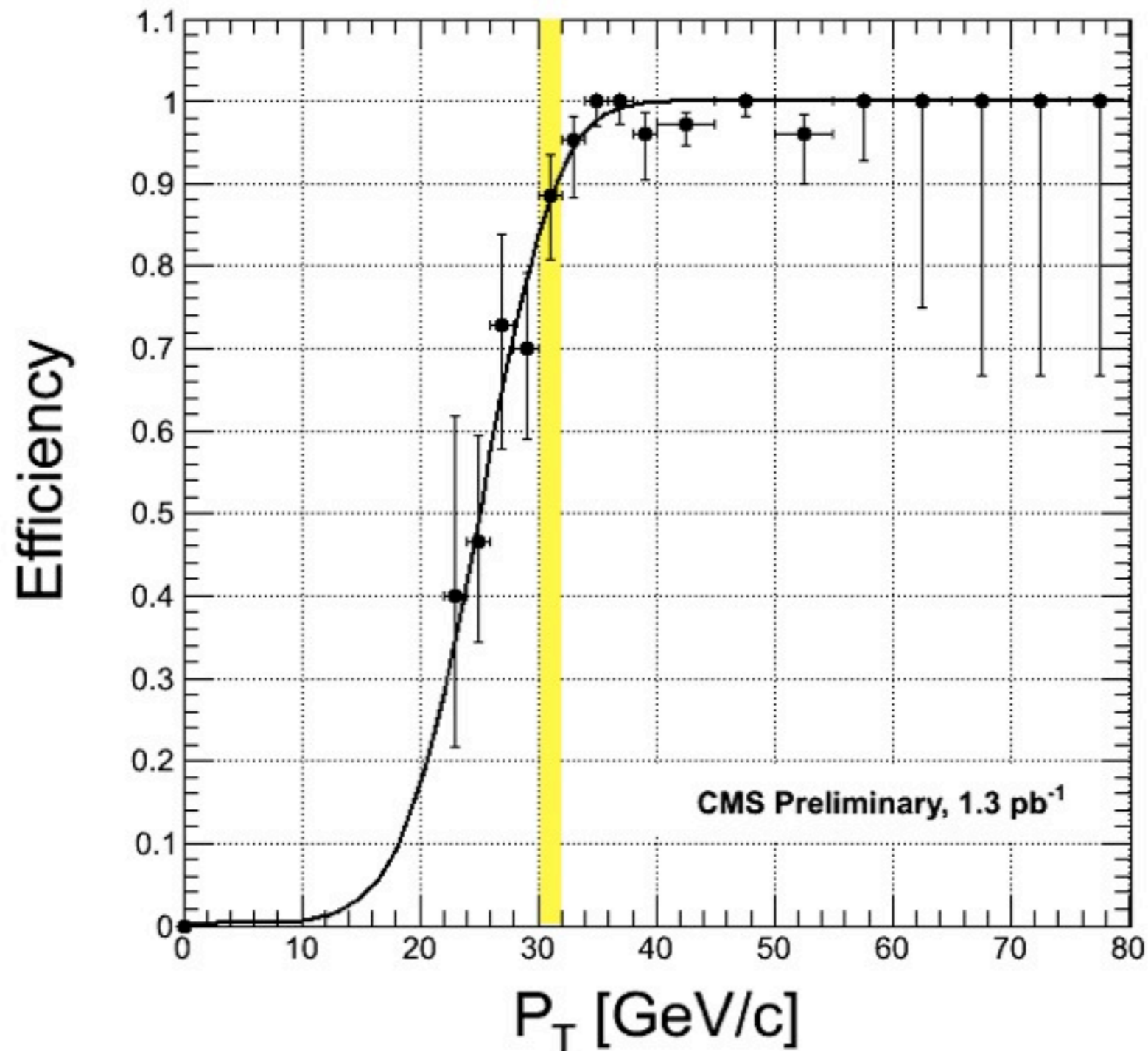
$$|\eta| < 1.1$$

N.B. In this plot, three known PHTFs, where DT trigger segments at MB2 have bad slope are not considered.

Turn-on expected to reach $\geq 90\%$ efficiency at the nominal cut.

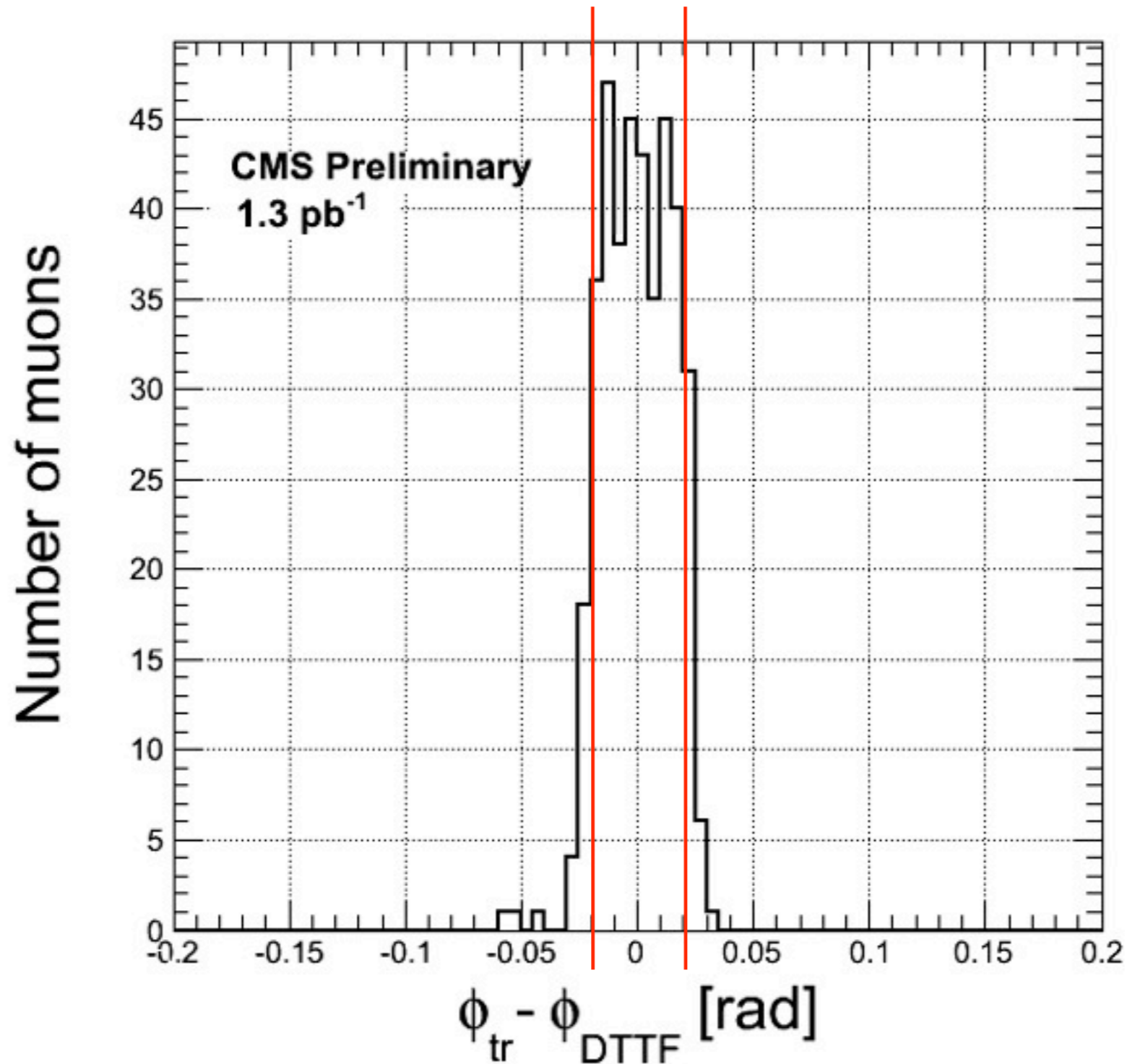
DTTF 30 GeV/c P_T Turn-on from Zs

$|\eta| < 1.1$



Turn-on expected to reach $\geq 90\%$ efficiency at the nominal cut.

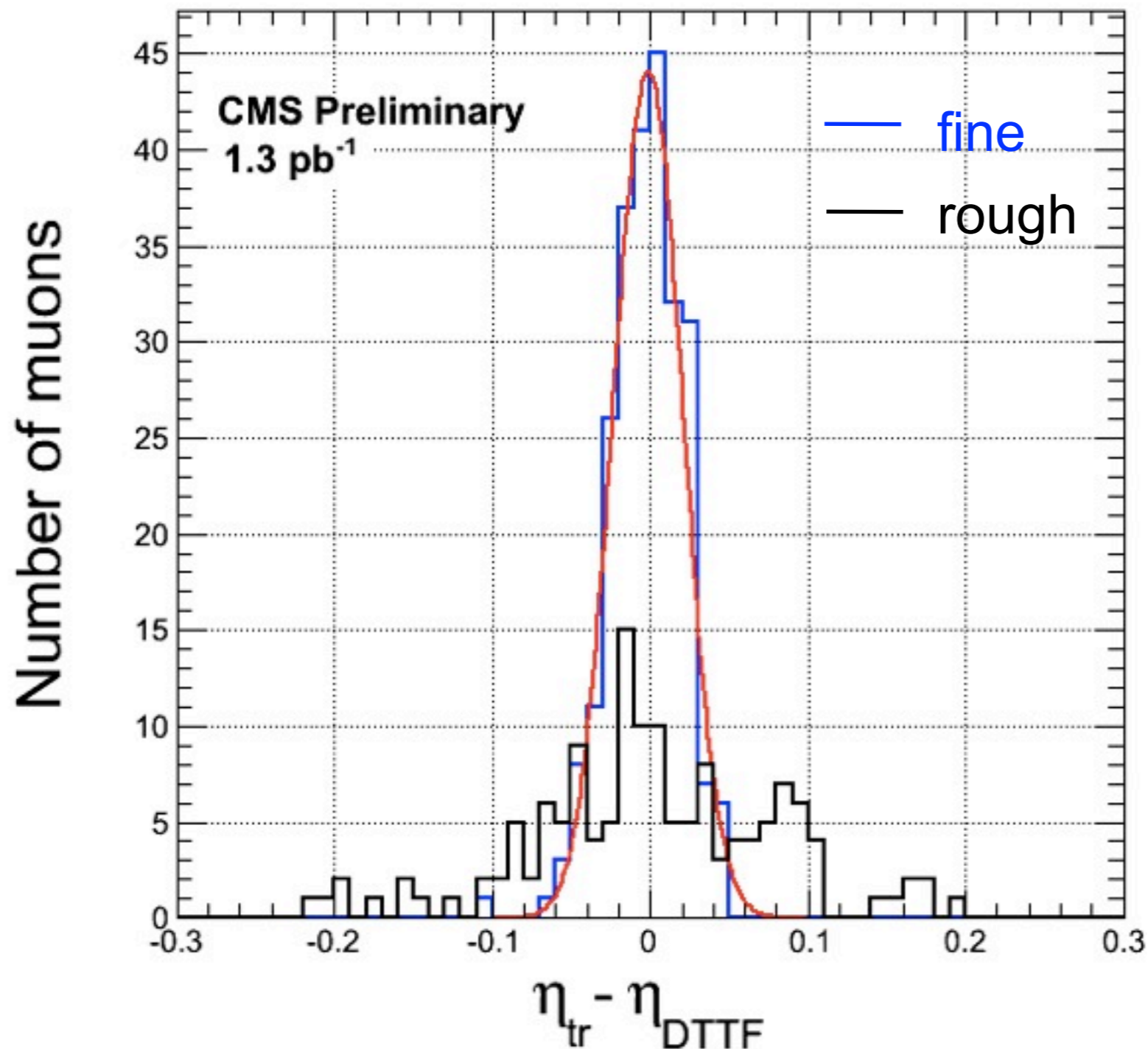
DTTF Phi Resolution from Zs



$|\eta| < 1.1$

DTTF ϕ bin size:
0.044 rad

DTTF Eta Resolution from Zs



$$|\eta| < 1.1$$

Fine η assignment
resolution:

$$0.021 \pm 0.001$$

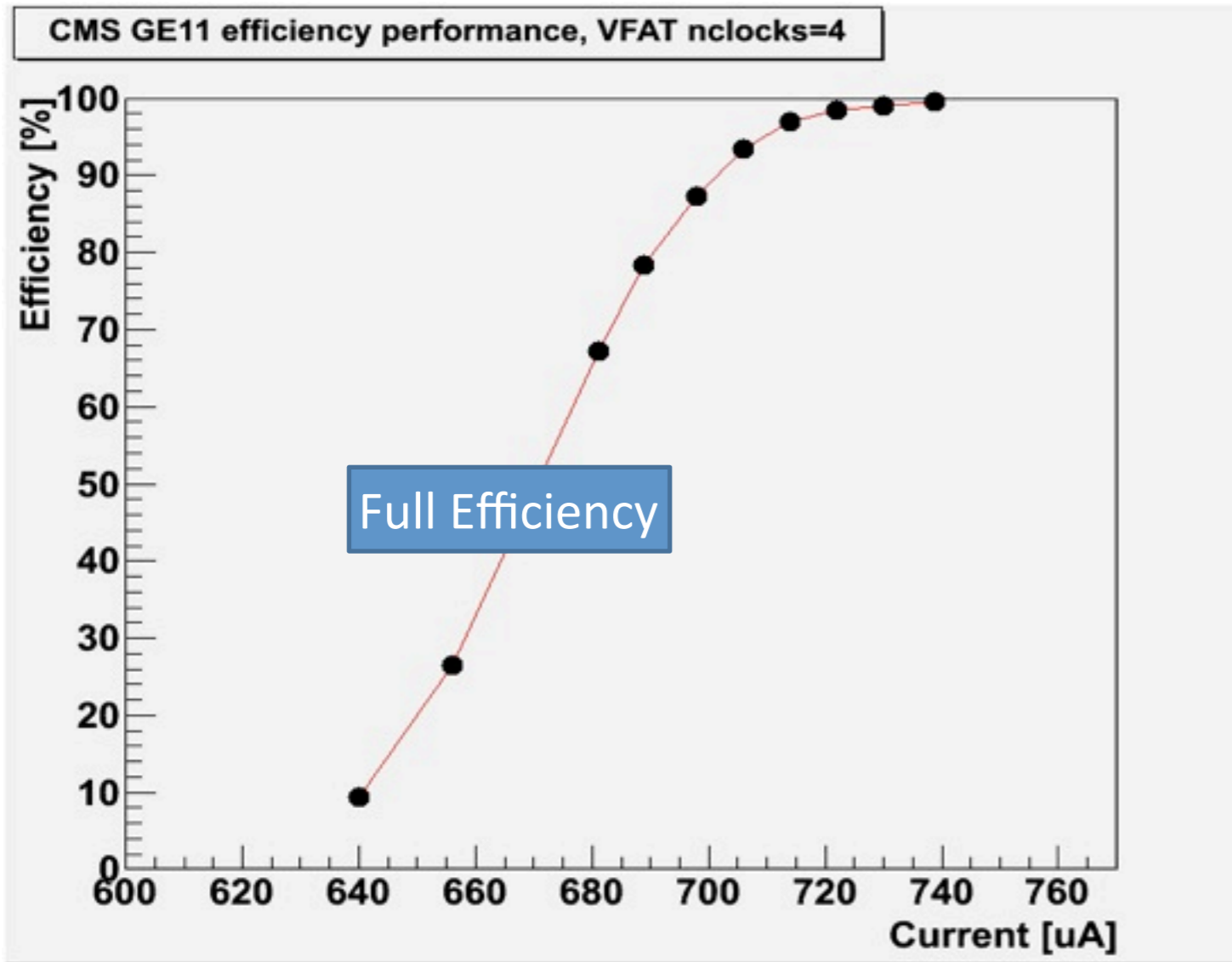
Expected:

$$0.025$$

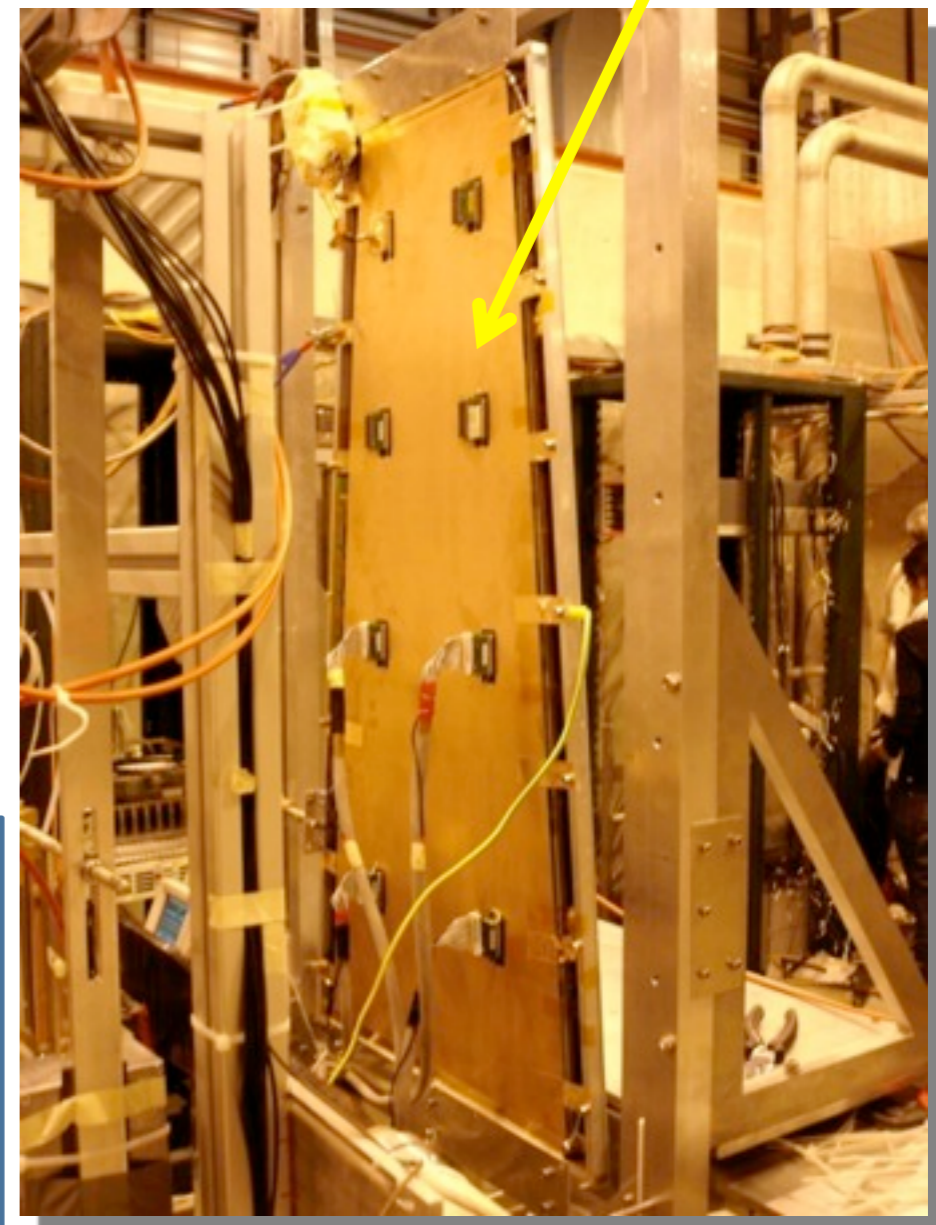
CMS TS-2008/008



CMS GE1/1 $1.6 > \eta > 2.1$ Investigating: Extension to 2.4 And adding detector in Barrel End-cap crack



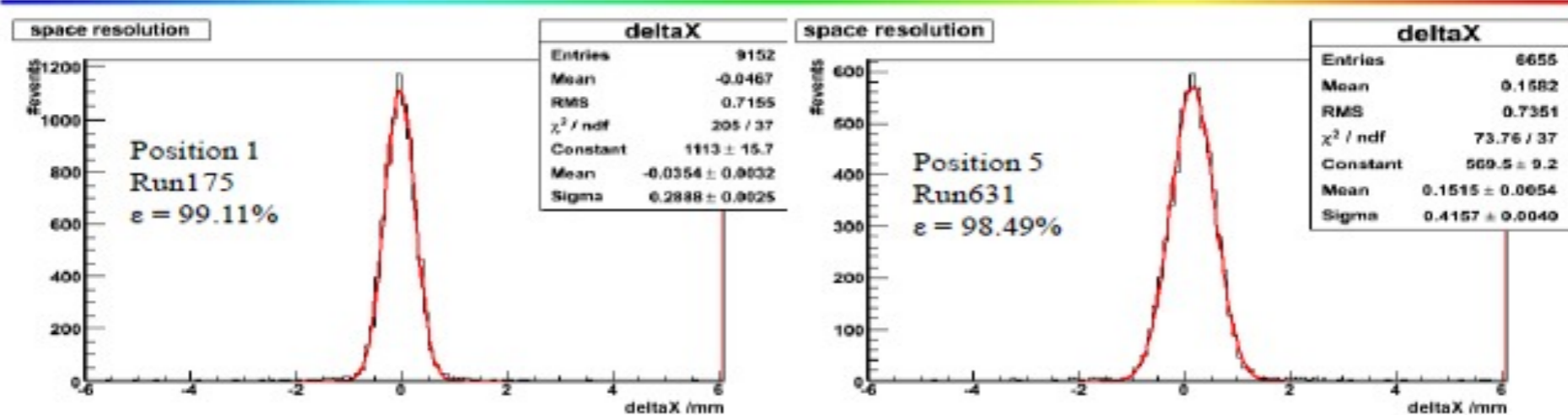
Large Prototype: GE1/1
BeamTest @ RD51 setup
October 2010



Rate capability : $10^4/\text{mm}^2$
Space/Time resolution: $\sim 100 \mu\text{m} / \sim 4\text{-}5 \text{ ns}$
Efficiency $> 98\%$; Excellent Long Term Operation
Gas Mixture: Argon CO₂ (non flammable mixture)
Large areas $\sim 1\text{m} \times 2\text{m}$ with industrial processes



Excellent Space Resolution: Measured with Large Proto at Beam Oct 2010



Position	1	2	3	5
space resolution (mm)	0.289	0.288	0.316	0.416
average pitch (mm)	1.06	1.05	1.16	1.49
average pitch/sqrt(12)	0.305	0.304	0.335	0.430



$$resolution \approx \frac{pitch}{\sqrt{12}}$$

Simulation Studies Started:

PAC Trigger performance with MPGD – Karol Bunkowski and team

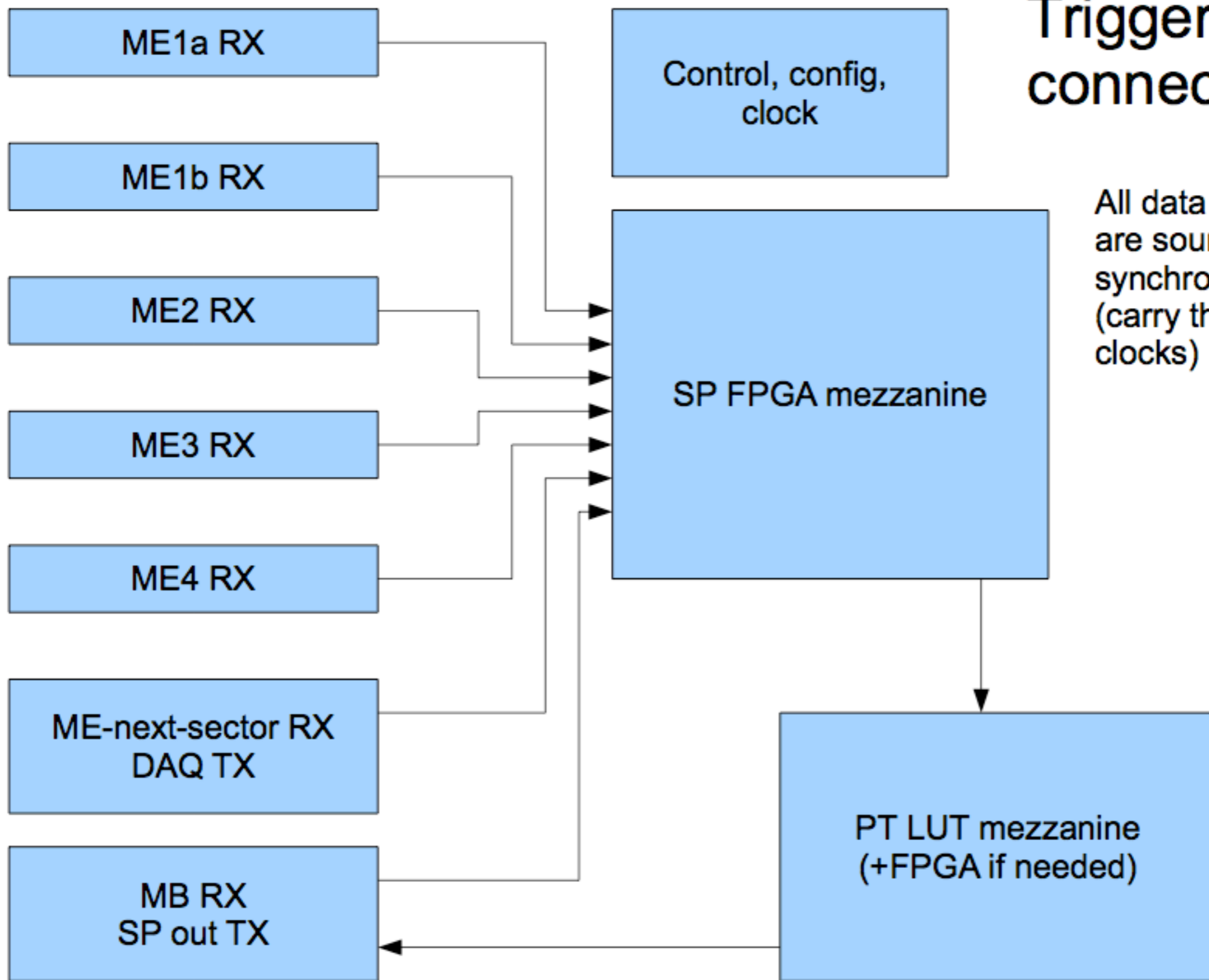
Muon Momentum resolution, geometry and multiple scattering effects at high pT: improvement with MPGD – Marcello Maggi and team

Tracking can be performed due to the excellent space resolution - in combination with CSC and inner detectors – no one is looking at this



CSCCTF in VME

- modular construction
- all logic on mezzanines (modules)
- main board:
 - linked connections with plenty of spare connections
 - adjustable DC-DC converters for each module
 - configurable DC power sequencers
 - provides easy upgrade path - upgrade only the module that needs upgrades, not entire board
 - use parallel low latency connections for trigger data
 - DAQ and control via serial links between FPGAs



Trigger data connections

All data connections are source-synchronous parallel (carry their own data clocks)

