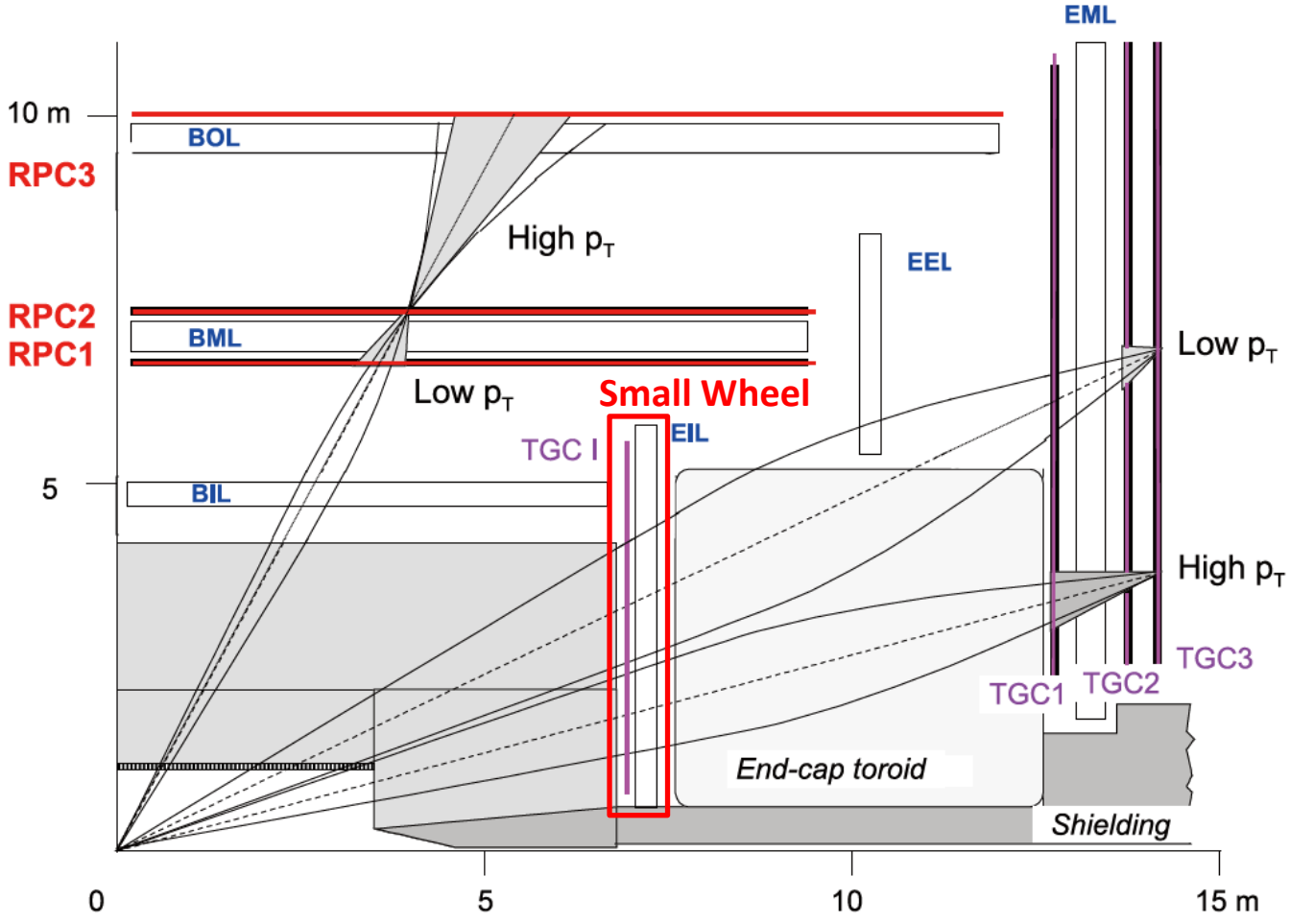
ATLAS small wheels and muon trigger upgrade

Osamu Sasaki
High Energy Accelerator Research Organization (KEK)

INPUTS from
RPC : S.Veneziano and G.Aielli
sTGC : N.Lupu, L.Levinson and G.Mikenberg
mMegas : V.Polychronakos
MDT : R.Richter and O.Sasaki

Present system and improvement scenario

Three stations (RPC1,2,3 and TGC1,2,3) are used inside/outside toroidal fields.



Introduction of 4th Trigger Stations

Barrel

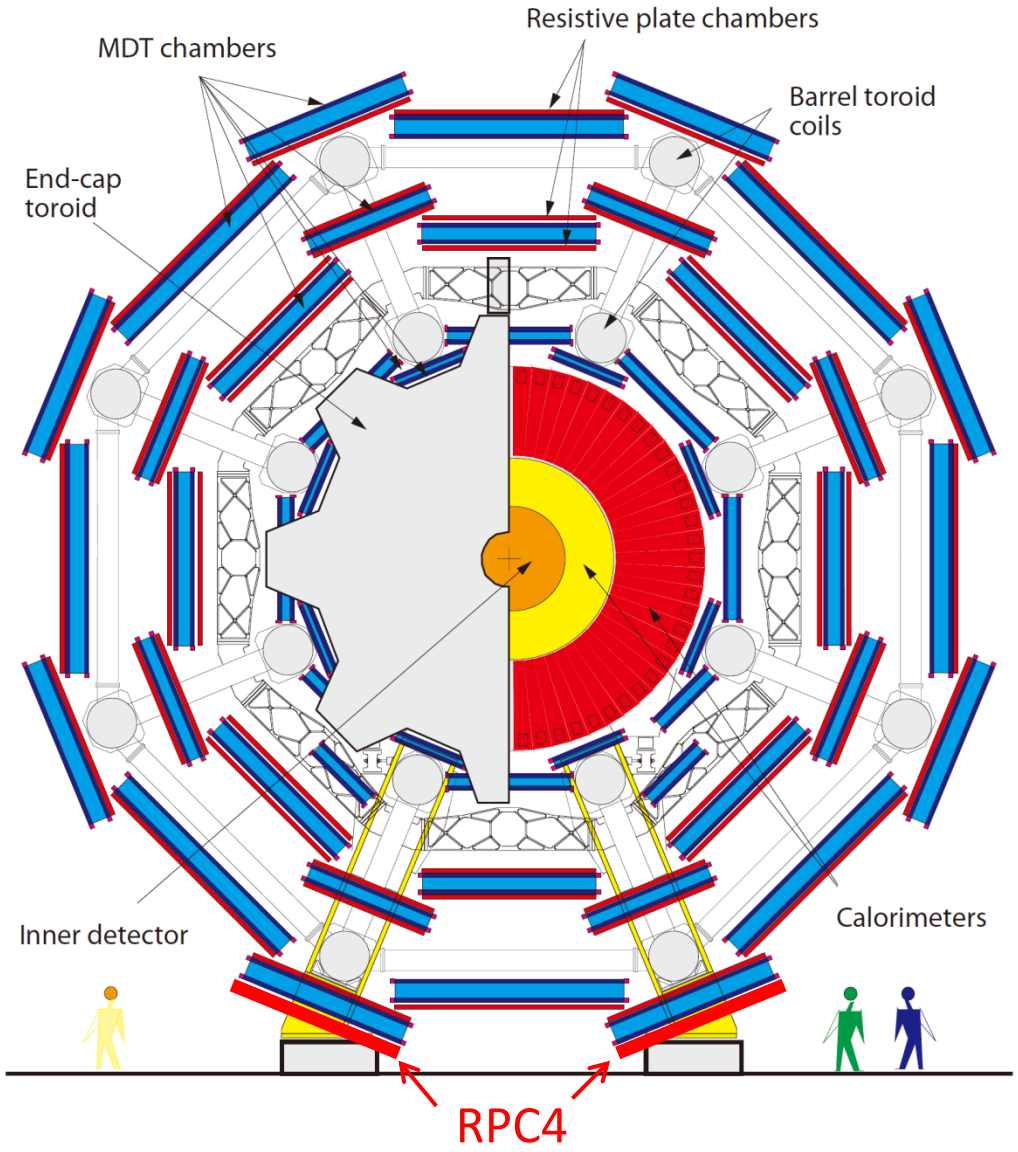
RPC4 in the feet region

Endcap

New detectors on the small wheel, having the capability to deal with LVL-1 trigger.

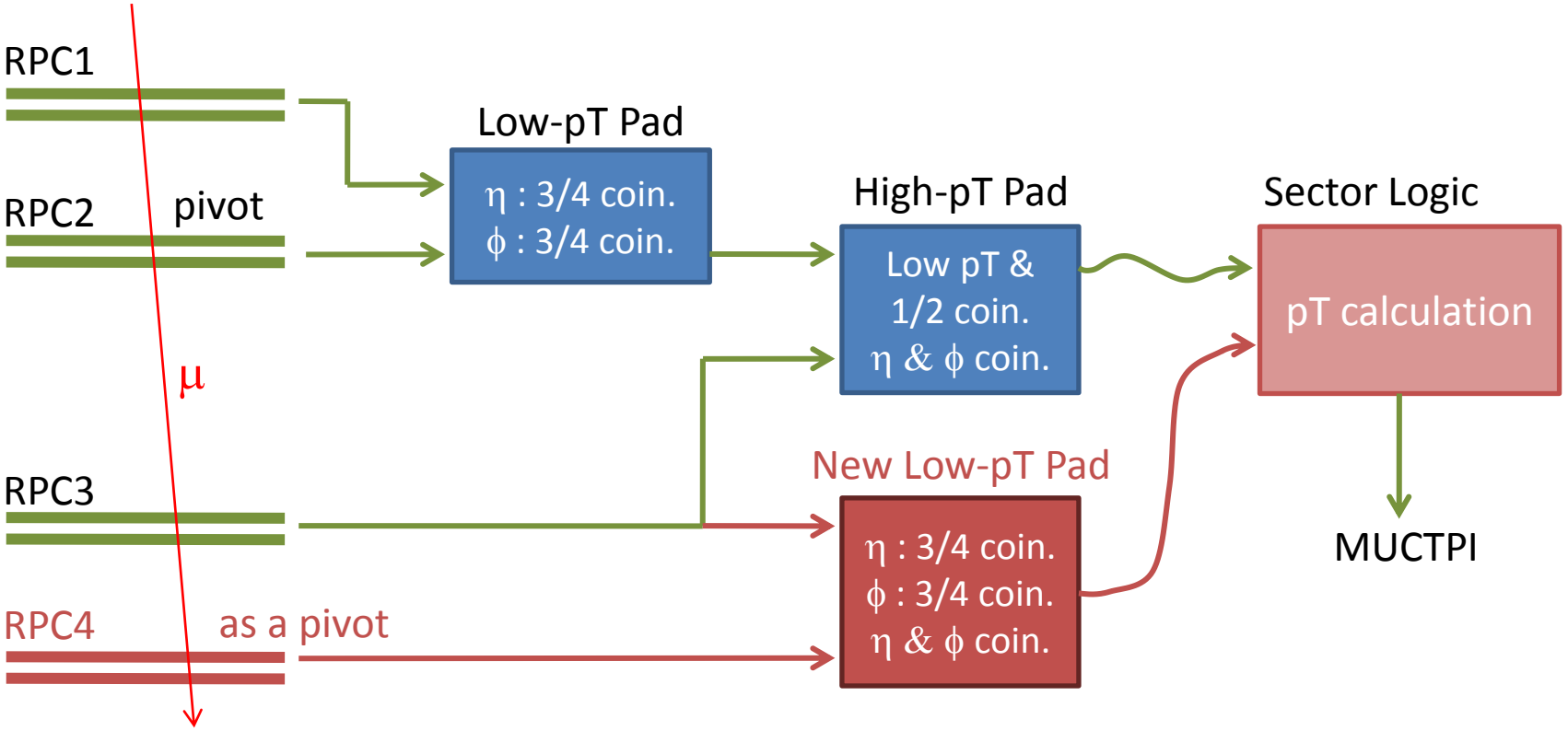
1mr incidence angle measurement

RPC Barrel Upgrade in the Feet Region



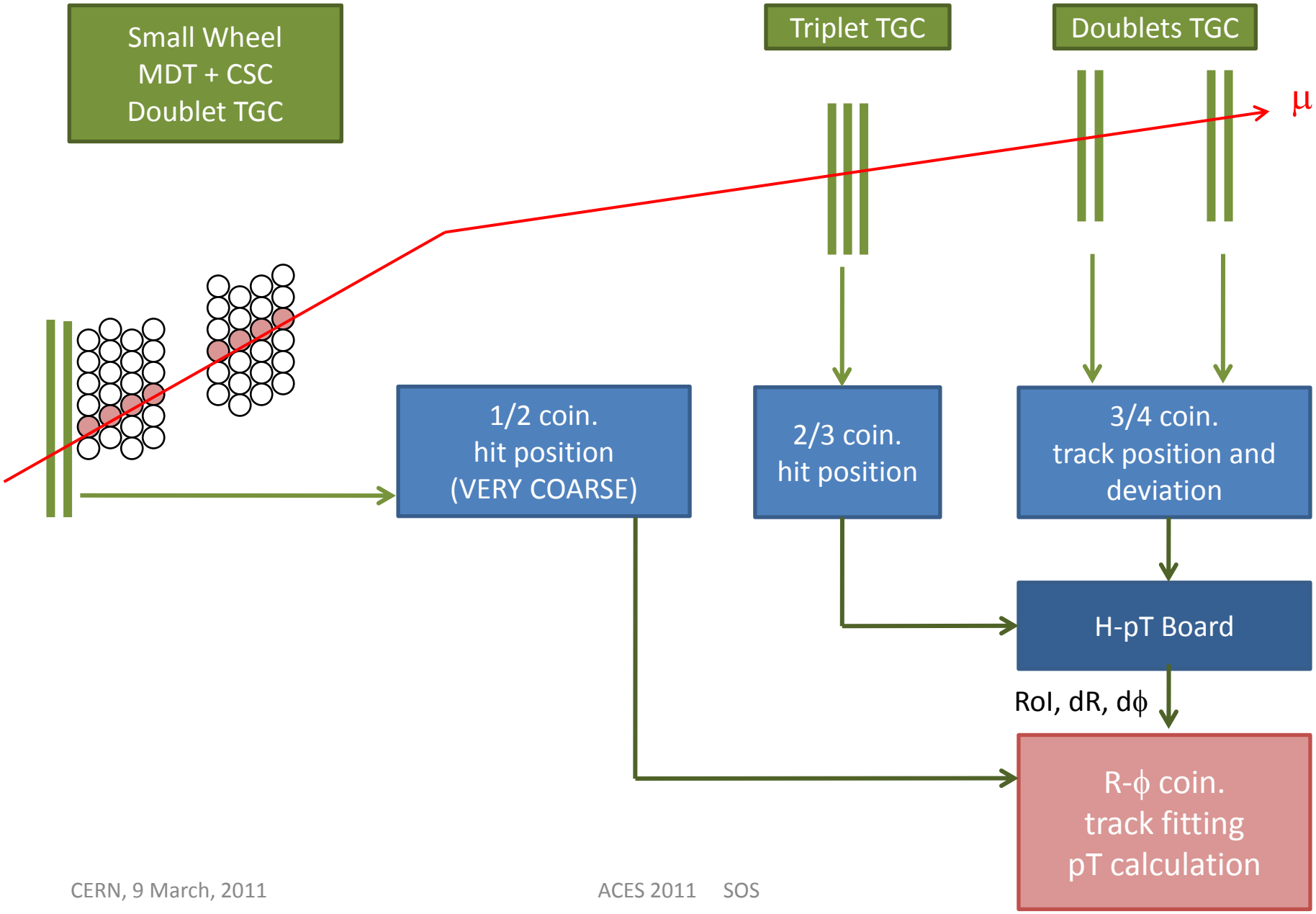
- LVL1 muon trigger efficiency in the feet sectors is about 50% lower than the one for standard sectors.
- In order to recover the efficiency loss, the fourth layer of the RPC (RPC4) has been installed, wherever possible.
- Improved to be 80% (pT = 20GeV).

Upgraded RPC system

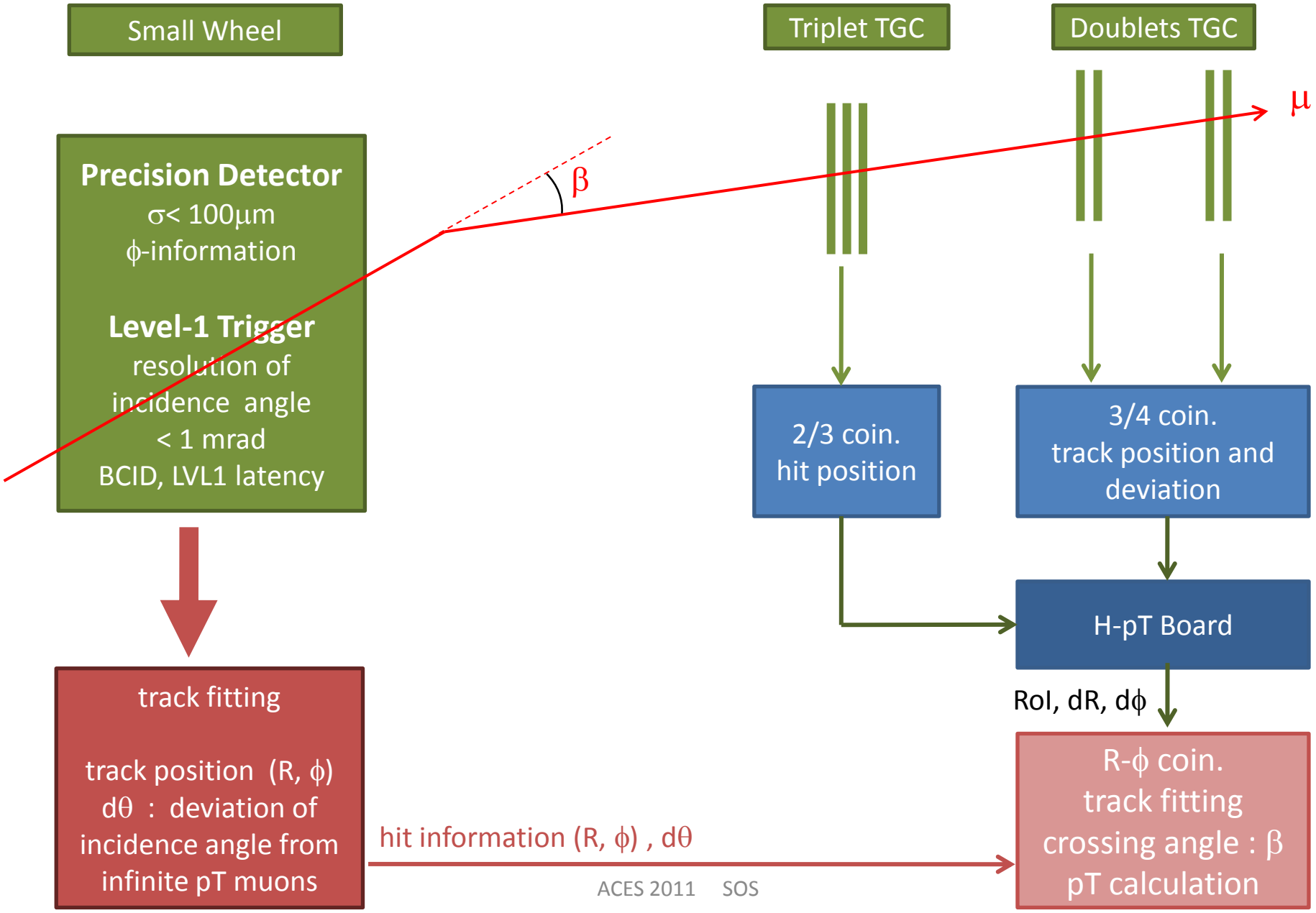


- 40 new Low-pT Pad boards with optical links and 56 splitter boards are needed.
- It is under study how to handle the new trigger outputs in terms of sector logic and MUCTPI.

Present detectors of SW + TGC of BW's



New detectors of SW + TGC of BW's

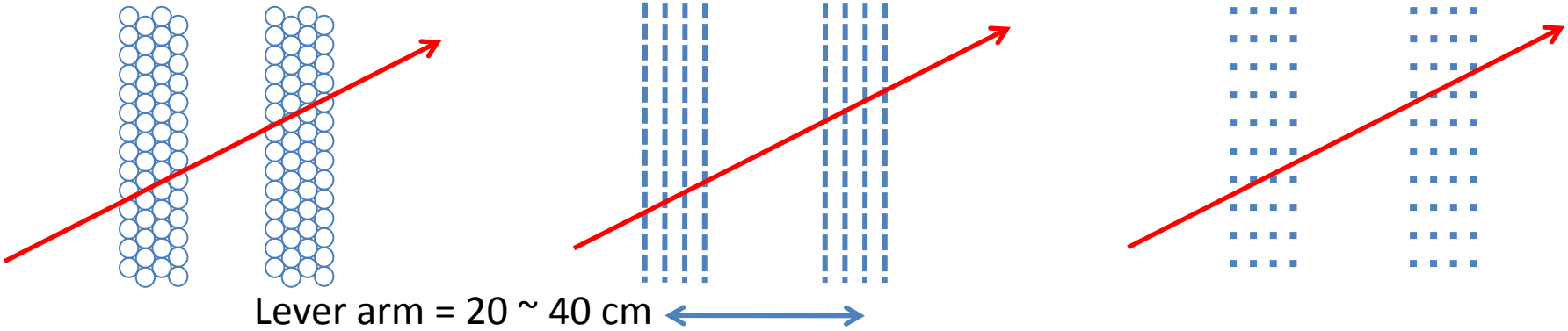


Detector Candidates for Level-1 Trigger of the Small Wheel

small tube MDT

Strips (microMegas, TGC and RPC)

Wires (TGC)



sMDT :
15 mmϕ tube, 50k ch.
200ns full drift time
Time measurement
25ns : ~ 1mm
No ϕ-information,
need some detectors
to provide ϕ

mMegas : 2M ch
0.5 mm pitch
sTGC : 400k ch
3.5 mm pitch

Need charge info. for
precision measurement.
Centroid circuit for LVL-1
Powerfull zero-suppression
scheme

RPC : a few 100k ch
2mm pitch
Trigger chamber
Sub-ns time of flight
Fast local trigger using
Maximum Selector

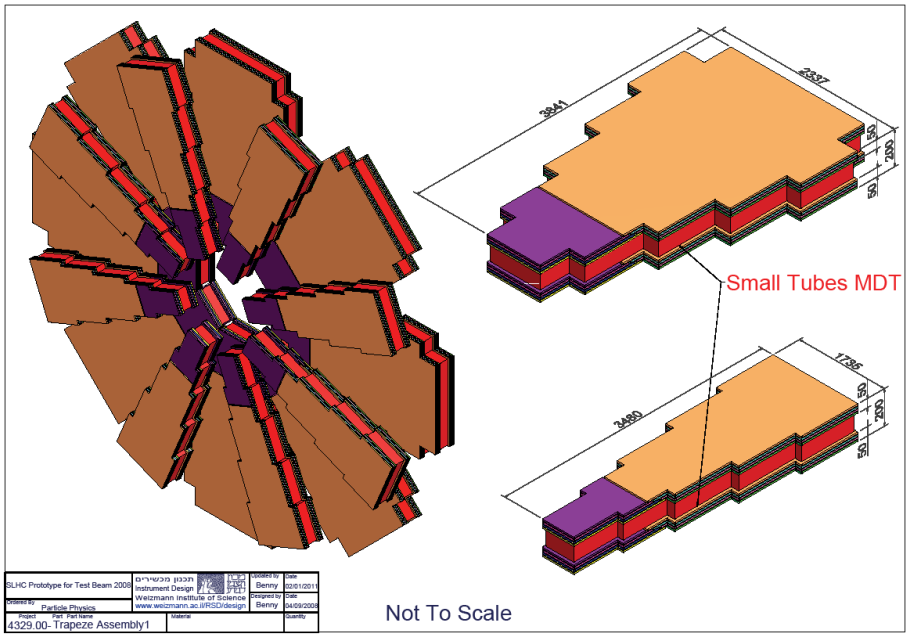
Conventional **TGC**
as a trigger chamber.
Timing pick up and
coarse track finding.

TGC for LVL-1 and precision measurement

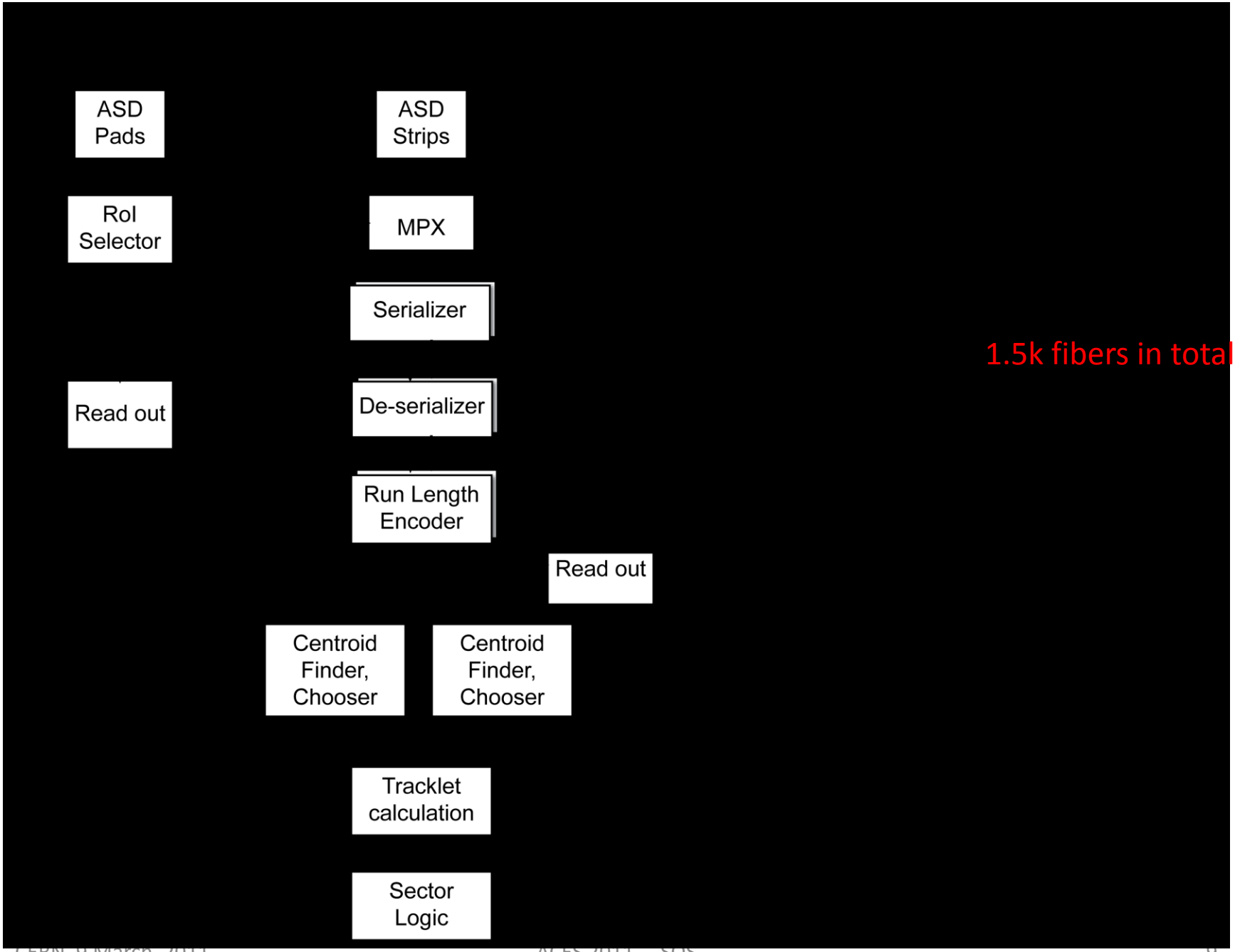
- Each of the so-called TGC packages consists of 4 TGC gaps.
  - Each gap contains 3.5 mm pitch strips (R), pad-wires (ϕ) and pads for local trigger.
  - ~400k independent electronics channels.

- Time-over-Threshold signals from strips are used as charge info. for precision measurement.
  - The position resolution with better than 100μm has been demonstrated in test beam.

- Hardware centroid circuits of ToT signals are used for LVL-1 trigger.

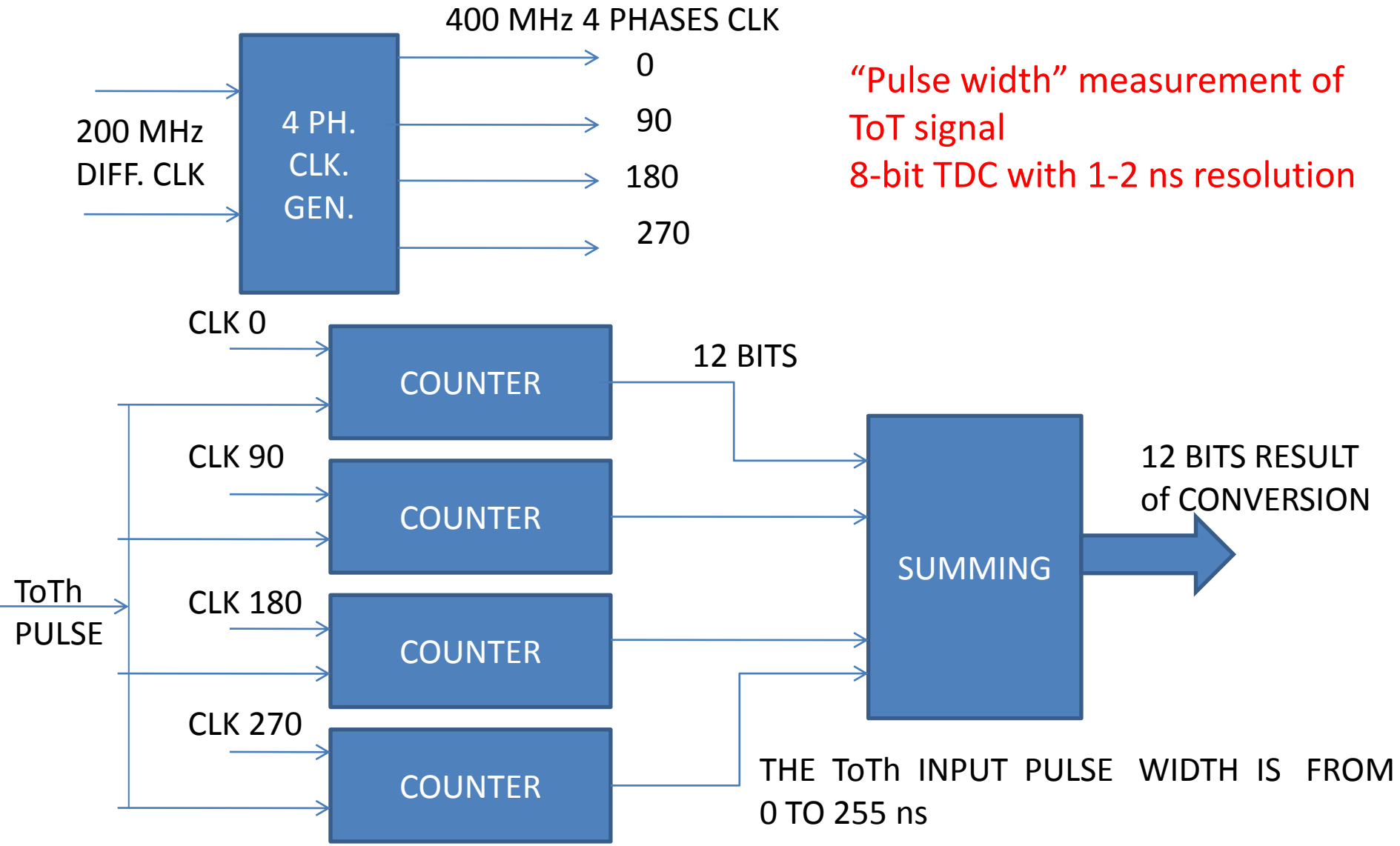


Layer	$\sigma_{corr}(\sigma_{nocorr})$ +/- $\Delta\sigma$ [μm]
1 new	66.2 (120.9) +/- 1.2
2 new	66.7 (79.8) +/-1.1
3 new	63.55 (75.95) +/-0.96
4 new	63.8 (116.4) +/-1.0
5 old	144.6 (264.1) +/-2.5
6 old	152.3 (182.1) +/-2.6
7 old	163.6 (195.6) +/-2.6
8 old	146.4 (267.2) +/-2.2



1.5k fibers in total

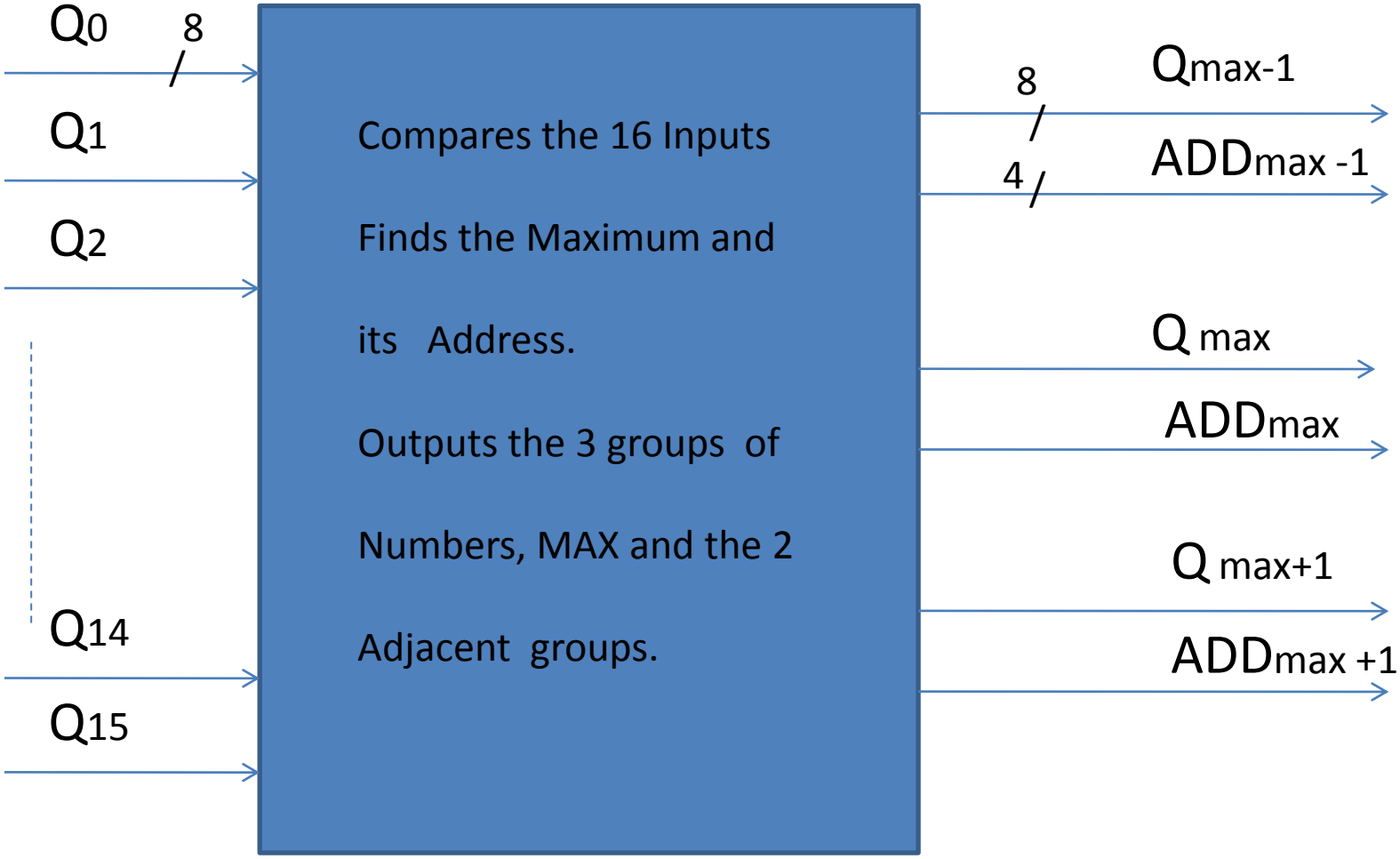
TDC BLOCK DIAGRAM (CONCEPT WHICH WORKS)

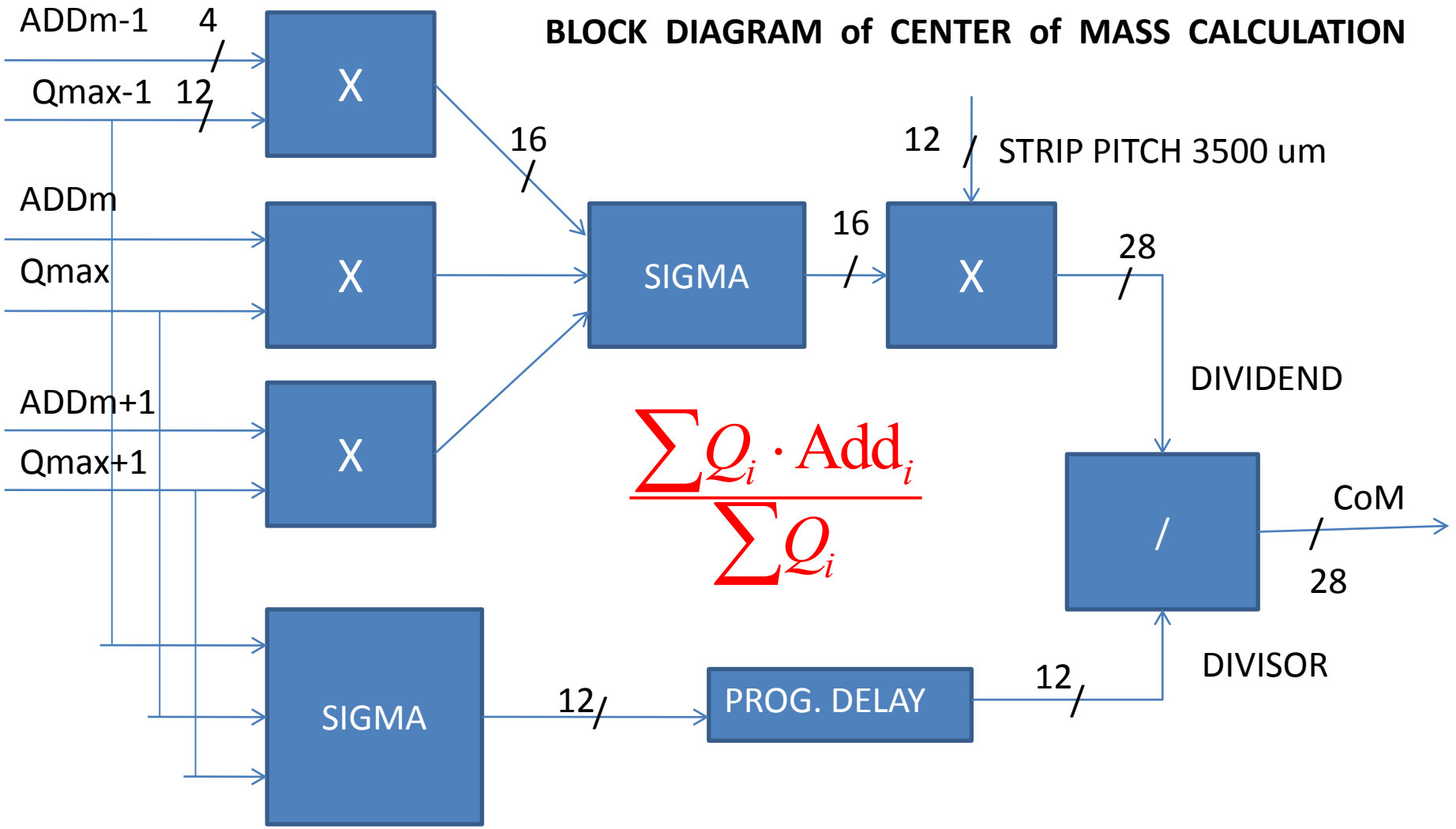


"Pulse width" measurement of ToT signal

8-bit TDC with 1-2 ns resolution

COMPARATOR & SELECTOR to find the MAXIMUM CHARGE and its INDEX





ADDi Relative address in the 16 strips slice

Qi Charge in units of TDC

Additional latency calculation

- The table shows the latency added by the insertion of the sTGC precision strip trigger logic into the existing path from the Inner Layer coincidence logic to the Sector Logic.
- We take as a model the Xilinx Virtex6.
- All numbers are estimates except that for the centroid finder for which a realistic design has been simulated.
- Clock speed = ~400MHz
- Yields 2.74/2.80μsec latency (Existing = 2.55μsec)

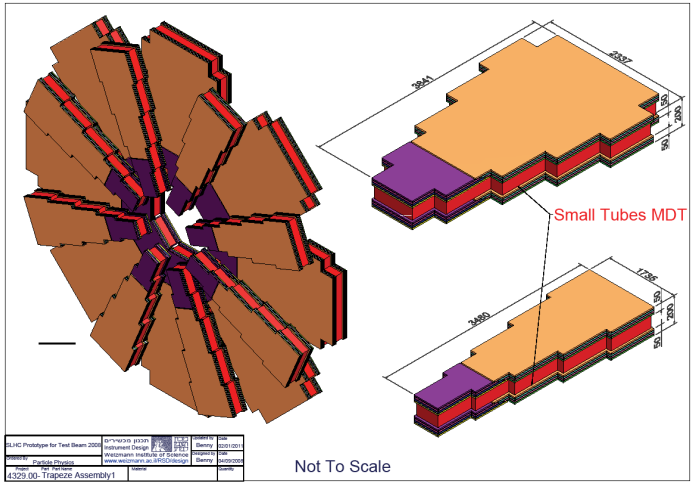
	Min (ns)	Max (ns)
deskew	25	25
ROI selector/ mpx	10	15
serializer	5	10
deserializer	8	16
RLE	16	24
latency for the last sample of the pulse	64	64
find largest signal	10	13
centroid of a layer	25	35
centroid chooser	10	12
centroid average	5	8
tracklet calc (LUT)	10	13
output serializer	5	10
	193	**245**

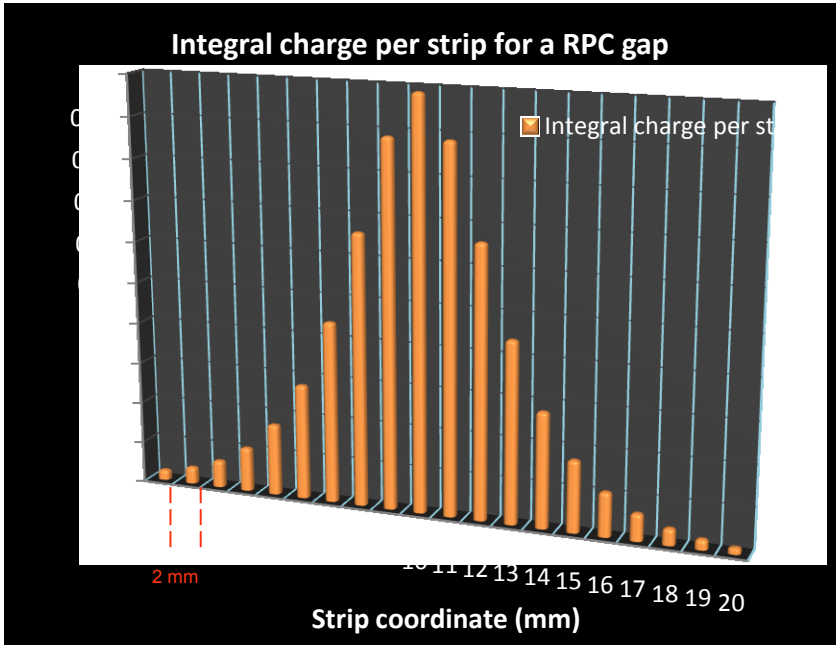
< 10 clk's

RPC based fast trigger scheme for the SW

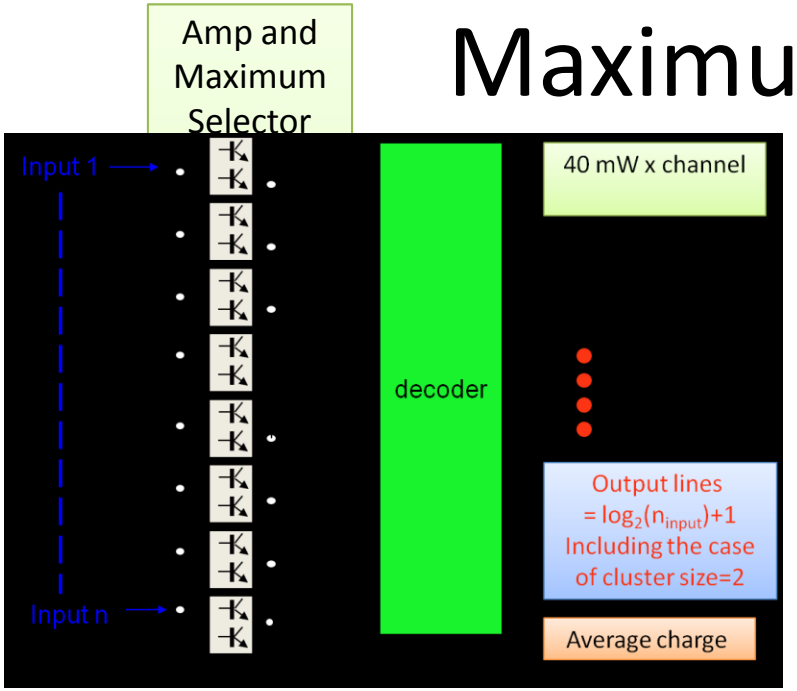
- **New RPC Front End** allowed a new working mode with a factor 10 less of charge per count → 10 KHz/cm^2 tested
- RPC is integrated mechanical structure of the MDT and shares services and readout
- Provides timing (sub-ns resolution) and second coordinate
- Tracking trigger: **a new type of**
  - low-cost
  - low-consumption
  - Fast
  - compact

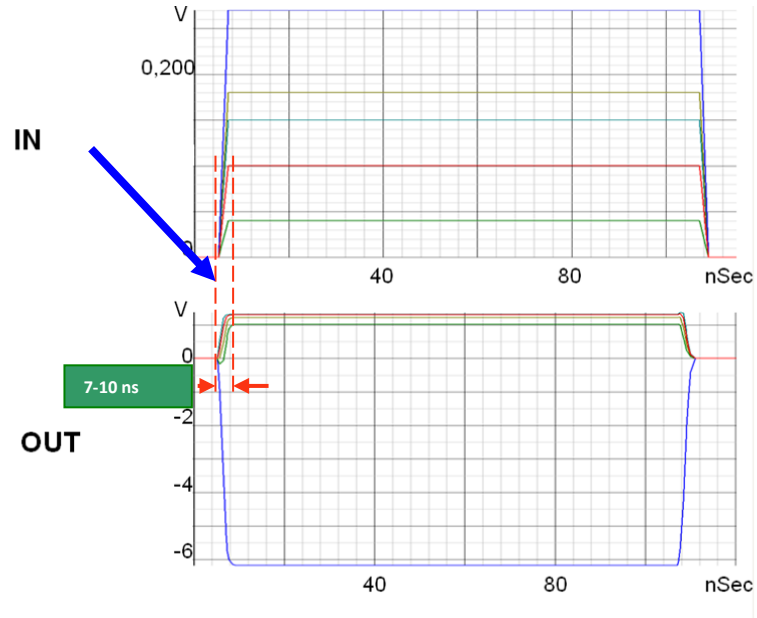
  electronic readout circuit (by R. Cardarelli) allows fast precision tracking for local trigger generation on the Eta.
- It works finding the maximum of the RPC charge distribution





Maximum selector

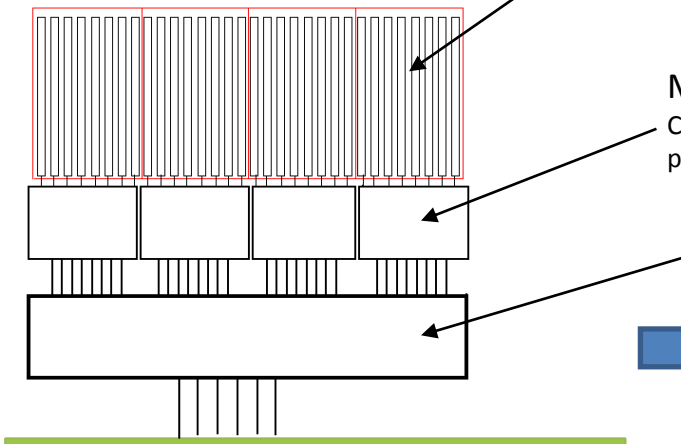




- N strips are processed at the same time (N can vary reasonably in the range of ~10)
- The Maximum selector amplifies the inputs and outputs a negative signal only in correspondence of the strip above a settable fractional threshold, normalized to the average charge provided
- The threshold is chosen to have one or two strips firing (cluster size 1 or 2)
- The decoder transforms the simple digital pattern in to a number representing the hit coordinate on the chamber
- The processing time of (7-10 ns) is highlighted in figure

Readout and trigger scheme example

Stripped readout plane

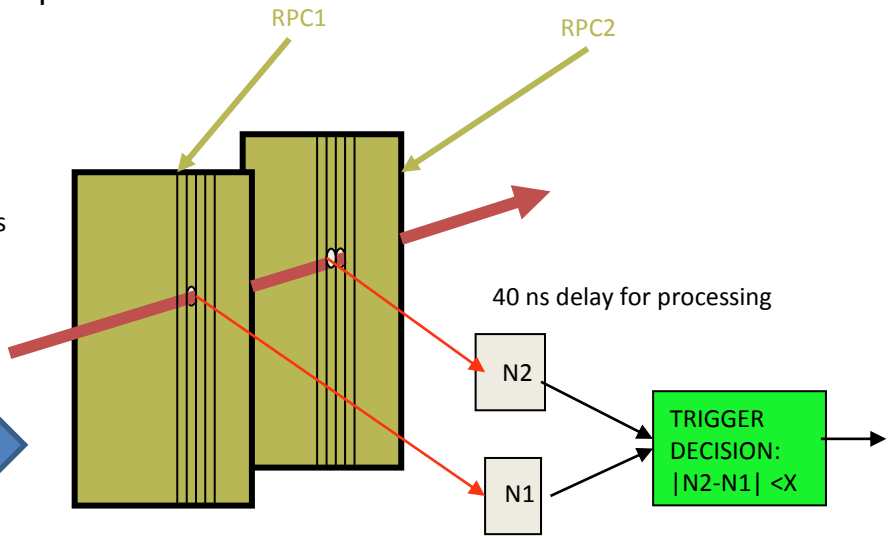


2 mm pitch micro strips grouped by 8

Maximum selector
Circuit needs 2 transistors per input channel

decoder

Output : binary number giving the position of the maximum; 8x4 strips =5 bits +1 for CS=2



Strip pitch **2 mm**

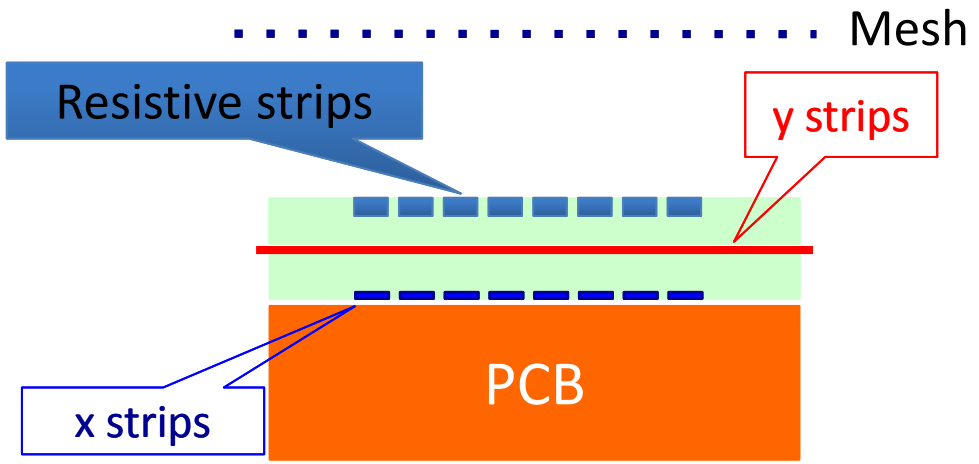
Single RPC plane spatial resolution

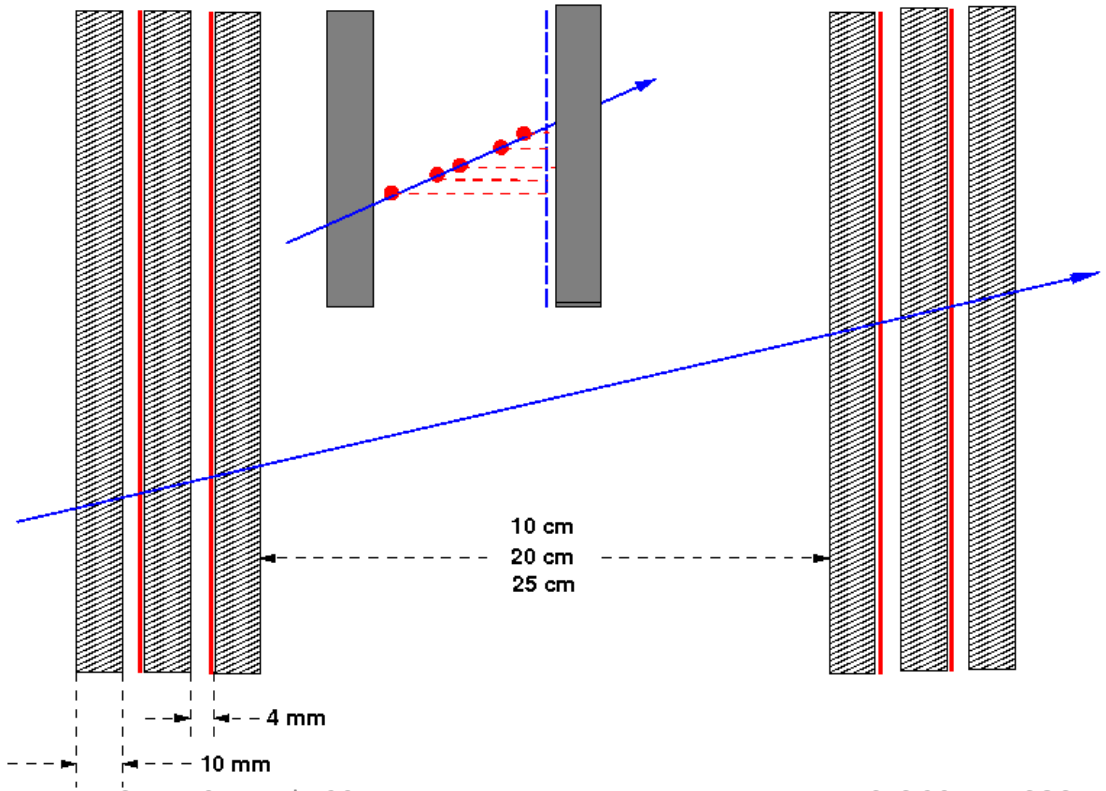
σ = 2 mm / √12 = **580 µm (only CS=1)**

σ = 2/3 mm / √12 = **190 µm (CS=1 or 2)**

It will be tested in the summer H8 test beam

MicroMegas



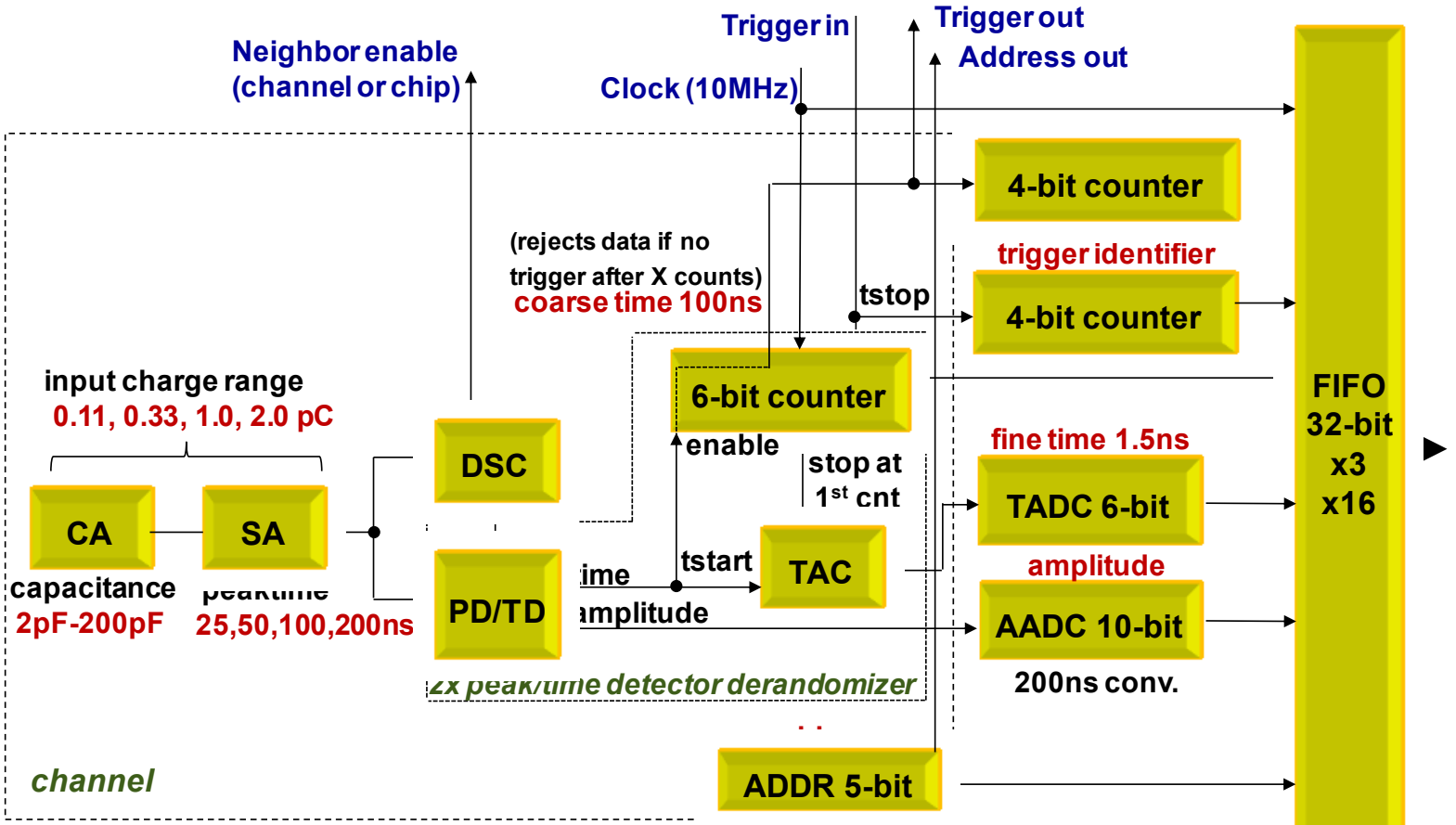


- 2-layer + 2-layer (4 gaps in total) mMegas is foreseen.
  - Charge information for precision measurement.
- Two-dimensional readout per gap (2D MM)
  - 2 M channels in total.
- Strips with 0.5mm pitch.
  - The pitch is fine enough for LVL-1 trigger to reconstruct and find a track with the required resolution using simple discriminator outputs of hit signals. (Information of charge is not necessary.)
  - 25cm lever arm achieves 1mrad angular resolution.

Some desirable features for mMegas frontend

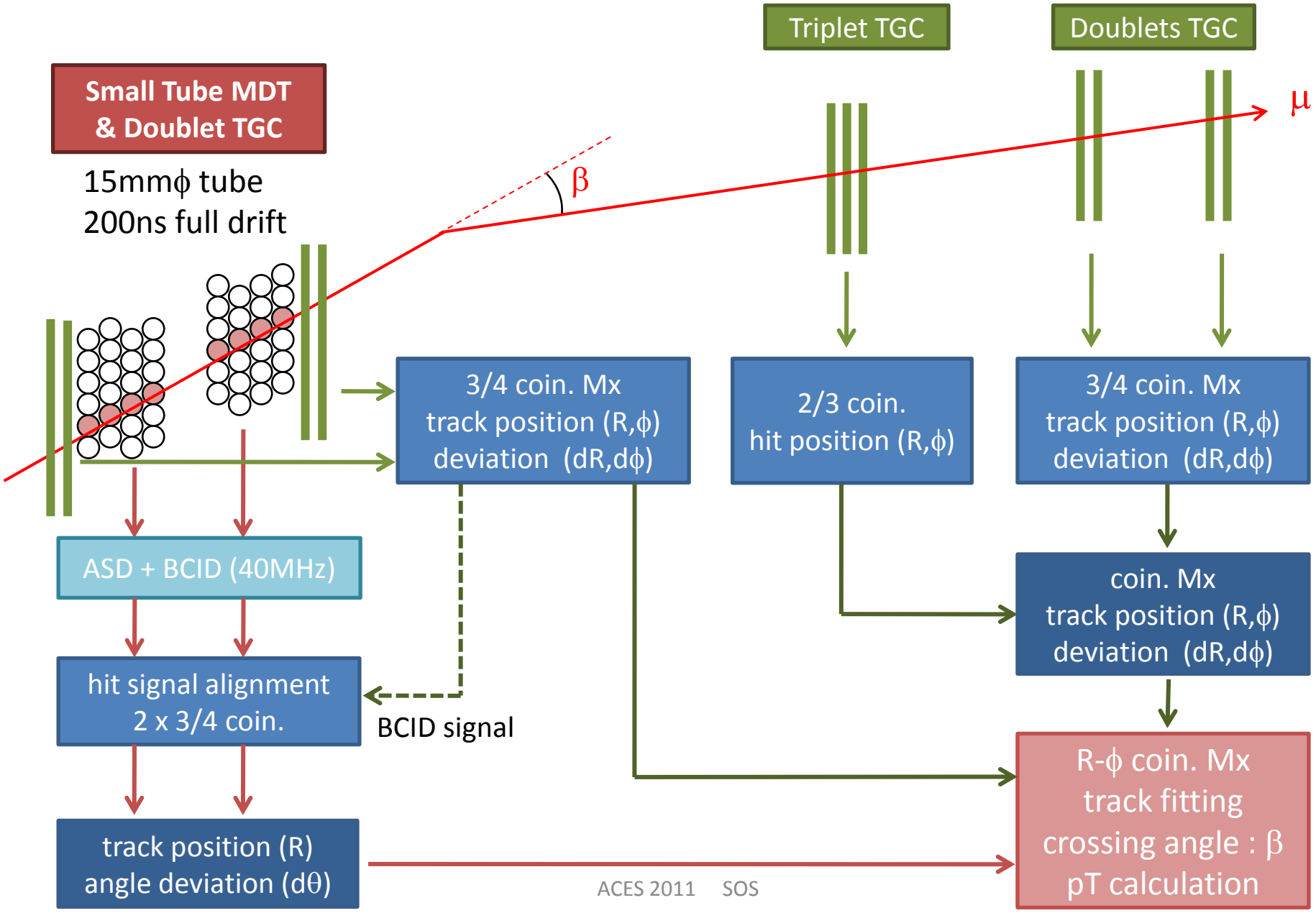
- Real Time Peak Amplitude, Time Detection and on-chip ADC (10-12 bits?)
  - Appropriate for a variety of detectors (mMegas, TGC, TPC, GEM, etc) requiring amplitude and time measurement
  - on-detector zero suppression, dramatic reduction of data bandwidth
- Neighbor channel enabling circuitry (allows relatively high thresholds without losing small amplitudes).
- 64/128 Channels/chip, simultaneous read/write with Derandomizing Buffers
- Able to provide Trigger Primitives for possible on-detector track segment finding logic
  - The address of the earliest cluster arrival associated with a given bunch crossing.
  - Powerful zero-suppression scheme has to be designed to transmit Trigger Primitives to USA15.
- Address of the strips can be directly used in a Look-up-Table, similar to FTK, in USA15.
- Detailed Specifications of back-end to be finalized.

VMM1 IC Block Diagram (not yet finalized)

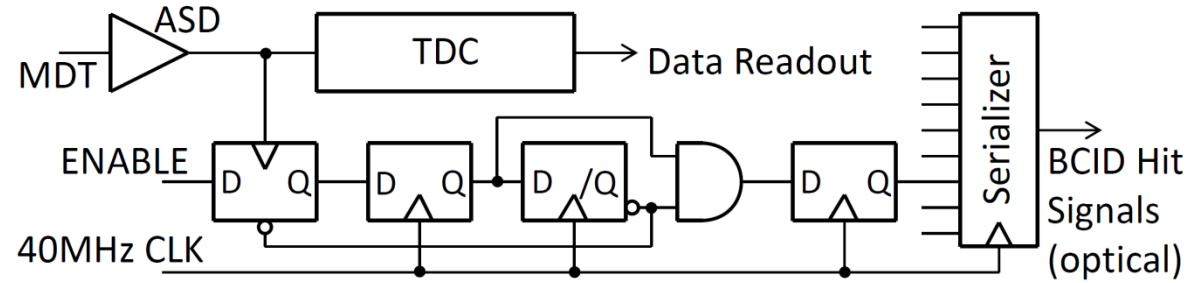


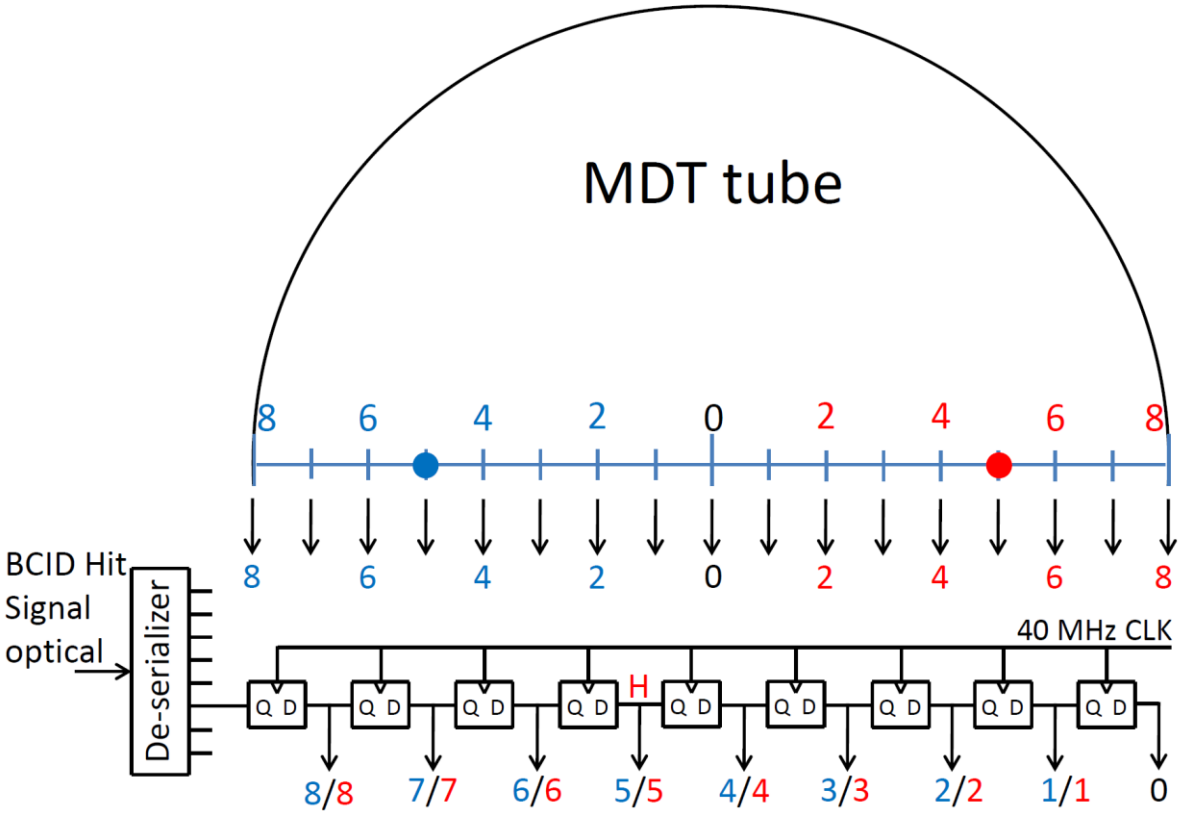
- 64 channels/chip, CMOS 130nm, 1.2V, MPW
- adj. polarity, adj. gain (0.11 to 2 pC), adj. peaking time (25-200 ns)
- derandomizing peak detection (10-bit) and time detection (1.5 ns)
- real-time event peak trigger and address
- integrated threshold with trimming, sub-threshold neighbor acquisition
- integrated pulse generator, calibration circuits, analog monitor, channel mask and temperature sensor
- continuous measurement and readout, derandomizing FIFO
- few mW per channel, chip-to-chip (neighbor) communication, LVDS interface

Small Tube MDT & TGC of SW + TGC of BW's



BCID and Decoding circuits

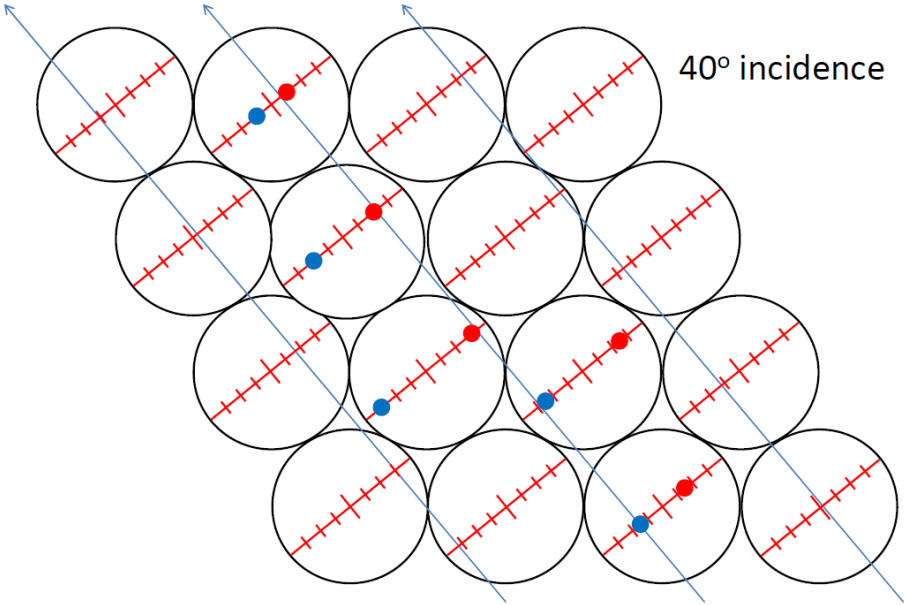


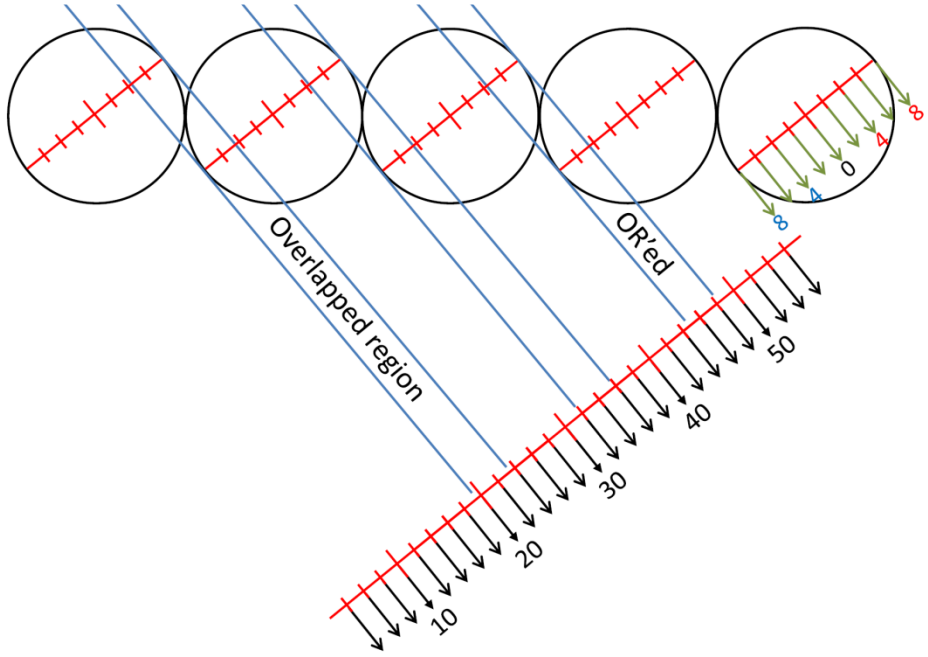


Leading edges of the hit signals from the ASD's are detected in each bunch (25ns), which corresponds to ~1mm drift. The BCID hit signals are serialized and transmitted to USA15 via optical links (GBT's). The signals from the MDT front-end boards are deserialized and fed to decoding circuits. Each MDT has a 9-stage shift register, which decodes the BCID hit signal to time/spatial-aligned hit signals [8,7,6,,,,2,1,0,1,2,,6,7,8]. A "hit signal" is then transmitted from a register to next from 8/8 to 0 at the 40 MHz clock. The colours (blue or red) correspond to the two possible drift directions of the drift electrons.

Spatial-aligned hit signals

Decoded hit signals from each layer are projectively aligned in accordance with the expected incidence angle of an infinite pT muon. Hit signals from the overlapped region of neighboring tubes are logical-OR'ed.



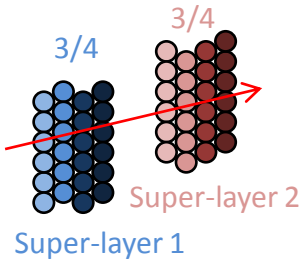


Station (4 x 2 layers) coincidence logic

Aligned hit signals from each layer (1,2,3,4,5,6,7,8 layers) : 1mm step

Bunch timing from TGC

0 1 2 3 4 ..... n n+1 n+2 n+3



Inner layers

The expected track deviations from infinite pT muons are less than ± 1° (pT > 20 GeV), so that one can restrict the track finding window to a very narrow range. 3-out-of-4 coincidence is imposed in each super-layer individually. The information of positions and track deviations from both super-layers are combined and the track candidates are extracted.

The bunch timing signal from TGC will be used to distill track candidates as well as the bunch identification.
The information of distilled tracks is sent to the Sector Logic.

The tracking efficiency, efficiency holes and the probability of the wrong tacking are to be estimated by the simulation works using real data.

track position/deviation

track position/deviation

track position/deviation

Latency Estimation (<3.2μsec)

Present TGC Level-1 Trigger

	nsec	CLK	Total CLK
TOF from interaction point to TGC	65	2.5	2.5
Propagation delay on wire/strip	15	1	3.5
TGC response	25	1	4.5
ASD	10	0.5	5
Cable to PS-Board (12.5m max.)		2.5	7.5
Variable Delay, Bunch ID, OR and signal routing		2	9.5
Variable Delay		1	10.5
3/4 Coincidence Matrix or 2/3 Coincidence Logic		2	12.5
LVDS Tx (SN65LV1023)		1	13.5
Cable to H-pT Board (15m max.)		3	16.5
LVDS Rx (SN65LV1224A)		2	18.5
Variable Delay		1	19.5
H-pT Matrix		2	21.5
G-Link Tx (HDMP-1032A) + Optical Transmitter		1.5	23
Optical Cable to USA15 (90m max.)		18	41
Optical Receiver + G-Link Rx (HDMP-1034A)		2.5	43.5
Sector Logic		7	50.5
Cable to MUCTPI (10m)		2	52.5
MUCTPI (4 + variable)		11	63.5
Cable to CTP (2.4m)		0.5	64
CTP (5 + varable[0-11])		6	70
Cable to LTPi (10m)		2	72
LTPi + LTP + TTCvi + TTCex		2	74
Variable Delay		2	76
Optical Cable to TGC frontend (110m)		22	98
TTCrq + fanout		3	101
Cable to PS-Board (5m max.)		1	102

2.55μsec

Small Tube MDT (SW) + TGC

	nsec	CLK	Total CLK
TOF from interaction point to SW (10 m)	34	1.5	1.5
Propagation delay along wire	25	1	2.5
MDT drift time (0 - 200 ns)		8	10.5
ASD	10	0.5	11
Bunch ID		2	13
Serializer (TLK2501 @ 80MHz) + Optical Tx		2	15
Optical Fibre Cable (90m)		18	33
Optical Rx + De-serializer (TLK2501 @ 80MHz)		3	36
Shift Register (28-steps, 0 - 200 ns)		0	36
coincidence		2	38
track find		2	40
encoding		1	41
MDT (SW) – TGC(BW) combined HERE			**44**
TGC R-ϕ coin. (LUT) MDT-TGC coin.		3	47
crossing angle calculation		3	50
pT calculation (LUT)		3	53
pT encoding		1	54
Cable to MUCTPI (10m)		2	56
MUCTPI		11	67
Cable to CTP (2.4m)		0.5	67.5
CTP		6	73.5
Cable to LTPi (10m)		2	75.5
LTPi + LTP + TTCvi + TTCex		2	76.5
Variable Delay		2	78.5
Optical Cable		22	100.5
TTCrq + fanout		3	103.5
Cable to Frontend Electronics		1.5	105

2.625μsec

Summary

- Barrel : RPC4 stations in the feet region.
  - Phase-0 upgrade

- Endcap : The Small Wheels are replaced.
- Strip readout TGC (sTGC), RPC, microMegas (mM), mPIC, small tube MDT (sMDT) are proposed for Level-1 trigger.
- Trigger schemes of sTGC and sMDT are shown and the latencies are estimated to be 4 -10 clk's longer than the present existing value.
  - The software code for the trigger simulation is being developed to study the algorithm of the track fitting, finding and pT calculation. We also have to evaluate the tracking efficiency, any efficiency holes and the probability of incorrect tracking using real data as well as Monte Carlo data.
- The RPC proposed to implement a fast readout providing tracking trigger built-in capabilities.

- Sector Logic Boards (RPC and TGC) will be developed to incorporate new trigger stations (RPC4 and SW) and to adapt to new MuCTPi.