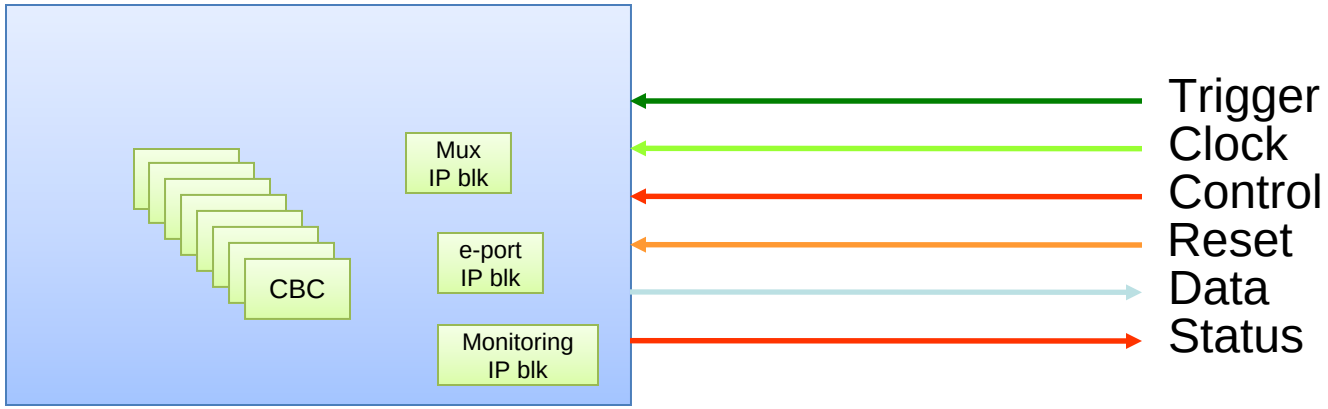
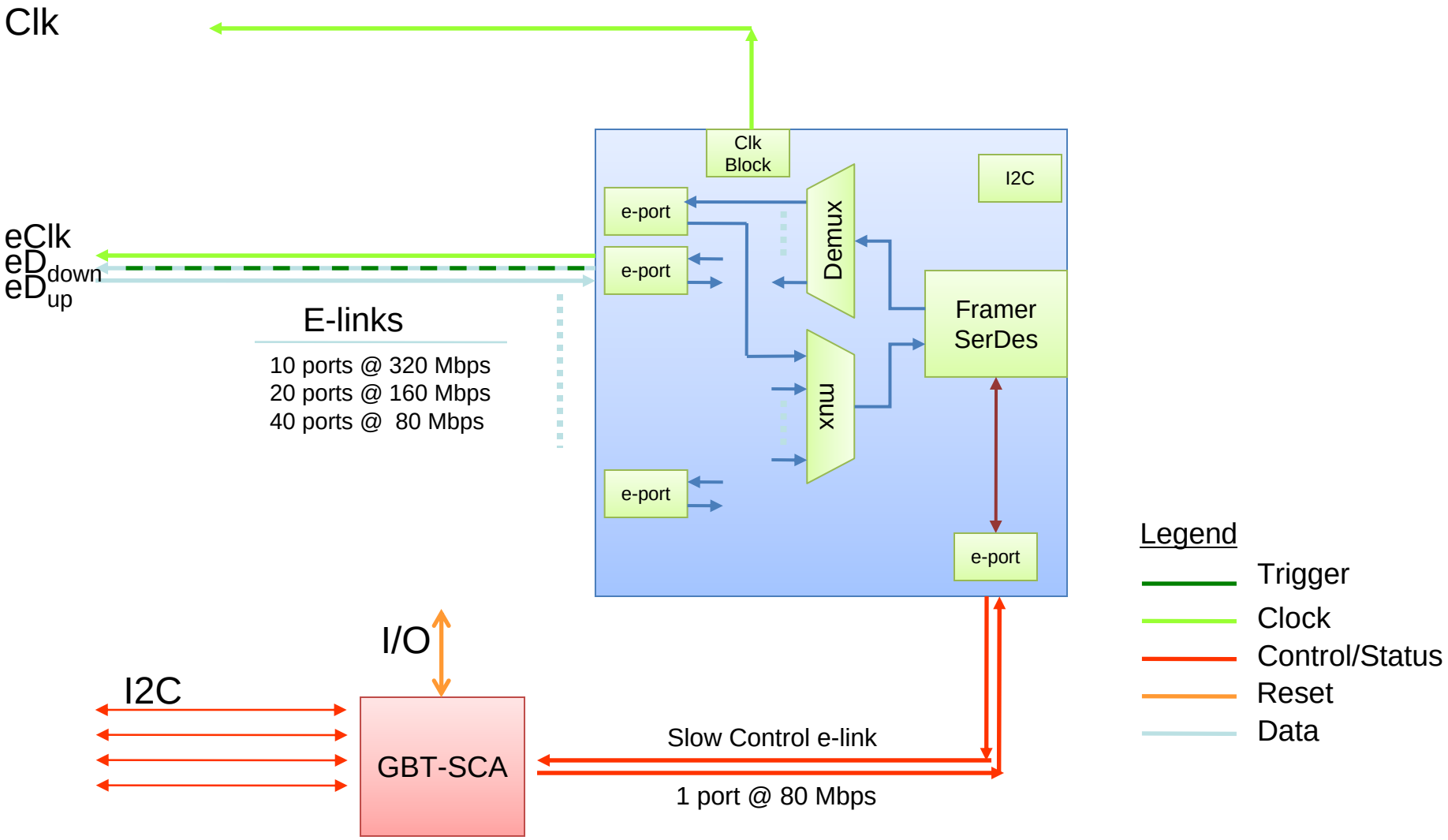
Architecture issues of new readout/control system

How to interconnect GBT and FE-modules

Front-End Module

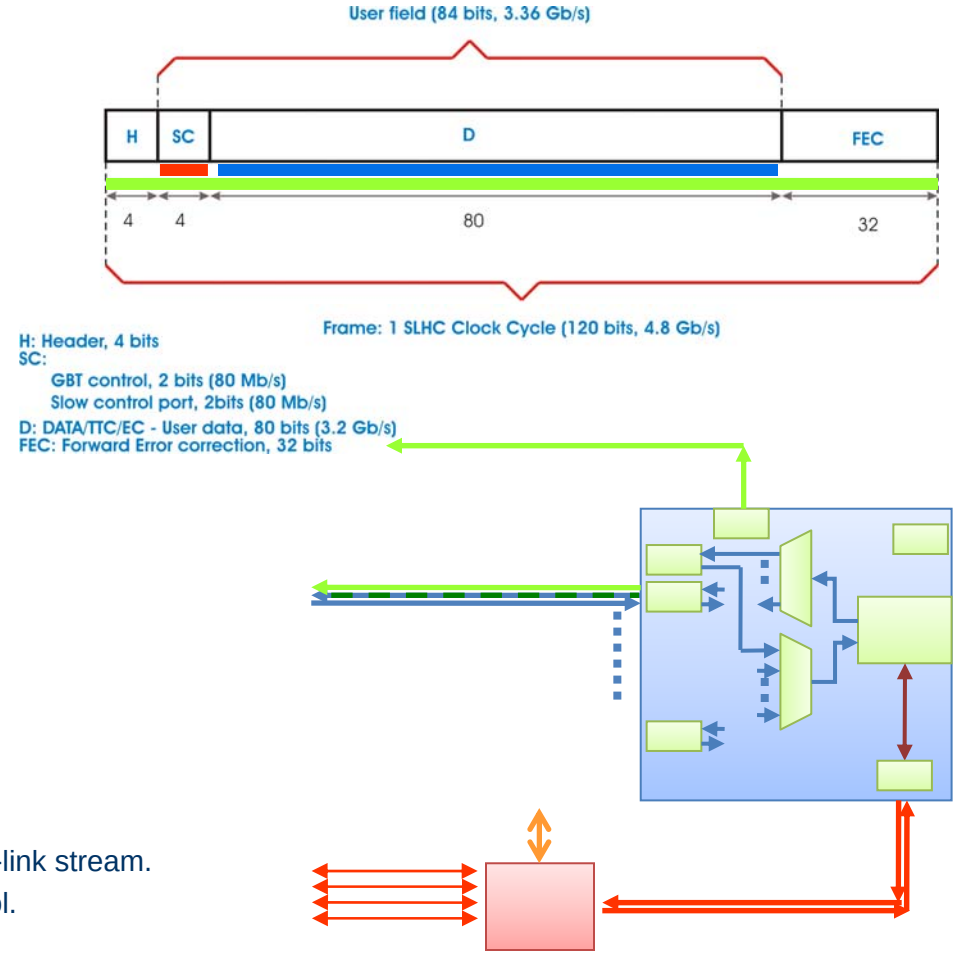


GBT


Clk
eClk
eD down
eD up
E-links
10 ports @ 320 Mbps
20 ports @ 160 Mbps
40 ports @ 80 Mbps
Clk Block
I2C
e-port
e-port
Demux
Framer SerDes
mux
e-port
e-port
I/O
I2C
GBT-SCA
Slow Control e-link
1 port @ 80 Mbps
Legend
Trigger
Clock
Control/Status
Reset
Data

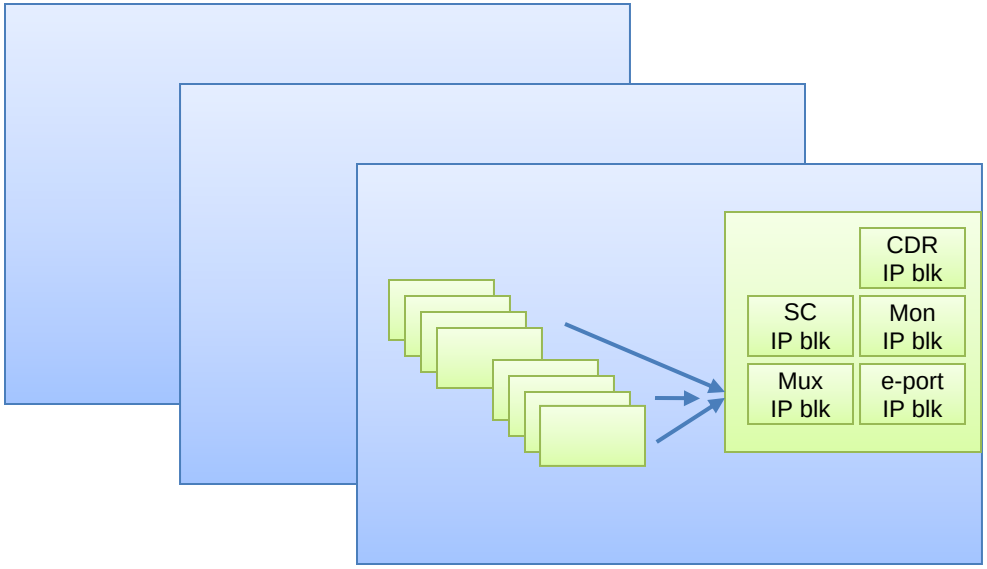
GBT Link Packet Format

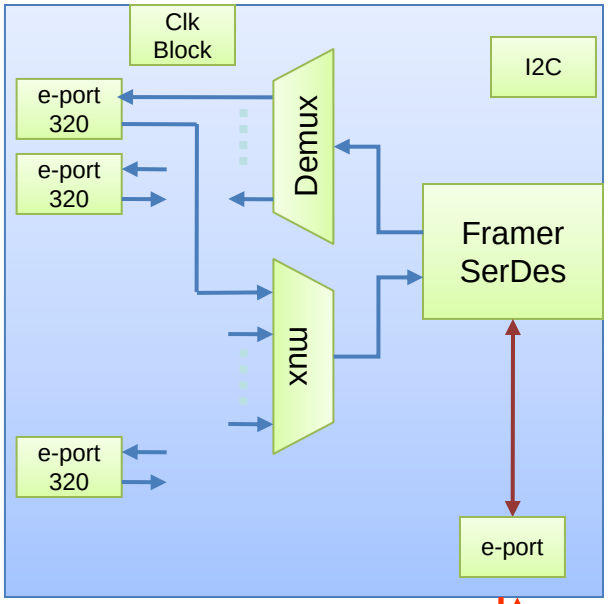
- Fixed packet length: 120bits
  - Packet transmission rate: 1/25ns
  - Data transmission rate: 4.8 Gbps
- Fixed bandwidth allocation:
  - Control path: 160 Mbps
    - 1 internal e-link (for GBT management)
    - **1 external e-link (for GBT-SCA chip)**
  - Data path: 3.2 Gbps
    - 10 e-links @ 320 Mbps
    - 20 e-links @ 160 Mbps
    - 40 e-links @ 80 Mbps
- Data flow:
  - Symmetrical, Bi-directional data transmission.
  - Transmission of GBT-packets is continuous.
  - Data from e-link ports are muxed/demuxed in the GBT-link stream.
  - GBT data path is unaware of the e-link transfer protocol.



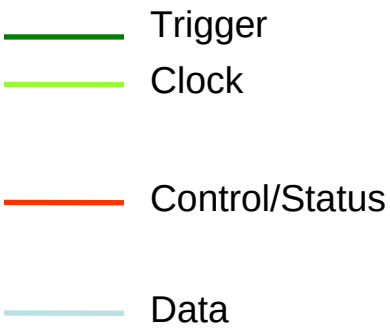
Adapted from P. Moreira's and K. Kloukinas' presentations

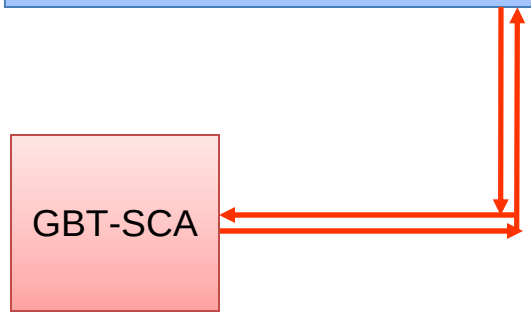
Interconnect options



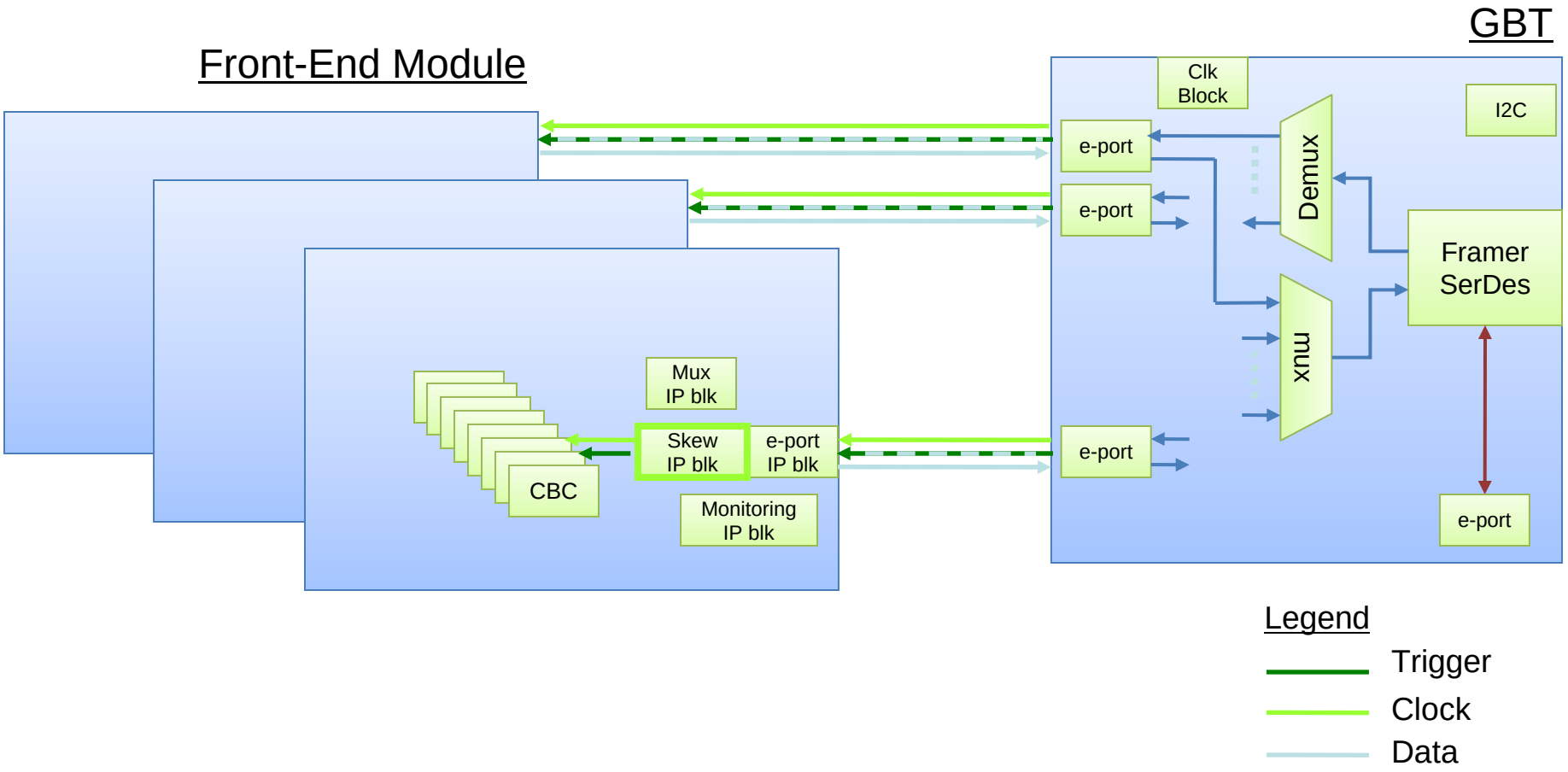


- Factorization:
  - A. timing
  - B. control
  - C. architectures

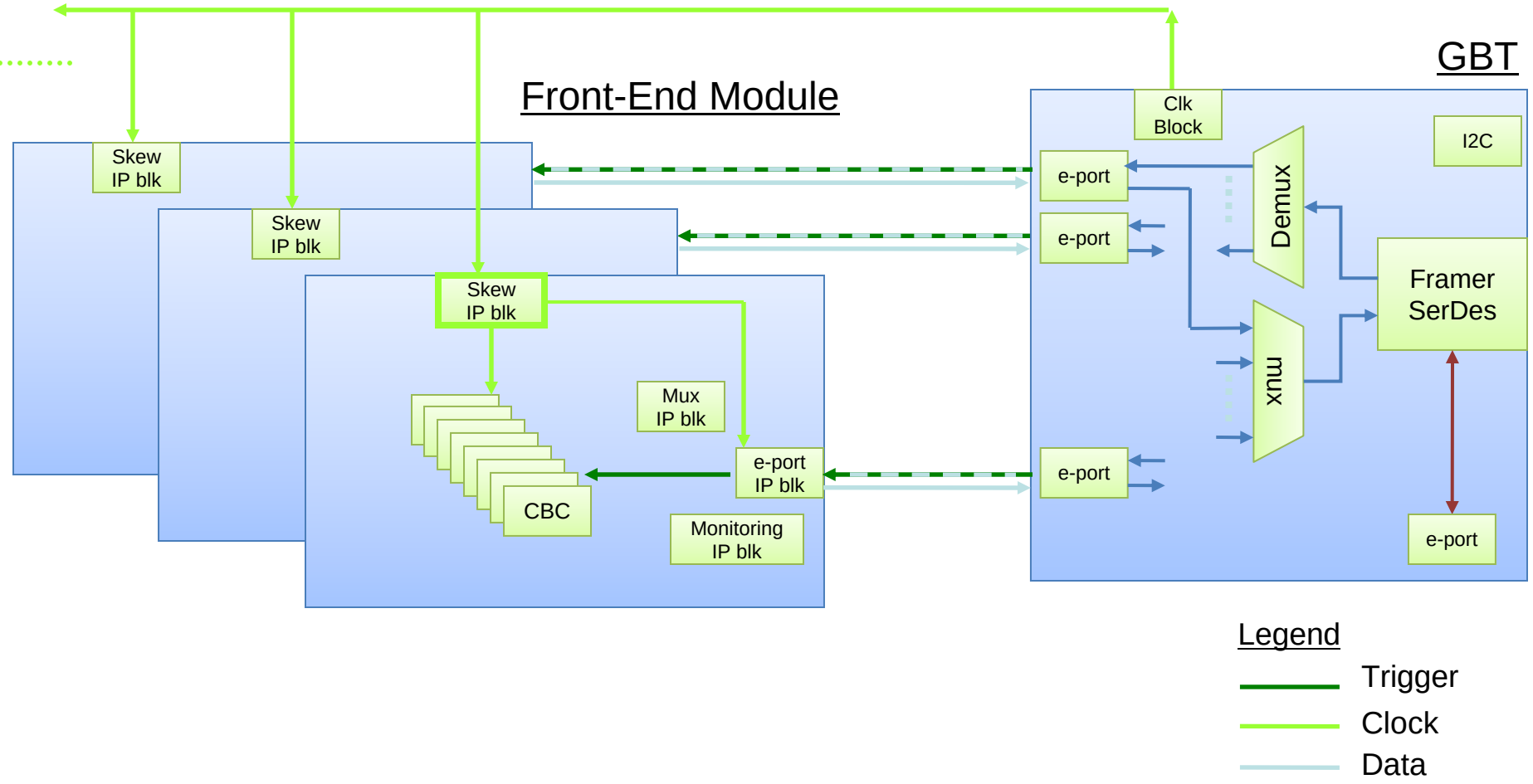




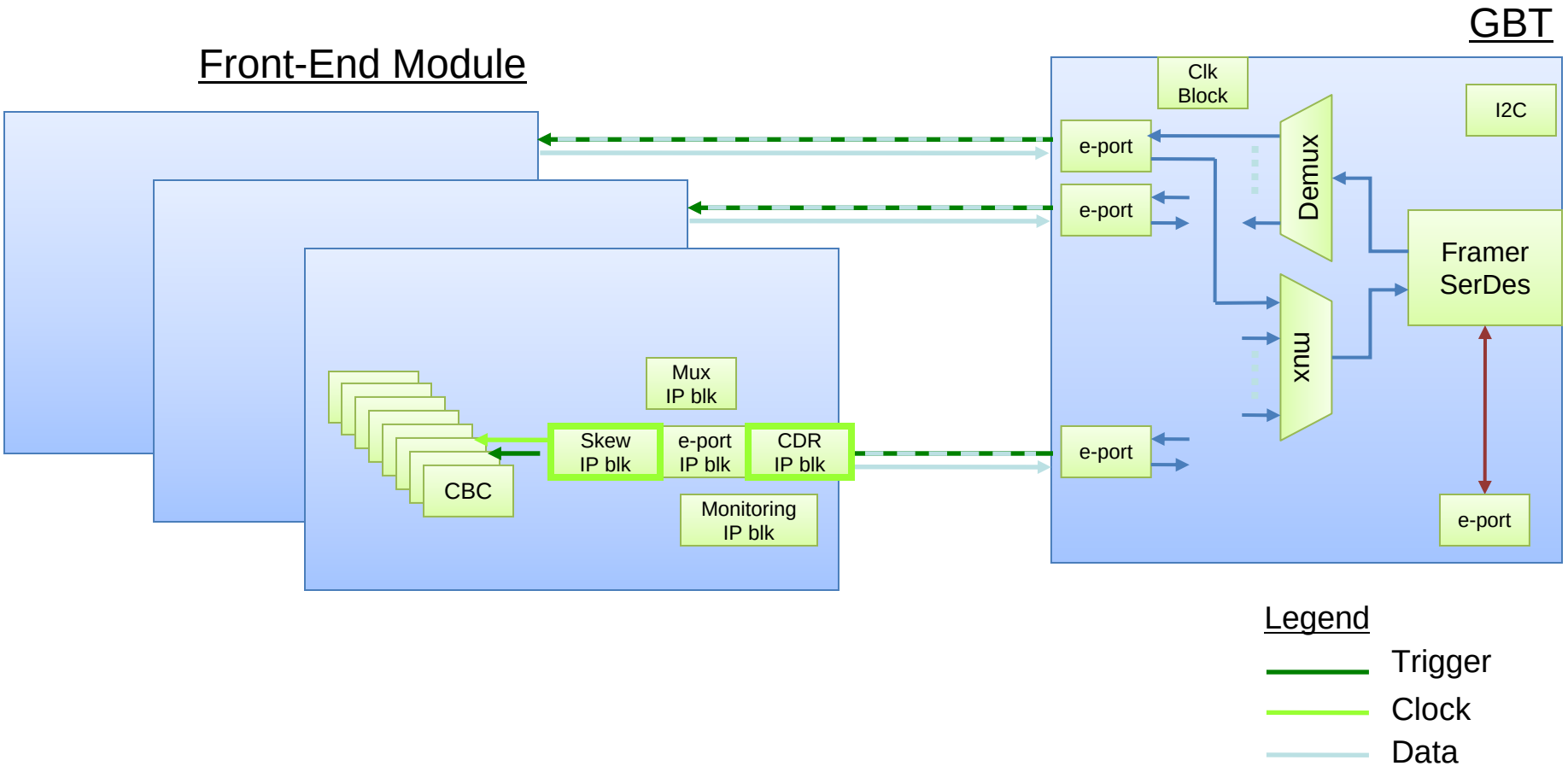
A. Clock and Trigger distribution 1/4



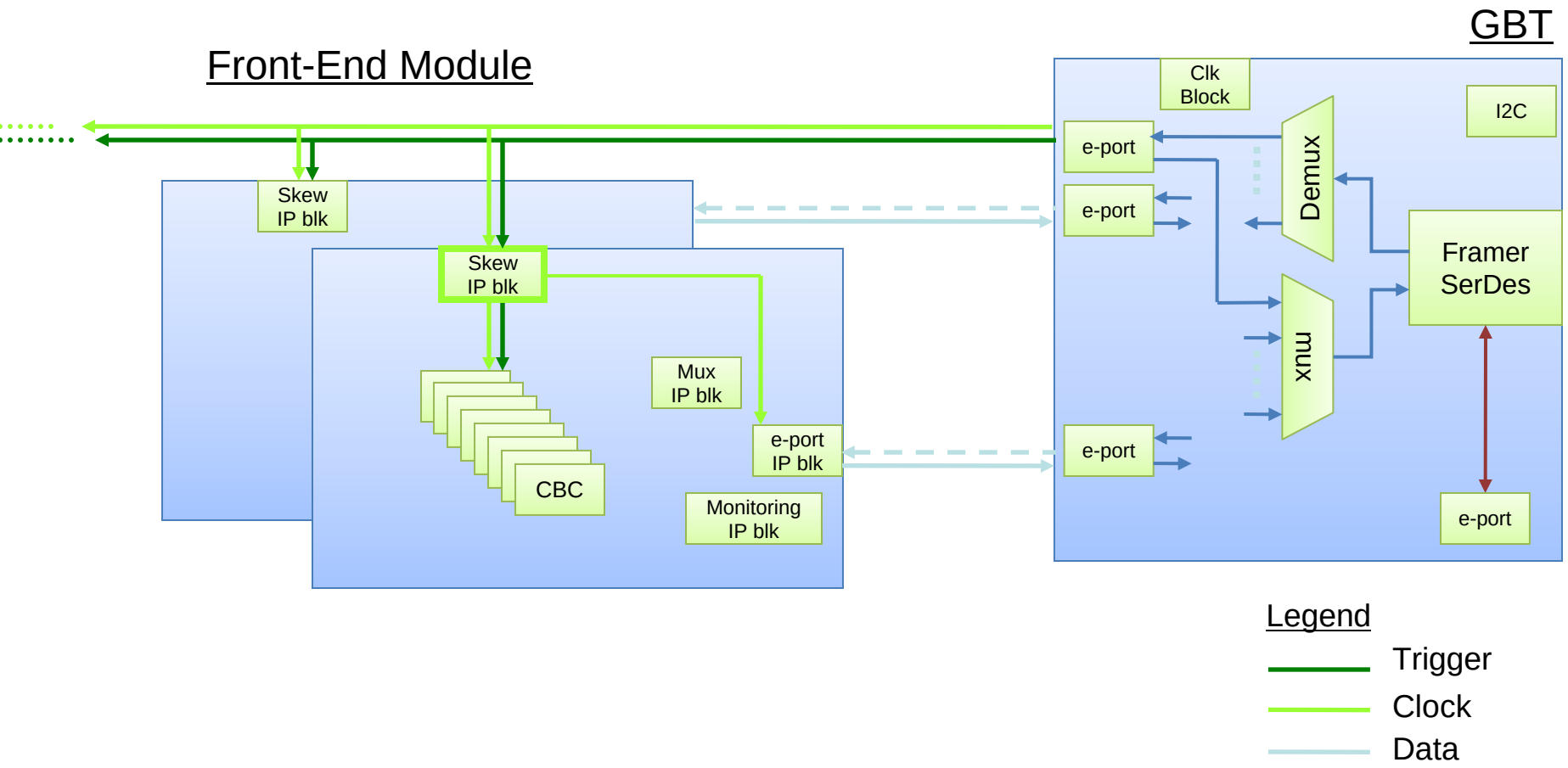
A. Clock and Trigger distribution 2/4



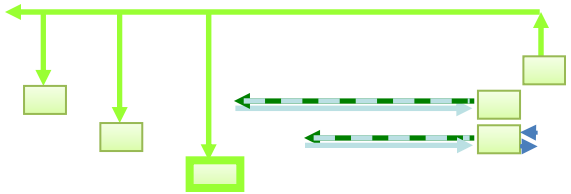
A. Clock and Trigger distribution 3/4

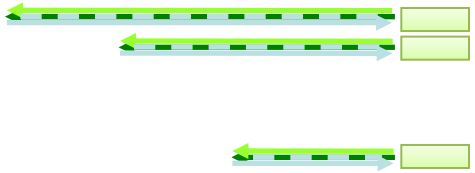


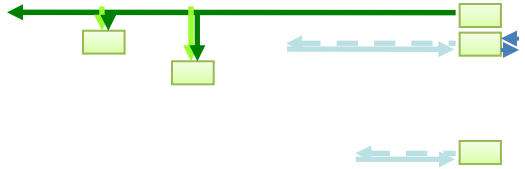
A. Clock and Trigger distribution 4/4



A. Clock and Trigger distribution alternatives

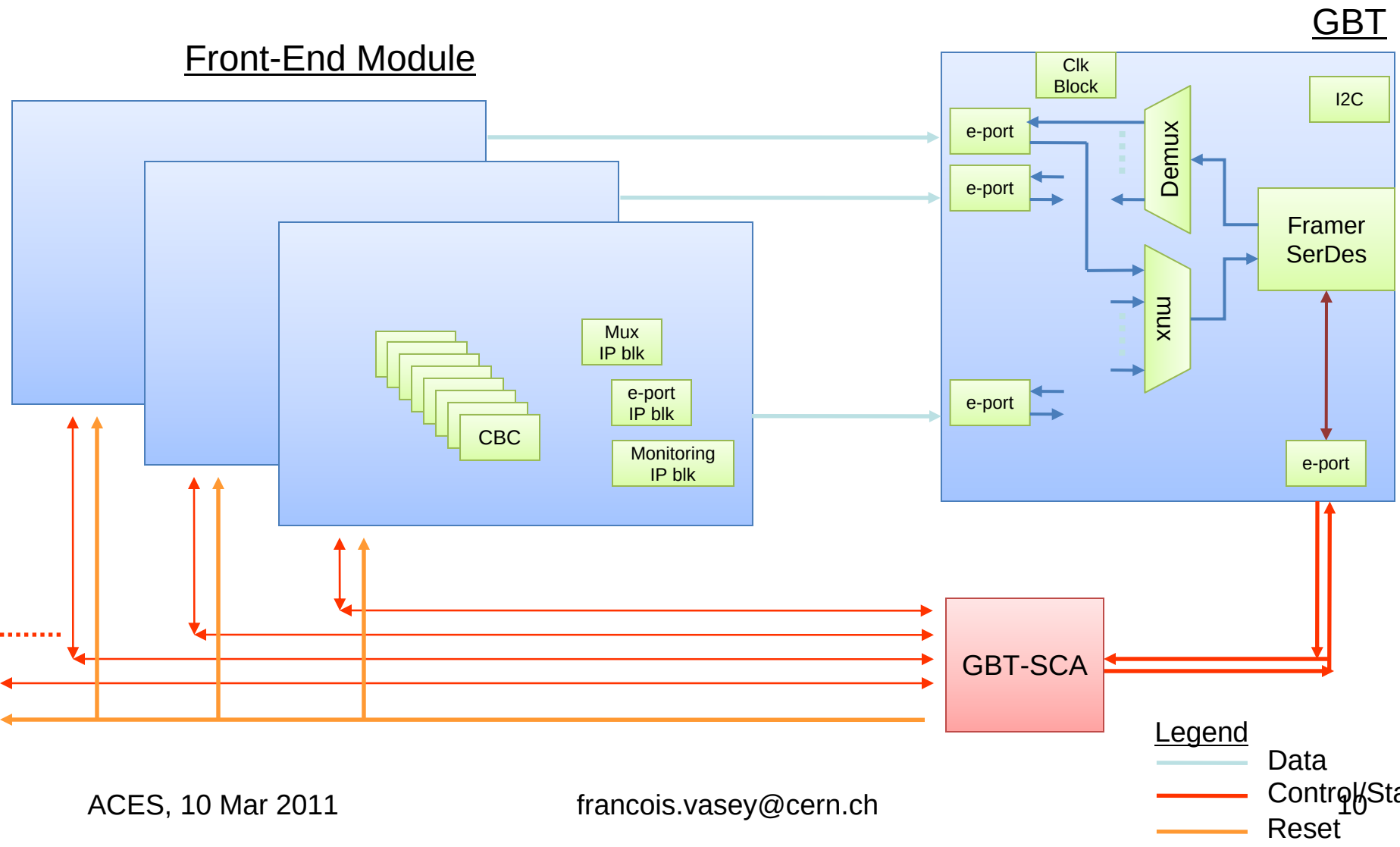




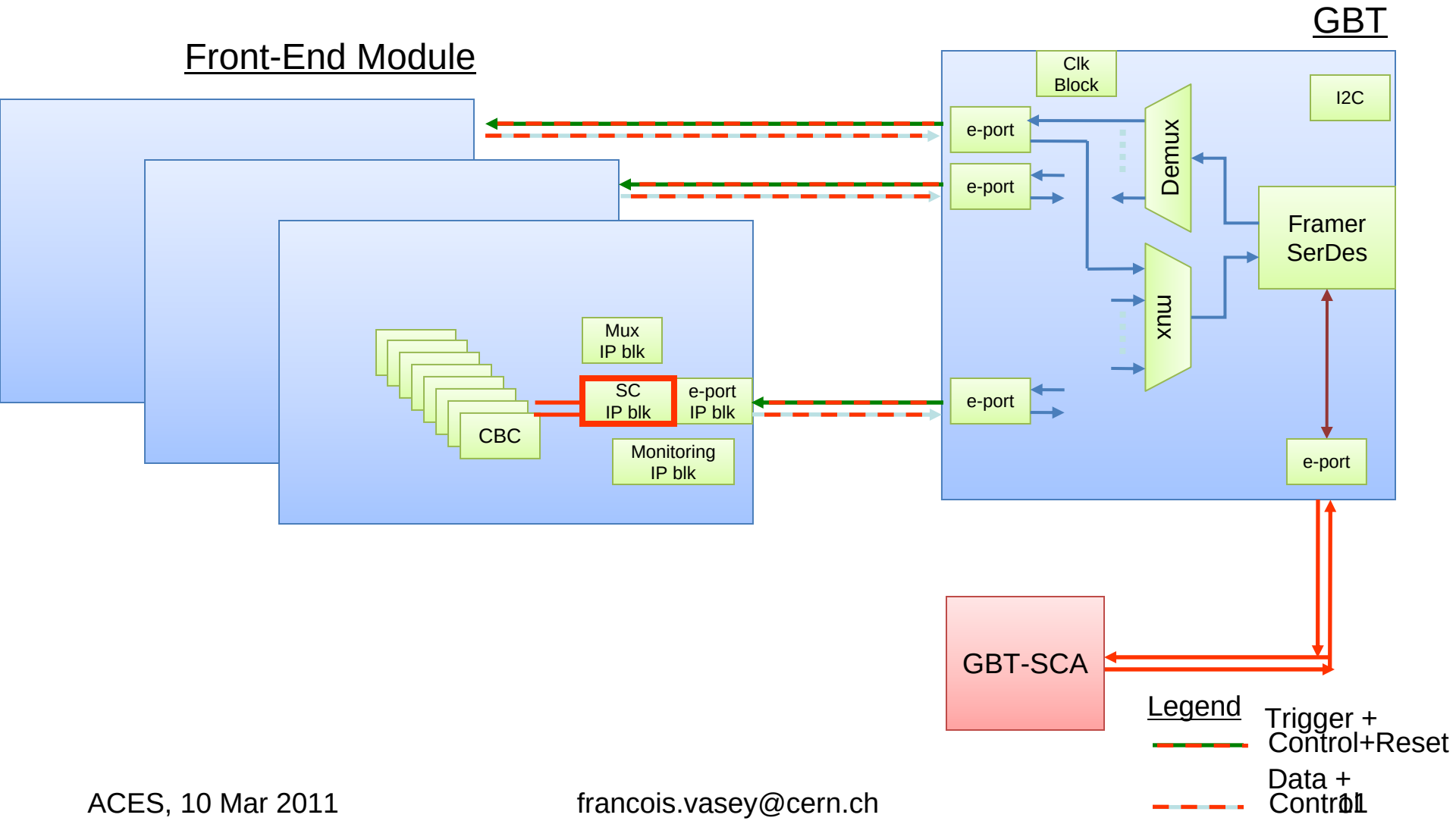


Use GBT Clk block	Use GBT data e-link clock	Use dedicated GBT e-link
Clock line is MLVDS multi-drop	Each front-end module is linked with individual e-port Clock or Clock extracted from e-link data (requires CDR IP blk)	Clock line is SLVS, multi-drop to be confirmed
Trigger sent as e-link downstream data. Up to 8 bits (320Mbps e-port) per Trigger event, to be shared with data	Trigger sent as e-link downstream data. Up to 8 bits (320Mbps e-port) per Trigger event, to be shared with data	Trigger line is SLVS, multi-drop to be confirmed. Up to 8 bits (320Mbps e-port) per Trigger event, dedicated
Multi-drop line is potential single point of failure		Multi-drop line is potential single point of failure
Downstream e-link receiver must recover phase	e-link has dedicated timing	One e-port sxclusively used for clock and trigger distribution

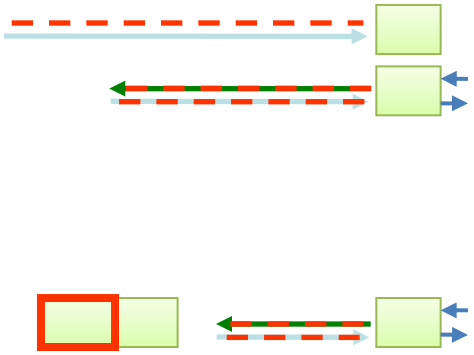
B. Control distribution 1/2



B. Control distribution 2/2

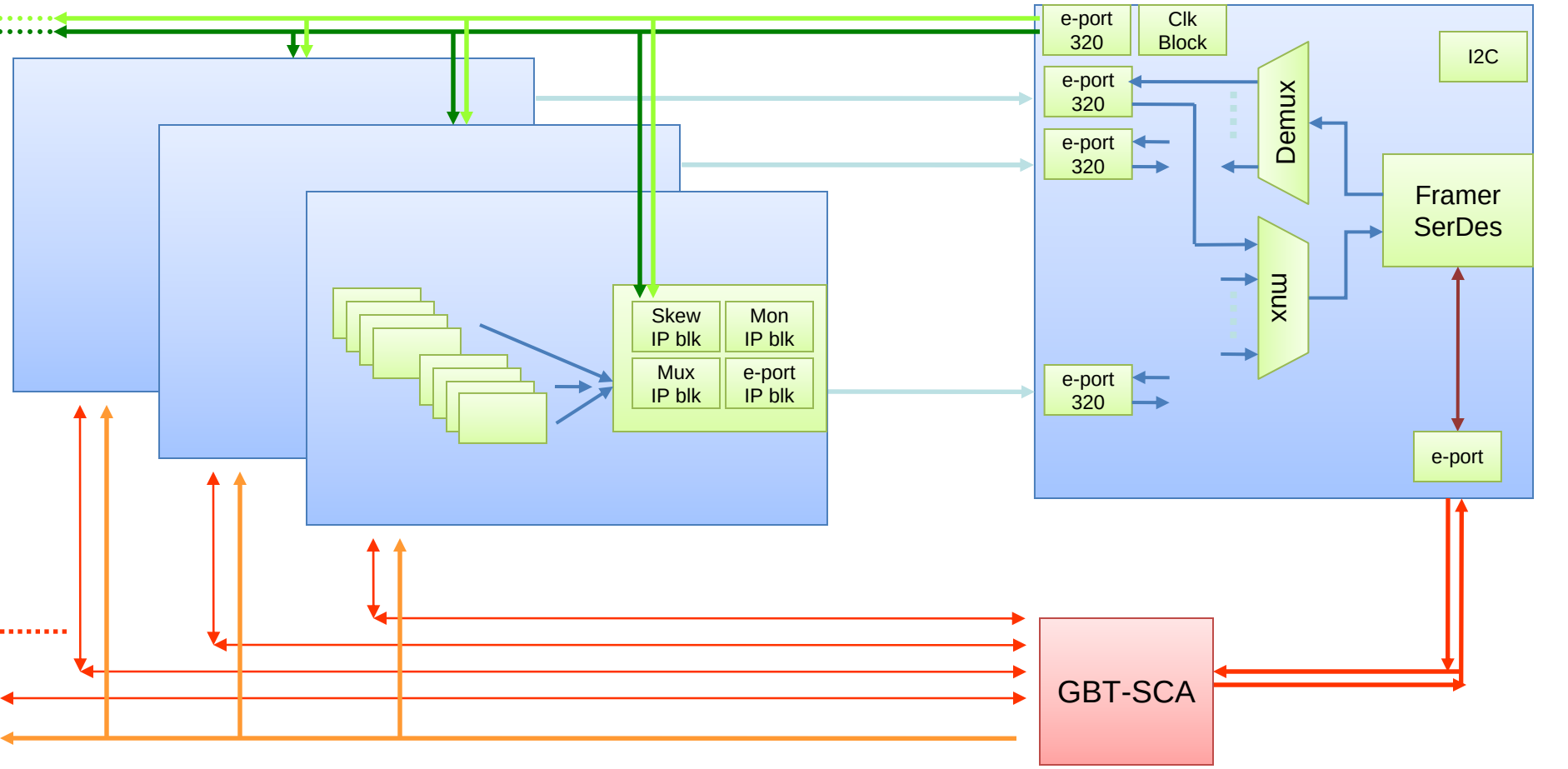


B. Control distribution alternatives

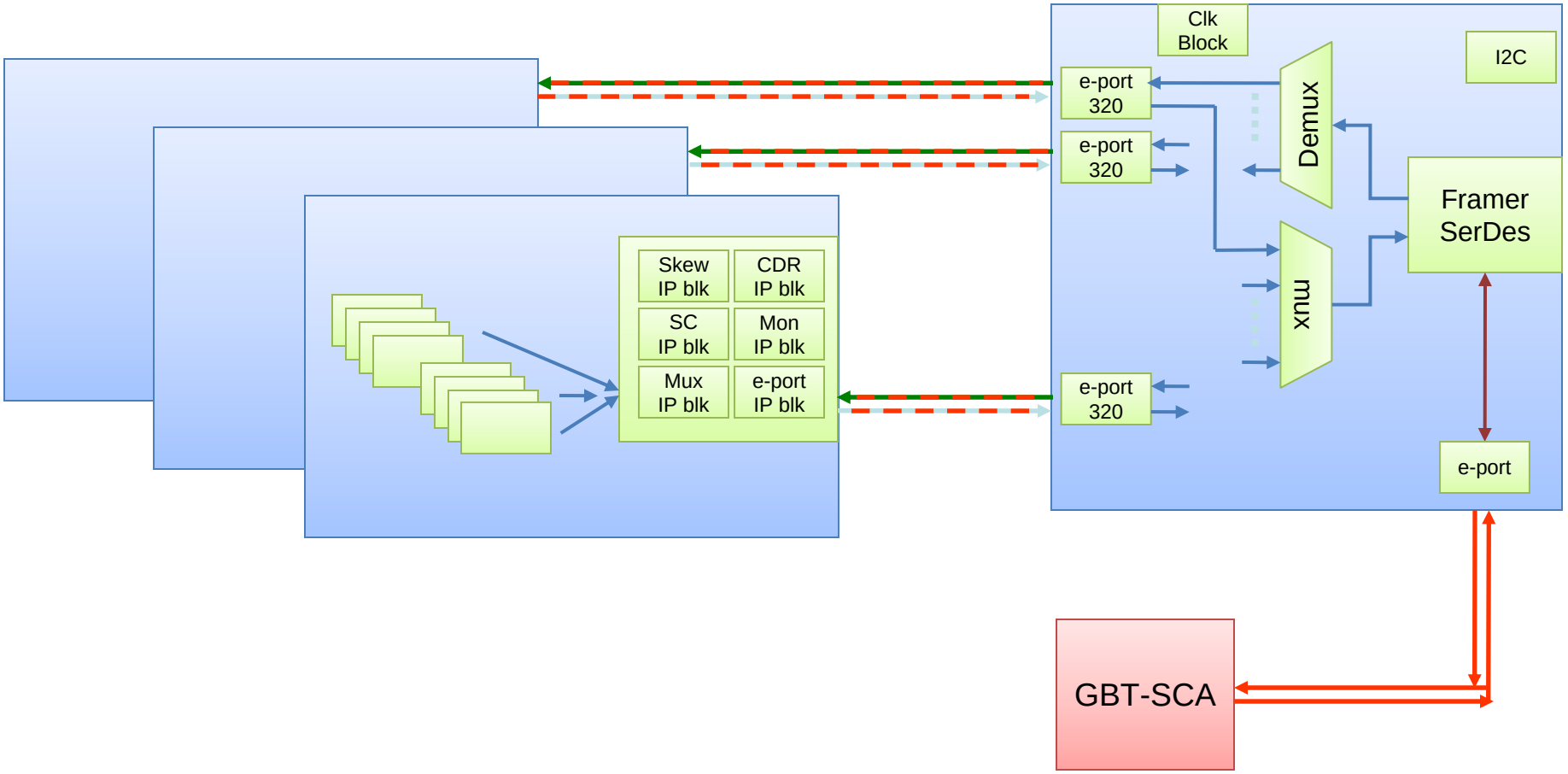


Using GBT-SCA	Using GBT e-link
Controls transit through I2C buses. One multi-drop I2C bus serves all ASICs on one front-end module	Controls transit through e-links. E-port must manage and distribute local communication to all ASICs on front-end module (SC IP blk)
Control bandwidth shared and limited to 1Mbps (100kbps) per front-end module	Control bandwidth of >80Mbps per front-end module
Dedicated control path Dedicated multi-drop reset line driven by SCA I/O port	Trigger + control + reset share downstream e-link. Data + status share upstream e-link
GBT-SCA and multi-drop reset line are single points of failure	No need for off module I2C lines

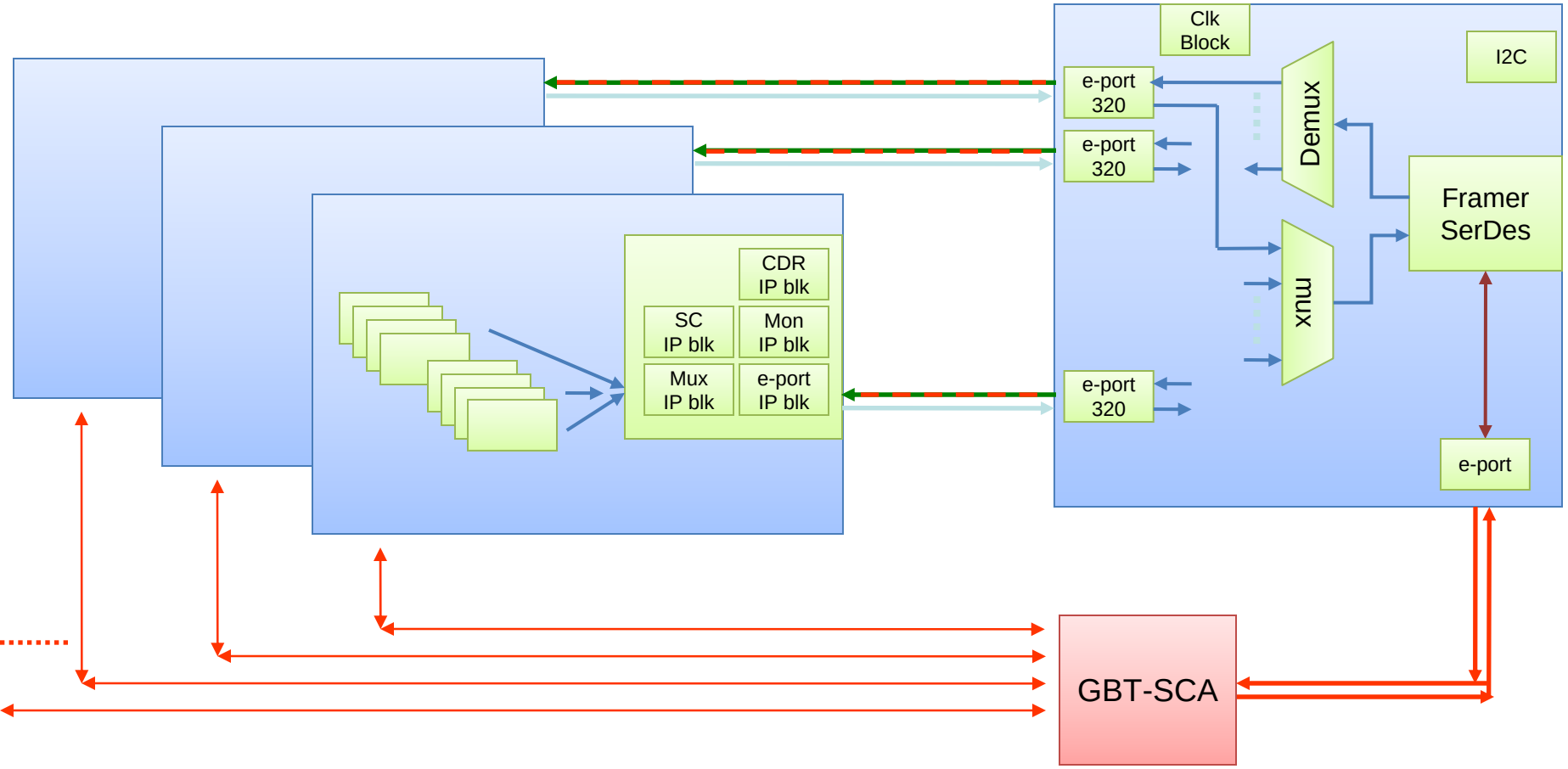
C. Architectures 1/3



C. Architectures 2/3



C. Architectures 3/3



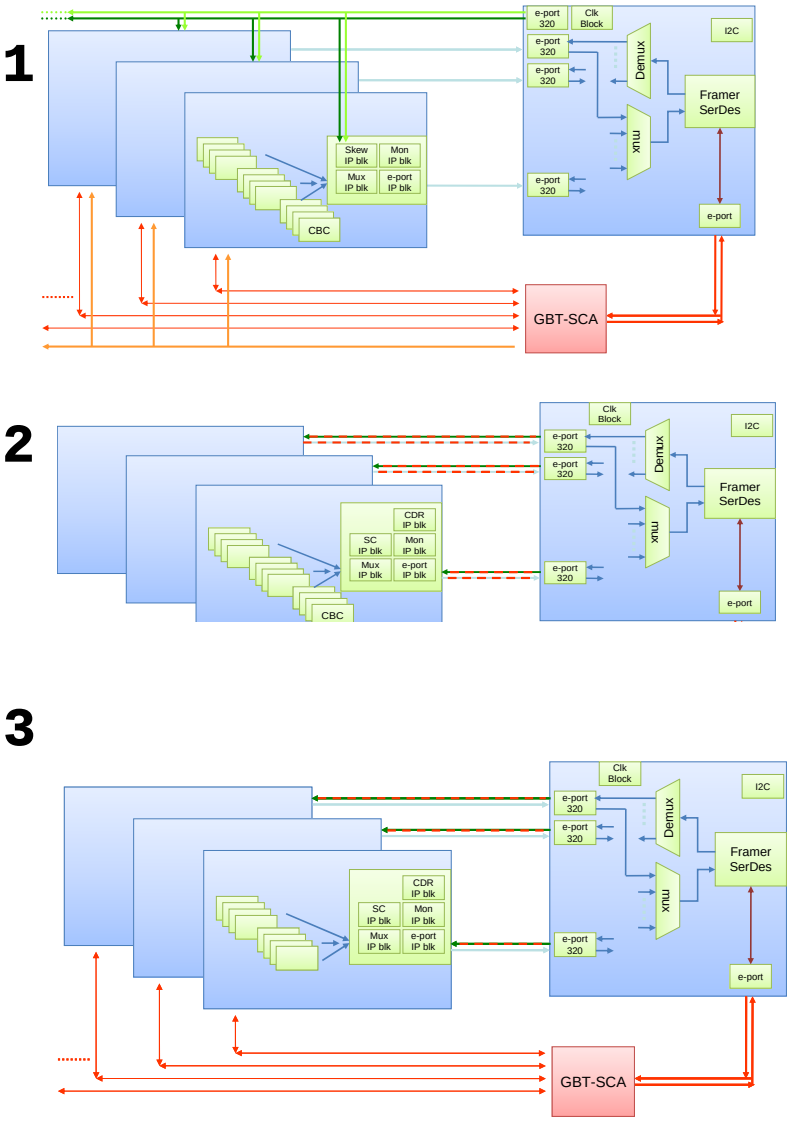
Legend

- Trigger
- Clock
- Control/Status
- Data

Architecture BC

Conclusions

- Many architectures are possible (and combinations of them!)
- Choice driven by:
  - Cabling budget
  - Power budget
  - Control bandwidth
  - System level flexibility
  - Readout bandwidth efficiency
- CMS Tk opted for architecture 3
  - No multi-drop lines
  - No sharing of readout path
  - Possible redundancy of controls (I2C and elink)
  - Allows to progress with system architecture work and mechanical concept design
  - Baseline for the time being, to be rediscussed under the light of new layouts, modularities, etc.



Backup

CMS Strip Tk rod