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ACES 2011 Thursday 10th of March
Trackers Upgrade for Phase 2

Strips Readout Architecture and ABCN 130 nm Front-End ASIC

Speaker : F. Anghinolfi

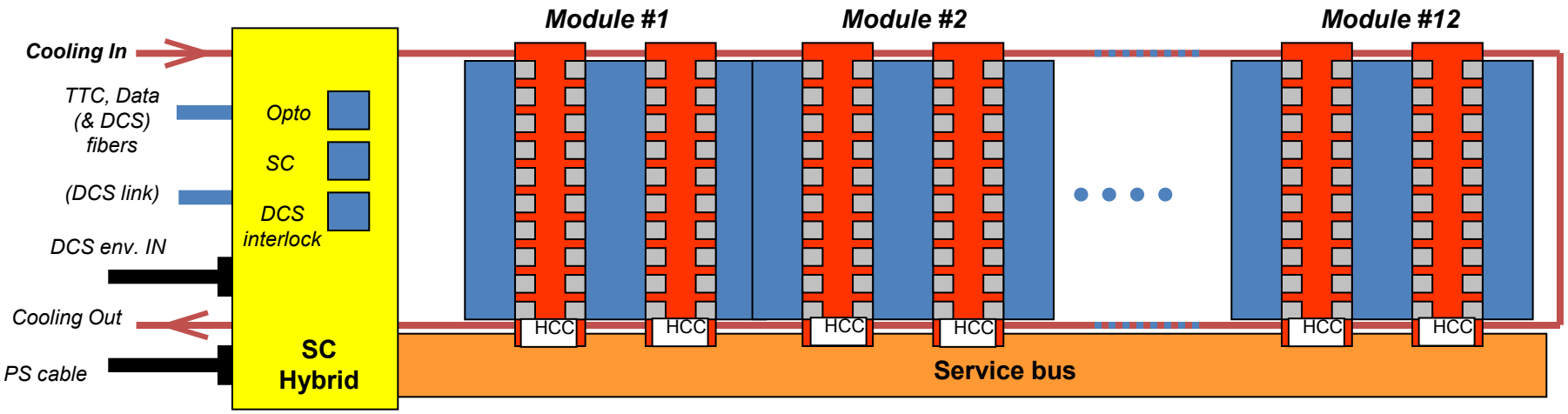
Krakow, Penn U., CERN, Geneva U., RAL, Birmingham, KEK, UCL, UCSC ….

To situate the project

- **Replacement of the existing ABCN25 (CMOS 250nm) for prototyping of Silicon strips stave/module construction**
  - ✓ **More realistic power schema (1.3V instead of 2.5V)**
  - ✓ **256 channels (strips) instead of 128 per ASIC (material reduction)**
- **Major Changes**
  - ✓ **L0/L1 data flow control (Track Trigger)**
  - ✓ **Fixed size Data packet format (1 or 2 cluster/packet, robust against harsh environment)**

ATLAS Strips Readout Concept (Barrel)

ACES 2009

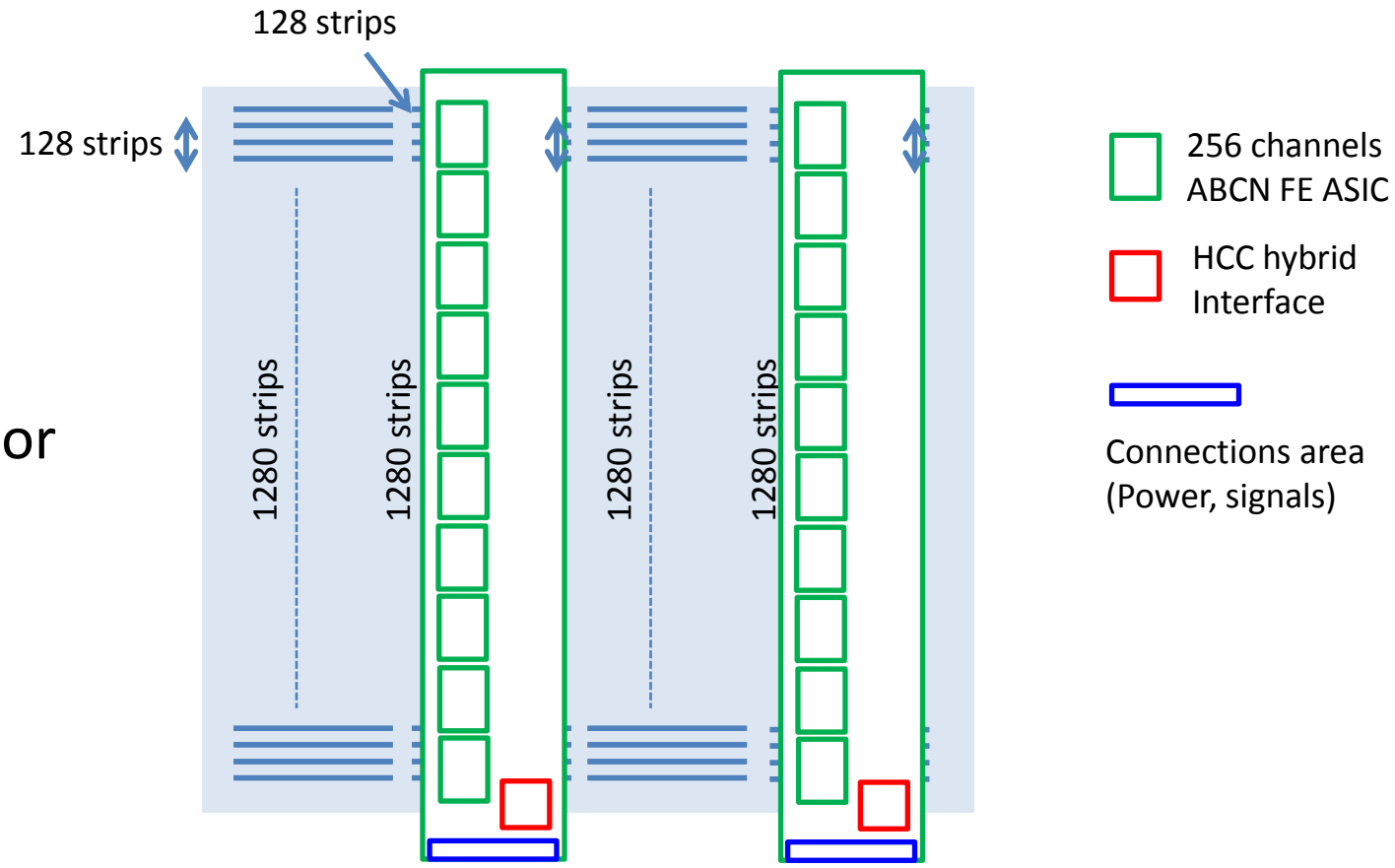


Barrel “short” strips stave : 12 sensors of ~ 10x10cm

Sensor : 1280 strips with ~ 80 microns pitch per row
4 rows with ~ 2.5 centimeters strip length

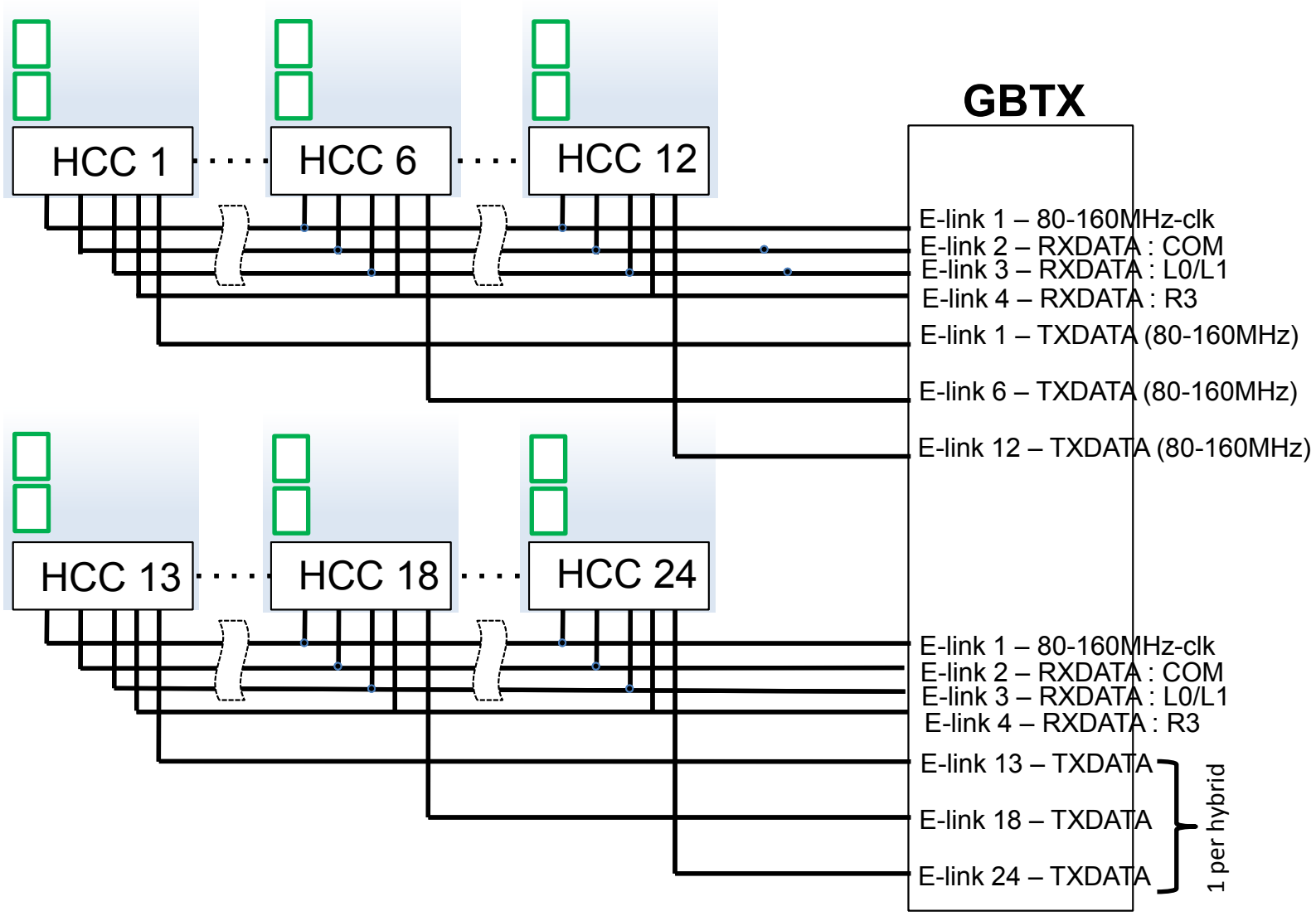
Short Strips Hybrid model

Hybrid over strips detector



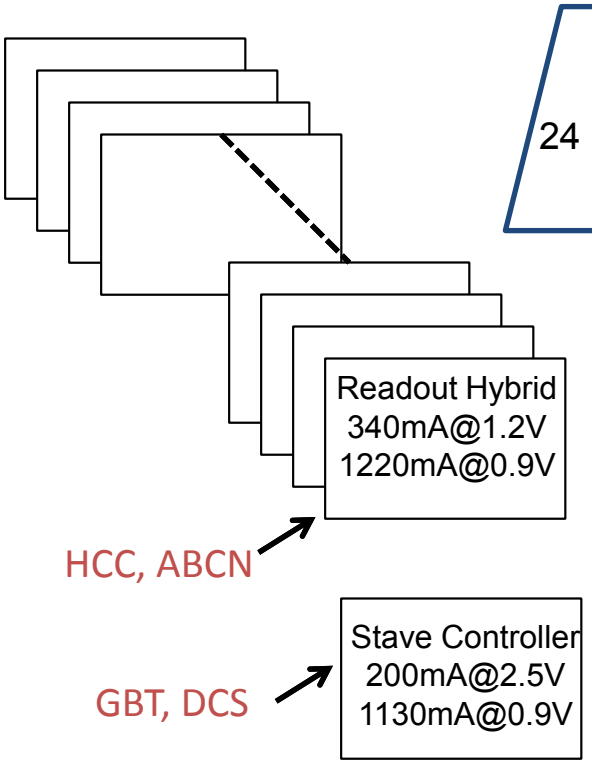
Recent proposal : 256 channels per FE ASIC (10 ABCN per Hybrid)

Hybrid readout through the GBT system



E-link connections btw. 12 modules (24 Hybrids) to GBTX e-links

Power estimates for one short strips single side stave

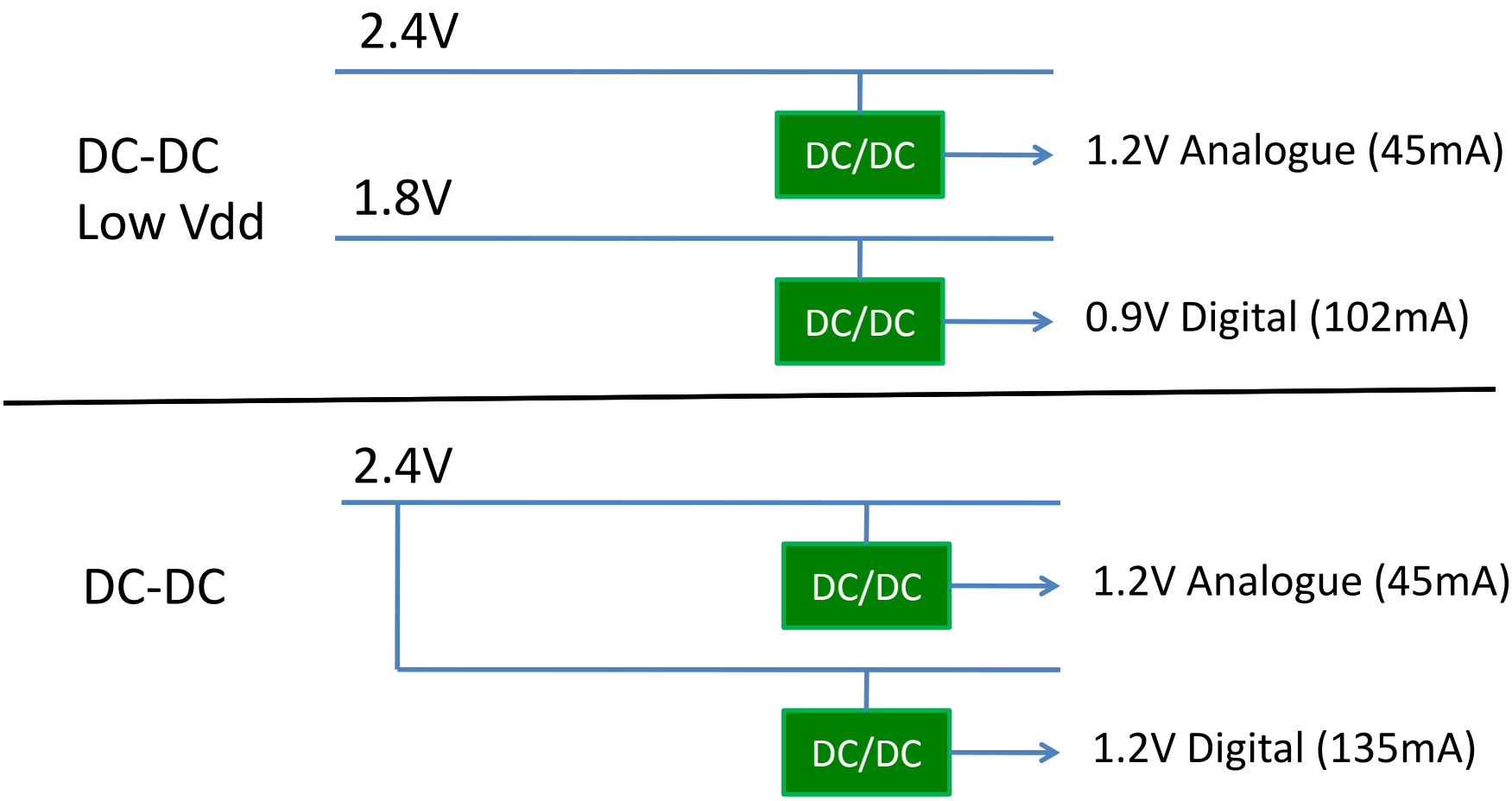


@Vddd = 0.9v	Current	Power
DC-DC	4.1 A	48.6 W
Serial Power	1.8 A	54.9 W

One example for Power numbers, single-side stave with short strips.
Several variants exist

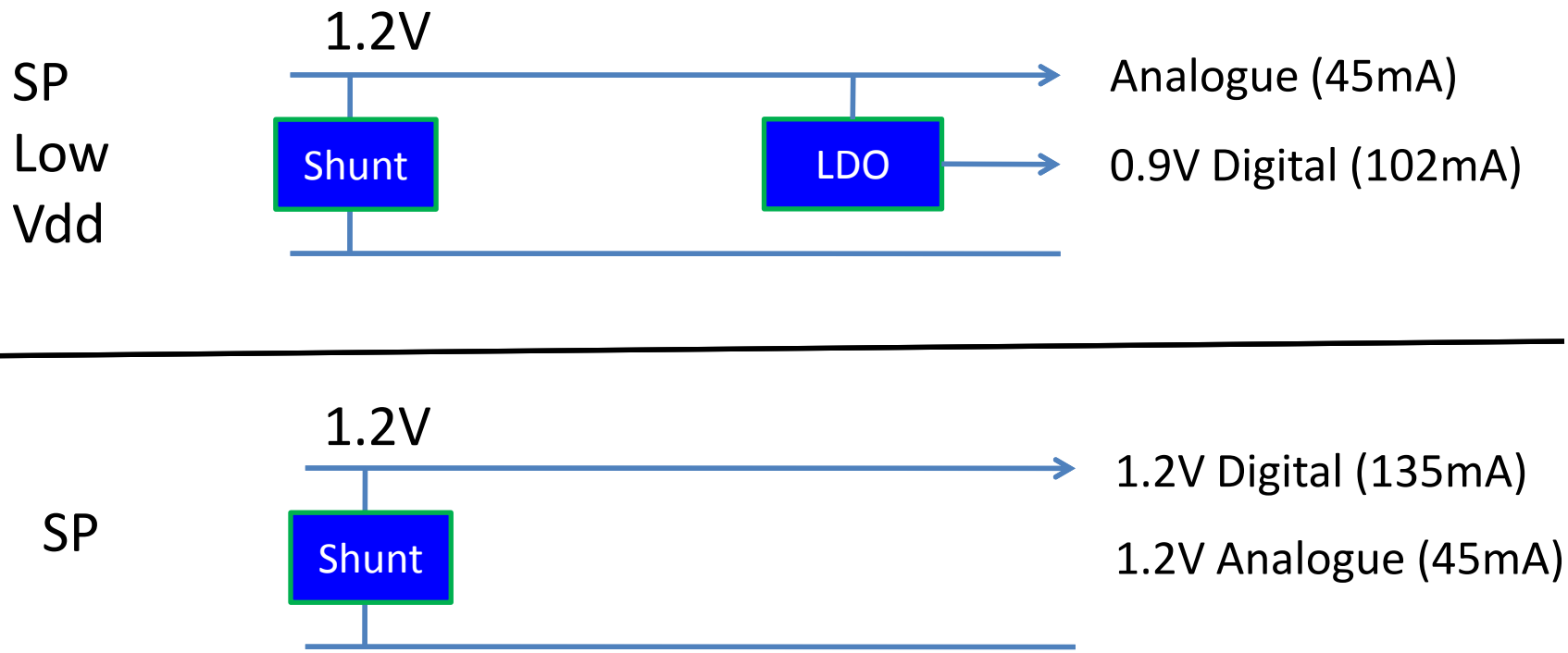
Using VDD digital at 0.9V will be reconsidered after measurements of the SEU cross-section versus VDD

ABCN-130 Powering Schema DC-DC options



There are discussions on placing the DC-DC converters on-chip or on a separate flip-chip

ABCN-130 Powering Serial Power (SP) options

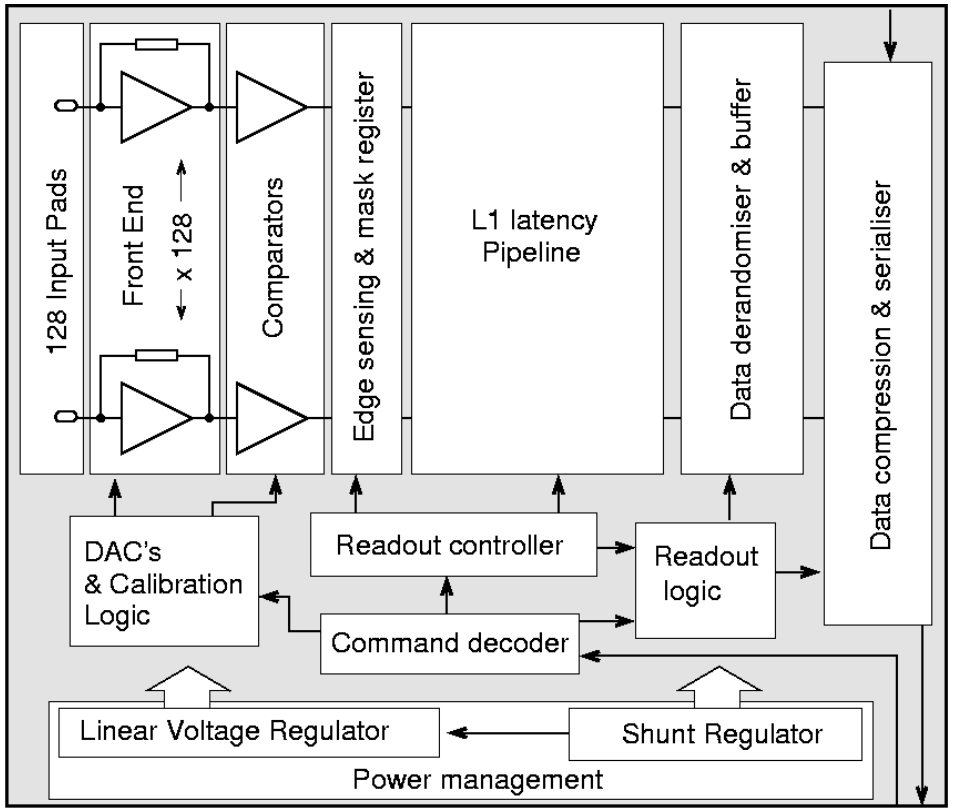


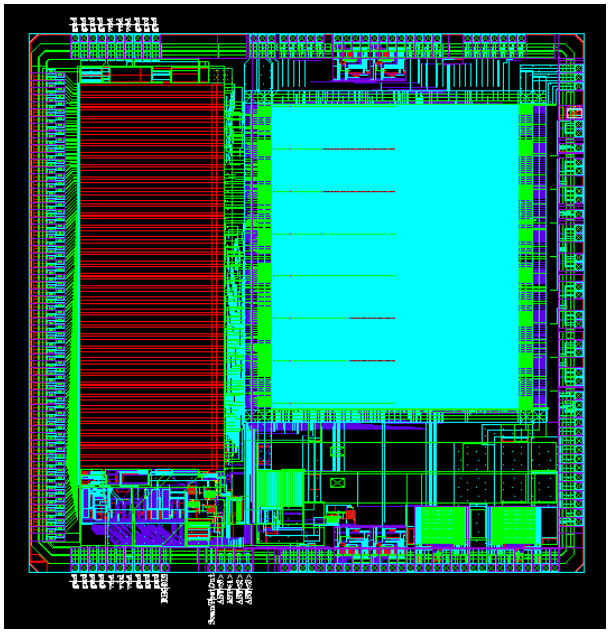
The shunt device is distributed across FE chips, controlled by a common feedback loop

Towards ABCN 130 implementation

- The present ABCN25 realization
- Elements for ABCN 130
- New features in ABCN 130

ABCN25 Strips Readout Asic



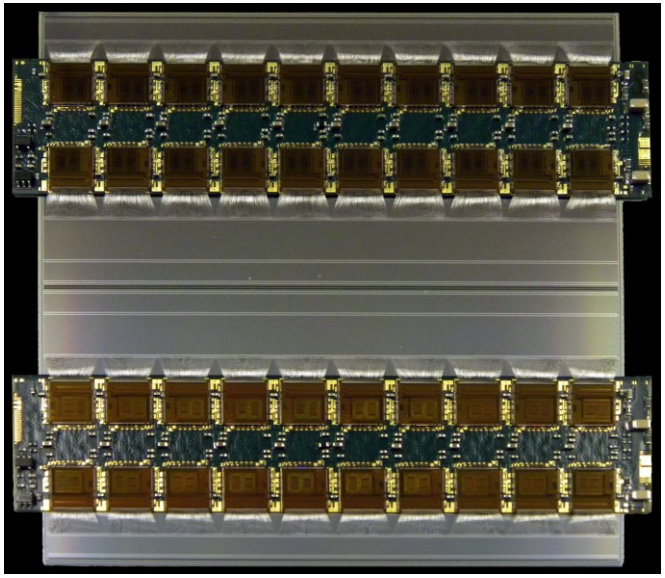


7.7 x 7.5 mm^2

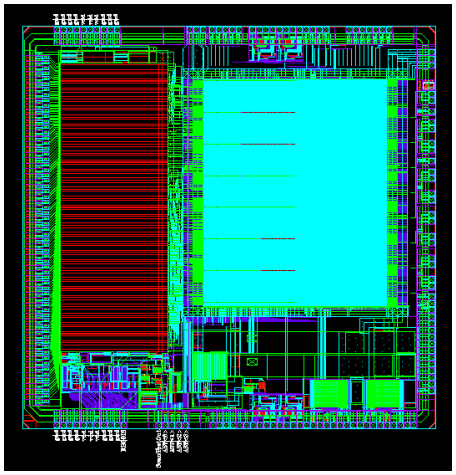
128 channels
35mA @ 2.0V Analogue
135mA @ 2.5V Digital

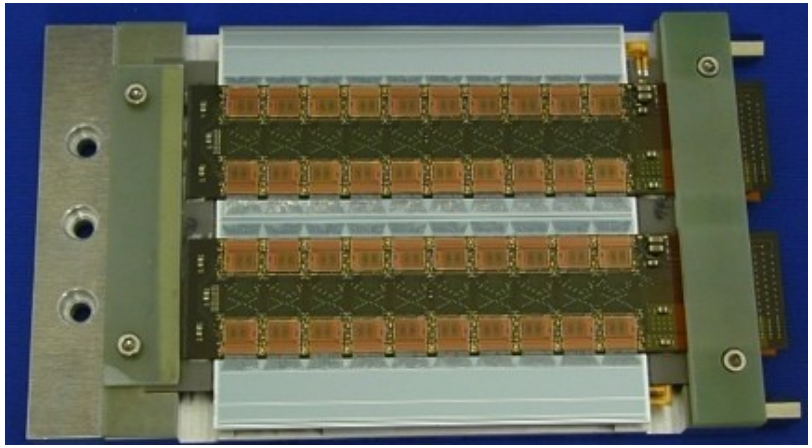
Existing vehicle for hybrid/module/stave developments

ABCN25 Strips Readout on Hybrids



US/UK version





GVA-KEK version

Modules and stavelets are tested with both serial or DC/DC powering sytems (but 2.5V)

ABCN 130nm : What is new/changed ?

- ✧ 256 channels (strips) per ASIC
- ✧ Dual Trigger (L0/L1) data flow control
- ✧ Fixed size data packet per ASIC
- ✧ Extended SEU protection (not commented here)

Maintained :

- ✧ Serial or DC/DC power schema compatible

ABCN 130nm : Front-End Prototype

130nm Front-end (J. Kaplon)

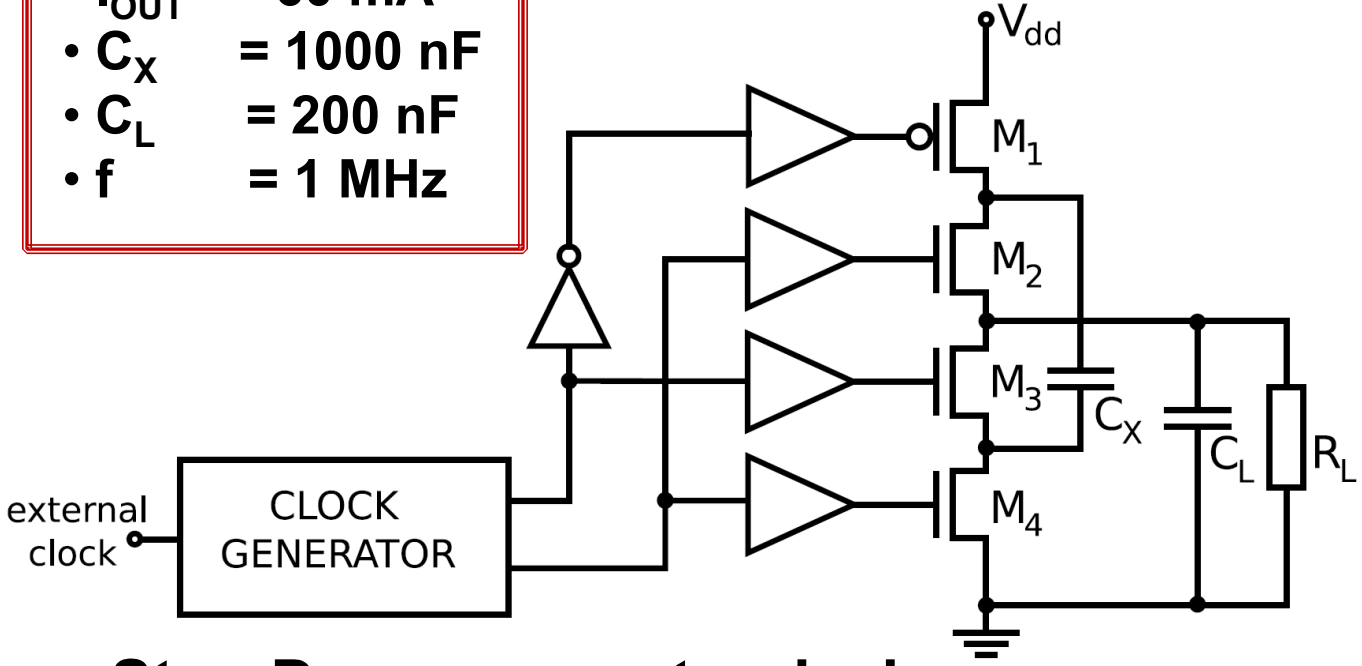
- Channel 22um x 700um (w/o bonding pad area)
- Gain 100mV/fC
- Linear range 4fC (saturation at 6fC)
- Peaking time 22ns
- Current consumption of the front end channel; Iinput+80uA (Iinput = 100-160uA)
- Power consumption @ 1.2V : 220 – 290uW / channel
- Noise estimates →

Det. Cap	I_leakage	I_input	ENC
5p	0	100uA	800e-
5p	600nA	100uA	850e-
10p	0	160uA	1000e-
10p	1.3uA	160uA	1150e-

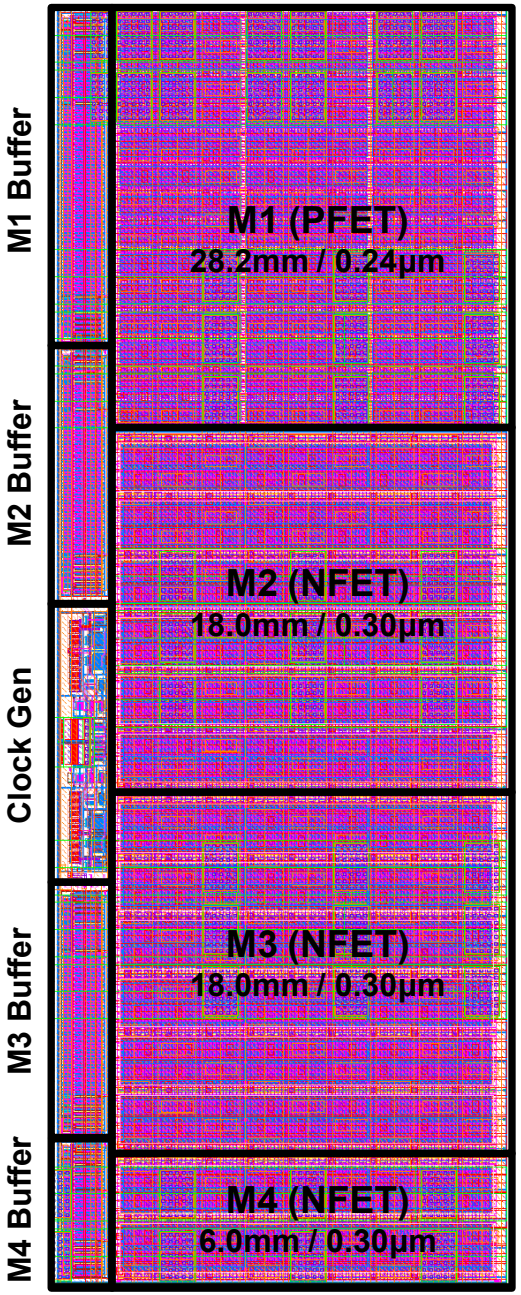
ABCN 130nm : DC/DC prototype

- V_{DD} = 1.9 V
- V_{OUT} = 926 mV
- I_{OUT} = 60 mA
- C_X = 1000 nF
- C_L = 200 nF
- f = 1 MHz

Power Efficiency (including all circuitry) **= 97%**

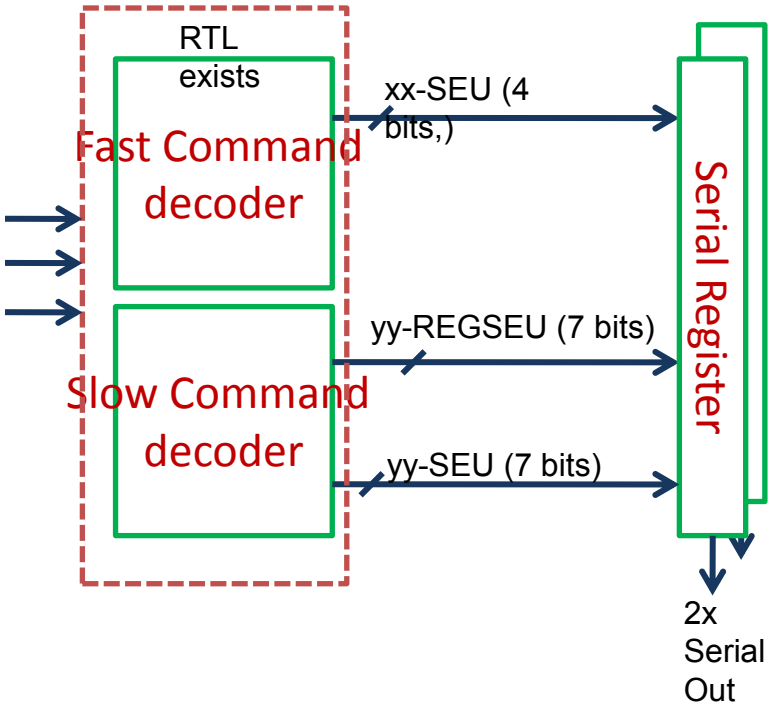


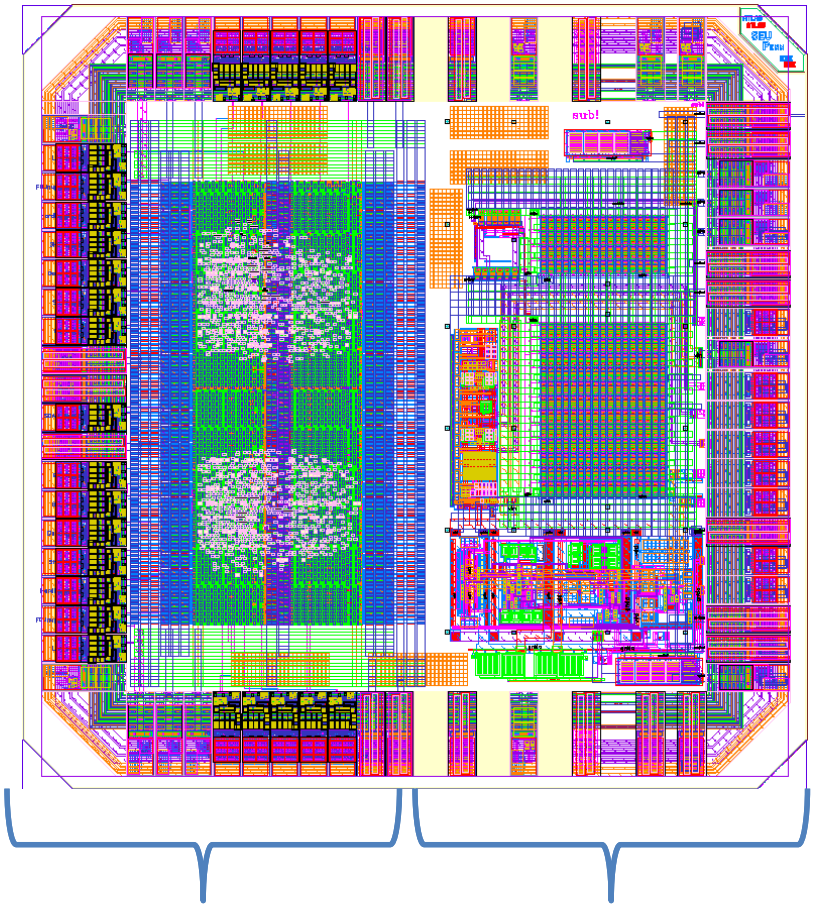
Step-Down converter design
M. Bochenek



ABCN 130nm : SEU Logic prototype

SEU Logic circuit





SEU Logic part
(F. Anghinolfi,
K. Swientek)

SPP Elements
(M. Newcomer,
N. Dressnandt)

ABCN 130nm : L0/L1 Data Flow Control

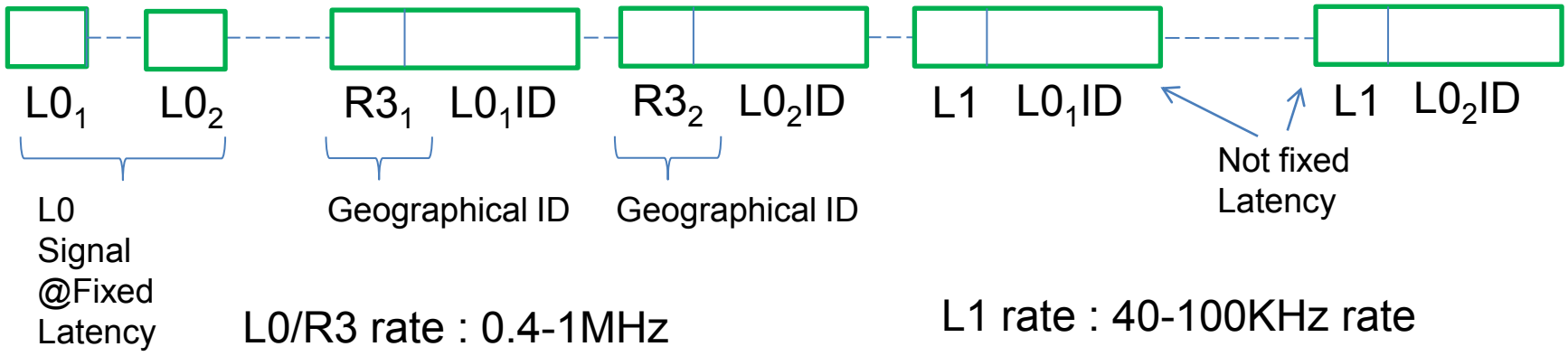
An early “fixed” latency L0 trigger is received by all FE Asics

A fraction of the detector (10%) receives a Readout Region Request (R3) to readout hit patterns relative to one L0

At reception of an L1 trigger tagged with L0 identifier, the whole detector is readout

ABCN 130nm : L0/L1 Data Flow Control

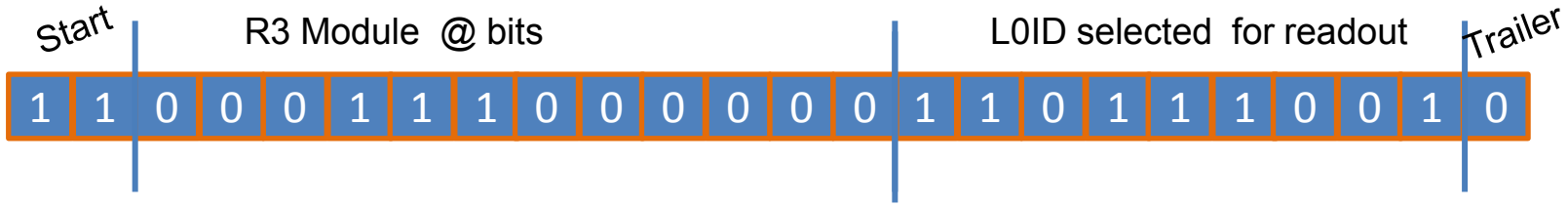
Trigger command with L0/L1 capability



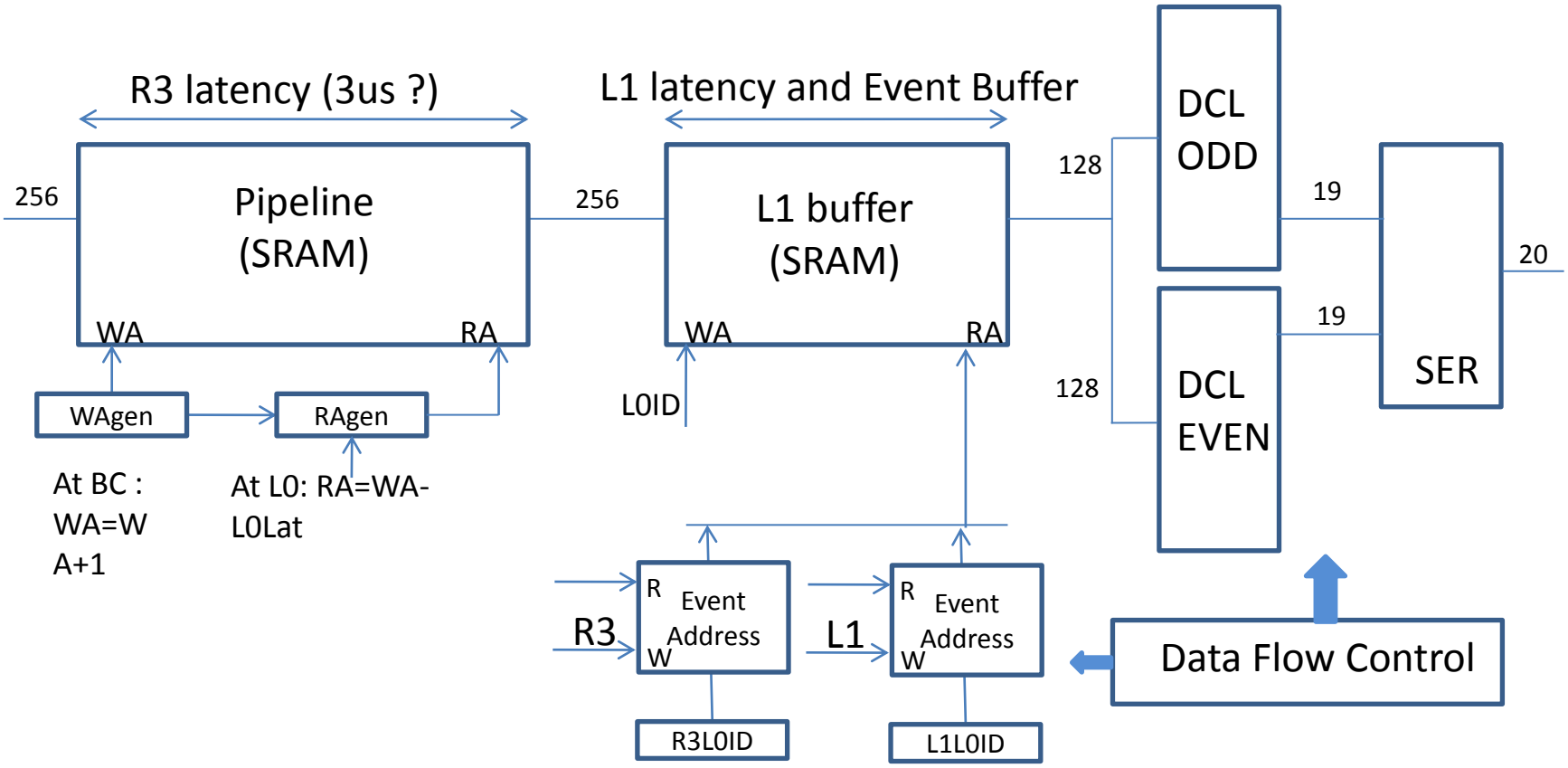
Physically there are 2 x 80Mbits/s lines carrying the above information :

L0/L1 : L0 bit sync with one phase of BC, L1 bit with the other phase of BC

R3 : R3 Packets (Header + Geo address + L0ID)



ABCN 130nm : L0/L1 data Flow Control



Radiation tolerant (TID &SEU) SRAM design by CERN/MicroElectronics

ABCN 130nm : Data Packets

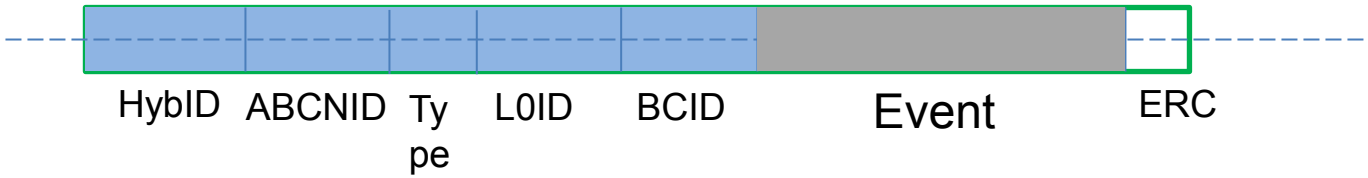
- In previous ABCD/ABCN : Data packets are built with data from adjacent chips (data concatenation built with a time constrained token signal, data packet built by a “Master” function)

- Now it is proposed “Independent Fixed size Data packets” per ABCN chip : it has impact on BW, but independent data packet carry its complete identification pattern : corruption means one packet loss only. One packet payload has room for one or two* hit/cluster physics data of the same event.

  * : still under discussion

ABCN 130nm : Data Packets

Data Packet Proposal



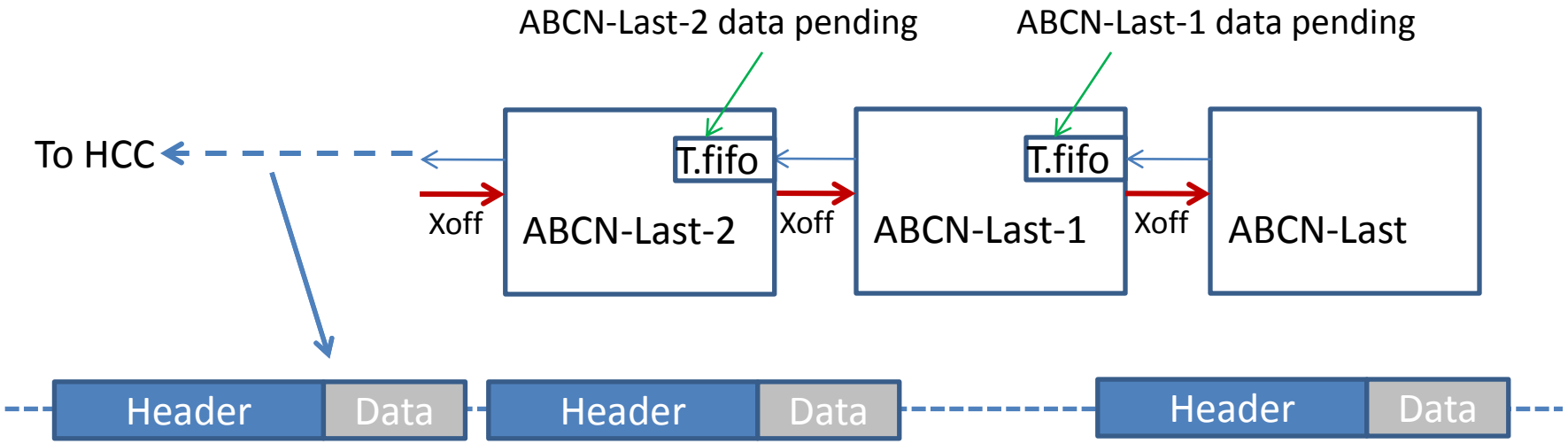
Hybrid_ID	5 bits	24 hybrids per half single sided stave
ABCn_ID	4 bits	10 ABCn per hybrid
Data_Type	3 bits	L1 data, L0 data, registers, etc.
L0ID	8 bits	Should be large enough to cover the L1 latency. Assumed 1MHz L0 rate, 256µs latency
BCID	8 bits	12 would be safer but 8 are sufficient as it is used in conjonction with L0ID
Total		***28 bits***

Strip_ID	8 bits
BC n-1 n n+1 for Strip_ID	3 bits
BC n-1 n n+1 for Strip_ID+1	3 bits
BC n-1 n n+1 for Strip_ID+2	3 bits
BC n-1 n n+1 for Strip_ID+3	3 bits
Total	***20 bits***

Preformat for 4 adjacent channels : <mean> cluster size 2.35

ABCN 130nm : Data Packets Transmission

Data is passing in a daisy-chain formed by a group of 5 chips on the hybrid.
Data is passing to the HCC and from there sent through the GBT system

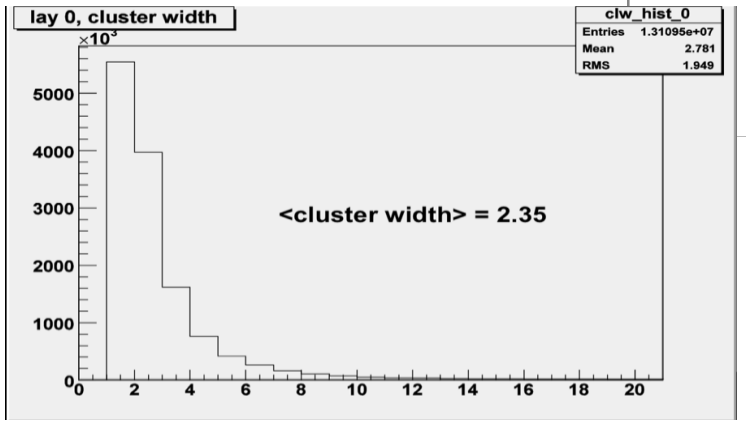


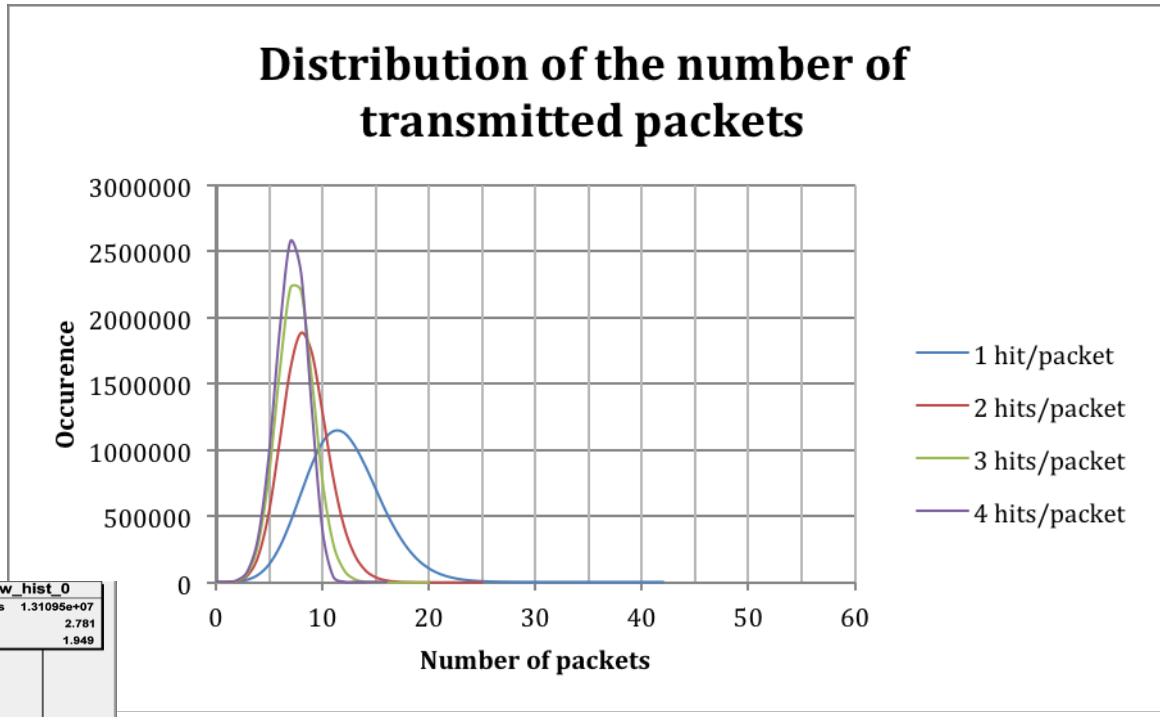
Xoff control : no timing constraint, one FIFO and some add. Logic in each chip, readout starts from last chip of the chain

ABCN 130nm : Data Packets Transmission

#hits in 256 ch	Probability
0	0.111
1	0.222
2	0.238
3	0.190
4	0.132
5	0.068
6	0.027
7	0.009
8	0.002

Simplified model giving the number of hits distribution in a 256-channel ABCN for a 5.10^{34} $cm^{-2}.s^{-2}$ luminosity

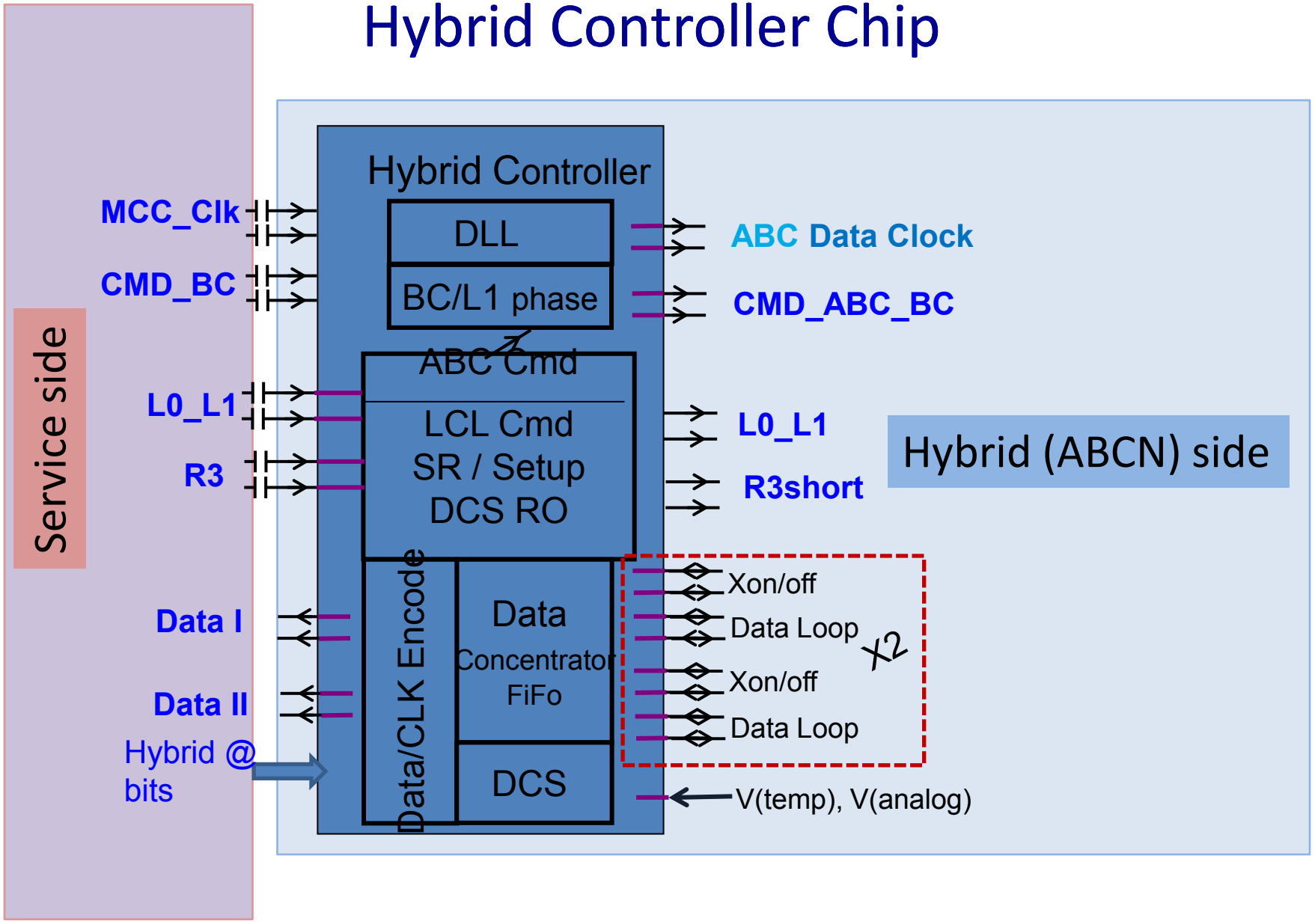




Distribution of the number of packets transmitted by a readout hybrid in the case a packet contains 1, 2, 3 or 4 hits for a 5.10^{34} $cm^{-2}.s^{-2}$ luminosity (100K events).

To be confirmed : only extrapolation from 128 channels case

Hybrid Controller Chip



ABCN-130 : Projection

Actually building specifications together with new functionality

Analogue Front-End well under control

Powering schema not fixed

Digital parts adapted for Track Trigger/Data reduction

Less than 1mW per channel ABCN budget

New event data transmission schema

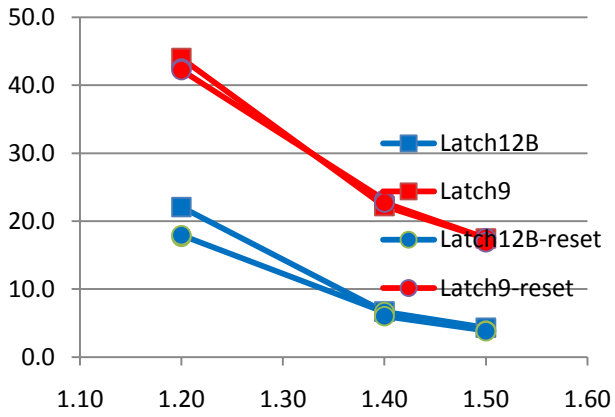
Expected “readiness” 2nd semester 2012

Backup Slide

130nm SEU cross section

(Data from the Pixel Group)

- What was tested : {Standard ARM}, {DICE}, {DICE + Triplication}
- What was tested : dependence over VDD (x5-10 in the range 1-1.5V)



STD	DICE	DICE triplication
5E-15	1-5E-16	<E-17

(My) Approx of Pixel SEU Test results, should be verified

- What (has to) should be tested : {Standard IBM}, {Standard IBM + triplication}, {DICE with IBM-like cell}, all with T3 layout now