

Tell40: an ATCA readout board for LHCb



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Outline

- **Upgrade motivation and challenges**
- **Preliminary R&D developments**
- **Tell40 architecture**

LHCb Upgrade

Motivation

- Current system expected to collect $\int \mathcal{L} \sim 5 \text{ fb}^{-1}$ in the next 5 years of operation.
- After that time, statistical precision of measurements increases very slowly.

Goal is to augment the statistical power to study new physics by:

- Increasing the instantaneous luminosity from 2×10^{32} to $10^{33} \text{ cm}^{-2}\text{s}^{-1}$
- Improving the trigger efficiency for hadronic channels
 - Collect $\int \mathcal{L} \geq 50 \text{ fb}^{-1}$

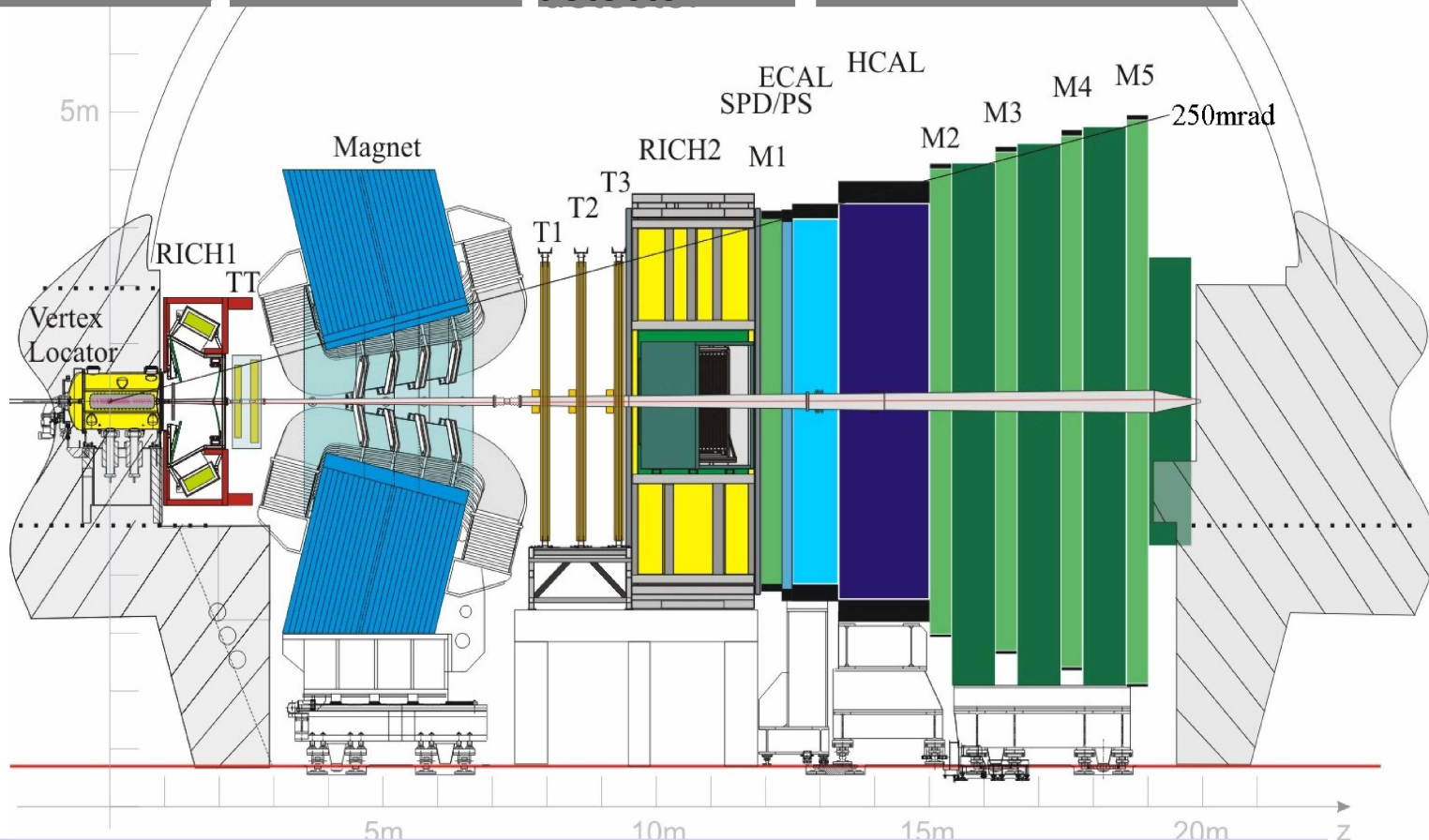
Detector Upgrade

VELO
New pixel system

TRACKING
New TT and IT

RICH
New photon detector

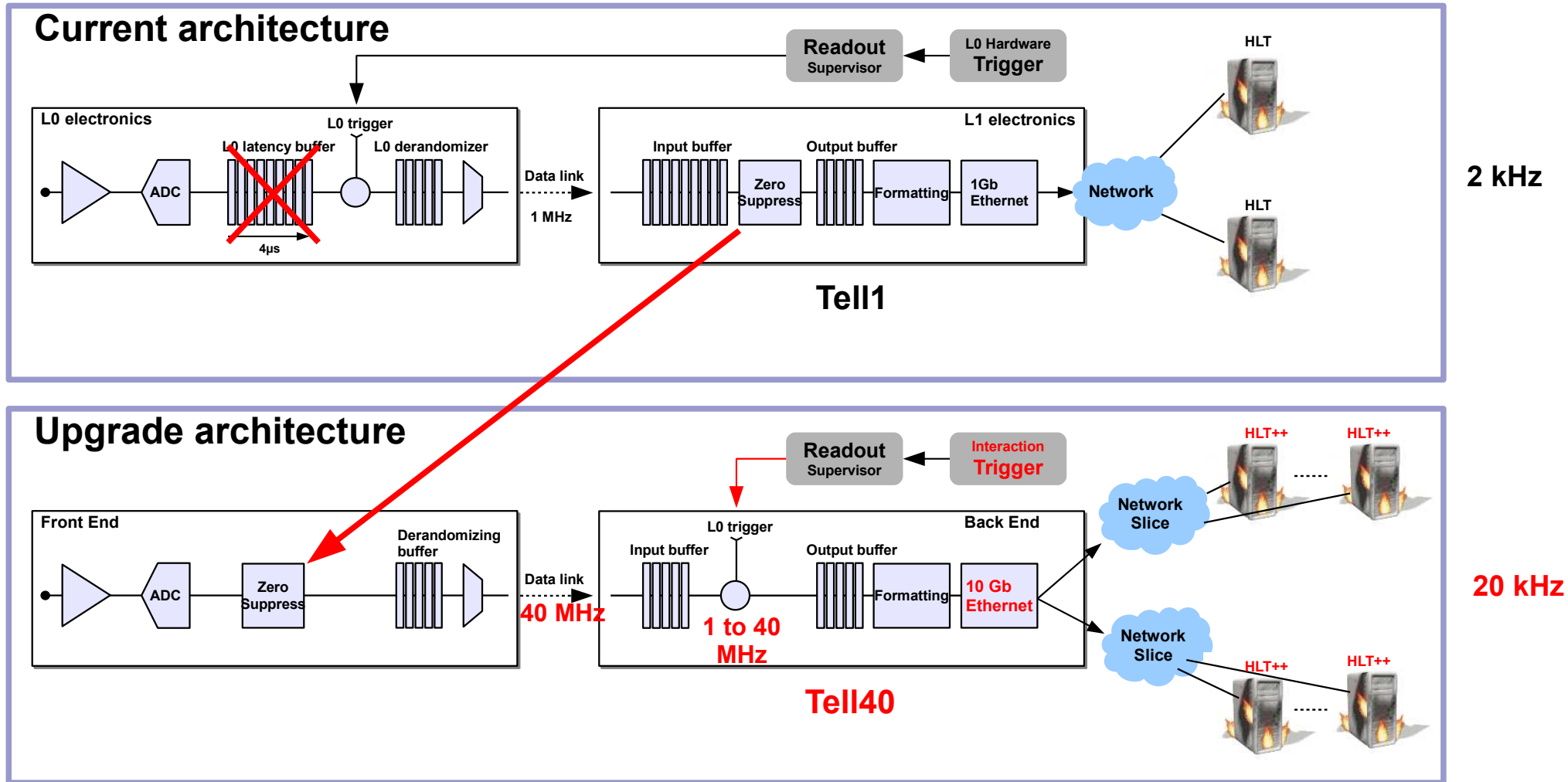
CALO + MUON
Remove M1



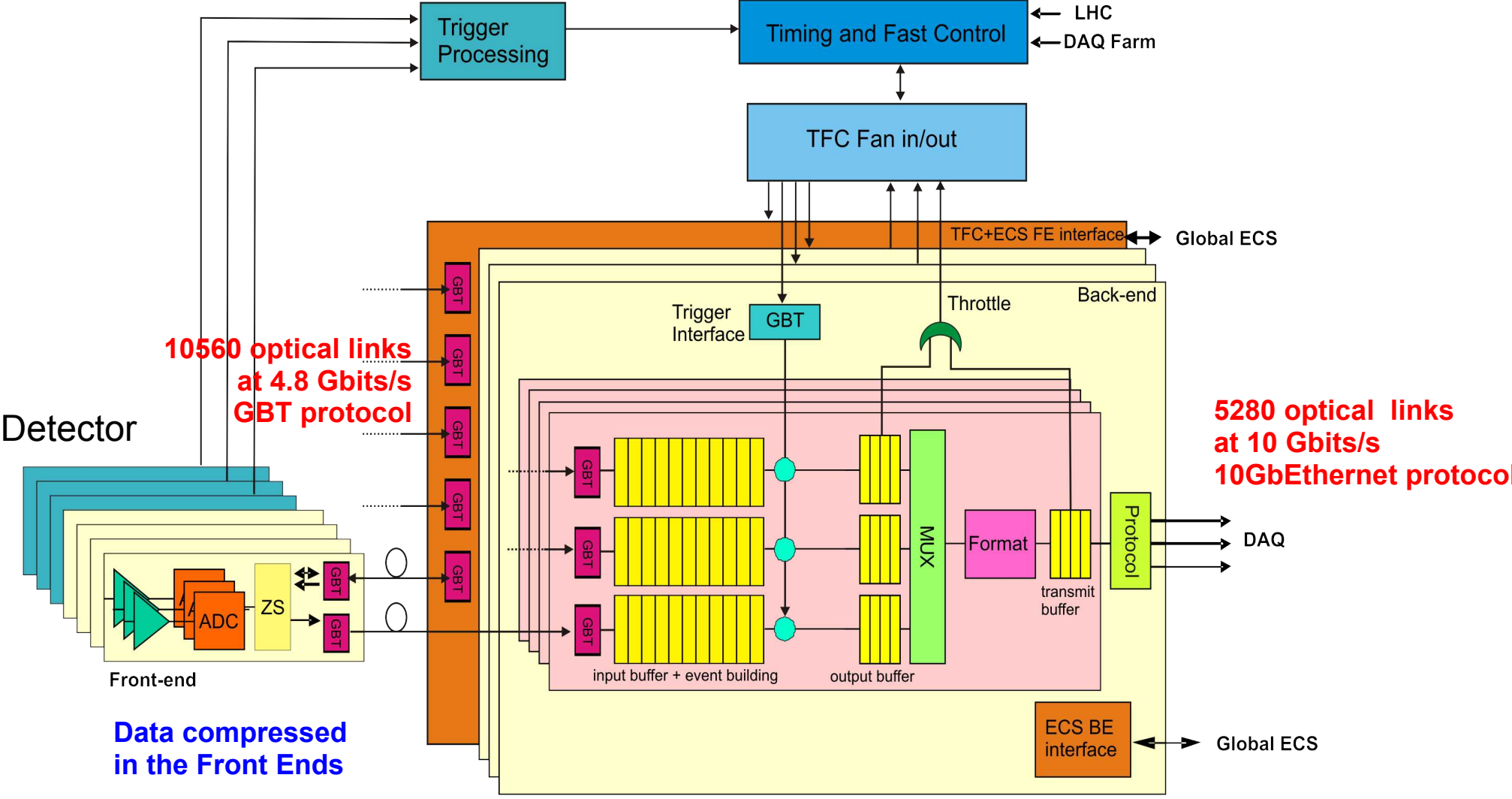
Replace nearly all the front-end electronics + DAQ network

More details in Ken Wyllie presentation

Radical change of trigger concept



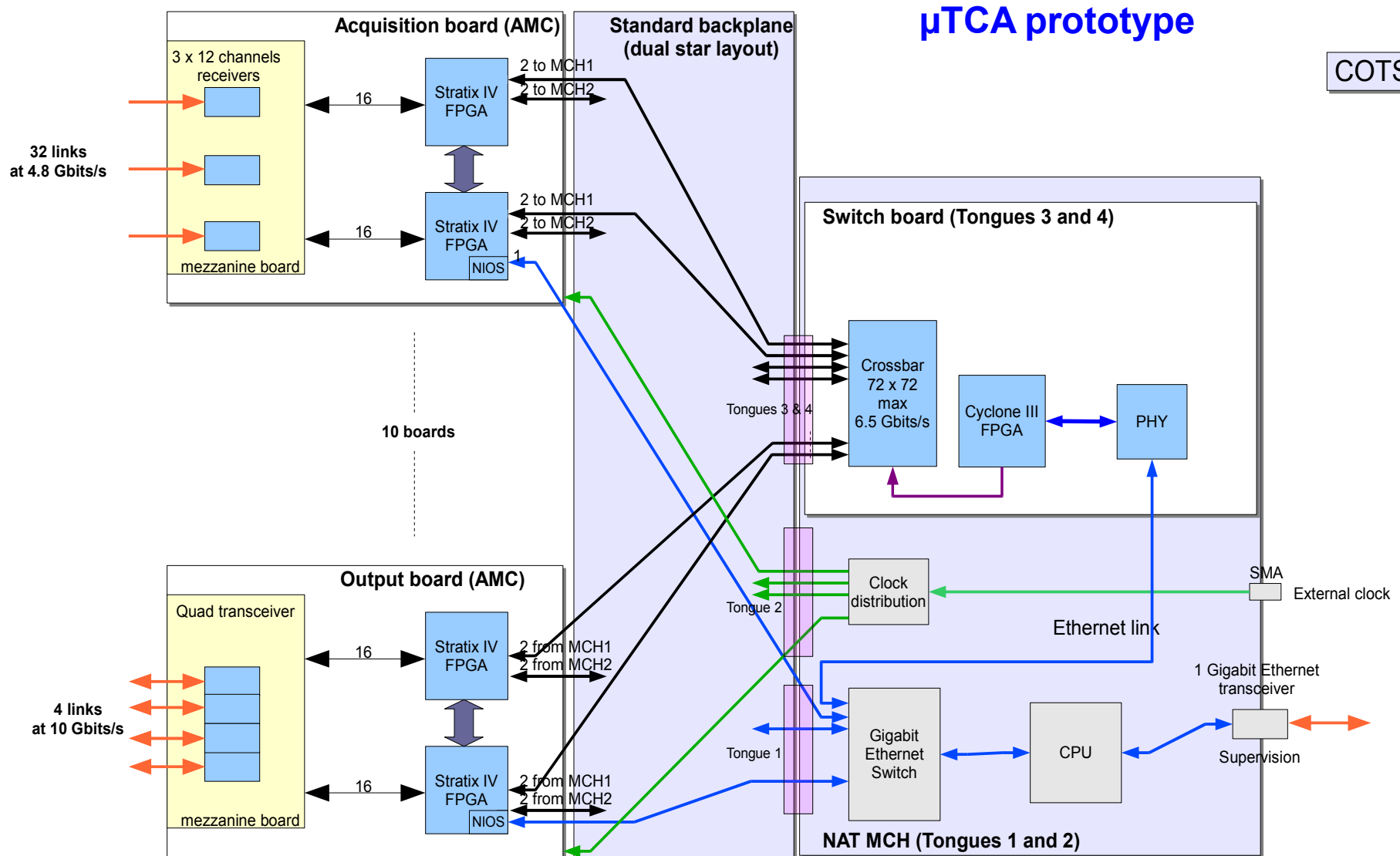
LHCb read-out requirements



Output data flow = Input data flow

Preliminary developments

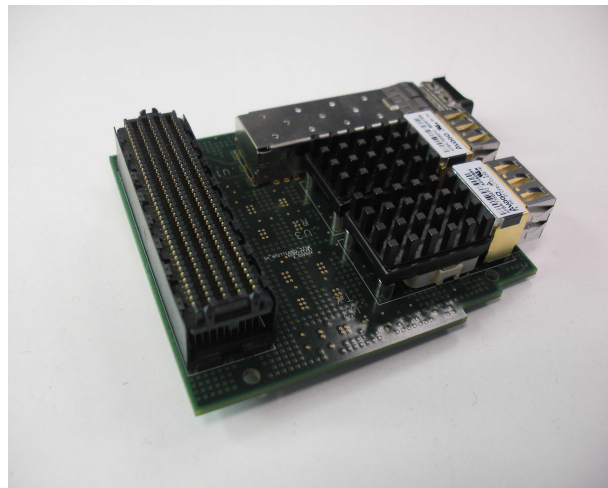
Design and test of basic building blocs



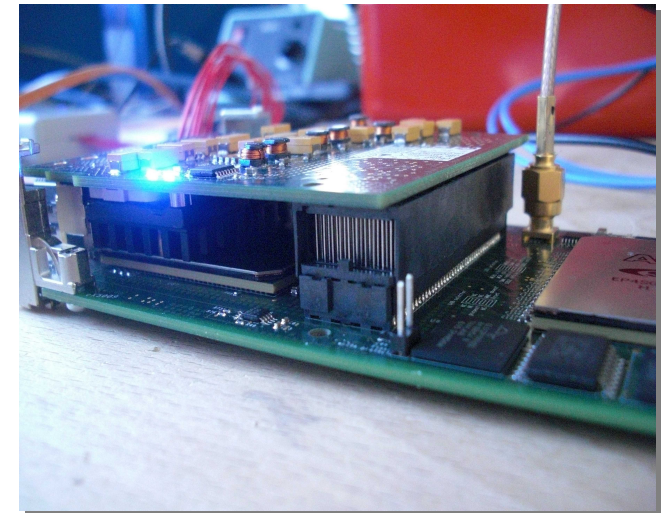
AMC board and mezzanine



AMC board

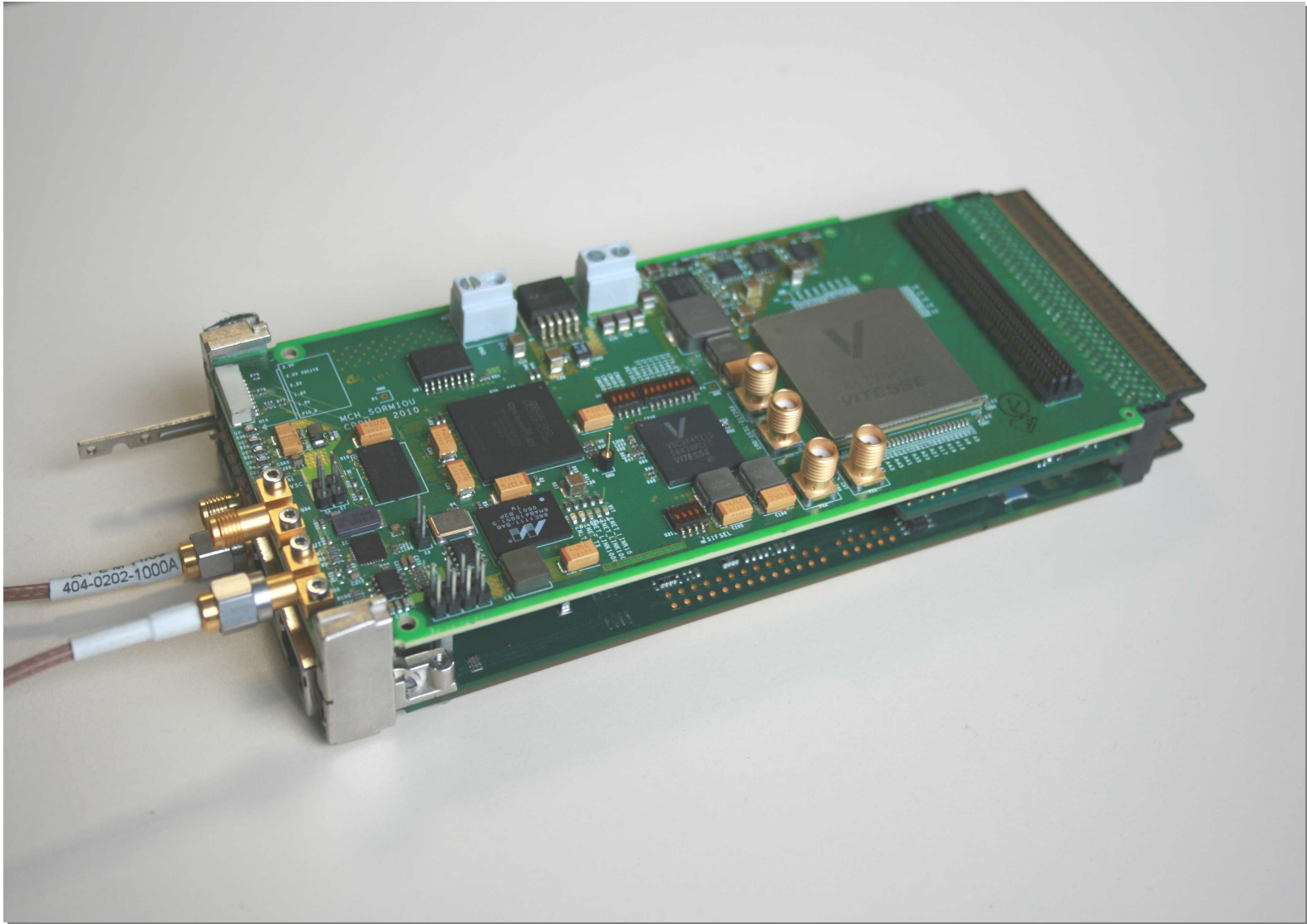


Mezzanine



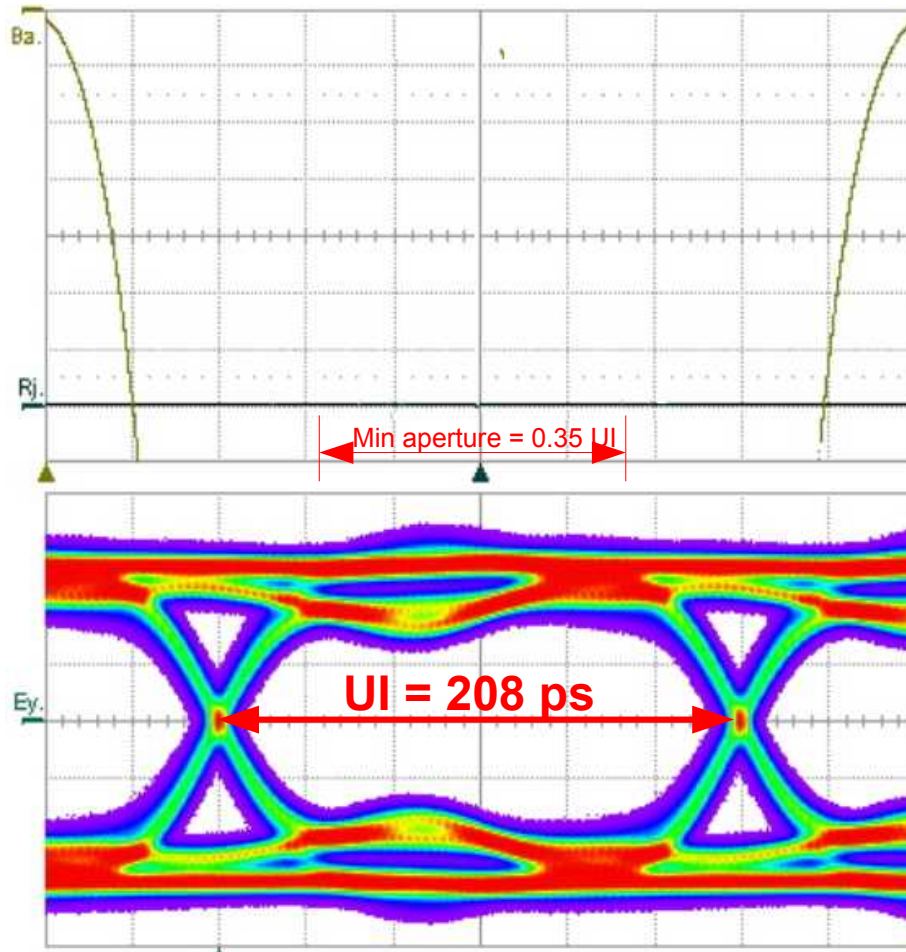
Mezzanine mounted

MCH board

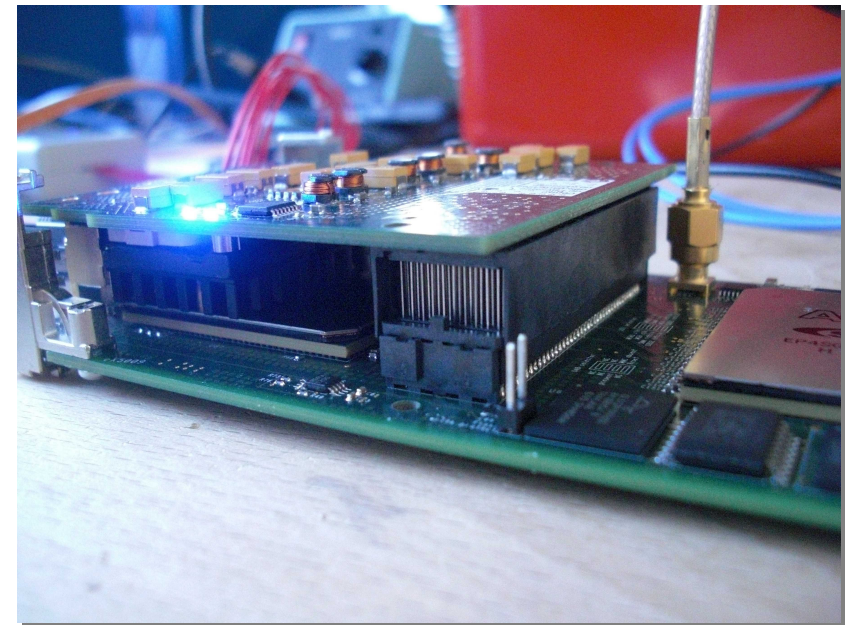


Measurements at 4.8 Gbits/s

Serial link at 4.8 Gbits/s with GBT protocol

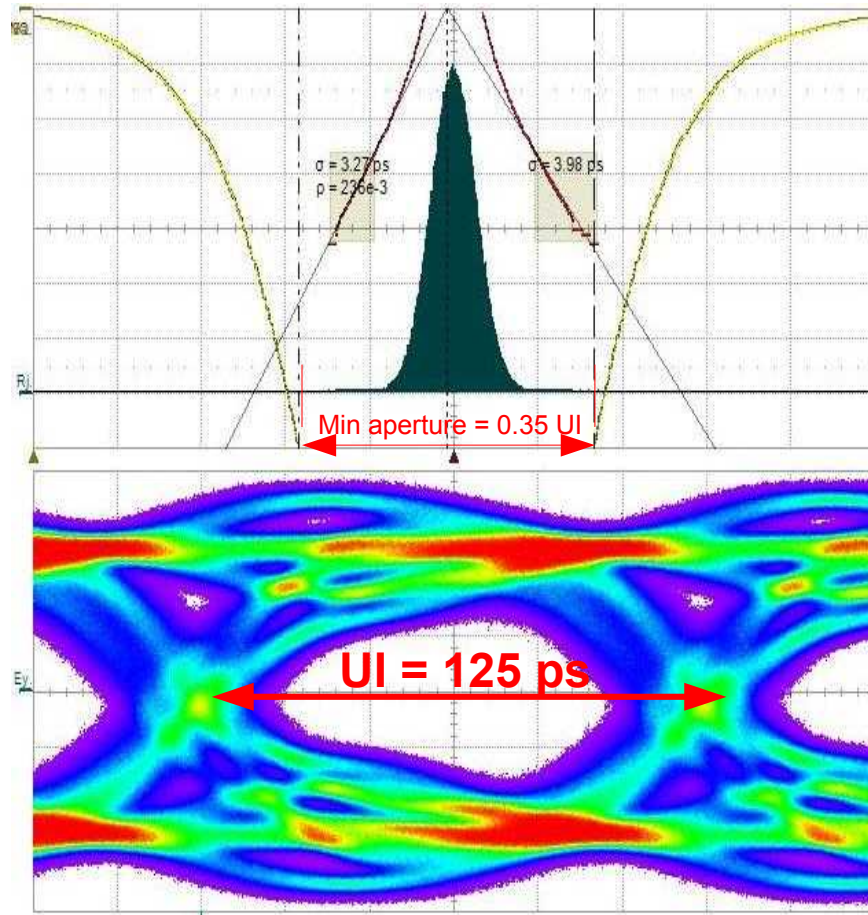


- ◆ Measured jitter at 10^{-12}
Total : 40 ps (p to p)
Random : 2.4 ps
Deterministic : 7.8 ps
- ◆ Estimated error rate :
much less than 10^{-16}



Measurements at 8 Gbits/s

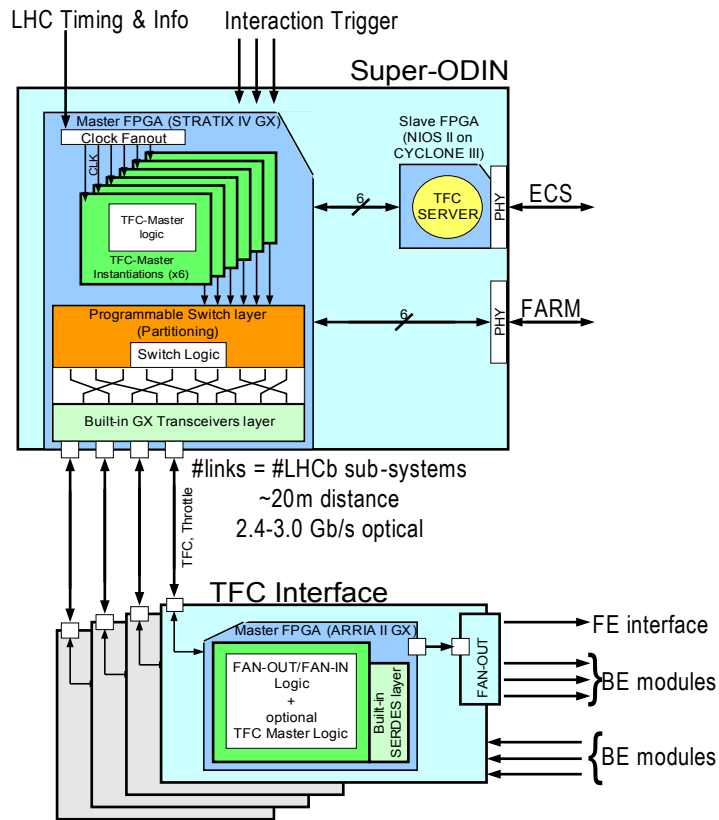
Serial link at 8 Gbits/s with GBT protocol



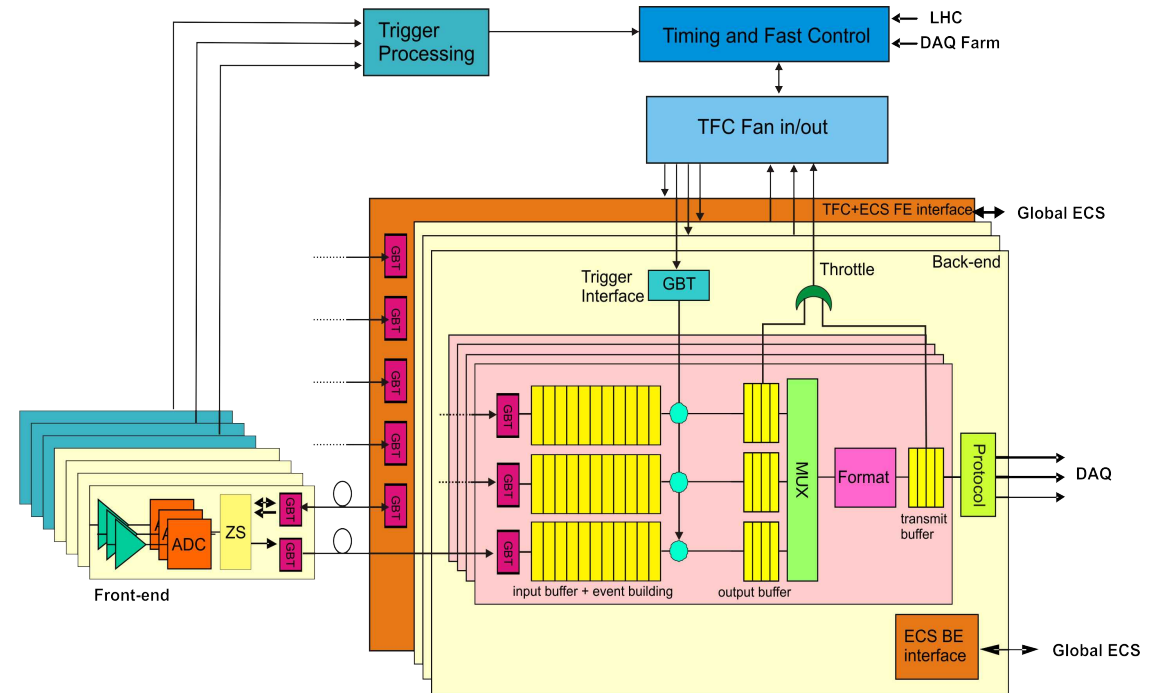
- ◆ **Measured jitter at 10^{-12}**
Total : **73 ps (p to p)**
Random : **3.0 ps**
Deterministic : **33 ps**
- ◆ **Estimated error rate :**
 10^{-16} without pre-emphasis nor equalization
- ◆ Closure of eye diagram: inter symbol interference due to attenuation of high frequencies

Generic board set for LHCb

Single board for several requirements ?



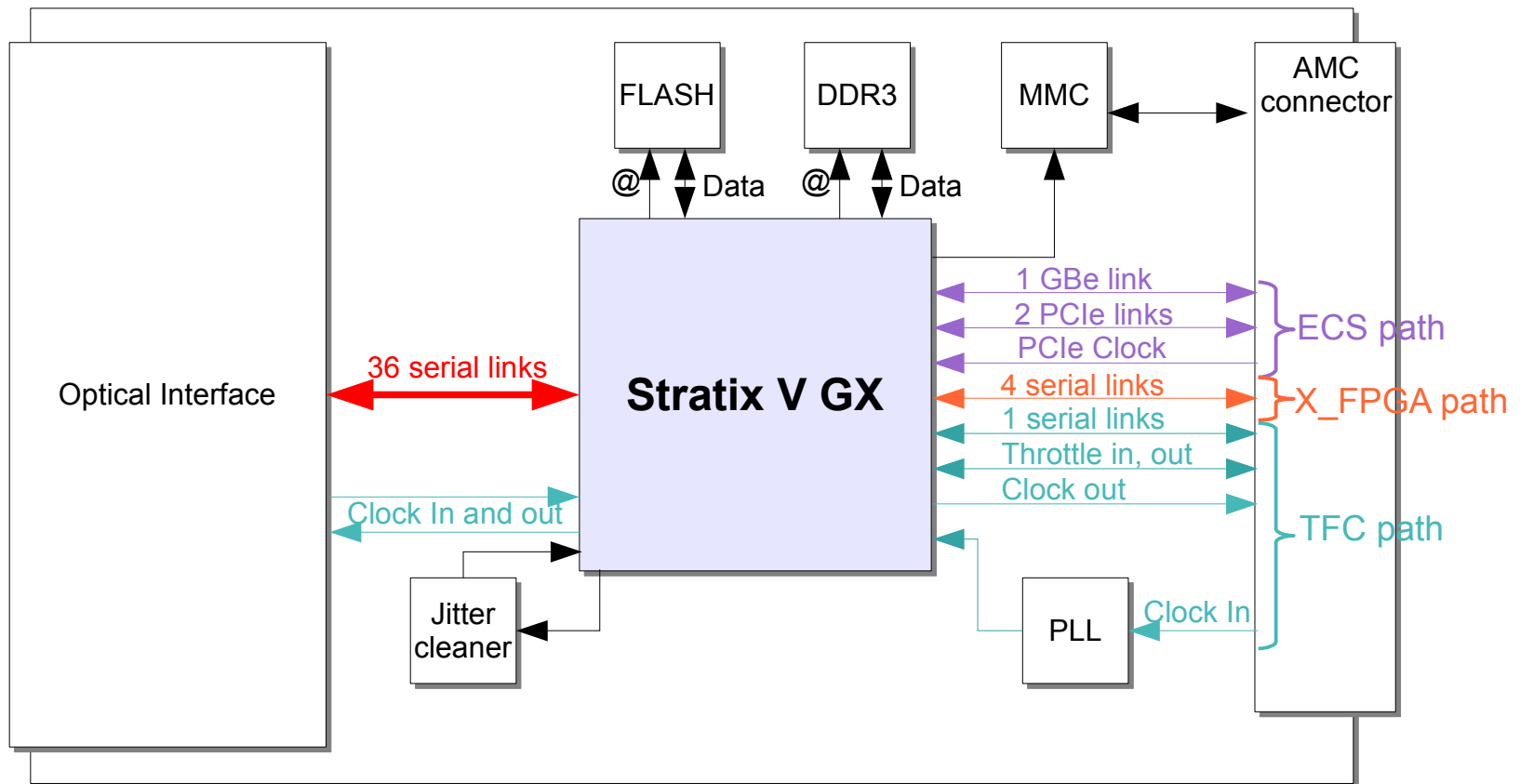
Timing and Fast Control Supervision



Acquisition and ECS

Generic AMC board

Replace 2 stratix IV GT by one Stratix V GX

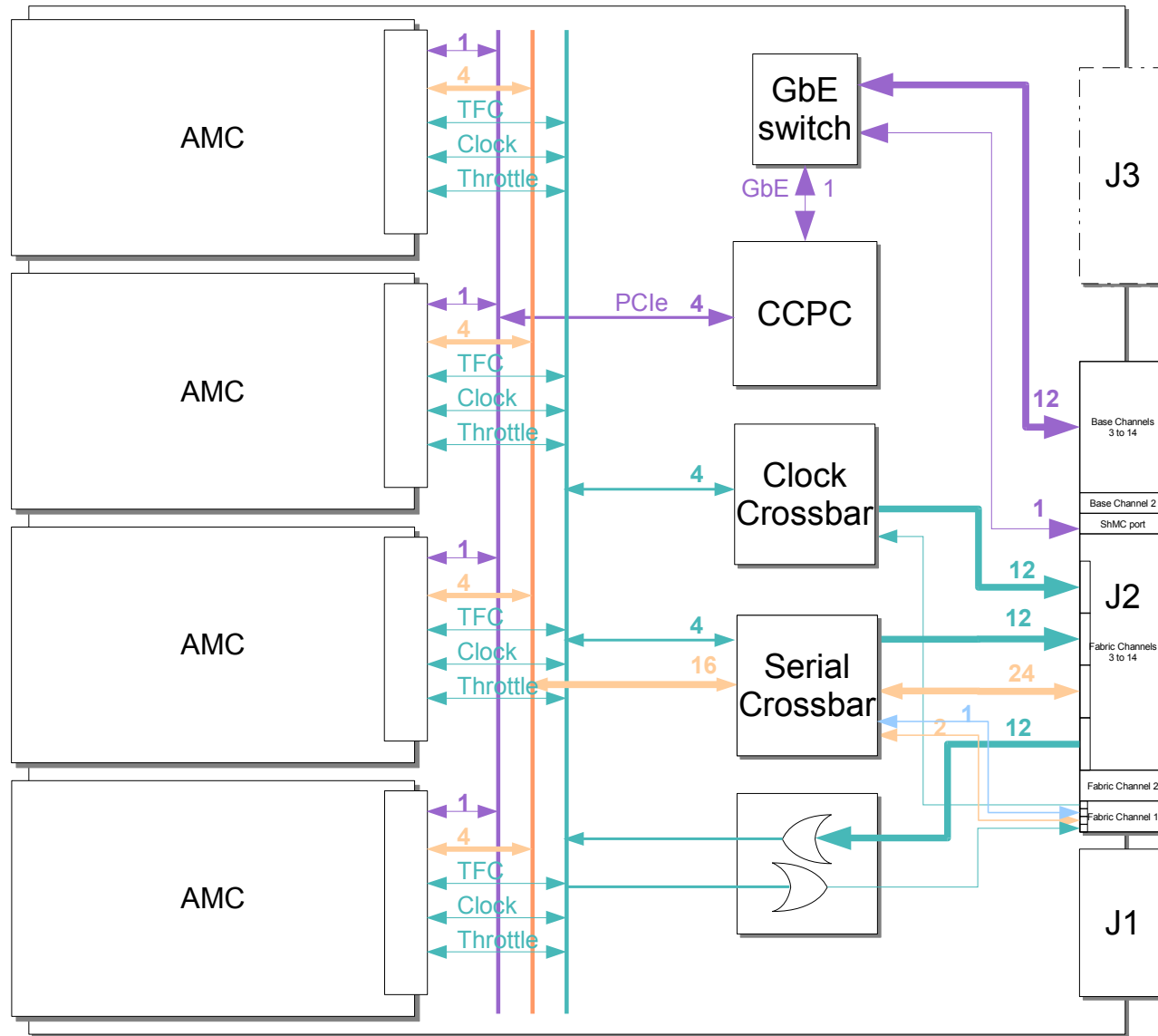


Generic ATCA board

Input:
96 GBT links

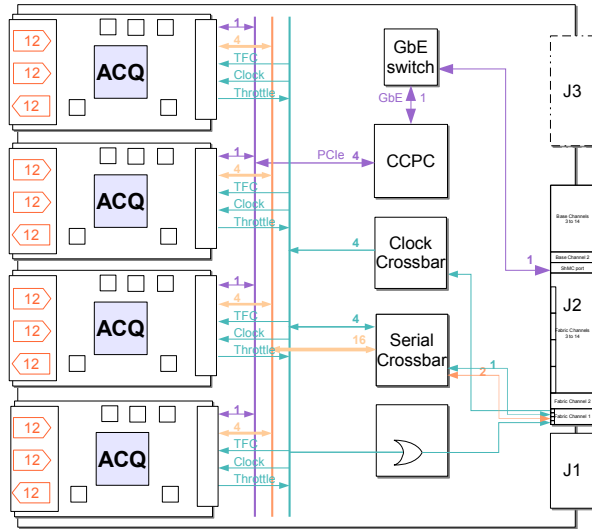
Output:
48 10GbE links

110 boards
needed for
readout

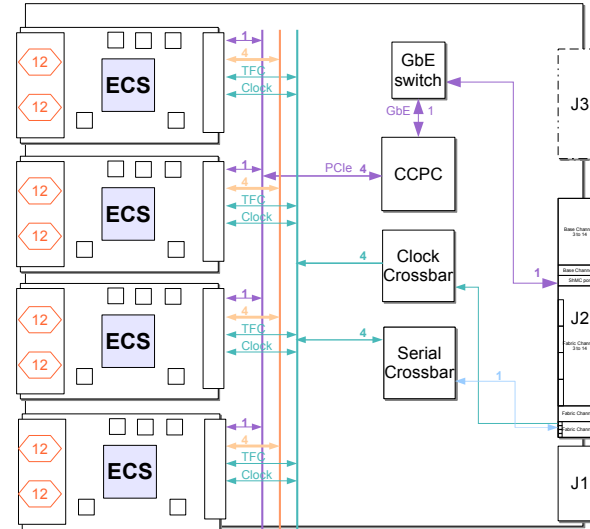


ATCA + AMC → Many Configurations

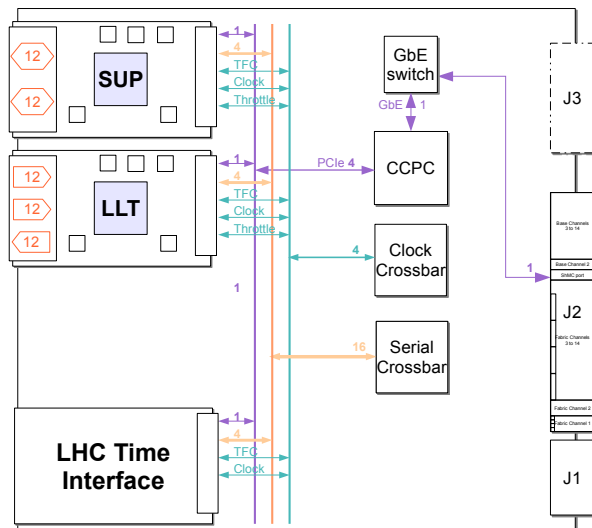
Aquisition
or
Trigger board



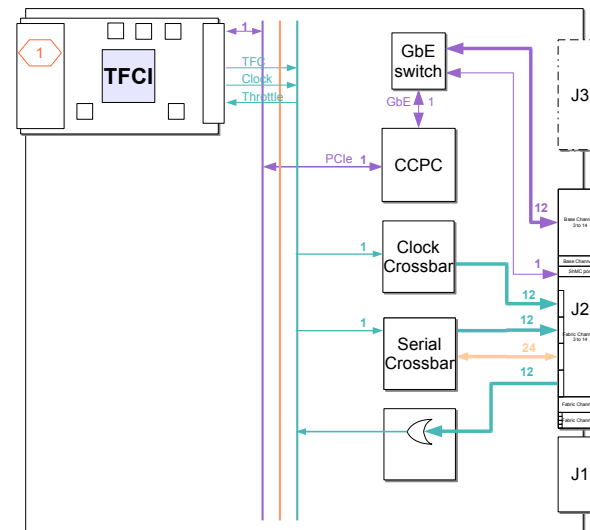
ECS



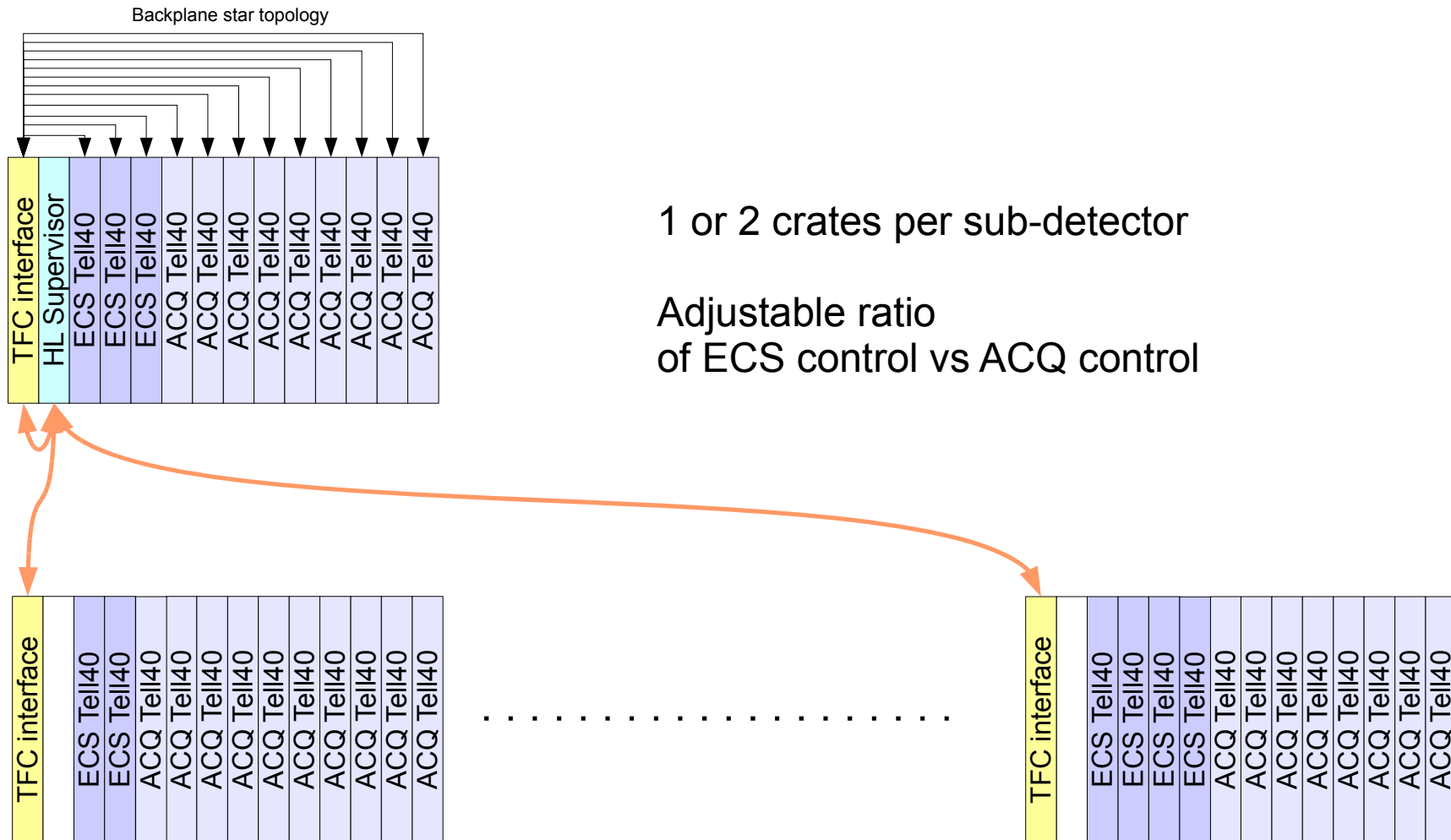
High level
Supervisor
+
Low level
trigger



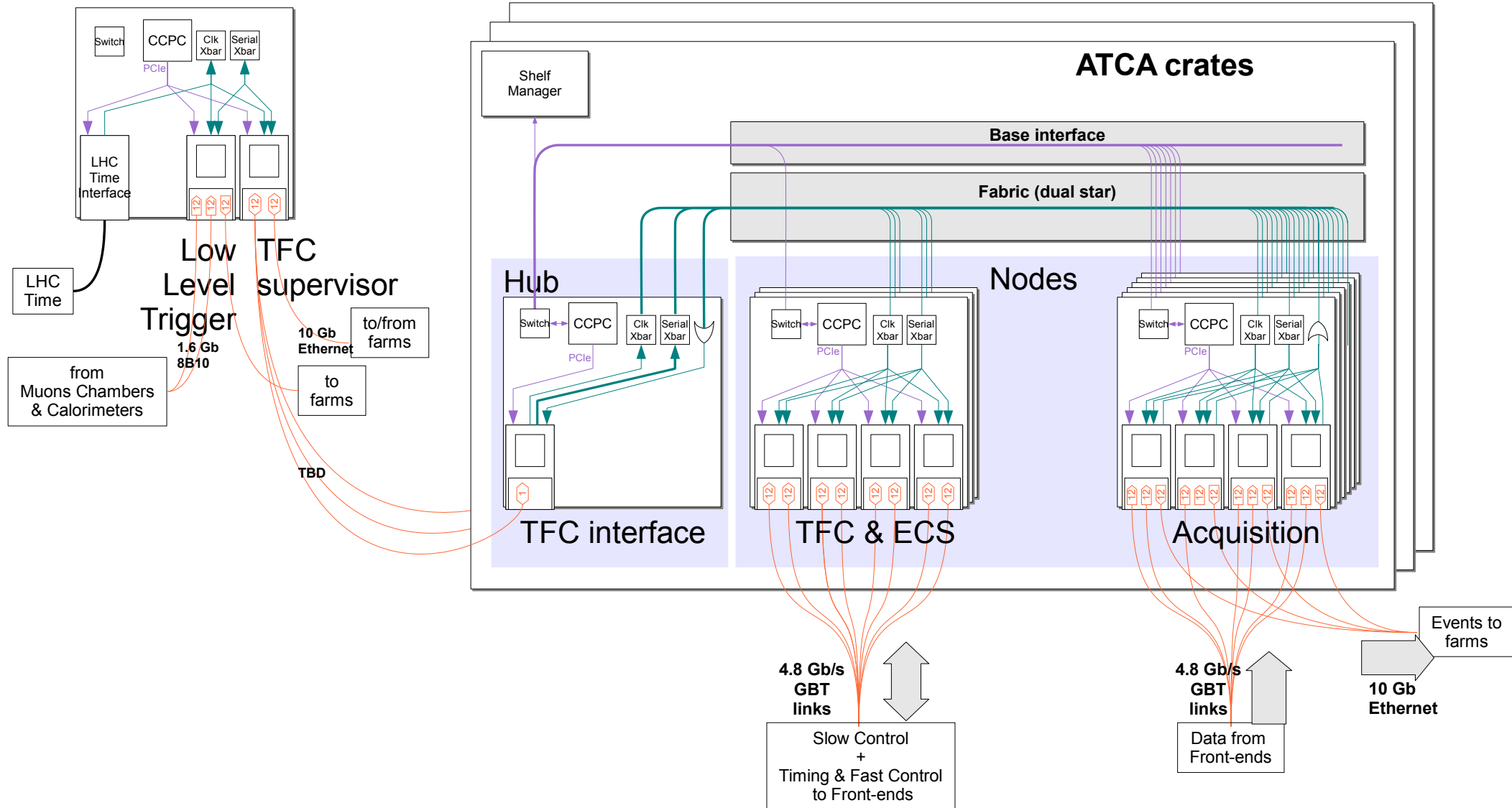
Timing and
Fast Control
Interface



Exemple of clustered architecture



Detailed architecture



Summary

- Flexible architecture relying on ATCA powerful connectivity
- Design of a generic board addressing most needs for readout, slow control and time distribution
- Quick customization and upgrade by designing simple optical mezzanines
- Design starts now
- Full prototype beginning 2012