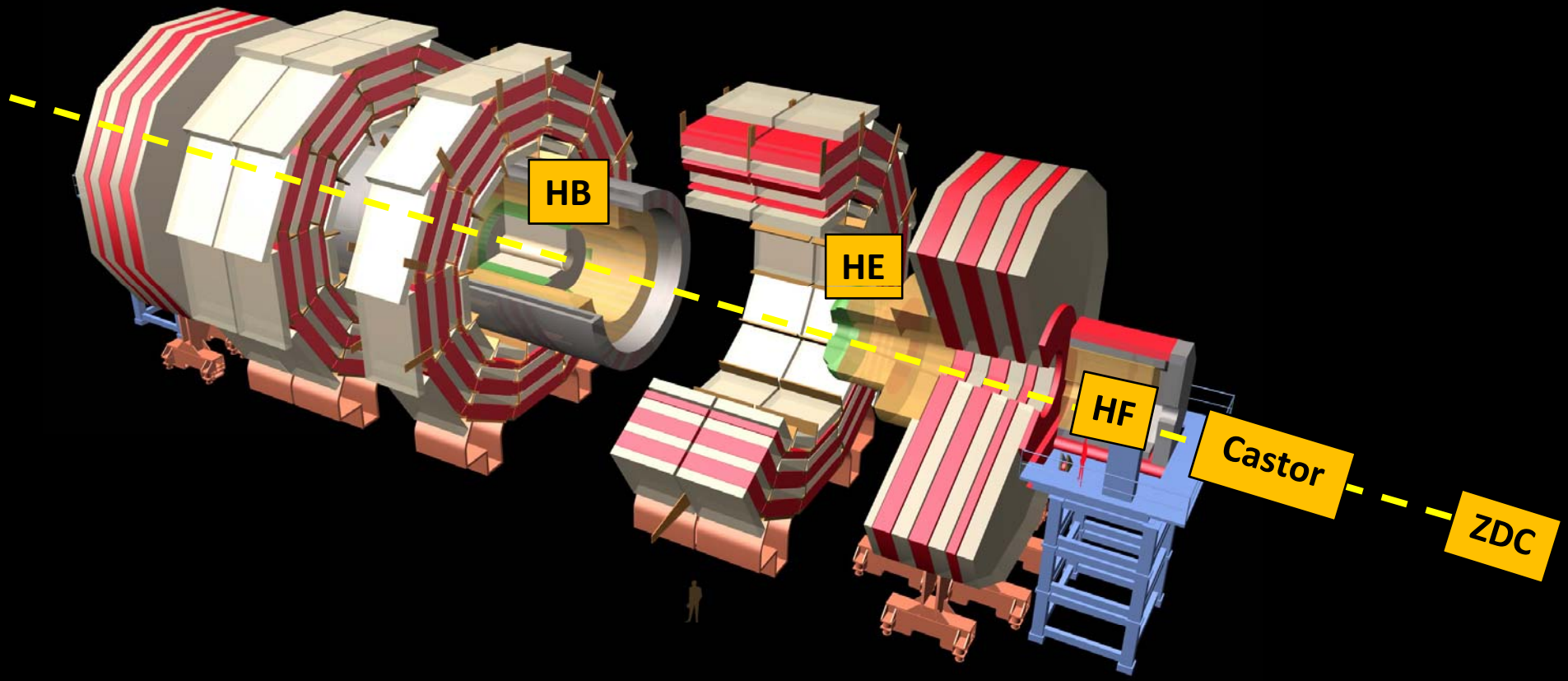
CMS HCAL electronics

Tullio Grassi for the HCAL collaboration

ACES 2011

CERN, 9-10 March 2011

Existing CMS HCAL



- ~ 6000 channels from Hybrid photo-diodes (HPDs, on HB and HE)
- ~ 3000 channels from Photo-Multipliers Tubes (PMTs, on HF, Castor, ZDC)
- Dynamic range from 1 fC to 10000 fC (HF case). Noise RMS < 0.5 fC
- Full readout every 25 ns .
- Generate trigger data in the counting room, keeping the time-alignment

Upgrade of CMS HCAL: Overview

Motivations: well described by Jordan Nash earlier today

Requirements:

- support new photo-sensors (SiPM in HB and HE. “Newer” PMT in HF)
- increase the number of channels by a factor of 3 or 4
- add timing information (TDC), useful to reject anomalous signals

Installation and commissioning of HB and HE Front-End electronics: during a long shutdown after 2015.

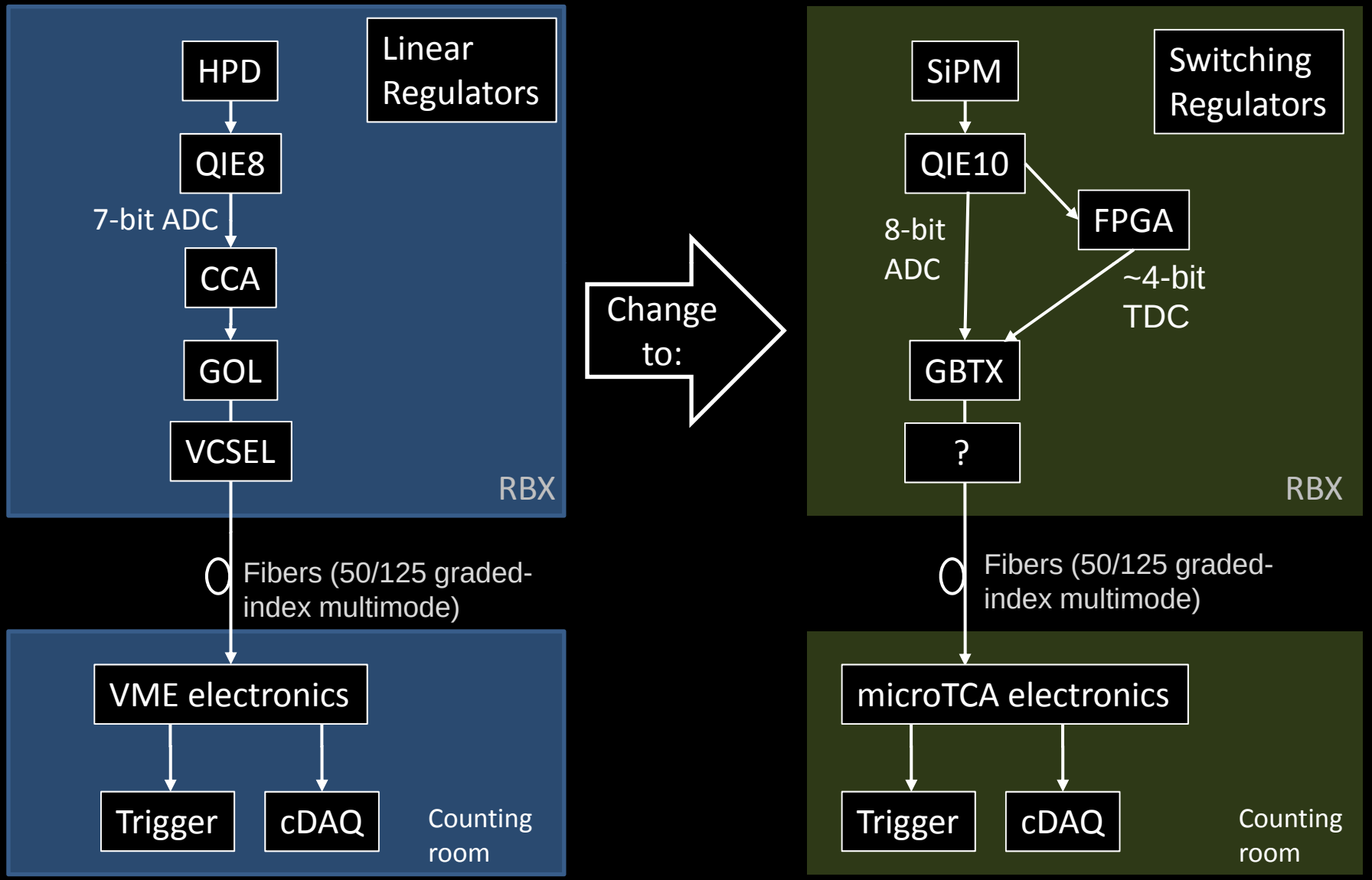
Environment:

- Total radiation dose = 10 krad
- Neutron fluence = $10^{13}/cm^2$
- Charged hadron fluence =2 x $10^{10}/cm^2$
- Magnetic field = 4 Tesla

Infrastructure: very limited possibilities to change power cables, optical fibers, cooling pipes, on-detector mini-crates (“Readout Boxes” a.k.a. RBX).

HB HE data-path:

Existing vs Upgraded



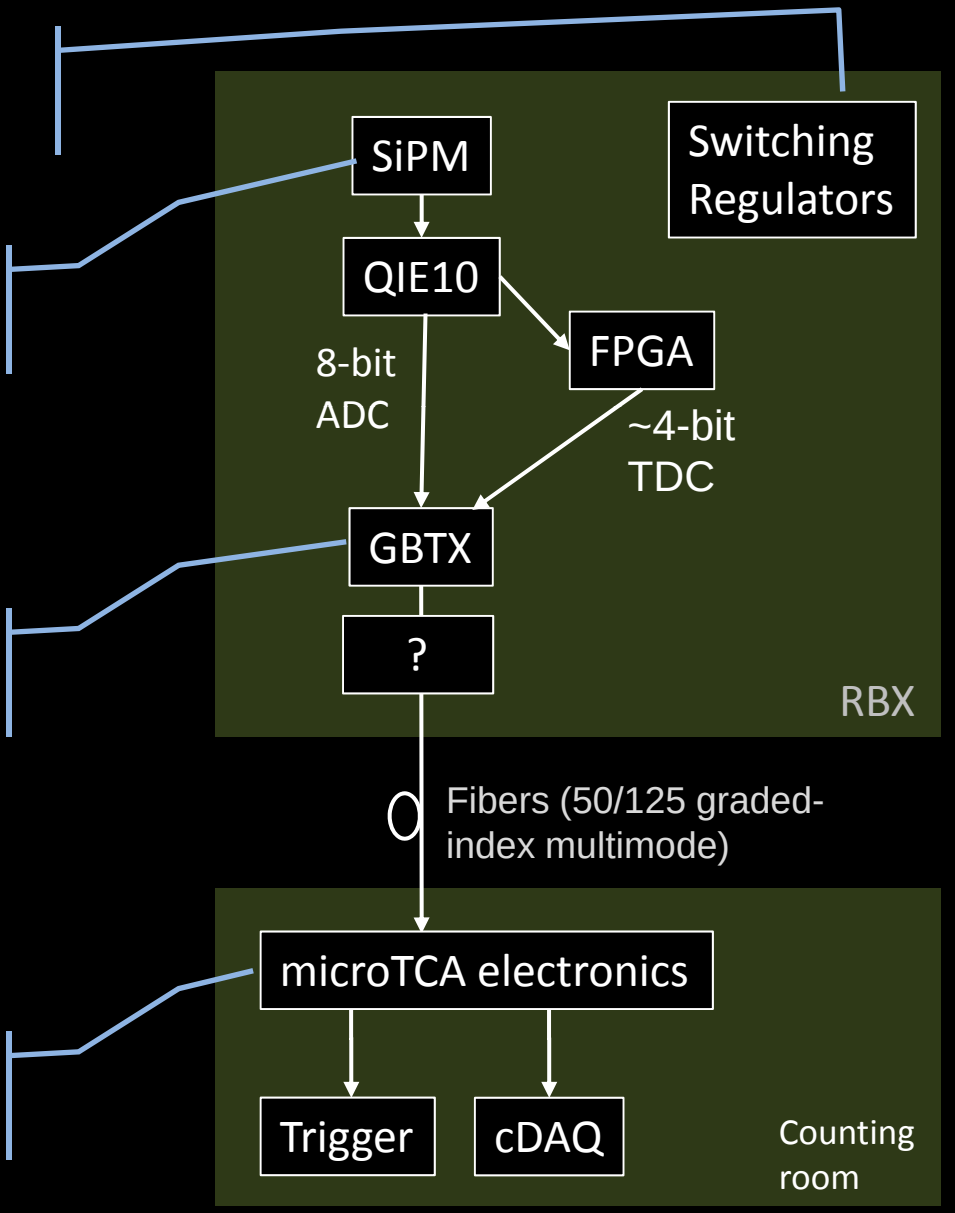
References to detailed information

Preliminary system tests presented by Cristian Fuentes at the Power Working Group:
http://indico.cern.ch/conferenceDisplay.py?confId=127662

Arjan Heering will presented it later today:
http://indico.cern.ch/conferenceOtherViews.py?view=standard&confId=113796

Paulo Moreira will presented it tomorrow:
http://indico.cern.ch/conferenceOtherViews.py?view=standard&confId=113796

Eric Hazen will presented it tomorrow:
http://indico.cern.ch/conferenceOtherViews.py?view=standard&confId=113796



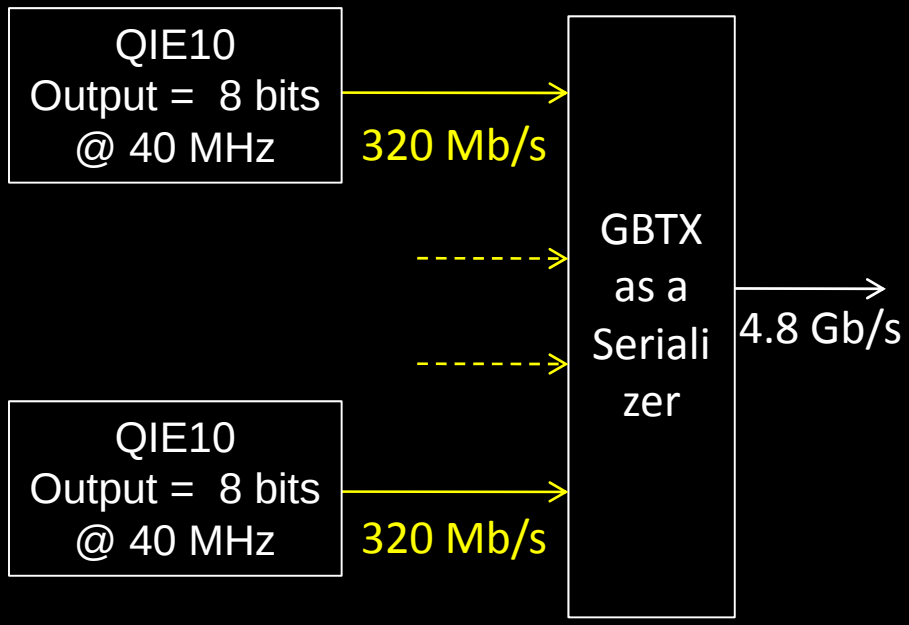
The new charge-integration ADC chip: QIE10

- migration to a finer process technology (AMS 0.35µm SiGe BiCMOS) 
- input impedance matched to the new photo-sensors 
- greater dynamic range (3fC , 330pC) 
- encoded output, 8 ADC bits at 40MHz
- circuitry to insert time-markers or other word-alignment strategies 
- 320Mb/s serialized output data. This has two advantages compared to the parallel output of QIE8: it allows reducing the power consumption and it requires fewer connections on the PCB pack. 
- output (“signal-over-threshold”) for the TDC
- 4 identical circuits on a single chip (increased channel density)
- clock phase adjustments
- additional supply voltage (3.3V). This allows to save power by generating the 3.3V on an off-chip switching regulator

Readout issues

Requirements:
- ability to tune the sampling clock of the QIE10 ADC
- stable latency across power cycles
- high density of channels

QIE10 generates 320 Mb/s of payload data. The GBTX E-ports accepts 80, 160, 320 Mb/s. We'd like to send data to the GBTX using its 320Mb/s E-ports, but this leaves no room for encoding or framing…



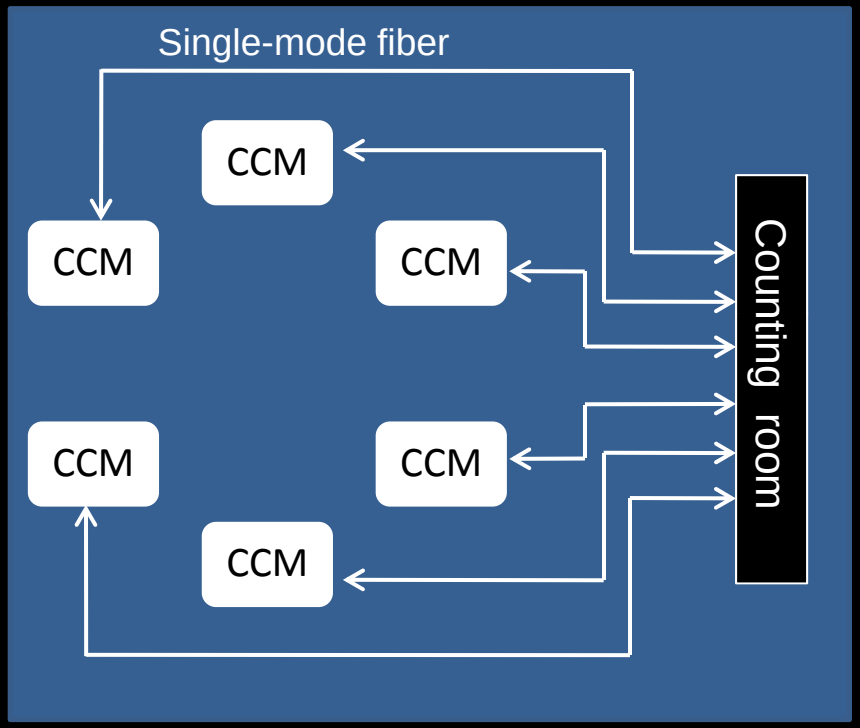
Problem 1: sampling phase at the GBTX input.

Problem 2: identify the boundaries of the 8-bit words.

Problem 3: channel-to-channel alignment.

Ideas: do timing-calibration runs, inject known data patterns during orbit gaps. Avoid long string of zeroes in the payload…

FE control:
Existing scheme and weaknesses

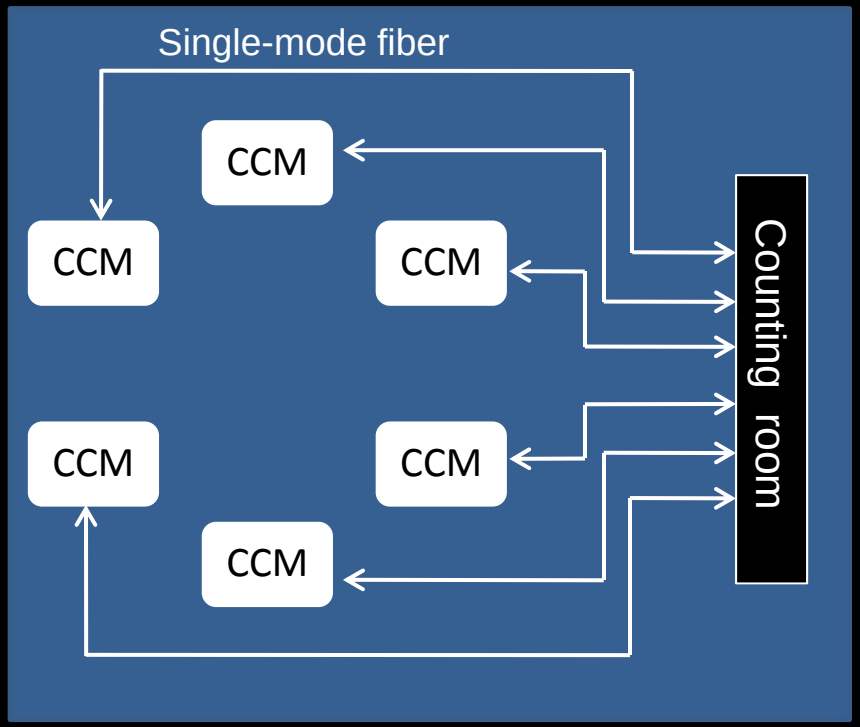


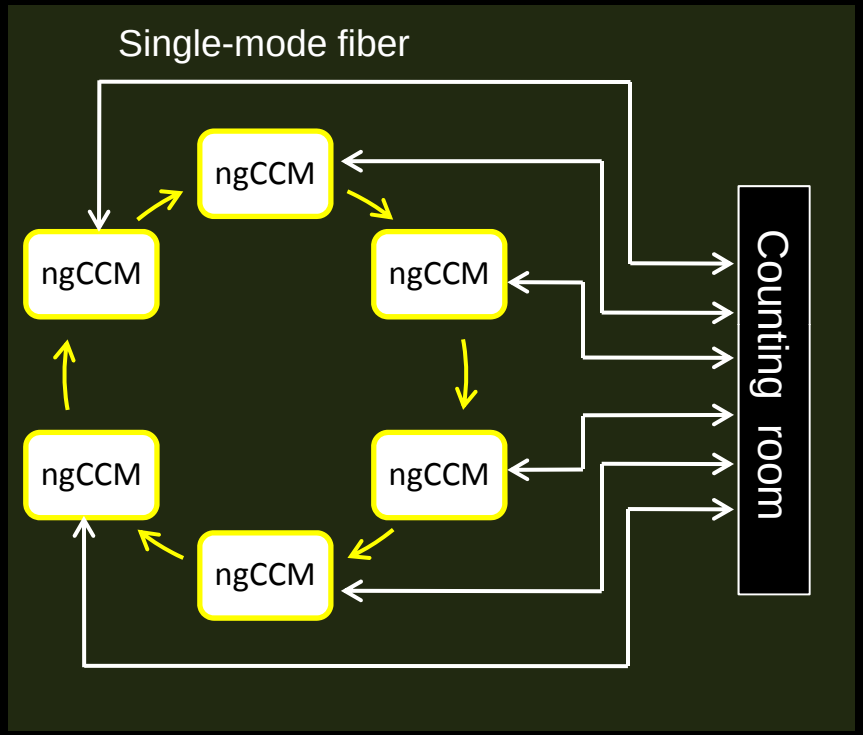
In the existing system a Clock and Control Module (CCM) controls 72 data channels.

The communication is point-to-point from the counting room to each CCM.

If a control link or part of a CCM breaks, we would loose all channels.
This is considered not acceptable.

FE control: Existing vs Upgraded





New redundant control path: ~2-meter links inside the HCAL space.
These links create a ring of 18 ngCCM's and can provide the clock and a few essential commands, in the case that the main control link breaks.
Our baseline is to use FPGA and Cern SFP+ technology [presented by Jan Troska on http://indico.cern.ch/conferenceDisplay.py?confId=126772].
Need to define a line coding (looking at 5b6b and FF-LYNX)

Radiation issues

We will use some commercial-grade components.

Need to verify TID tolerance and to mitigate single-event effects (SEE).

Example: Actel ProASIC3L or ProASIC3E flash-based FPGA.

TID: initial tests from Syracuse University (LHCb) show that it can survive 90 krad.

SEU: TMR mitigation with automatic tools (http://www.actel.com/documents/SynplifyRH_AN.pdf)

SEGR: Single Event Gate Rupture, it can happen if the FPGA is reprogrammed while exposed to radiation. The solution is to reprogram the FPGA only when there is no beam or other source of radiation.

SEL: monitor the current ; if it is above a threshold do a power-cycle. How? There are commercial circuits that can do that, but they have to be qualified for radiation.

FPGA-radtol interest group (https://twiki.cern.ch/twiki/bin/viewauth/FPGARadTol/InformationOfInterest)

We will use other commercial components, with similar issues.

Infrastructure

The cooling system is designed to remove 200 W per Readout Box. The existing Readout Boxes dissipate “only” 90 W. The goal for the upgraded Readout Boxes is to dissipate < 200W (with ~4x increase in data) .

→ switching regulators will play a key role

Very difficult to lay more cables to the detector. The upgrade plans do not assume to change the cabling.
This limits the bandwidth to send TDC bits to about half of the channels
→ FPGA reprogrammability can play a role to decide where and how to do TDC.

The existing power supplies from CAEN are not compatible with the upgraded system

→ need to specify and purchase new power supplies.

→ we have an estimate compatible with our budget

Conclusions

We have an organic plan for the upgrade of the HB, HE front-end electronics.

In the current plan, the architecture will remain similar to the existing system, with the addition of some redundant elements, in order to improve the reliability.

Most of the changes are on the Readout Modules and on the Clock-and-Control Modules.

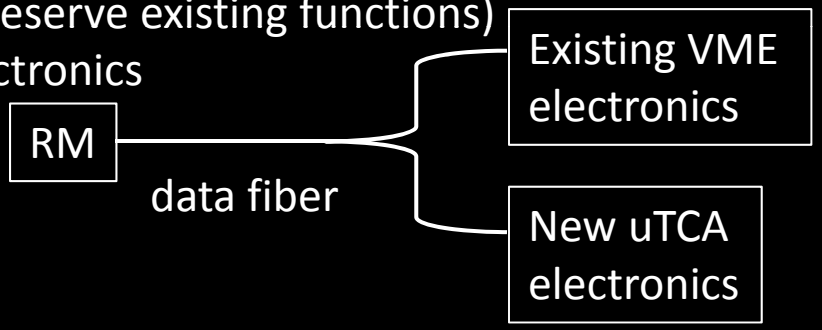
The present R&D is focused on the components and their interfaces
→ need to ensure that the upgrade plan and the components evolve together.

Backup slides

HB HE draft installation plans

2013 shutdown:

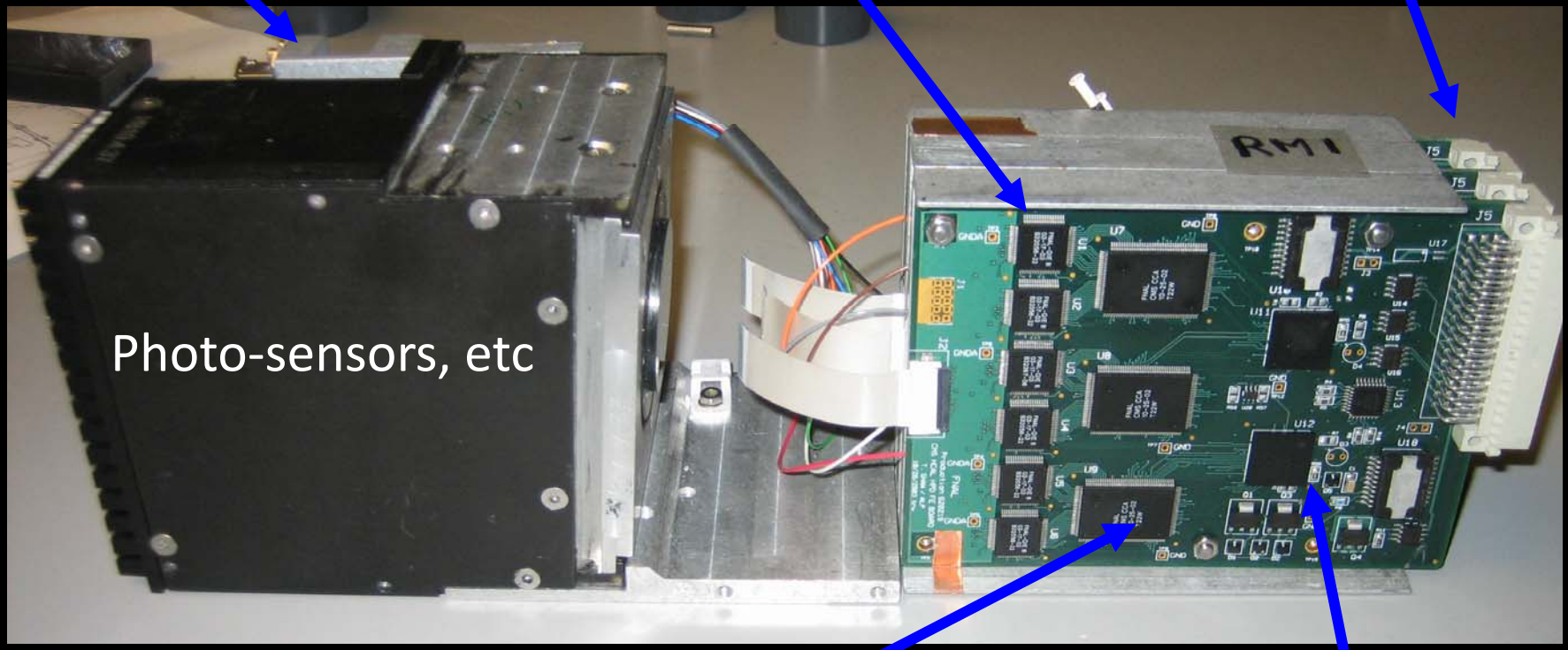
- install optical splitters on a few data fibers
- one side goes to the existing VME electronics (preserve existing functions)
- the other side of the splitter go to new uTCA electronics
- test the new uTCA electronics “parasitically”



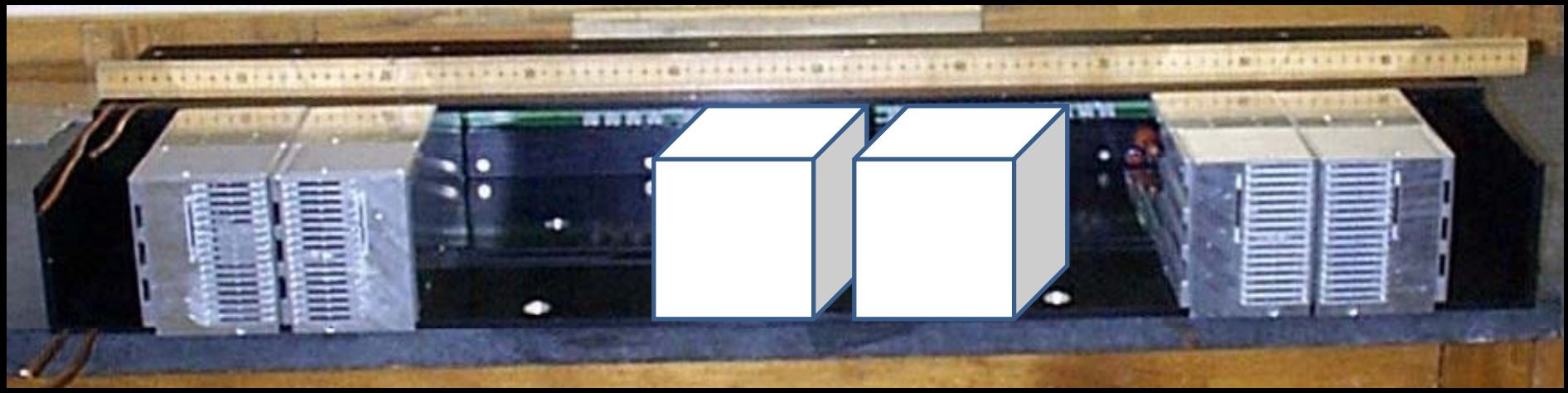
- We are considering to replace completely the counting room electronics n 2013, in order to reduce the workload on the following shutdown

2014: production of electronics modules
2015: test of the production modules
2016: Burn-in in Bld 904
~2017 shutdown: Complete installation

Current HB Readout Module (RM)



Existing On-Detector Electronics: Readout box (4 RMs) ↔ 20° of HCAL



RM RM CCM Calib. unit RM RM