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Fixed-Latency, Multi-Gigabit Serial Links with FPGAs

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Summary

Most of the off-the-shelf high-speed Serializer-Deserializer (SerDes) chips do not keep the same latency through the data-path after a reset, a loss of lock or a power cycle.
This implementation choice is often made because fixed-latency operations require dedicated circuitry and they are usually not needed for most telecom and data-com applications. However timing synchronization and triggers systems of the HEP experiments would benefit of fixed-latency links.
In this work, we present a link architecture based on high-speed SerDeses embedded in Xilinx Virtex 5 and Spartan 6 Field Programmable Gate Arrays (FPGAs). We discuss the latency

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