Upgrade of the ATLAS MDT Front-End Electronics

Radiation-tolerant ASIC- and FPGA-design

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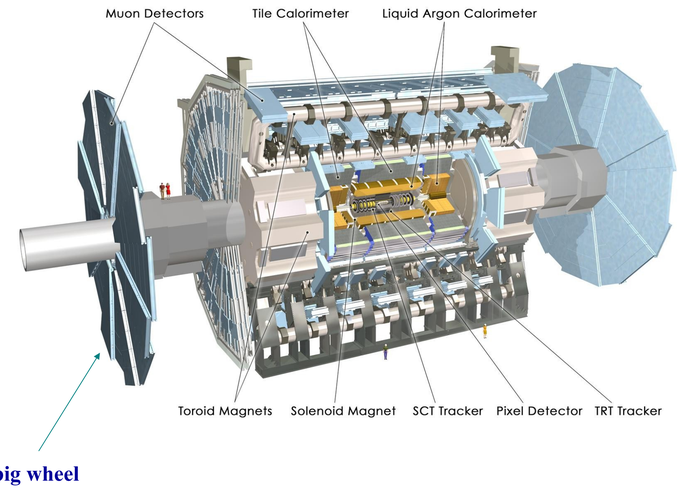
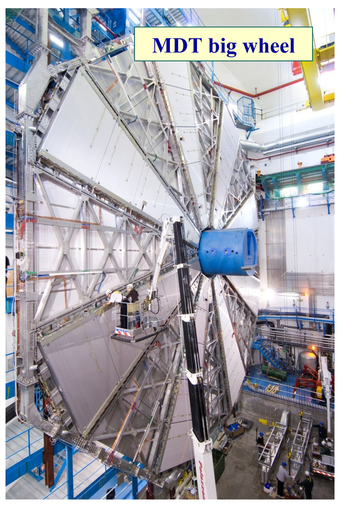
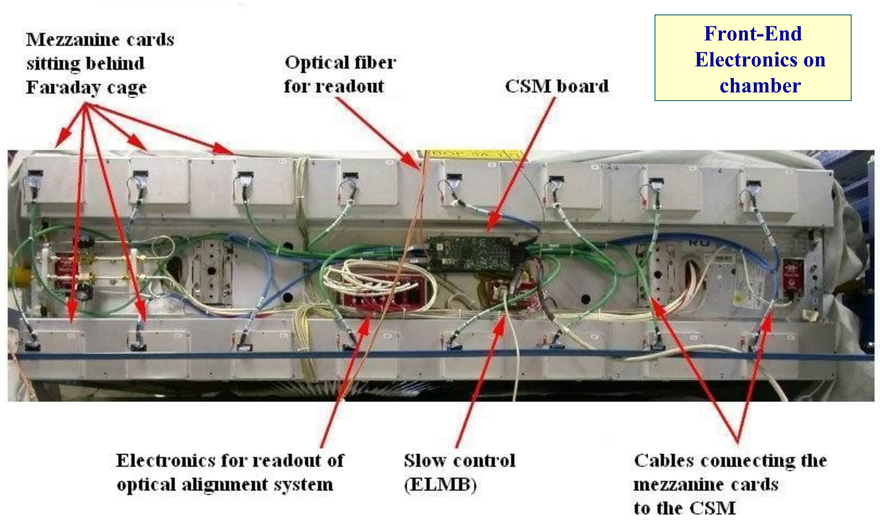
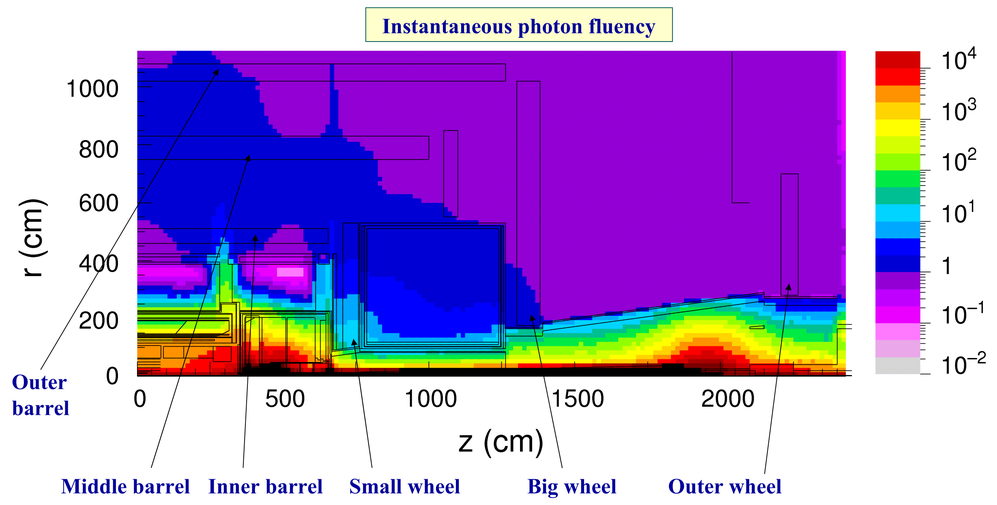


Muon Detector





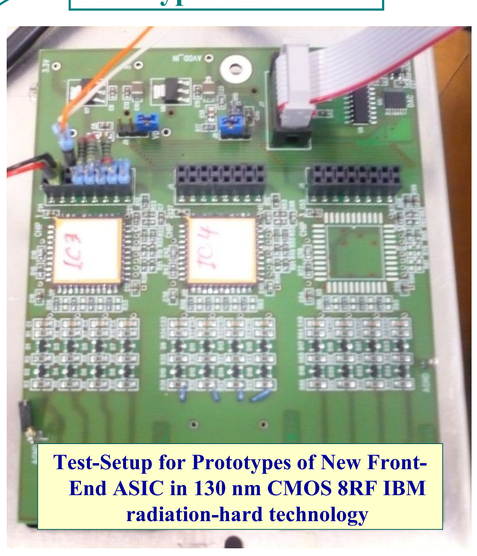
Radiation Environment

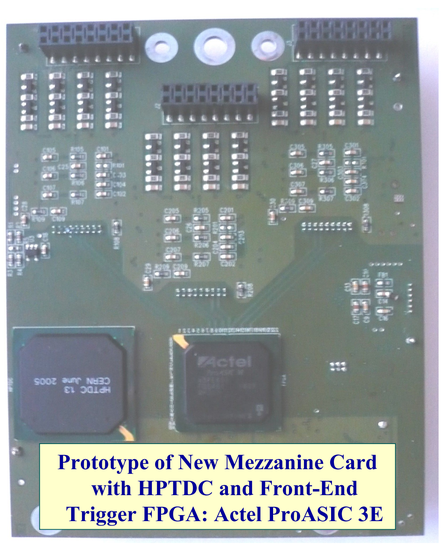


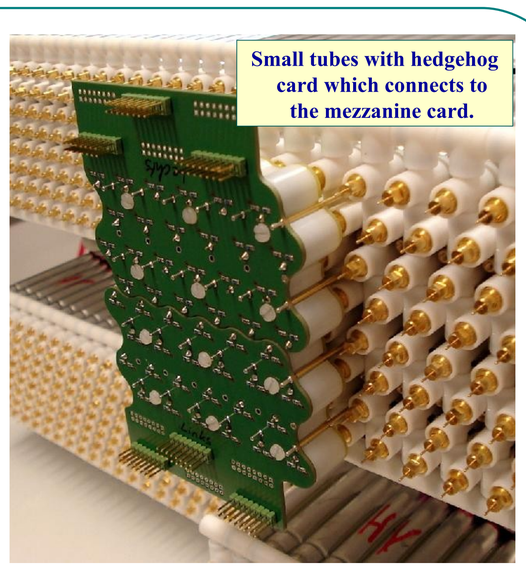
Motivations for Upgrade

- Radiation tolerant electronics for sLHC
- Small tubes (1.5 cm diameter instead of 3 cm)
  => shorter drift-time and dead-time
- Fix some know issues in front-end
- Implement high p_T front-end trigger
  => increase spatial trigger resolution
  for details, see “ATLAS muon trigger upgrades” presented by Robert Richter
- Use GBT for readout and slow control
- Cope with increased background
- Lower noise and cross-talk
- Re-spin of old chip (in HP 0.5um) not feasible

Prototypes and Studies


Test-Setup for Prototypes of New Front-End ASIC in 130 nm CMOS 8RF IBM radiation-hard technology


Prototype of New Mezzanine Card with HPTDC and Front-End Trigger FPGA: Actel ProASIC 3E


Small tubes with hedgehog card which connects to the mezzanine card.

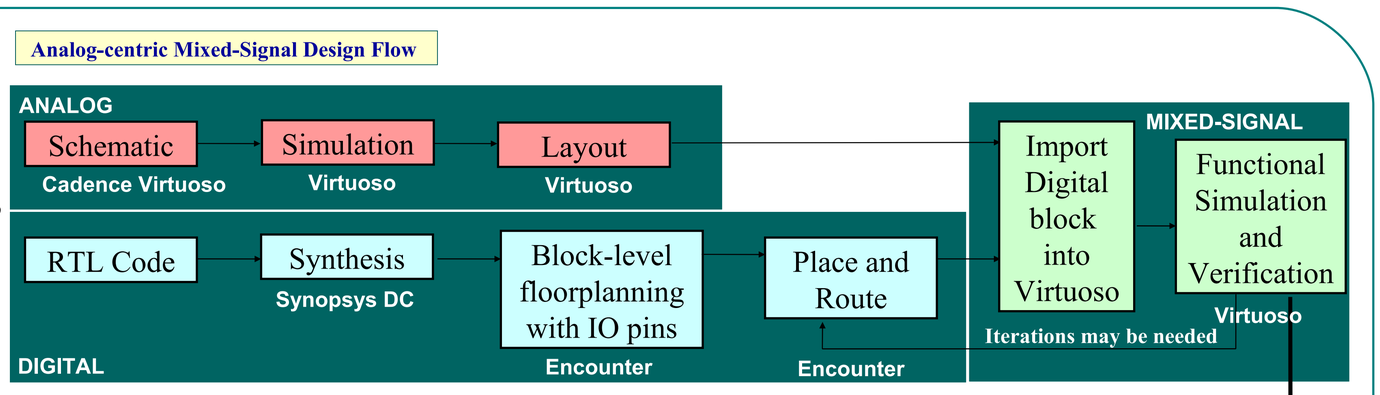
ASIC Design

- 4-channel ASD Lite Version 1: Designed in IBM 8RF-DM 130nm technology, consisting of analog blocks only. (Tapeout 2010)
- 4-channel ASD Lite Version 2: ADC/DACs (8 bit), JTAG test interface in Verilog, internal biasing, switched-cap Wilkinson ADC, and improved LVDS output drivers (Tapeout 2011)

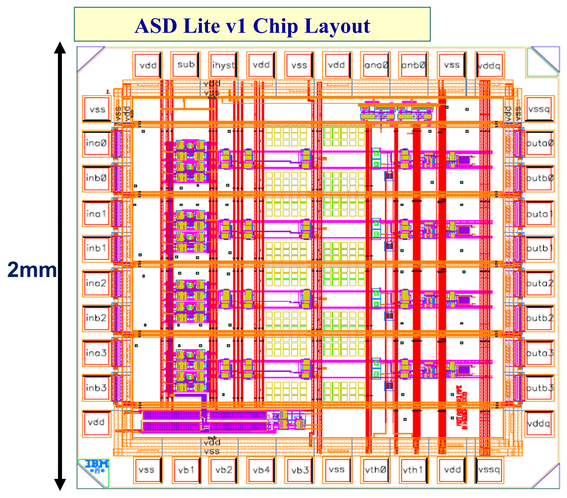
Technology Comparison

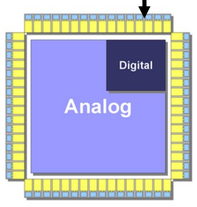
Technology	IBM 8RF-DM	IHP SGB25VD-TM2	Lfoundry LF150
Drawn MOS Channel Length	130nm	250nm	150nm
Technology Type	RF CMOS	SiGe CMOS	RF CMOS
Bipolar devices available	NO	YES (VP, VS, VH, VHP)	YES (Basic 3.3V NPN)
Metal Layers	8 (3 Thick Analog Metal)	5 (2 Thick)	6 (1 Thick)
Operating Voltages	1.5/2.5/3.3V	1.8/2.5V	**1.8/2.5/3.3/5V**
CMOS MOS types	Regular, Low Vt, Low Power, Reg IO, 3.3V IO, RF	Regular, RF	Regular, Low-leak, RF, Native, Isolated
Triple well possible	YES	YES (manual)	YES
PDK support	**good (through CERN)**	minimal	**good**
Rad hardness	**good (measured)**	**good (measured)**	**unknown**
Resistors	n+ diff, p+ p- poly, tantalum, nw diff	n+ poly, n- poly, p+ poly	nw diff, n+ poly, p+ poly, metal
Overall Variety of devices	High	Medium	High
MIMcap	2.05fF/um2 (4.1 for dual)	1fF/um2	0.98fF/um2
MPW/Enginnering run Cost	High	Medium	**Low**
Frequency of MPW run	Medium	Medium	**High**
PDK / Compatibility with tools	Good	Minimal	**Good**
MPW submitted through	CERN, MOSIS	Europractice MPW	Europractice MPW
Experience (Previous MPW submitted)	**2**	**2**	0
LDMOS module available	NO	YES	YES
Fab Location	Burlington, USA	Frankfurt-an-der Oder, Germany	Landshut, Germany

Analog-centric Mixed-Signal Design Flow



ASD Lite v1 Chip Layout





Tools used (from Europractice):
- Synopsys Design Compiler
- Cadence Virtuoso 6.1.3 and Calibre
- Cadence Encounter 8.1

Results:
- Measured low noise and channel-to-channel crosstalk
- Good analog channel performance
- Successful neutron irradiation test showed minimal degradation

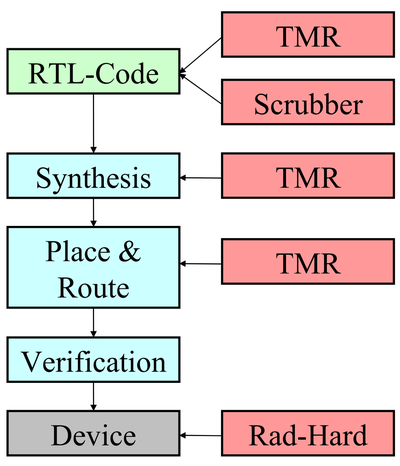
Things to improve
- LVDS drivers and supply coupling
- Use triple-well nfets for better noise immunity

Radiation Issues

General fault types
- User data SEU (Single Event Upset)
- Single event transients (SET)
- Silicon Effects (Surface + Bulk)
  - Latch-up
  - Changed transistor parameters
  - Physical destruction

FPGA specific faults
- Configuration SEU (in S-RAM based devices)
- FPGA SEFI (Single Event Functional Interrupt)

Radiation-tolerant FPGA Design



- Custom RTL-Code
- Vendor IP-Block

- Full flexibility, comprehensive
- Time consuming
- Error prone, detailed knowledge mandatory
- Often lack in documentation + support

PRECISION RAD-TOLERANT SYNTHESIS

TMRTOOL

- Easy to use, flow well documented
- Good overall results
- Expensive (no discount on licenses)
- Limited flexibility

- Xilinx Virtex QPro
- Actel RT ProASIC 3E

- Prototyping with normal FPGAs
- Improved radiation tolerance off the shelf
- Expensive and hard to get
- Limited in speed and device features