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Upgrade of the ATLAS MDT Front-End Electronics

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Summary

For running the ATLAS muon spectrometer with S-LHC, the readout electronics of the precision tracking chambers (Monitored Drift Tube chambers) needs to be upgraded. On the one hand, the radiation hardness of the individual components must be increased. Another motivation is the implementation of a high energy muon trigger in the front-end, which provides more precise information than the trigger chambers. This will increase the trigger efficiency due to a better separation between background and physics data.

The analogue part of the system is implemented in an ASIC using the 130 nm CMOS 8RF IBM radiation hard technology. A first prototype chip with reduced features has been made and was successfully tested in 2010. Two of the chips have been irradiated with a neutron beam up to 3.9e14 n/cm^2. After cooling down, they were measured again and found fully operational and with very little changes. Based on the results and experience, a new version of the ASIC was designed and is currently being manufactured.

The improvement of the trigger has been developed conceptually. Its implementation in the new front-end readout electronics and integration in the ATLAS trigger scheme seems feasible. Currently we are building a setup to test the trigger scheme and to demonstrate that our idea is working. For reasons of flexibility and ease of use, we implement the logical function in an FPGA. Although in the current phase we are not focusing on radiation hardness, we use a flash-based Actel ProASIC3E chip, which can be replaced with a special radiation tolerant version later on. As it is not susceptible to SEUs in the configuration memory like the S-RAM based Xilinx Virtex-II FPGA used in the current front-end, it is a promising candidate for the upgrade electronics.

We will present our experience with radiation tolerant ASIC and FPGA designs and will be keen on discussing and sharing valuable knowledge with people working in the same field.

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