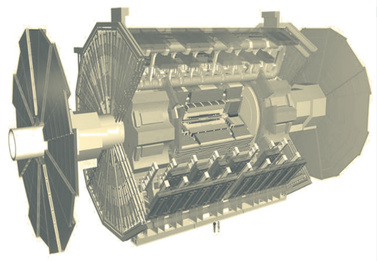

The Fast Tracker Real Time Processor and Its Impact on the Muon Isolation, Tau & b-Jet Online Selections at ATLAS

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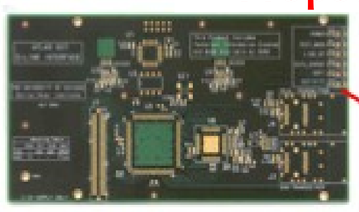
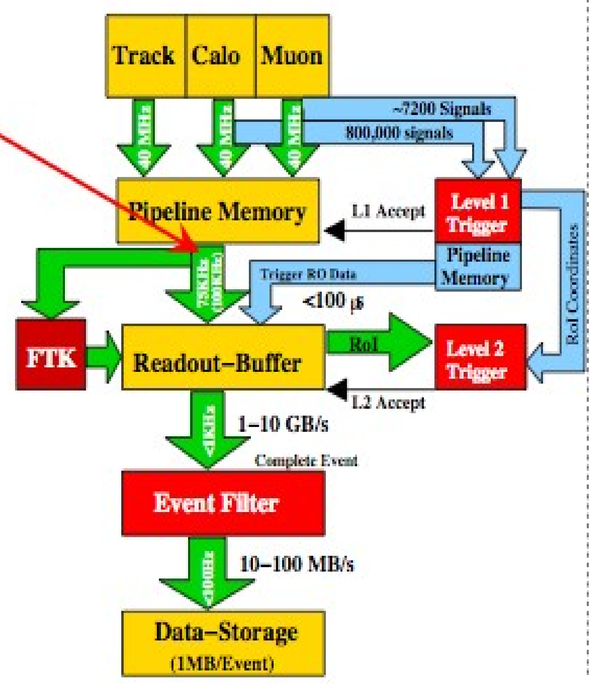
on behalf of the FTK Collaboration

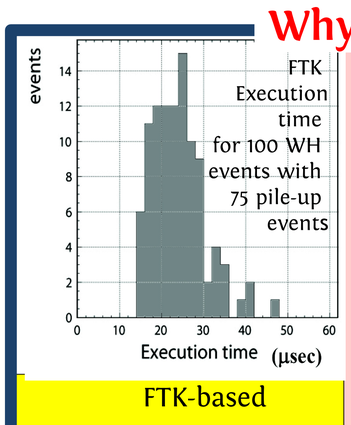
Proposed FTK in Trigger System



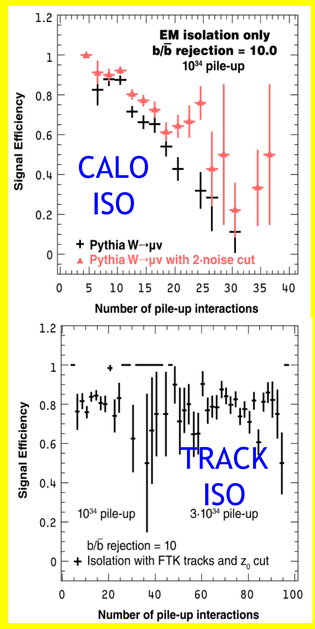
- The FTK system receives data from ReadOut Drivers (RODs)
- ROD output is duplicated by a dual output board
- Tracks reconstructed by the FTK processors are written into ReadOut Buffers (ROBs) for use at the beginning of LVL2 trigger processing
- FTK operates in parallel with the silicon tracker readout following each LVL1 trigger



Why Add a Hardware Tracker?

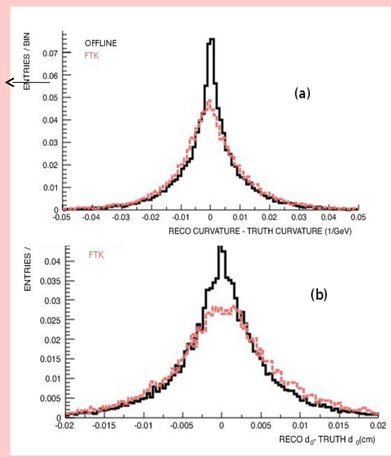


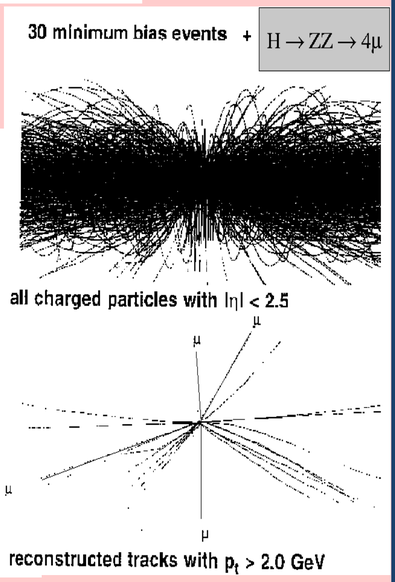
FTK-based μ isolation



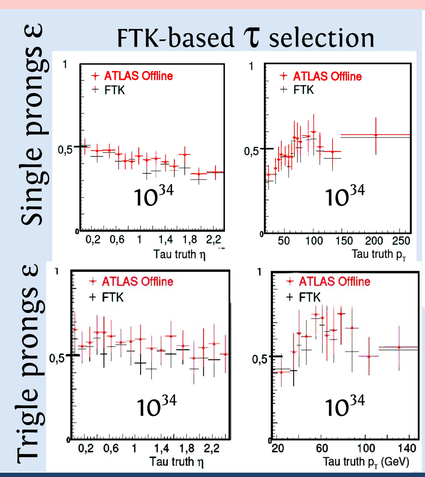
Event clean-up in ~25 us

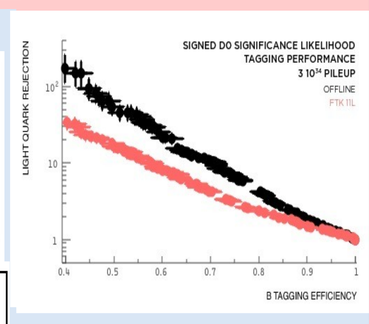
It reconstructs all tracks with Pt>1 GeV with good precision





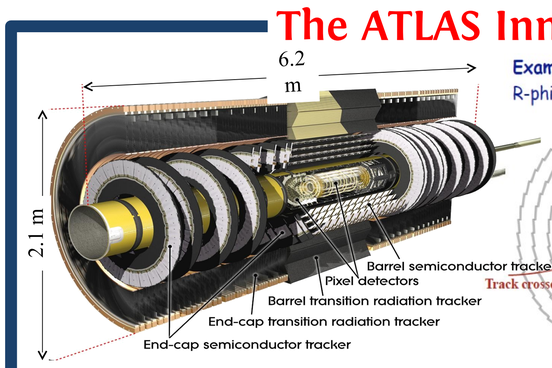
FTK-based τ selection



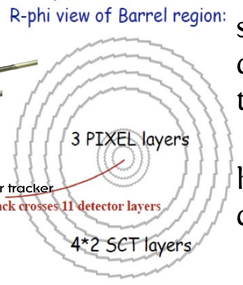


Fakes for both single & triple prongs: few ‰

The ATLAS Inner Detector (ID)



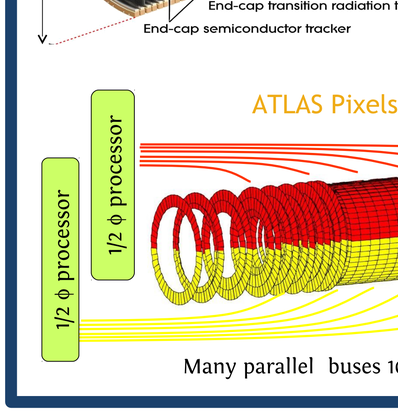
Example:
R-phi view of Barrel region:



ID: ~100 million channels of silicon pixel and strip (SCT) detectors and straw drift tubes

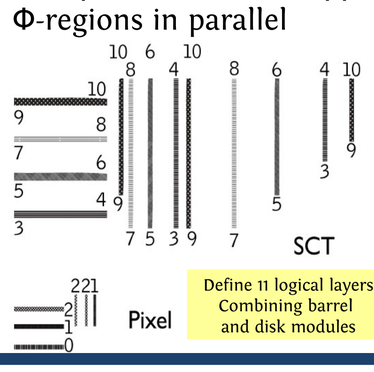
FTK uses pixel and SCT hit information to infer charged particle tracks

FTK processes 8 overlapping Φ-regions in parallel



Divide into 8 Φ sectors

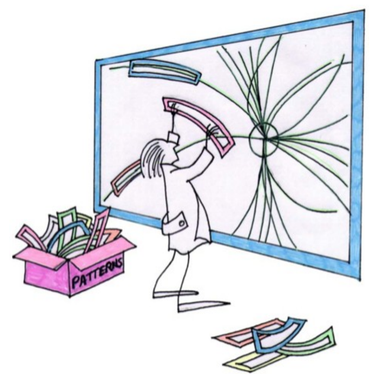
Allow a small overlap for full efficiency

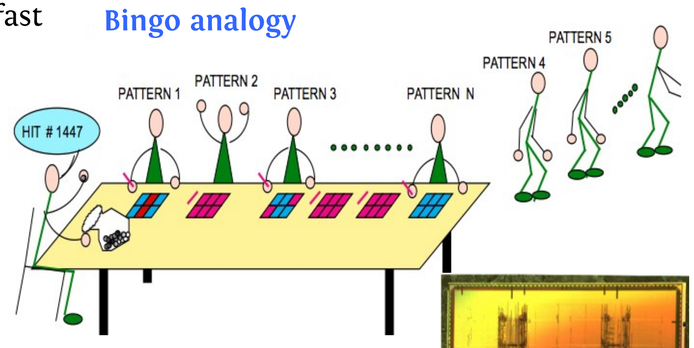


Pattern Recognition using Associative Memory (AM)

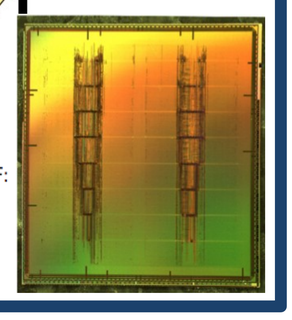
A large bank of pre-computed hit patterns is used for very fast tracking (memory → speed)

Bingo analogy



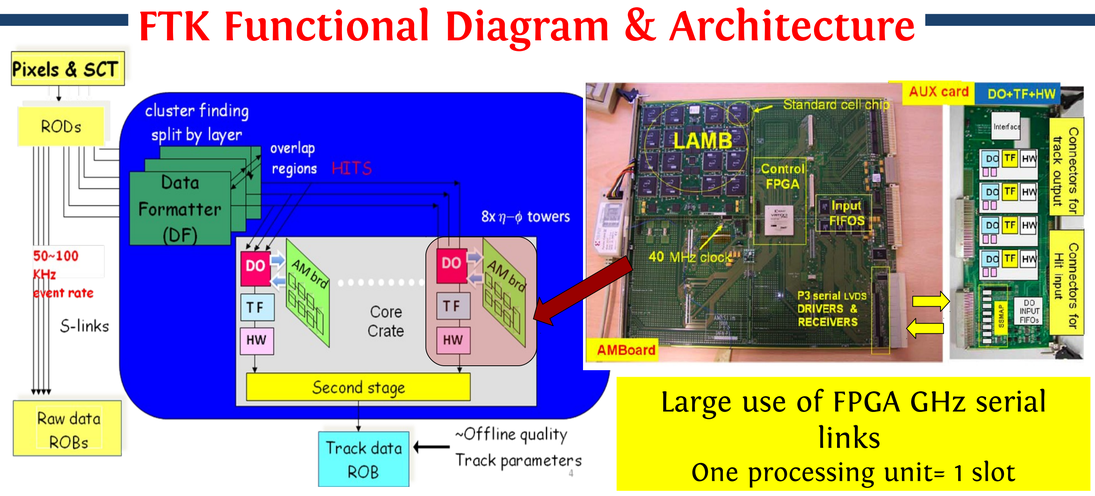


Linearized track fit using full-resolution silicon hits after pattern recognition



Current chip used at CDF: 0.18 μm custom cells, with 2500 pattern/chip. *IEEE Trans.Nucl. Vol. 53 Page(s):2428 - 2433*

FTK Functional Diagram & Architecture



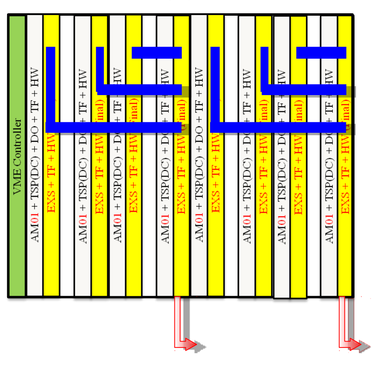
Large use of FPGA GHz serial links
One processing unit= 1 slot

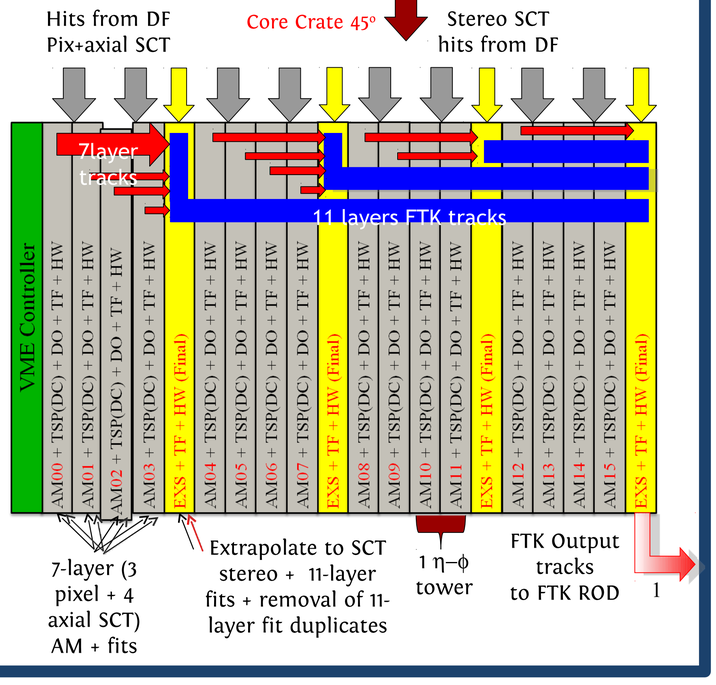
Highly parallel data flow: 64 η - Φ towers in 8 core crates and 4-fold parallelism within each tower (for 3×10^{34})

A scalable system

W 75 pile-up events
8 Core crates,
16PUs/crate,
64 eta-phi towers

W 17 pile-up events
8 PUs, one per Φ sector
Everything in a single crate





7-layer (3 pixel + 4 axial SCT) AM + fits

Extrapolate to SCT stereo + 11-layer fits + removal of 11-layer fit duplicates

1 η–φ tower

FTK Output tracks to FTK ROD

The chip under development

Control logic in Standard Cell : fast development and reliability
+
Associative Memory bank in Full Custom : high density, low power, better performances
(both in TSMC 65nm technology)

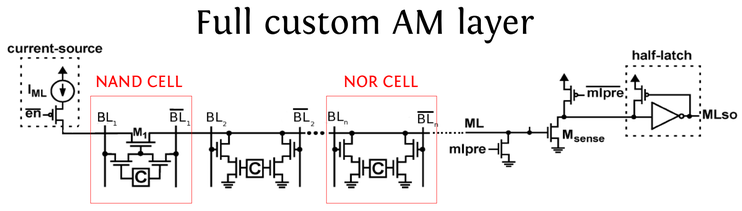
First prototype (2011): 8k patterns/chip
Production (>2014): 80k patterns/chip
(old chip 5k patterns/chip, 6 bus instead of 8, no don't care, 100 mm² vs 12 mm²)

New in this chip
Ternary logic

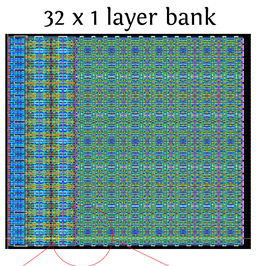
Special bits can store values 0 1 X (don't care)

Very useful in FTK:
- Smaller banks
- Lower roads rate

Full custom AM layer



32 x 1 layer bank



High density:
- 8x **12 bit** (binary) + **3 bit** (ternary)
- majority logic
- readout tree

~550 x 1.8 μm

Low power:
- Current race scheme
- Selective precharge

50% less power