ATLAS pixel electronics
RD for upgrade inner pixel layers

A.Rozanov (CPPM-IN2P3-CNRS) 10.03.2011

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Outlook

Challenge for internal pixel layers at HL LHC
High density direction: exploring 65 nm technology
3D electronics direction: Tezzaron-Chartered 130 nm technology
Radiation hardness of Chartered process
Testing Chartered technology with FE-C4-P1 ,P2,P3
Tezzaron-Chartered MPW run
FE-TC4-P1 chip
Plans

HL LHC

HL LHC maximum achievable luminosity 10^{35} cm^{-2} sec^{-1}
After luminosity leveling 5 10^{34} cm^{-2} sec^{-1}
But probably 50 ns bunch crossing, high pile-up 230 events
Integrated luminosity 3000 fb^{-1}, total dose of 500 MRad in b-layer
To keep the performance one need to improve pixel granularity:

- **reduce occupancy**
- **improve resolution**
- **improve two track resolution**
- **split merging clusters in dense jets**
- **reduce inefficiencies in the readout**

Two solutions

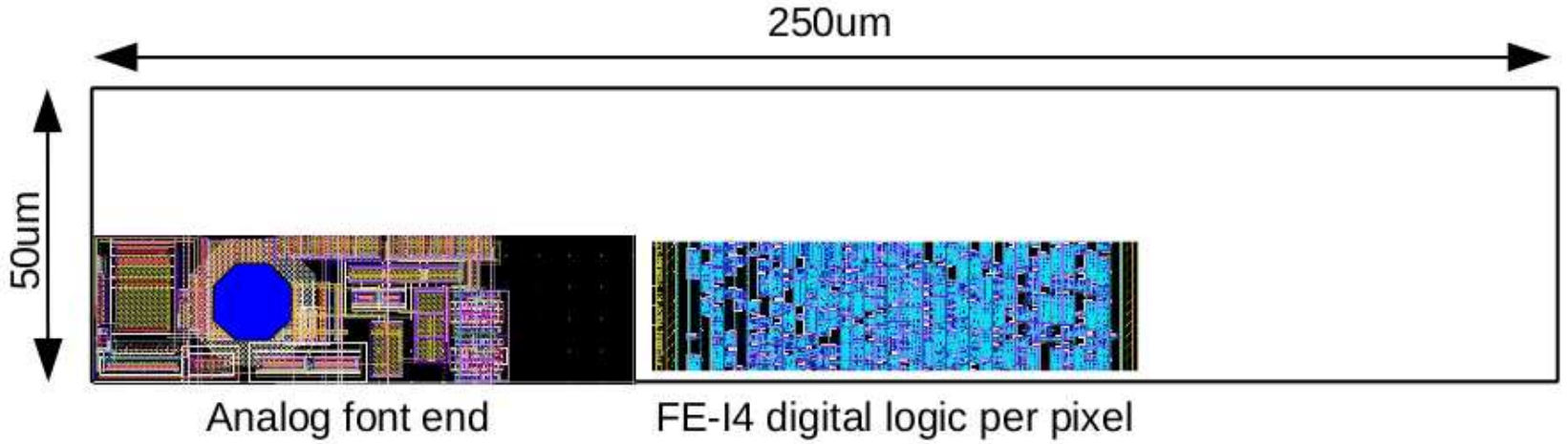
- **move to higher density technology like 65 nm**
- **move to 3D electronics with TSVs**

If both works, combination of two approaches is also interesting

65nm Feature size

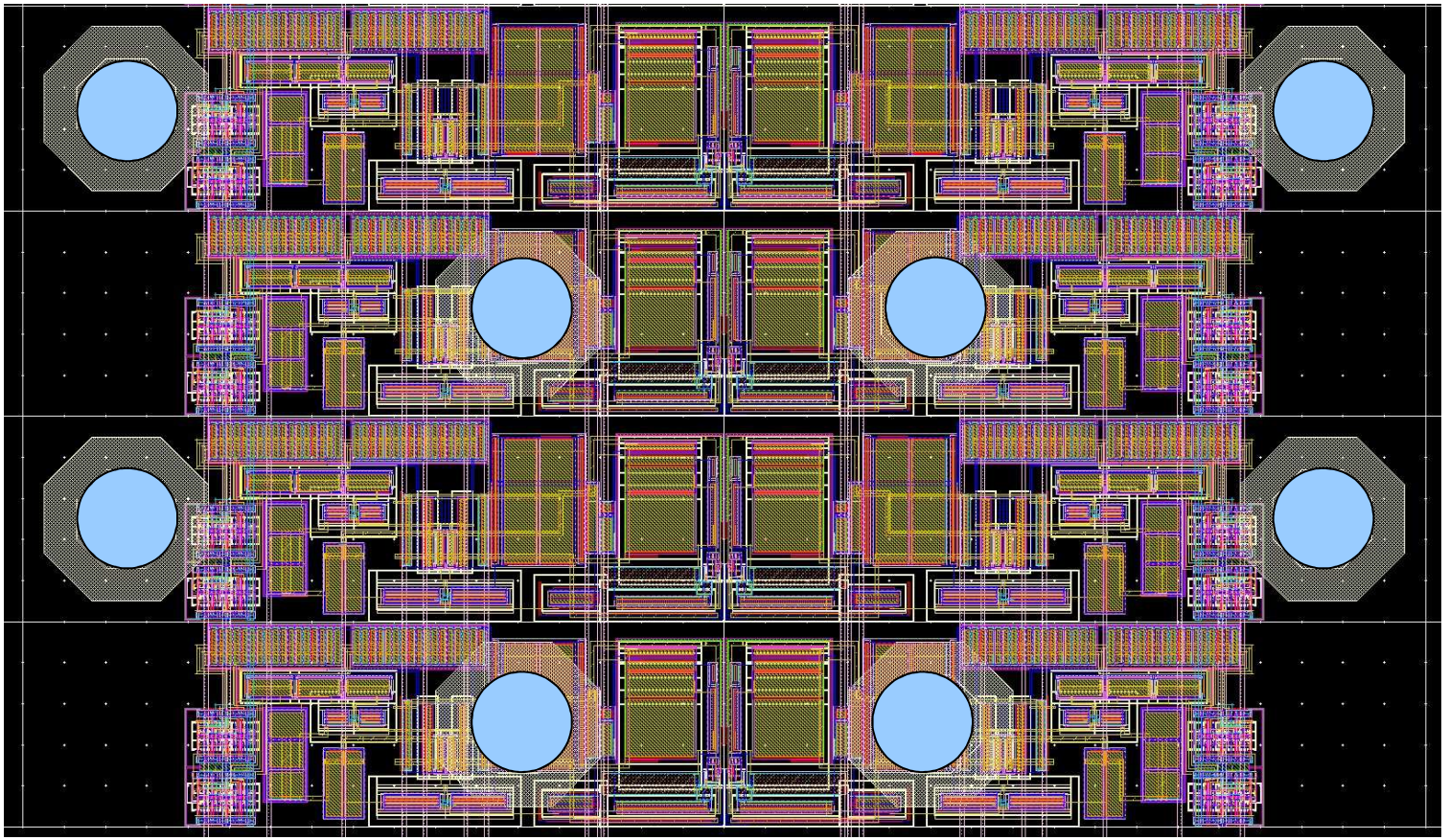
- Should give factor of 4 area reduction for digital circuits compared to 130nm.
- Conventional wisdom is that analog circuits cannot be reduced because intrinsic gain of transistors is no better in 65nm
  - But front end size is not all determined by gain (eg. There are capacitors, switches, interconnects, and all of those do scale)
  - Approach followed is to reduce analog complexity /performance and compensate with digital signal processing. This reduces not only size but also power.
- First prototype analog test chip in 65nm about to be submitted (TSMC)

- 65nm pixel layout shown below inside FE-I4 pixel outline



Synthesized in 65nm kit. For illustration only. Not in test chip.

65nm analog pixel array with staggered bumps

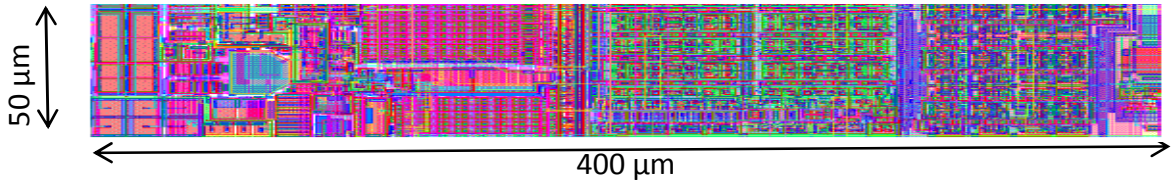


50µm center-to-center bump spacing. 16 column x 48 row array in test chip.
25µm pixel pitch in R-Phi
Z length to be adjusted as needed for future digital region design. Expect ~150µm

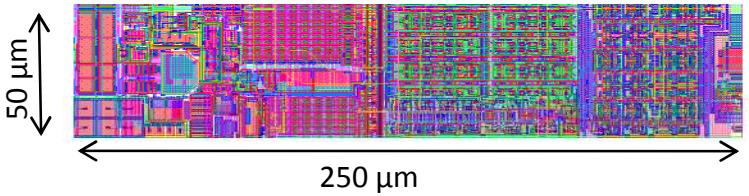
Simulated analog performance

- Initially simulating with 4.5µA per pixel (1.2V rail)
  - This is a little more per unit area than 10µA/pixel in FE-I4 analog.
- Design works down to ~2µA / pixel, but must optimize biases.
  - Goal is in the range 2-3µA / pixel
- Load: 300fF, return to baseline: 300ns, leakage current: none
- Noise = 115e-
  - Noise increases slowly as supply current is reduced. Noise is not our problem to further reduce current.
- Timewalk: ~40ns for 1000e- above threshold
  - Need 4000e- above threshold to get timewalk<25ns
  - Timewalk does get worse as supply current is reduced. This is the limiting factor to reduce current
  - BUT SOME TIMEWALK IS OK
    - Recall our approach is to reduce analog performance and compensate with digital processing.

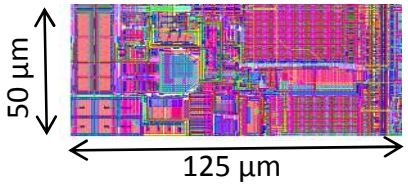
3D approach: ATLAS Pixel Front End size

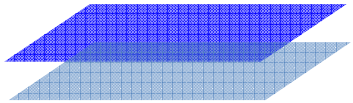


FE-I3 CMOS 250 nm

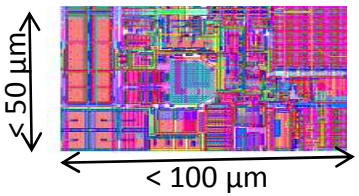


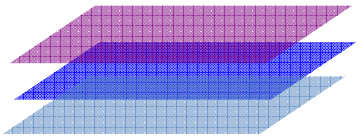
FE-I4 CMOS 130 nm





FE-TC4 CMOS 130 nm 2 layers





FE-X5-3D CMOS xx nm 3 layers

3D Tezzaron-Chartered approach

Two main questions:

Is Chartered 130 nm technology qualified for HL SLHC 500 Mrad dose ?

- **are basic transistors radiation hard ?**
- **portability of FE-I4 designs to Chartered ?**
- **rad hard SEU latches in Chartered ?**

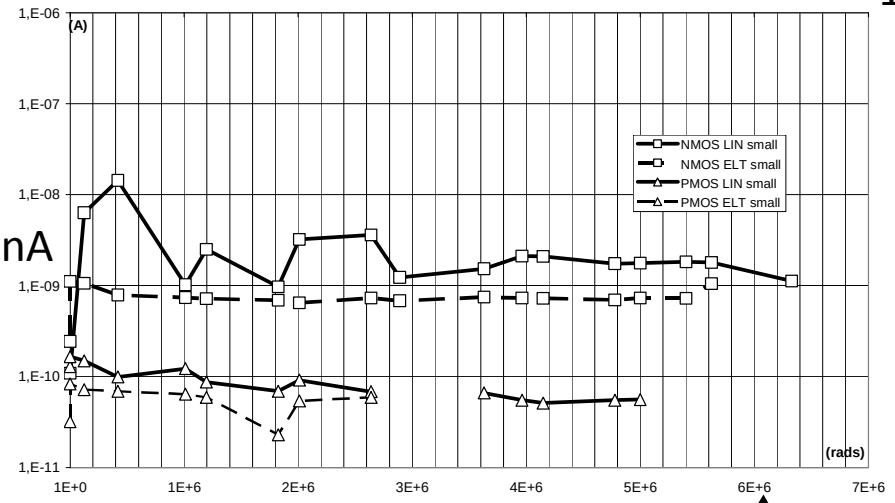
Is 3D Tezzaron integration achievable for HL LHC pixel chips?

- **tools availabiliy?**
- **MPW availability?**
- **yields**
- **electromagnetic pickups between tiers**
- **mechanical and thermo robustness**
- **radiation hardness**

Radiation test of Chartered transistors

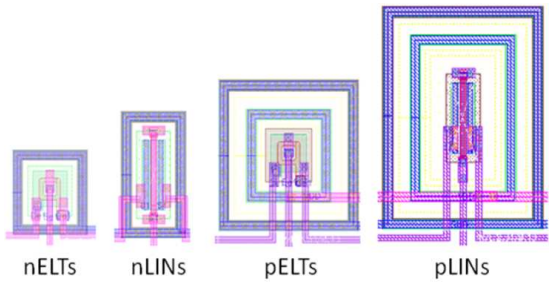
Test big(99.28/0.13µm) and small (2.31/0.13µm) transistors, PMOS and NMOS, linear and enclosed. Very small variations in leakage currents of PMOS and enclosed transistors, specially for slow rate irradiations.

1 µA



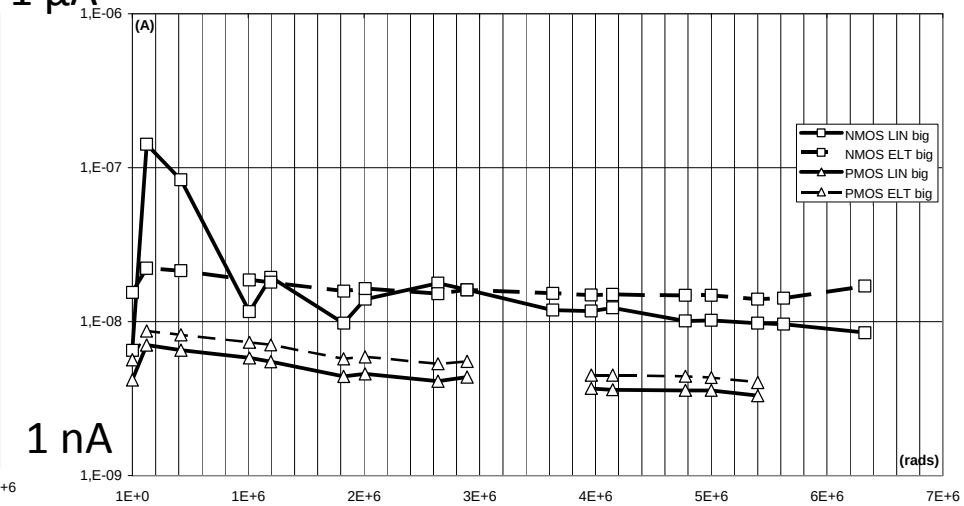
Small

1 nA



6 MRad

1 µA



Big

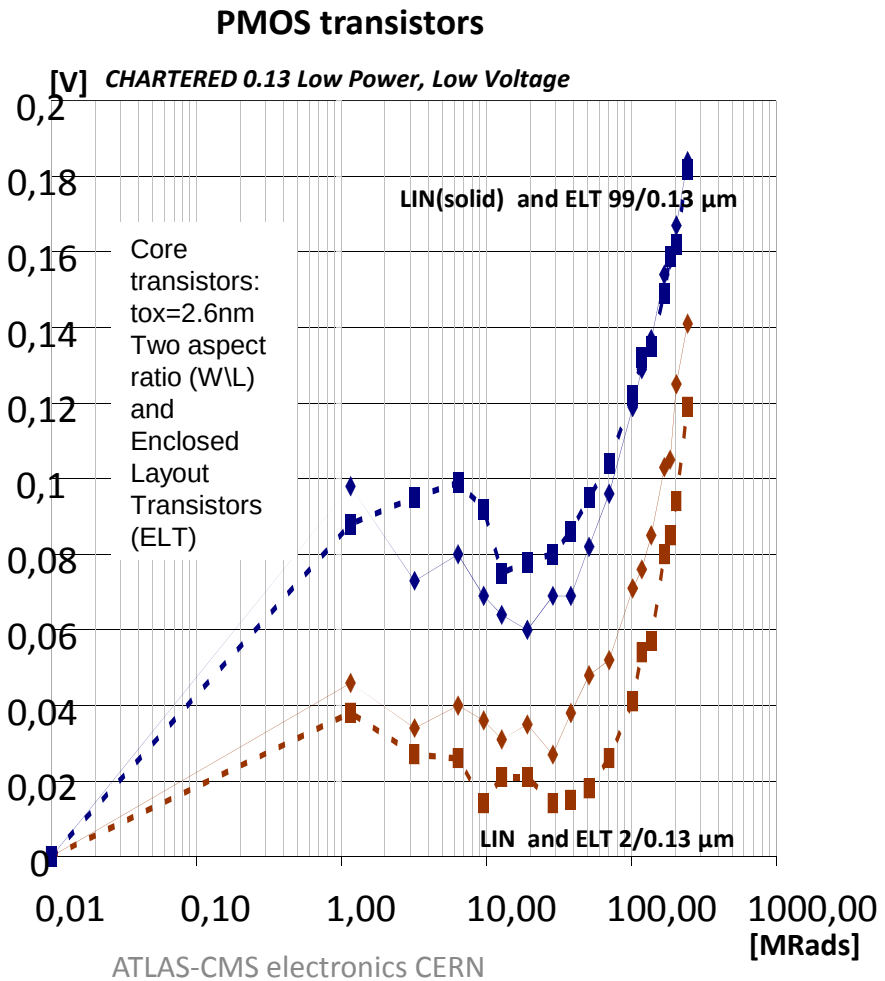
1 nA

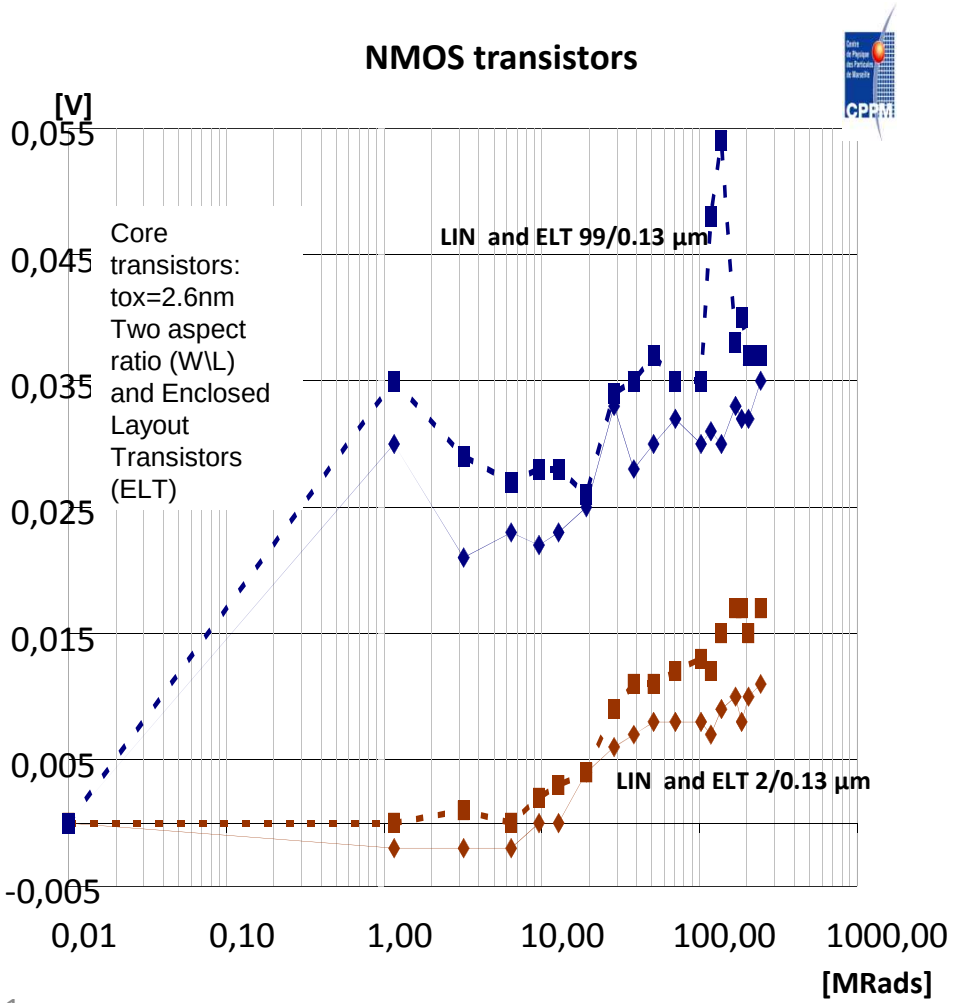
6 MRad

Gamma ray irradiations at CPPM (low dose and rate).

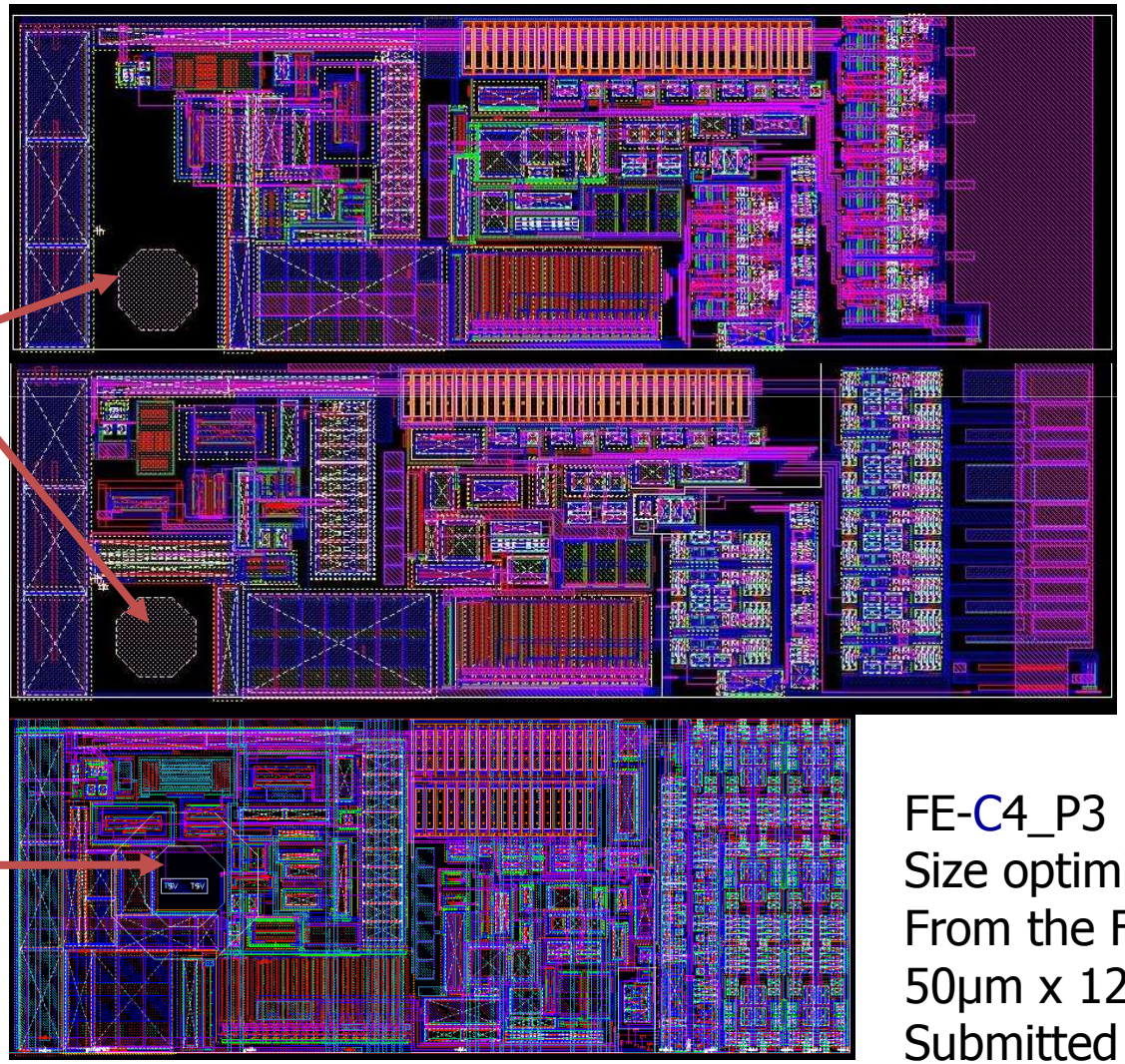
Threshold voltage variations with dose

Close results in linear and enclosed transistors





FE-C4-PX :
pixels size reduction



FE-C4_P1
From the FE-I4_P1
50µm x 166µm
Tested

FE-C4_P2
Electrical optimization
From the FE-C4_P1
50µm x 166µm
Tested

FE-C4_P3
Size optimization
From the FE-C4_P2
50µm x 125µm
Submitted February 2011

FE-C4-P1 test results

Porting FE-I4-P1 (61x14 pixel array 50*166 µm , chip 3x4 mm) into Chartered FE-C4-P1 in January 2009 by Bonn-CPPM-LBNL collaboration

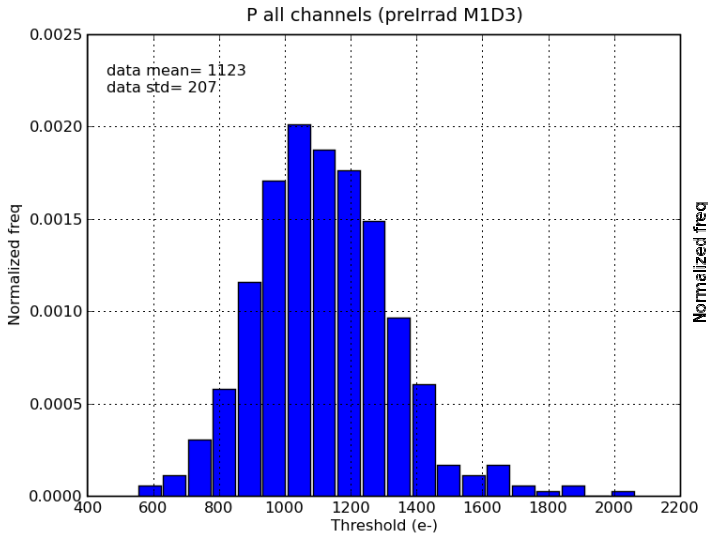
tests by Bonn-CPPM-LBNL in the labs, by CPPM on 24 GeV protons of CERN PS

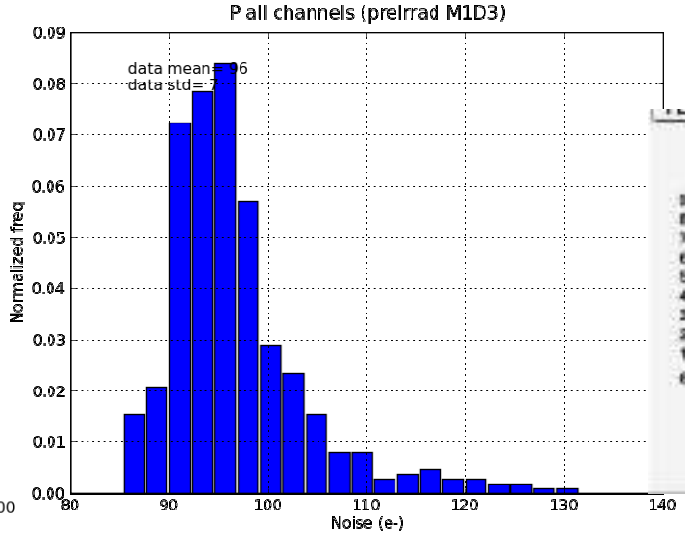
thresholds up to 1000 electrons, threshold dispersions 200 electrons

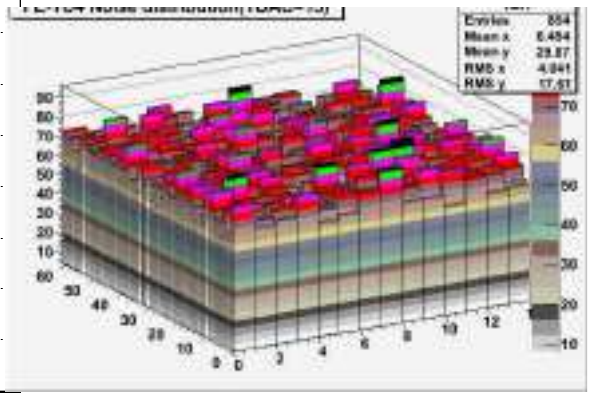
noise 70-100 electrons

normal SEU performance (as FE-I4-P1 or better), no digital problems up to 160 Mrad

after 400 Mrad, analog performance acceptable, noise increase to ~250 electrons







Transition from FE-C4-P1 to FE-C4-P2

After 160 MRad small percentage of DICE type latches in FE-C4-P1 are « Stick-to-One » both inside pixel and as inputs to DACs

Careful simulation of DICE lathes have shown the same « Stick-to-One » in the corners

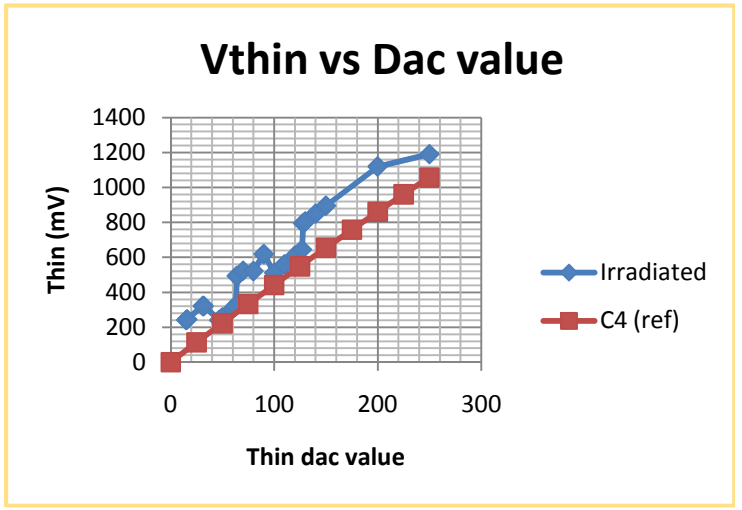
Explanation: not optimized choice of parameters for DICE latches

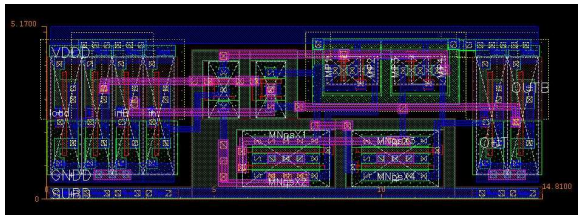
Irradiation tests with X-rays at CERN. After 230 MRads no degradation observed on FE-C4-P1.Does it mean the systematic difference between X-ray and proton ? More X-ray irradiation will be done to resolve it.

Action: correct and resubmit FE-C4-P2 with two variants of DICE latches

February 2010, get FE-C4-P2 chip from Chartered

After 400 Mrad proton irradiation DICE latches functions correctly.

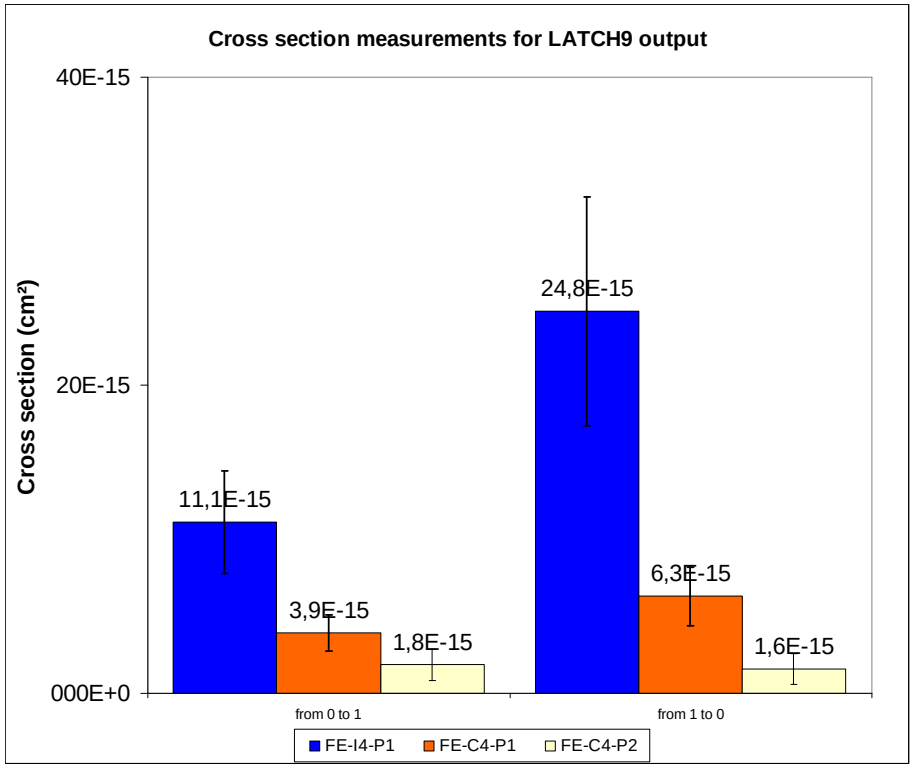


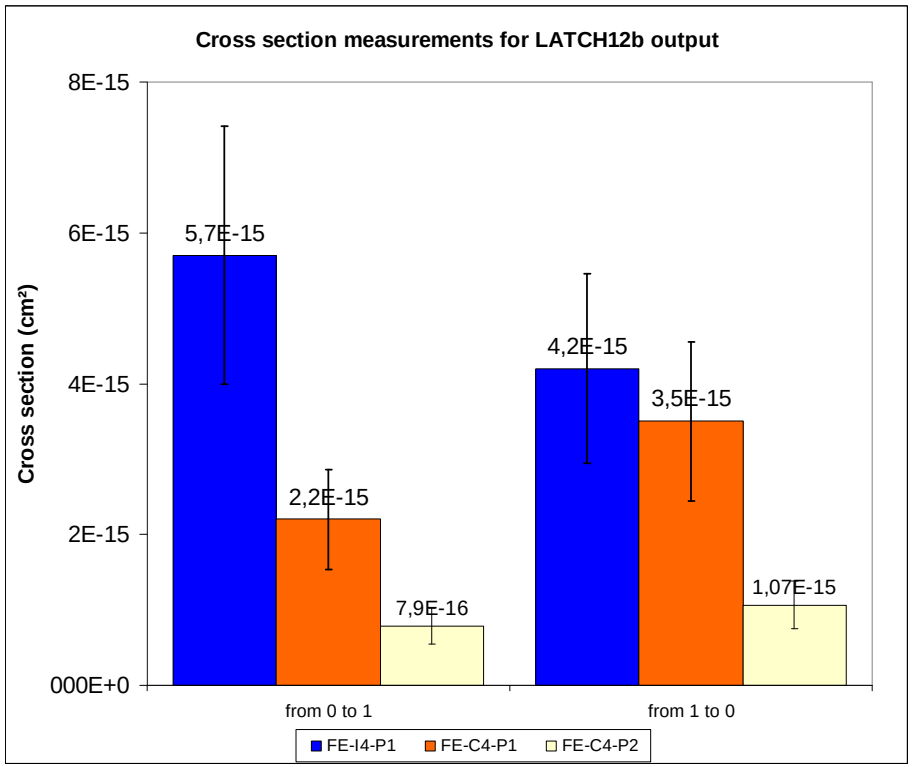


SEU performance

Dual Interlocked Storage Cell (DICE) with guard ring separation and separate nweel/pwell for NMOS/PMOS devices

FE-I4-P1 latch size 6.3x5.54 µm, separations : nmos 2.35 µm, pmos 0.83 µm
FE-C4-P1 latch size 6.0x5.70 µm, separations : nmos 3.68 µm, pmos 1.00 µm
FE-C4-P2 latch size 14.8x6.20 µm, separations : nmos 3.26 µm, pmos 2.02 µm





FE-TC4-P1

First 3D pixel chip FE-TC4-P1 submitted in August 2009 en 3 variants

FE-TC4-AEDS-P1 - analog tier LBNL-CPPM, digital tier simple « drums » by CPPM

FE-TC4-AEDC-P1 – complex digital tier close to final FE-I4 – by Bonn

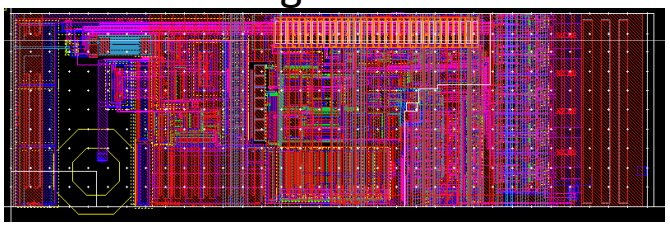
FE-TC4-AHDS-P1 - analog tier "holes" LBNL-J.Fleury(LAL), digital tier - CPPM

Pixel size 50 um x 166 um, analog tier is very close to FE-C4-P1

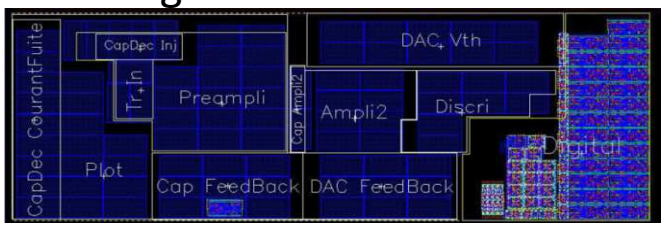
AE tier, DC tier, DS tiers tested separately February 2011

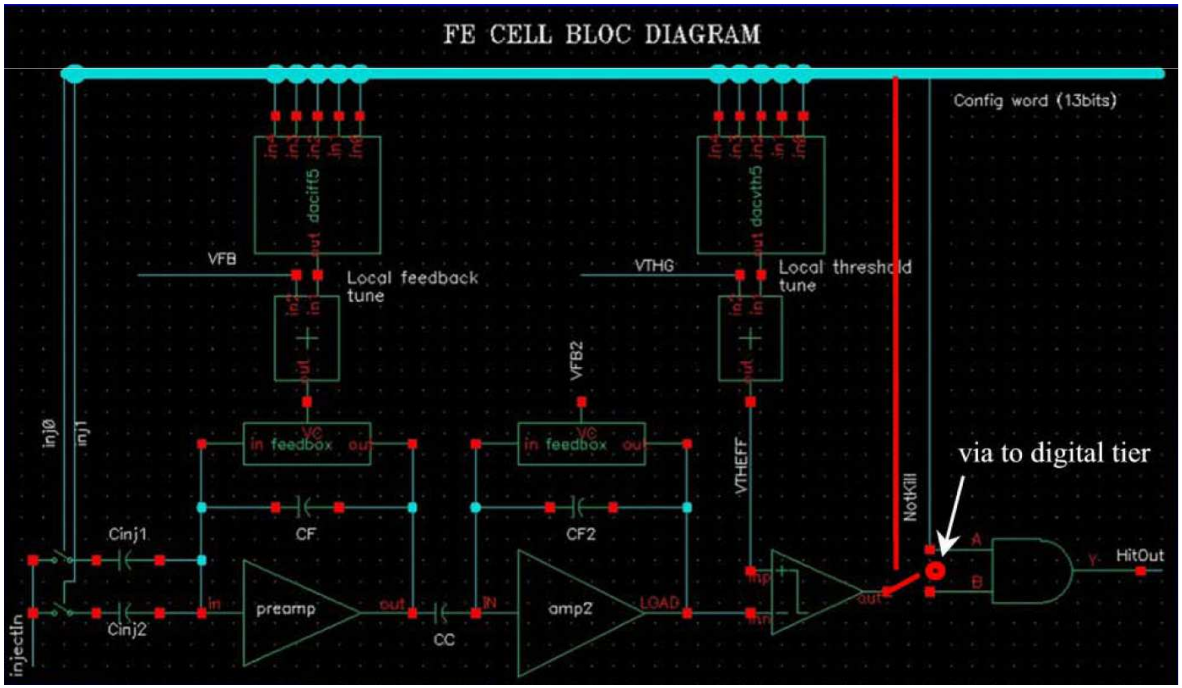
3D assembly AE-DC and AE-DS expected in April 2011

Analog AE tier



Digital DS tier





FE-TC4-P1

Pixel size 50 um x 166 um, analog tier is very close to FE-C4-P1
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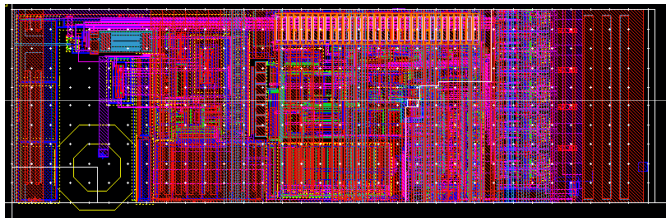
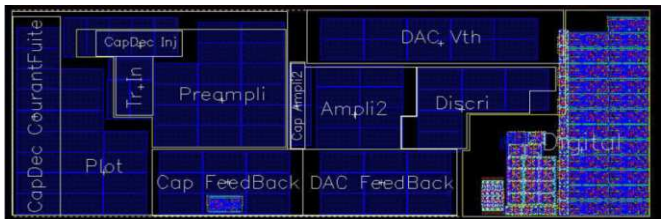
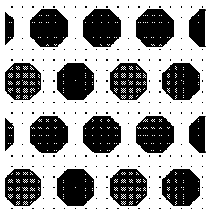


Analog AE tier

Digital DS tier

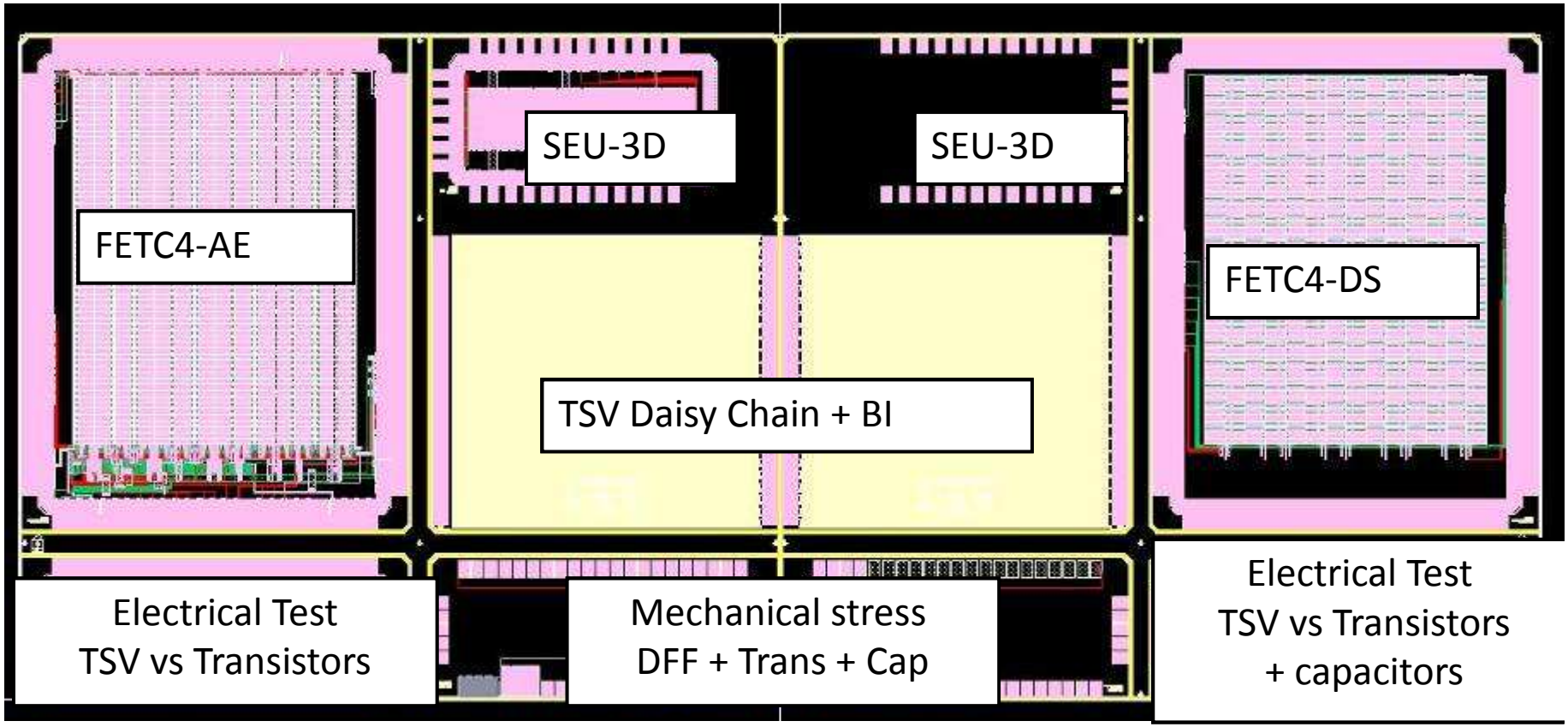




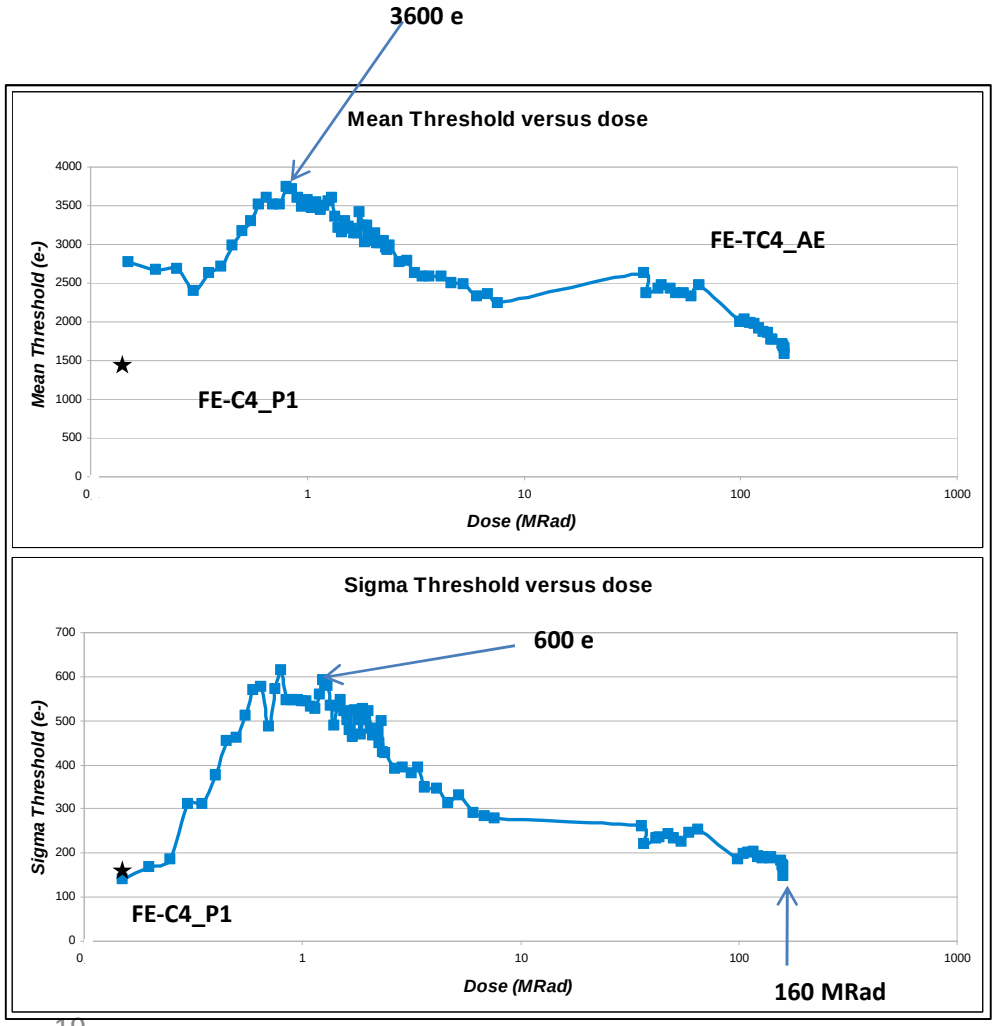
C-Band ATLAS

Corresponding Si detectors produced at Munich planar sensor run (H.Moser,A.Macchiolo)

Bump-bonding tests planned at IZM-Berlin.

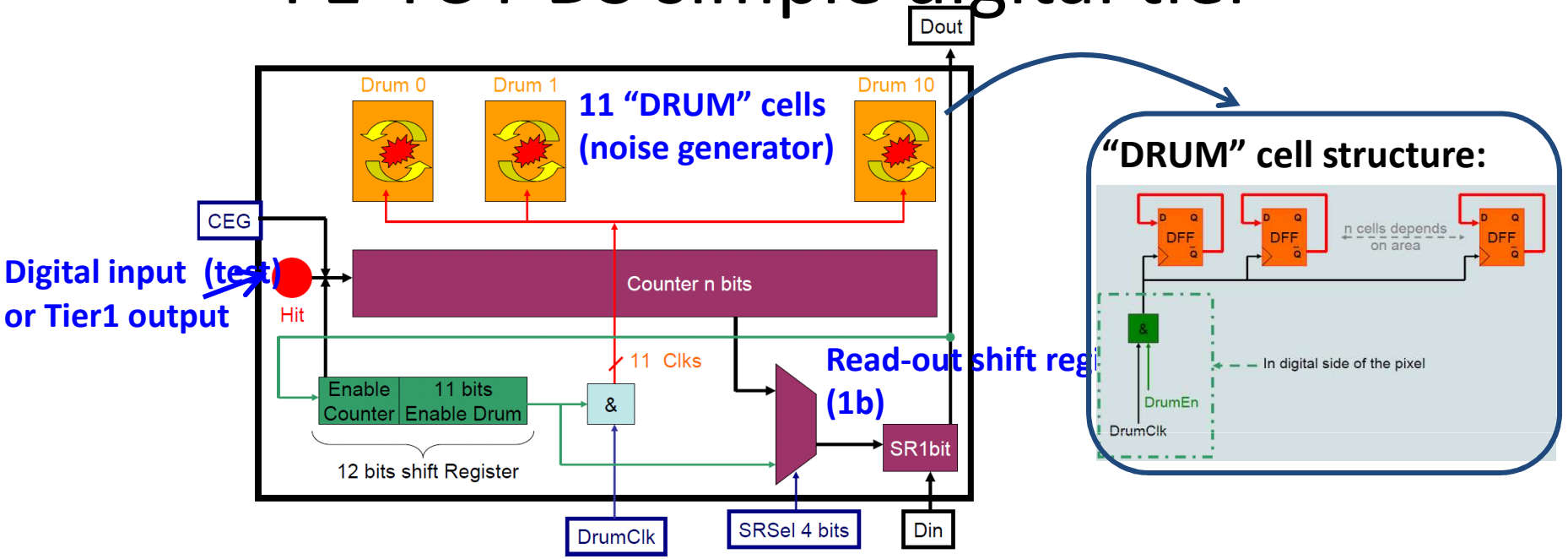


FE-TC4-AE tier X-rays radiations at CERN



- Noise peaks at 60 e at 1 Mrad and goes down to 45e at 160 Mrad
- Consistent results on chips with and without TSV on the input of amplifier

FE-TC4-DS simple digital tier



Test Shielding strategy :

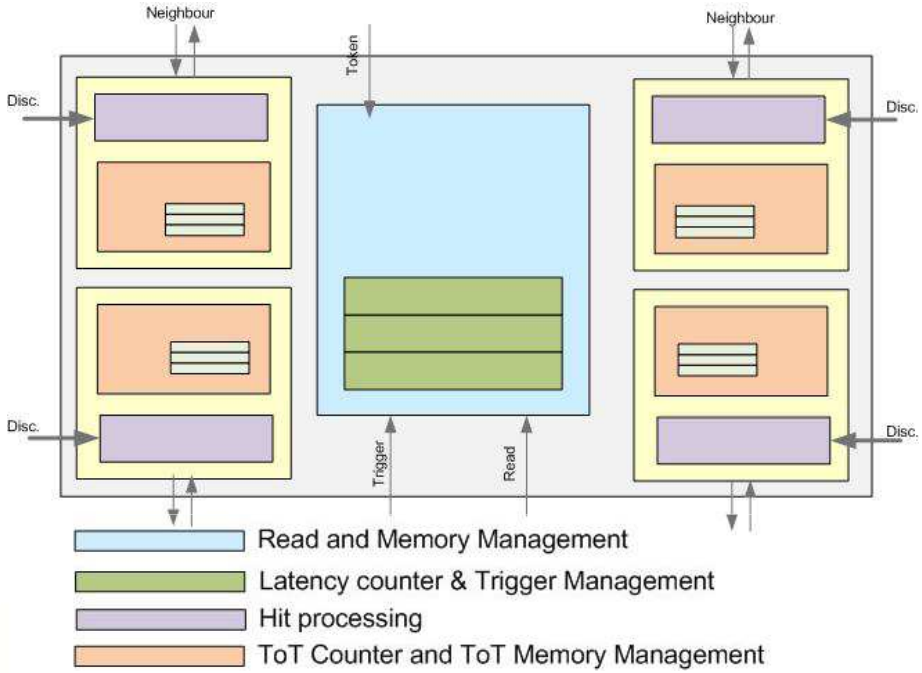
- 5 columns without any shielding (reference),
- 4 columns with shielding in metal 5,
- 2 columns with shielding in metal 3,
- 2 columns with both shielding.

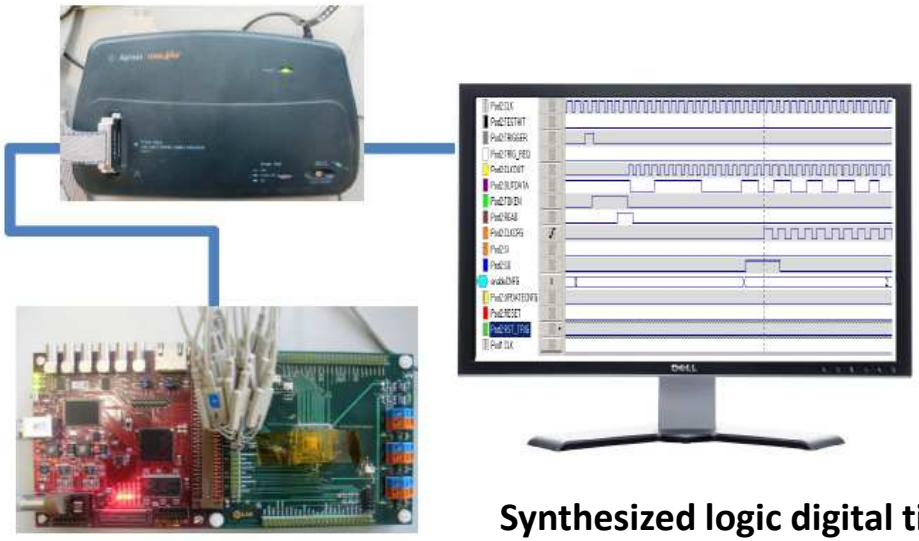
Tested at CPPM lab

FE-TC4-DC complex digital tier

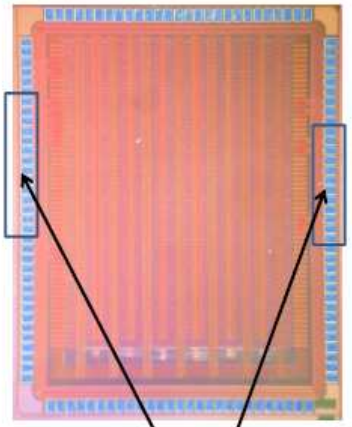
Read-out chip similar to FE-I4-A:

- **4-pixel region**
- **Simplified periphery and read-out control logic**
- **Fully tested in the Bonn lab**





Synthesized logic digital tier a la FE-I4 tested and functional



Short term plans

- Summer 2011: test of FE-TC4-P1 with simple and complex digital tiers to check the influence of the digital tier on the performance of analog tier, test of the TC test chip to qualify the quality of TSV and surface contacts, thermal cycling and irradiation tests to prove the thermal and radiation hardness of FE-TC4-1
- March 2011 increase the dose of X-ray irradiation for FE-C4-P1 to check if there is a difference between protons and X-rays for DICE latches
- 2011: submit FE-TC4-P2 (final analog 125 um, PLL, LVDS, Current Ref, pads, I/O, DACs etc)
- 2011: submit new version of OmegaPix with TC

Medium and Long term plans

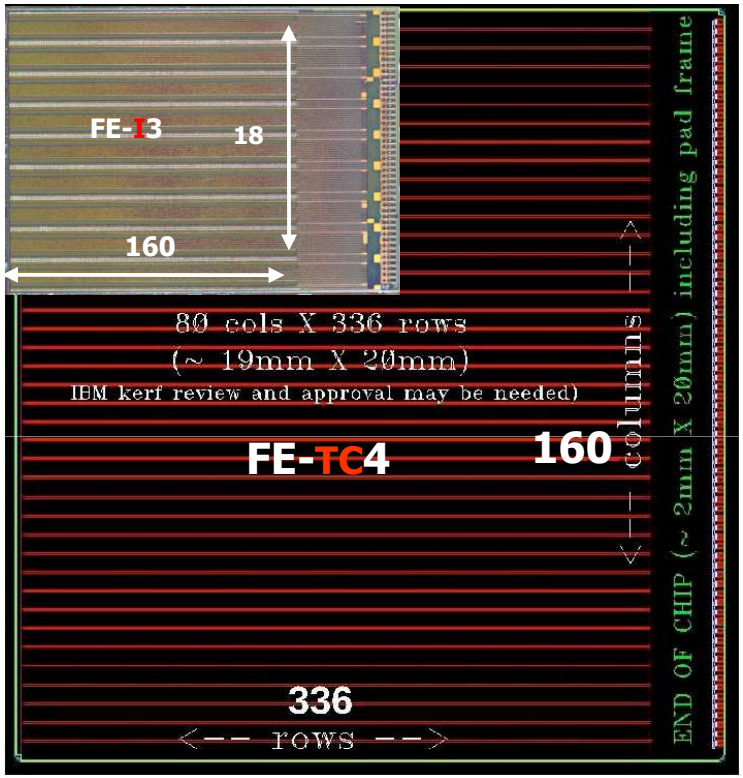
In case of positive 2011 tests: full chip FE-TC4-A submission in Tezzaron-Chartered MPW run

Pitch 50um x 125 um and very large matrix 336 x 80

FE-TC4-A with 19x20 mm will occupy 49% of Chartered reticule. Seems to be compatible with other HEP chips

Improve design for higher efficiency at SLHC luminosity 5 10^{34} $cm^{-2}sec^{-1}$ (clustering, buffers sizes, pixel pitches etc)

Further extension to higher density (90 nm, 65 nm) processes is very interesting in long term (more performance, functionality, compatibility Chartered/IBM)



Conclusions

• First test of analog pixels in high density 65 nm CMOS will be done soon. New approach of low power analog with performance compensated by complex digital processing.

- Basic Chartered transistors qualified for LHC
- Basic blocks of Chartered 130 nm CMOS pixels are radiation hard up to 400 Mrad
- Chartered DICE SEU tolerant latches pass now radiation and SEU tests
- We gained much better understanding of 3D chip design, need consolidation of PDK in only one version, one source and synchronization of verification tools with producers for next run
- Separate tiers tested already, first 3D electronics test in summer 2011
- FE-TC4 is the challenge to improve the physics performance of ATLAS at SLHC with 3D electronics technology

Special thanks

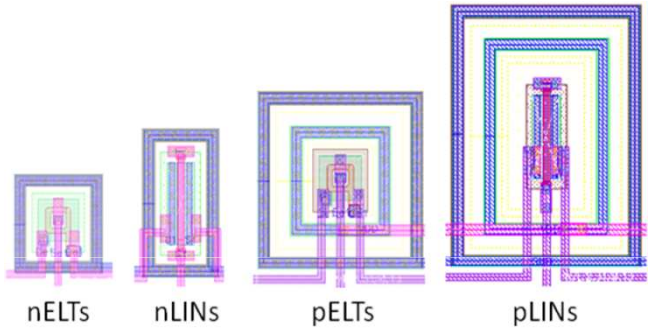
Maurice Glaser – support at CERN PS 24 GeV protons irradiation

Federico Faccio – support for CERN X-ray irradiation

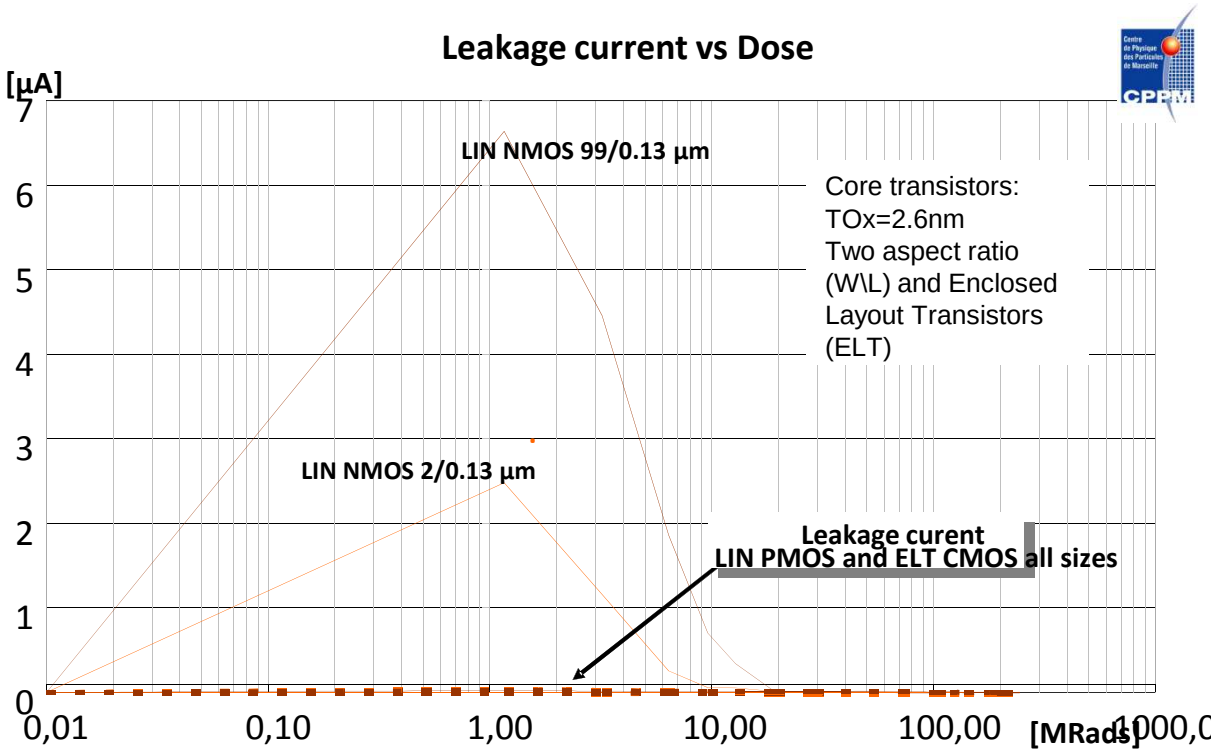
Spares

Radiation test of Chartered transistors

Test big(99.28/0.13µm) and small (2.31/0.13µm) transistors, PMOS and NMOS, linear and enclosed.



Gamma ray irradiations at CERN (high dose) and CPPM (low dose).



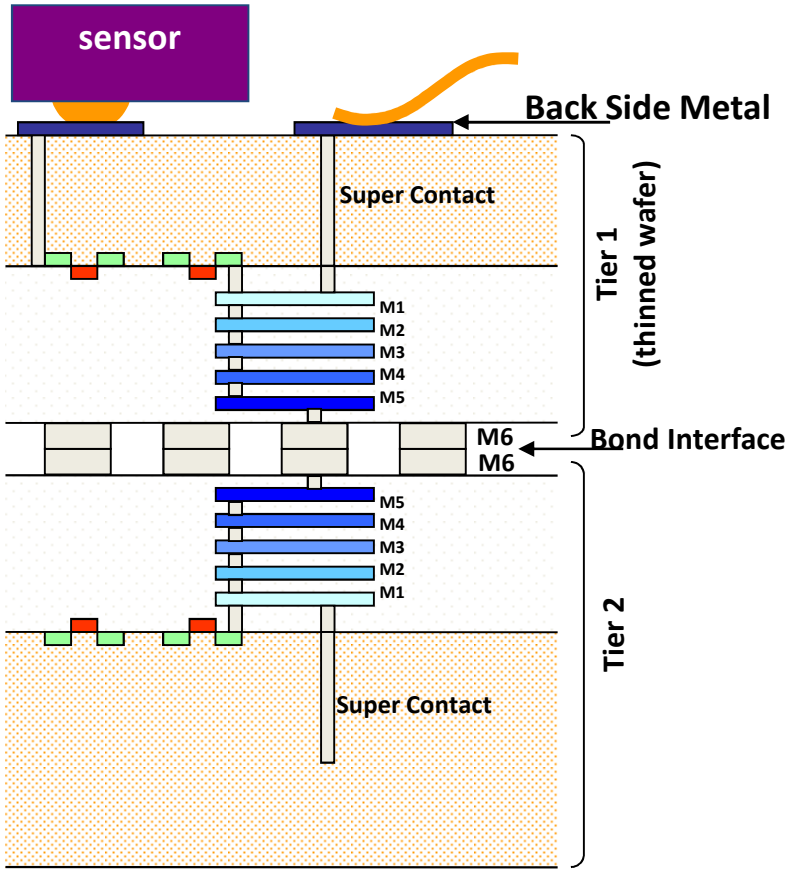
Tezzaron/Chartered 0.13 um Process

Large reticule – 25.76 mm x 30.26 mm

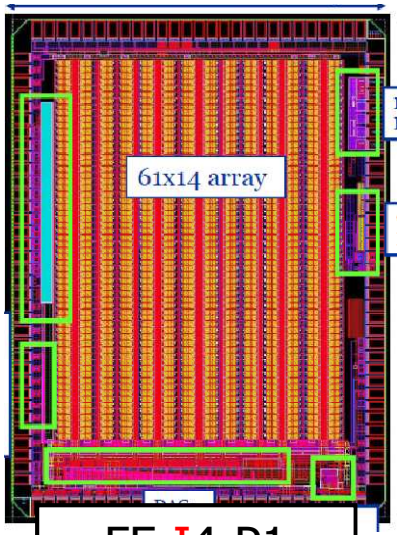
12 inch wafers

Features

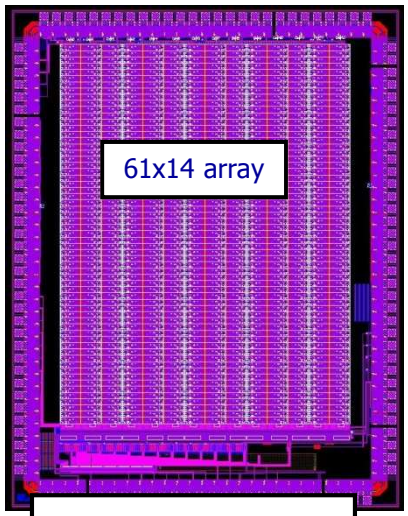
- Deep N-well,MiM capacitors – 1 fF/um^2
  - Single poly, 6 (8) levels of metal available, Zero Vt (Native NMOS) available, variety of transistor options (Nominal,Low voltage,High performance,Low power)
- Vias 1.6x1.6 x10um, pitch 3.2 um
- Bond points Cu 1.7x1.7 um, pitch 2.4 um
- Wafer bonding at 375 deg C
  - Alignment 3 sigma ~ 1 um
  - Missing bonds ~ 0.1 ppm
  - 1500 Temp cycling -65deg/+150deg on 100 devices without failures



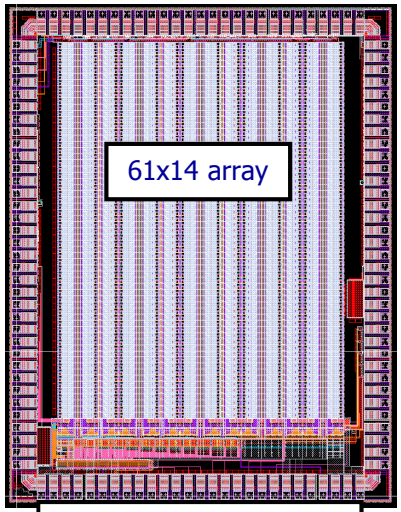
FE-X4-Pn gallery



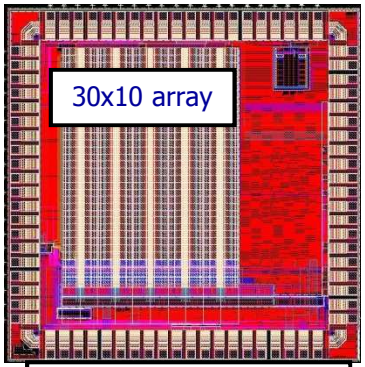
FE-I4-P1
4x3mm size
IBM 0.13µm LVT
8LM



FE-C4-P1
4x3mm size
CHRT 0.13µm LP
8LM



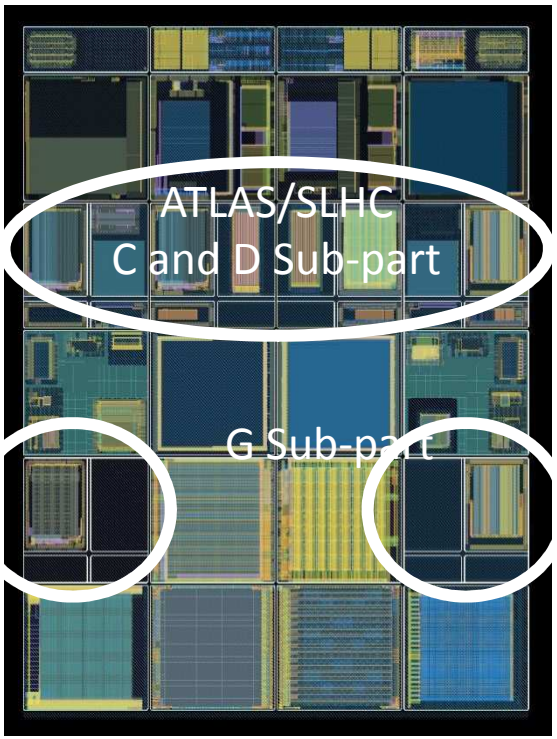
FE-C4-P2
4x3mm size
CHRT 0.13µm LP
8LM



FE-C4-P3
2.5x2.5mm size
CHRT 0.13µm LP
8LM

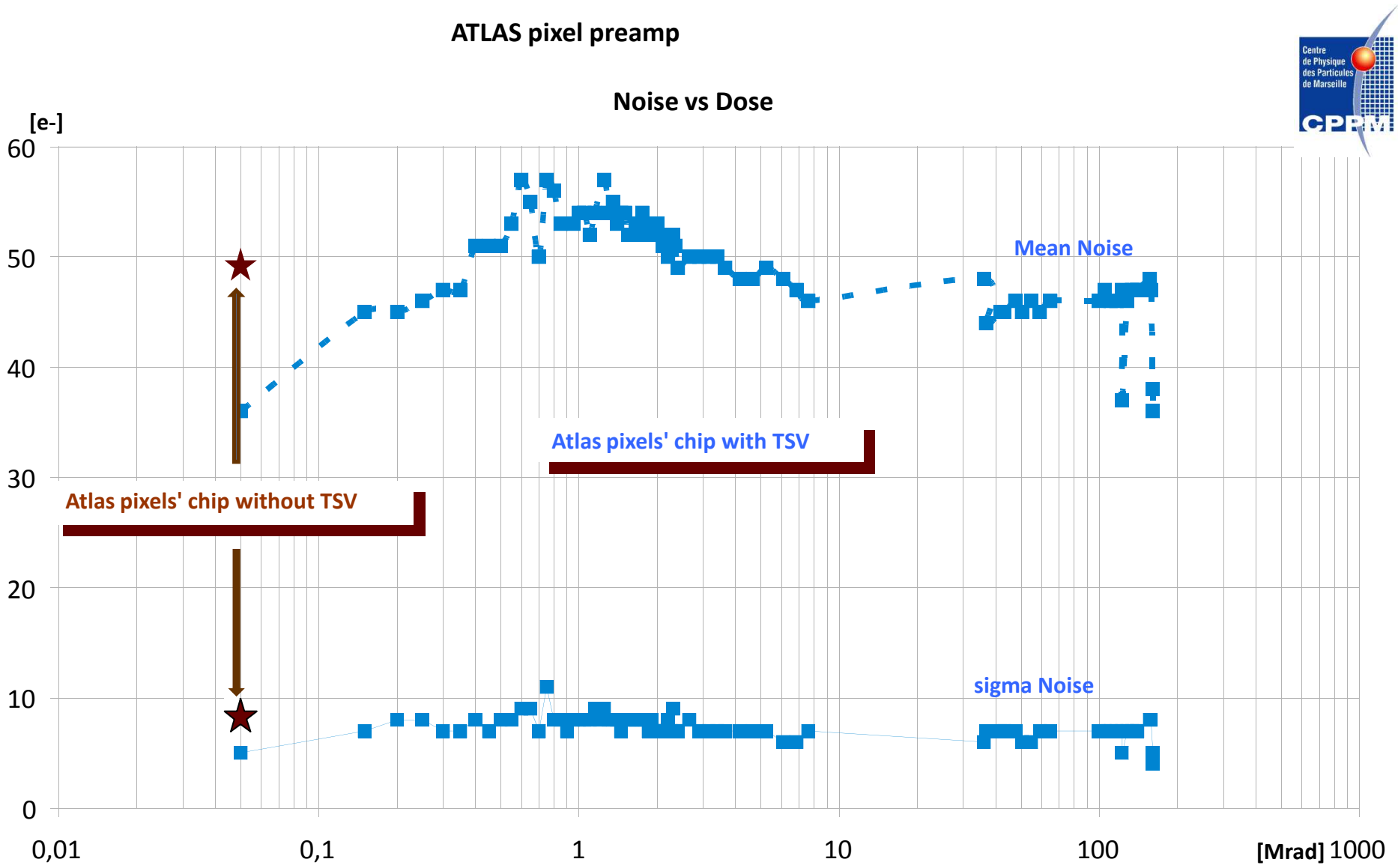
Fermilab 3D Multi-Project Run

- Fermilab organized a dedicated 3D multi project run using Tezzaron for HEP with submission in August 2009.
- 25 wafers from Chartered will be bonded by Tezzaron into 12 double wafers
- The wafers will be bonded face to face.



FNAL, Italy (Bergamo, Pavia, Perugia, Bologna, Pisa, Rome), France (Marseille, Strasbourg, Orsay, Saclay, Grenoble, Paris) +Bonn, LBNL

FE-TC4-AE X-ray irradiation

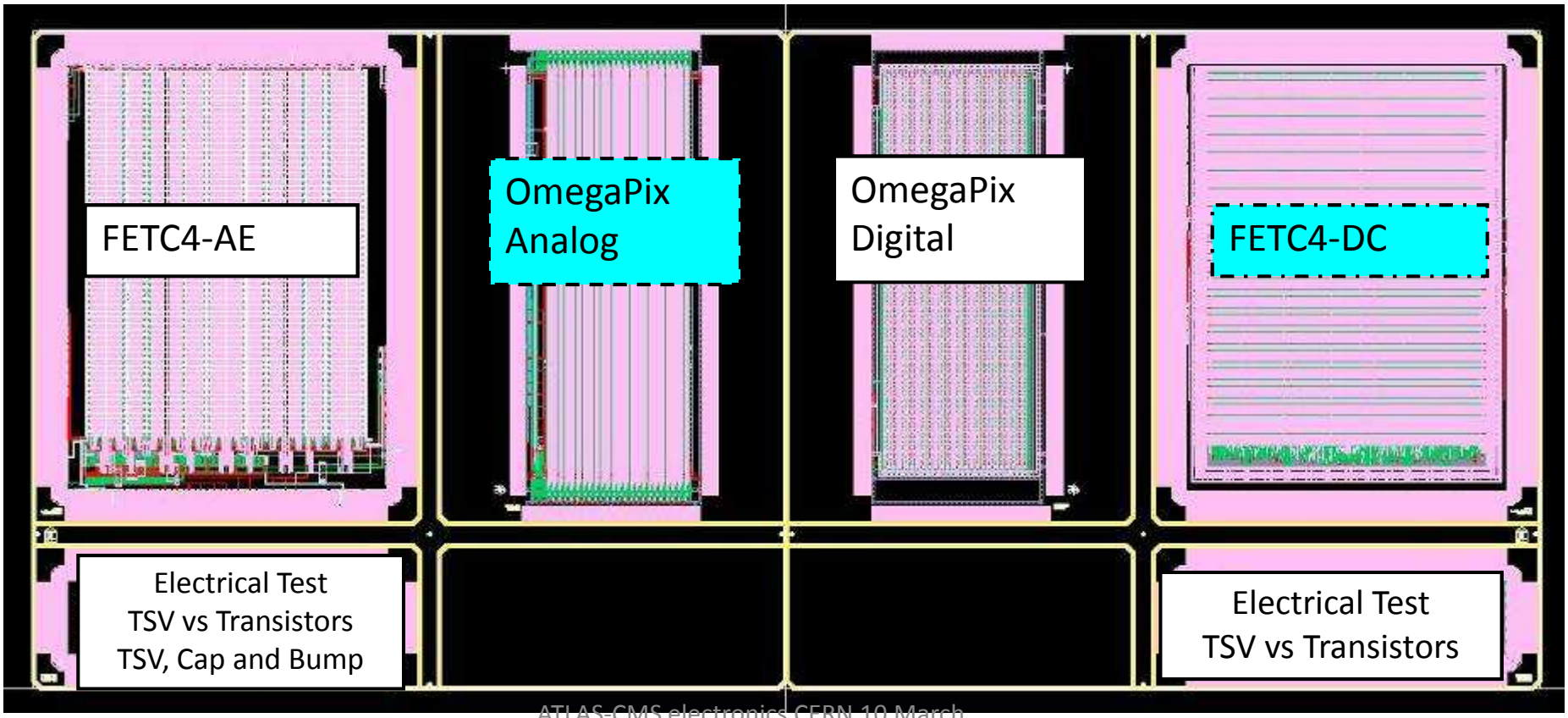


D-Band ATLAS

Exploratory OmegaPix chip (Orsay-Paris) with small pixel size 50x50 um, matrix of 24 columns x 64 rows

Goals: low threshold (1000 e), low noise 100 e) low consumption (3 uW/pixel)

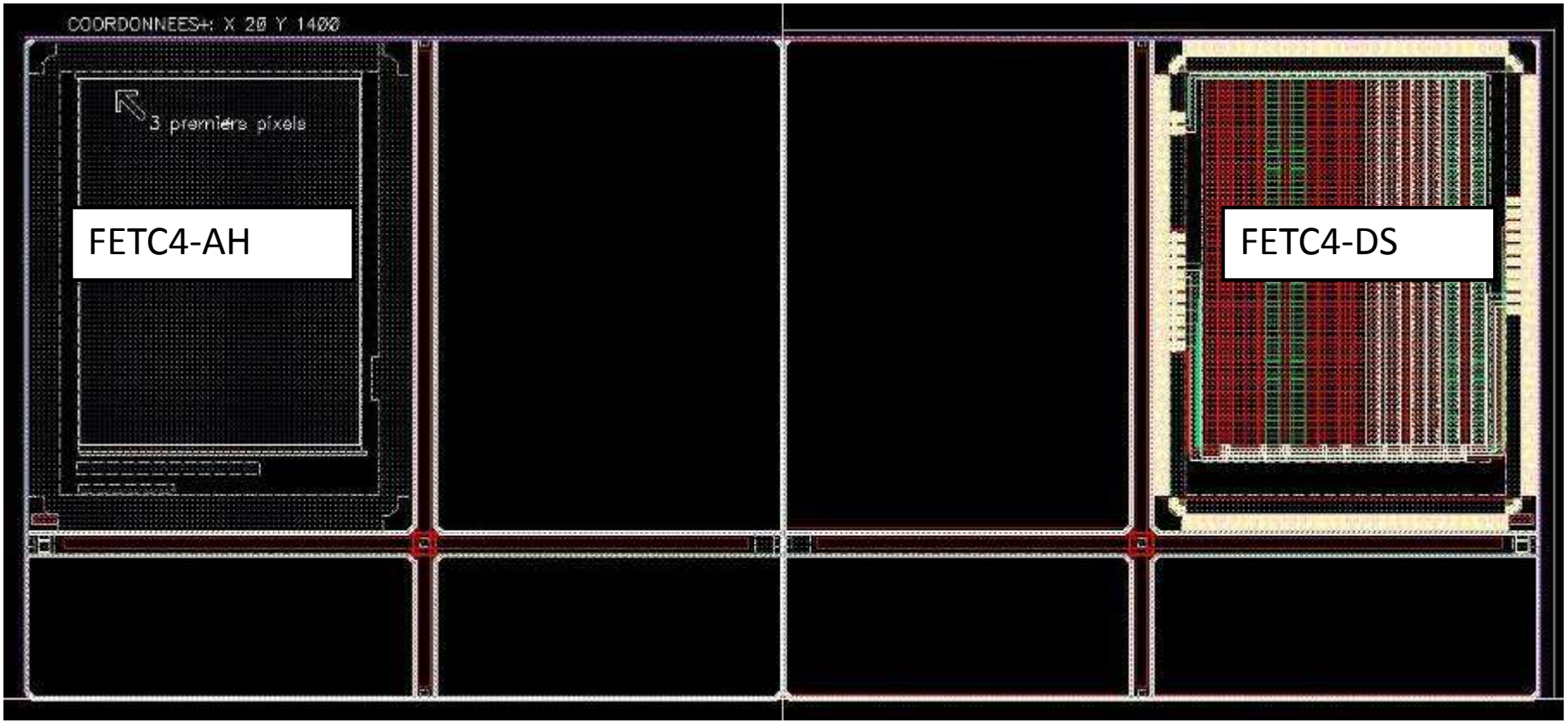
Reduced power voltage (1.2 V analog, 1.0 digital), feedback by parasitic capacitance



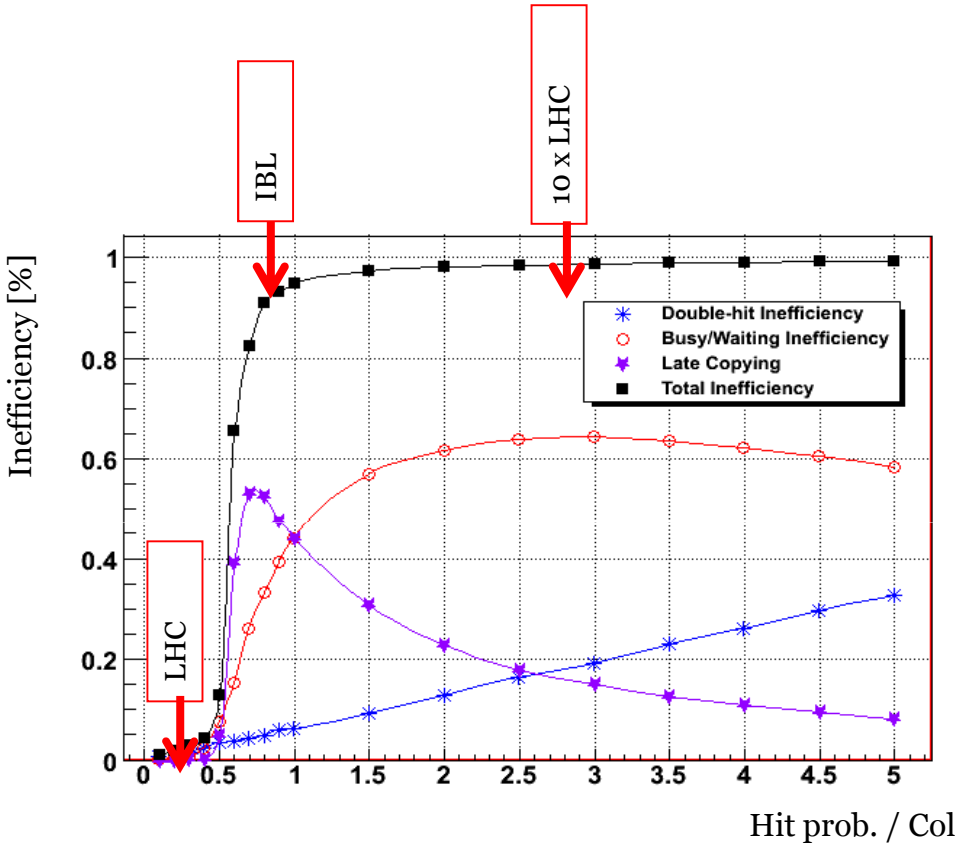
G-Band ATLAS

Design re-used by FNAL-CMS test SLHC chip with inverted polarity.

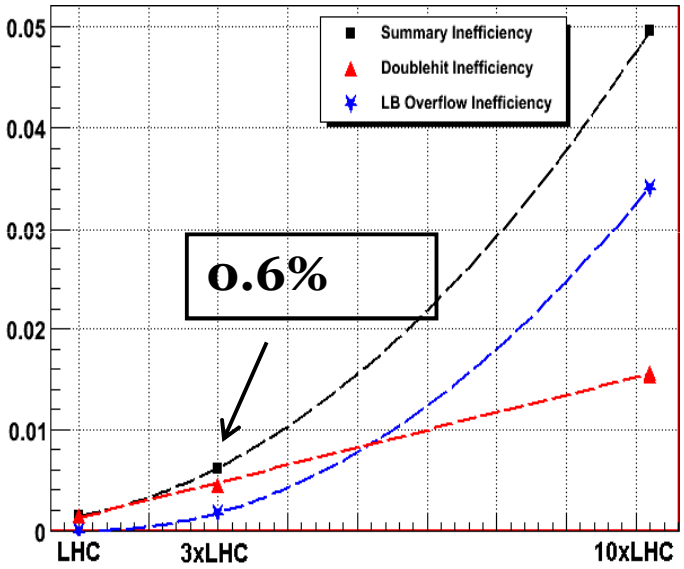
Very long waiting time due to numerous problems: difference in the DRC testing software used by designers and two producers, bugs in the software, misunderstanding of the design rules, change of the wafer layout for control marks by producer, too many fake DRC errors



FE efficiency



FE-I3 at r=3.7 cm



FE-I4 at r=3.7 cm

Mean ToT = 4

Organization of 3D electronics RD for SLHC

Workshop on 3D detectors LHC-ILC, Paris, 29-30 November 2007 by CNRS-IN2P3.

CPPM-IPHC-IRFU-LAL-Paris 3D collaboration formed, IN2P3 finance of 200K Euros (coordinator J.C.Clemens)

CPPM-LAL-Paris ANR “Vitesse” 3D RD (coordinator L.Abdenour)

3D will be part of Pixel FE electronics RD proposal

Vertical Integration Technologies for HEP, workshop, Ringberg castle, 6-9 April 2008, Max Plank institute (H.G.Moser)

ATLAS RD proposal for thin sensors with 3D integration was approved

3D collaboration organized by Fermilab (coordinator R.Yarema) through Tezzaron-Chartered

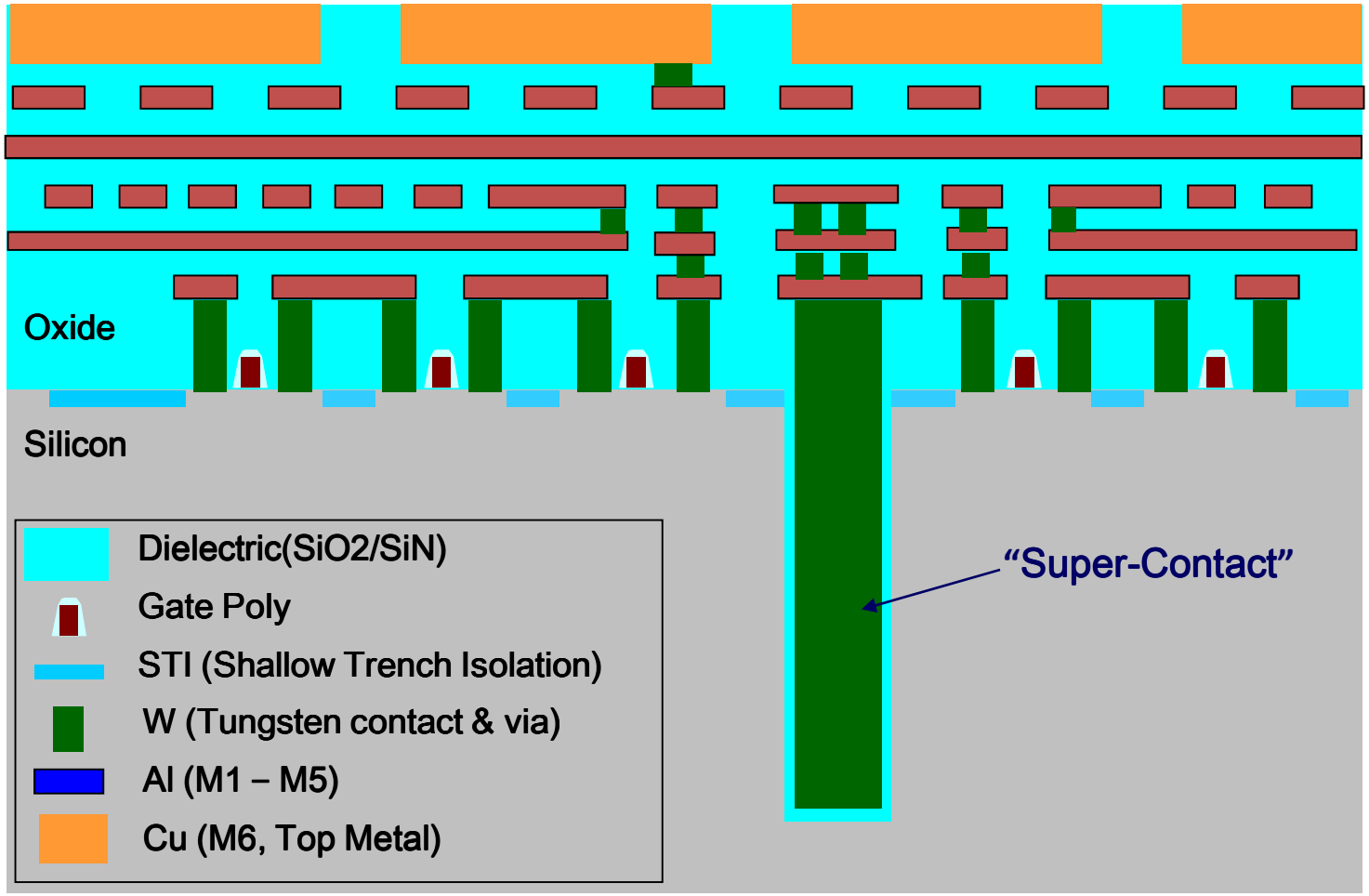
July 2009 submission of the first HEP 3D run, wafers expected in June 2010

March 2010 Workshop of the 3D consortium at CPPM, Marseille

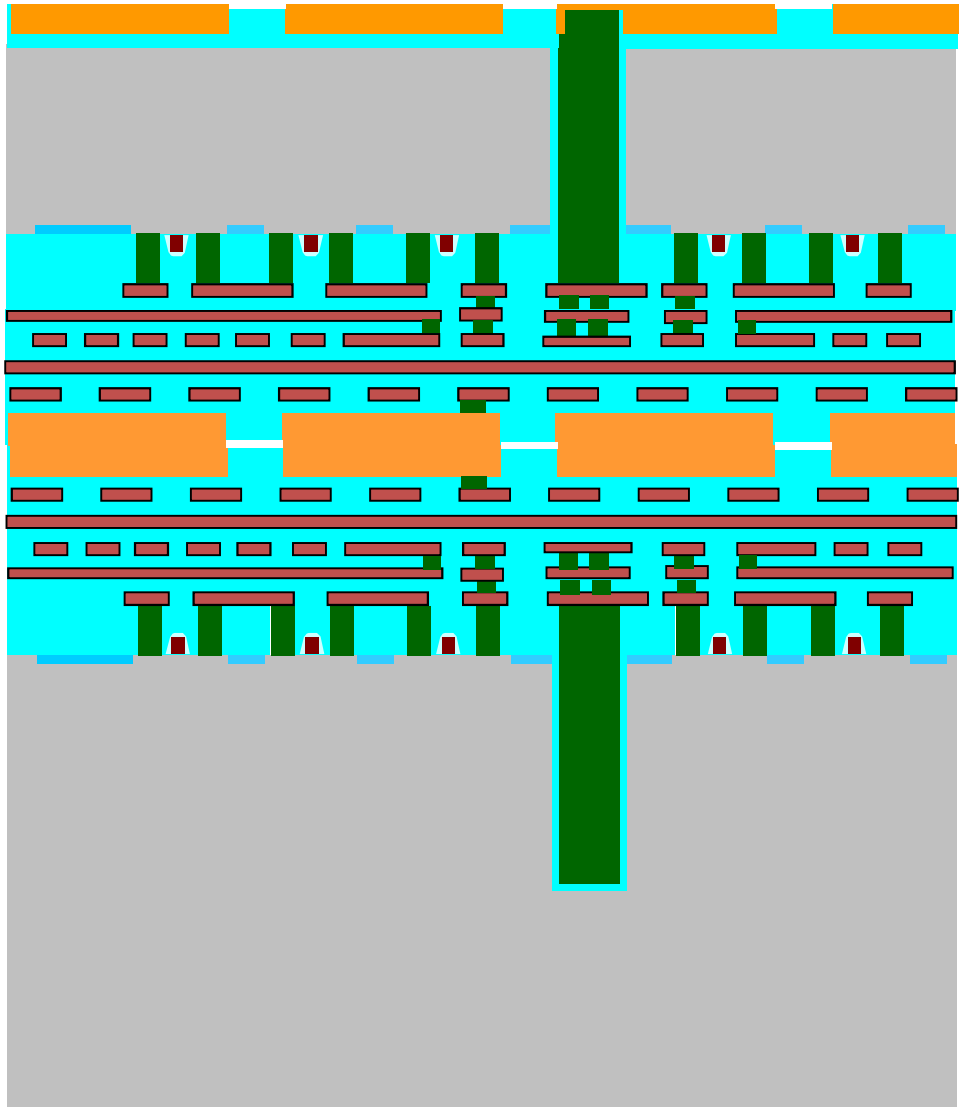
EU AIDA project with significant WP3 3D work-package

April 2011 expect first 3D wafers from Tezzaron-Chartered

A Closer Look at Wafer-Level Stacking



Next, Stack a Second Wafer Thin:



Chartered MPW runs

Test the basic properties of Chartered technology

Porting FE-I4-P1 (61x14 pixel array 50*166 µm , chip 3x4 mm) into Chartered FE-C4-P1 in January 2009 by Bonn-CPPM-LBNL collaboration,

Chips received in May 2009