A Full Slice Test Version of a Tentative Upgraded Readout System for TileCal

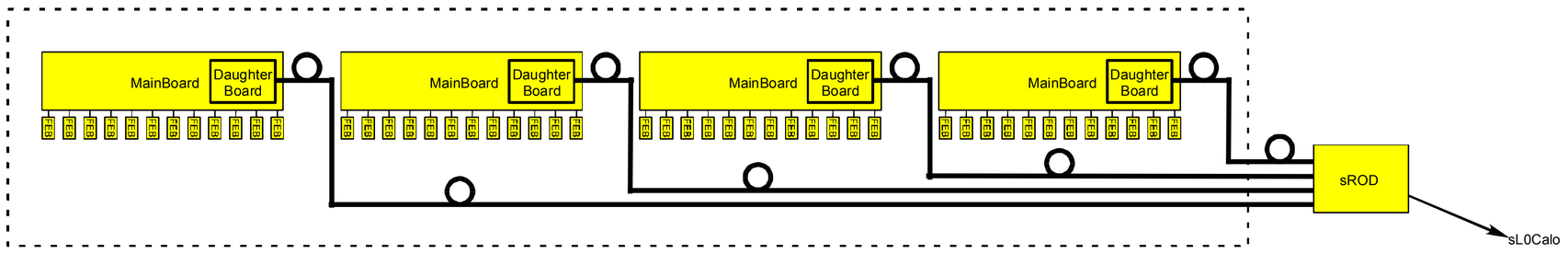
S. Muschter[a)], K. Anderson[b)], C. Bohm[a)], D. Eriksson[a)], H. Kavianipour[a)], M. Oreglia[b)] and F. Tang[b)]

[a)] Stockholm University

[b)] University of Chicago

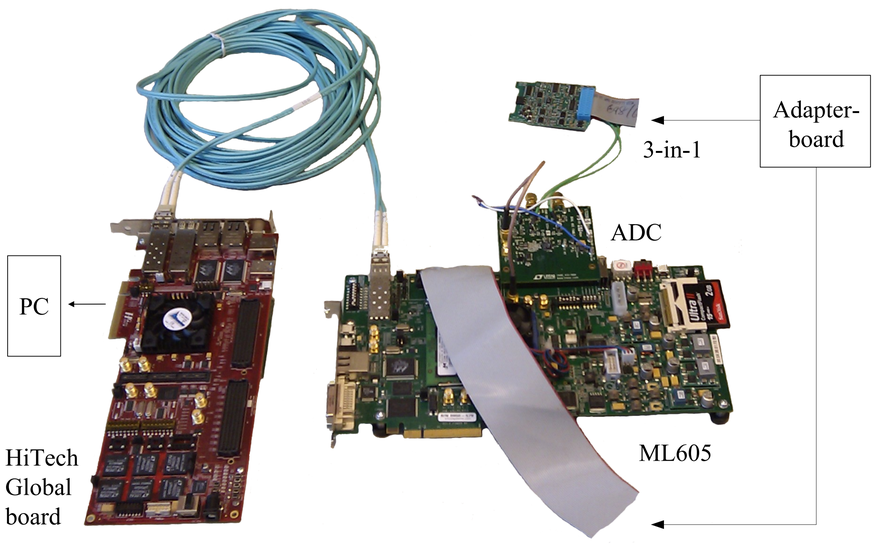
Introduction

The upgrade plans for the ATLAS hadronic calorimeter (TileCal) put high demands on the performance of the electronics. The full readout of all data requires higher bandwidth and the increased luminosity requires improved radiation tolerance. We have assembled a minimal TDAQ slice with the aim of implementing a tentative readout chain, starting with a newly developed analog front-end readout electronics board from University of Chicago (3-in-1 board) and ending with the storage of triggered data on a PC. With this setup we want to evaluate components and design aspects both separately and as a whole before final implementation in order to identify problematic areas as early as possible. Different parts in the slice will be replaced when more mature solutions are available. The aim is to have a working drawer ready for live testing in the detector by the end of 2012, during the phase 0 upgrade.



Test system

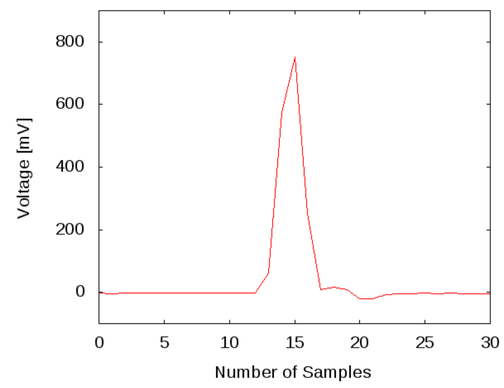
- The 3-in-1 board is used to generate well defined calibration pulses with user defined amplitude and frequency.
- The generated pulses are then sampled with the 12 bit LTC2264-12 ADC from Linear Technology.
- Both components are connected to a ML605 FPGA evaluation platform from Xilinx which is used for control, programming and readout of data to emulate the on-detector electronics.
- All sampled data from the ADC is sent via 100 m optical fiber to a PCIe FPGA evaluation platform from HiTech Global and finally stored on a PC.
- PCIe is used for communication between these two components to emulate the proposed ATCA standard for off-detector electronics.
- Data and control signals are transferred between the two evaluation platforms using optical communication at 5 Gb/s. Error correction capabilities and DC balancing are ensured by using the GBT-FPGA protocol.



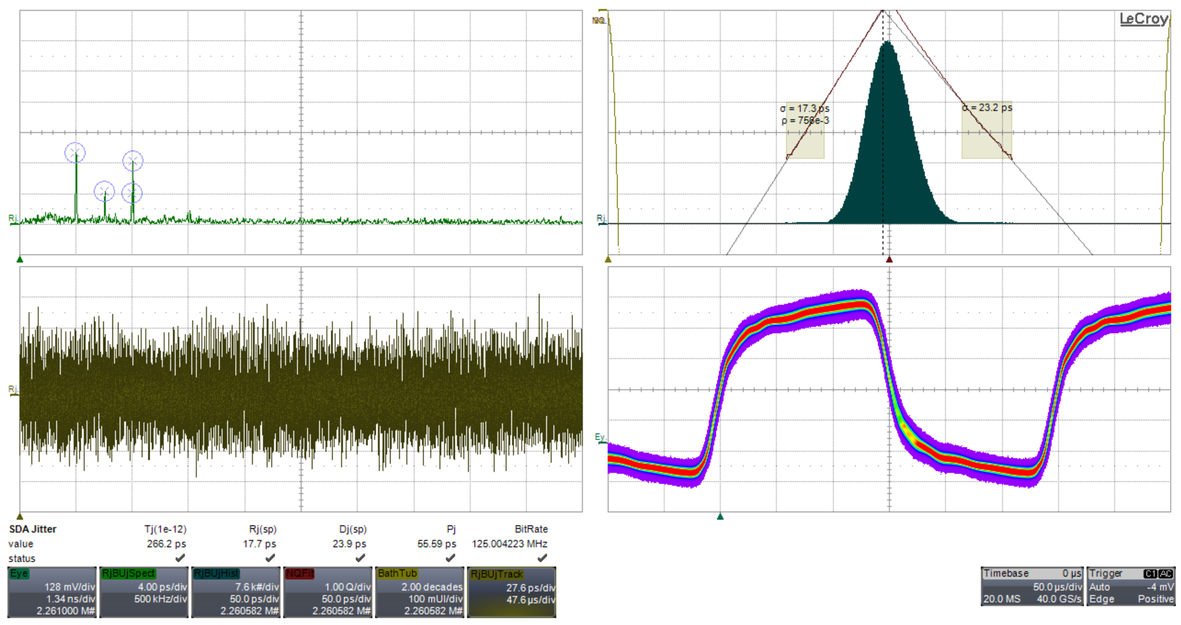
Test system for firmware and clock management

Results

- Using the test system we were able to record pulses like shown in the figure to the right.
- Data and control signals are processed using one global clock distributed from the off-detector electronics and recovered by the Virtex 6 Gigabit Transceivers (GTX).
- Preliminary measurements of the overall latency showed 56 bunch crossings corresponding to 55 bunch crossings calculated (off-detector →on-detector → off-detector).
- Jitter measurements of the recovered clock showed deterministic jitter of 26 ps matching the requirements for driving the GTX (30 ps for 5 Gb/s).



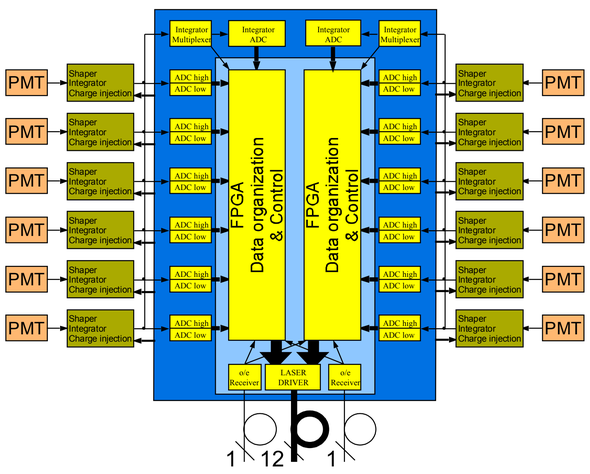
On the PC stored pulse



Jitter measurements of the recovered clock signal which is used to drive the GTX

Discussion

- The results are mostly what we expected but did not know as a fact. This will help to make the proper design choices when making layout of the prototype main board and daughter board.
- It was verified that it is possible to drive logic and GTX with the recovered clock signal extracted from one receiving GTX (recovered clock signal meets the requirements of the GTX) as we had expected.
- The jitter characteristics of the recovered clock signal are strongly depending on the clock management within the design and seem to be acceptable but need to be investigated more.



Tentative main- and daughter-board layout

Further Challenges

- Merge the current digitizer and motherboard design (giving 4 boards per drawer and 12 channels per board).
- The use of 12 bit ADC's will place strict demands on the PCB design not to worsen the 0.5 mV resolution.
- Separate the analog circuitry on the main-board from the high speed logic on the daughter-board.
- Implementation of different techniques to ensure sufficient radiation tolerance (error correction, triplication, …).
- Radiation tests with XILINX FPGA's
- A working drawer ready for live testing in the detector by the end of 2012