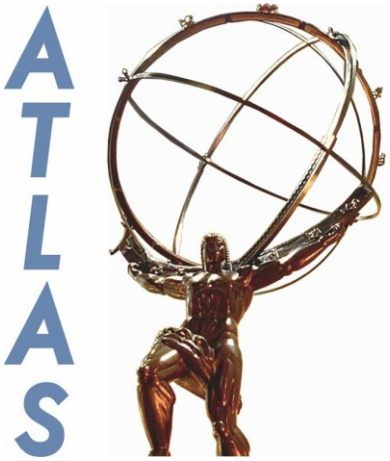


ATLAS Tracking Trigger

Matt Warren
on behalf of the ATLAS Upgrade community

ATLAS Upgrade is exploring L1 tracking trigger options

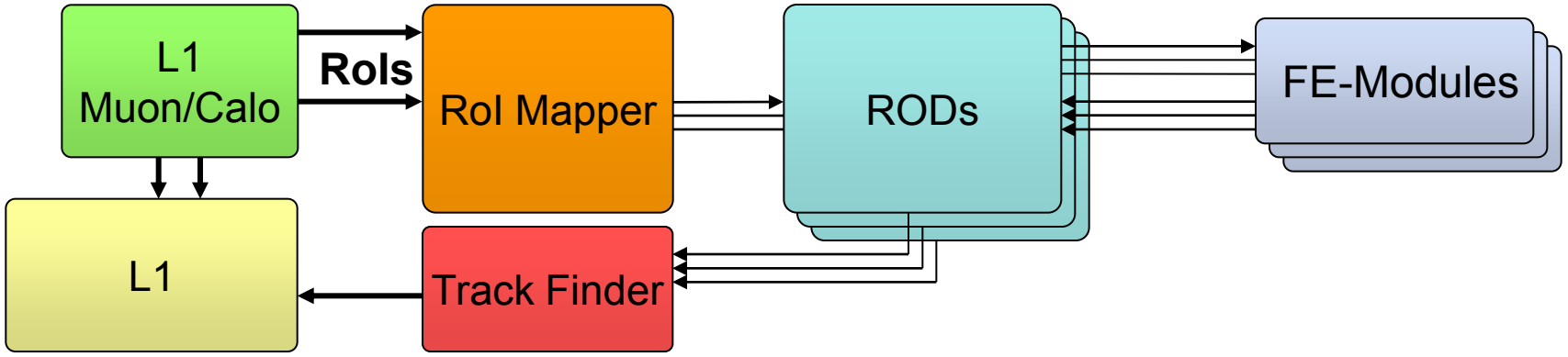
- Strips has been the main focus
- Simulation studies of L1 rates at high luminosities are ongoing
  - Will the upgraded L1 be able to cope?
  - What are the parameters for L1Track
  - Not discussed in this talk (see next ATLAS Upgrade Week)
- New trigger architectures under investigation
  - Regional readout - 2 stage trigger (Level-0/1)
  - Self-seeded trigger
- Some ideas are already in hardware designs
  - e.g. Strips ABC130

Regional Readout Concept

UCL

A portion of the tracker is readout prior to an L1 trigger

- Muon/Calo system identifies a region of interest (RoI)
- The RoI is mapped to set of front-end modules
- A Regional Readout Request (R3) is sent to these modules
- Modules send the regional data to Readout Drivers (ROD)
- The ROD forwards the data to the track finder
- Track finder contributes to L1 decision

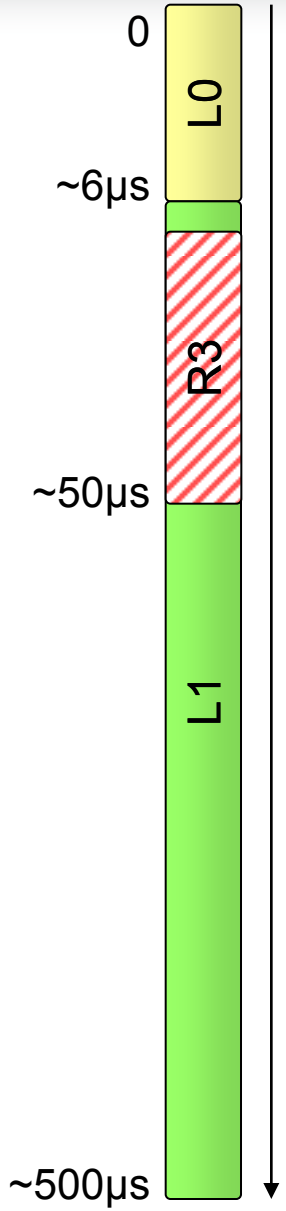


Regional Readout with L0 Buffer

UCL

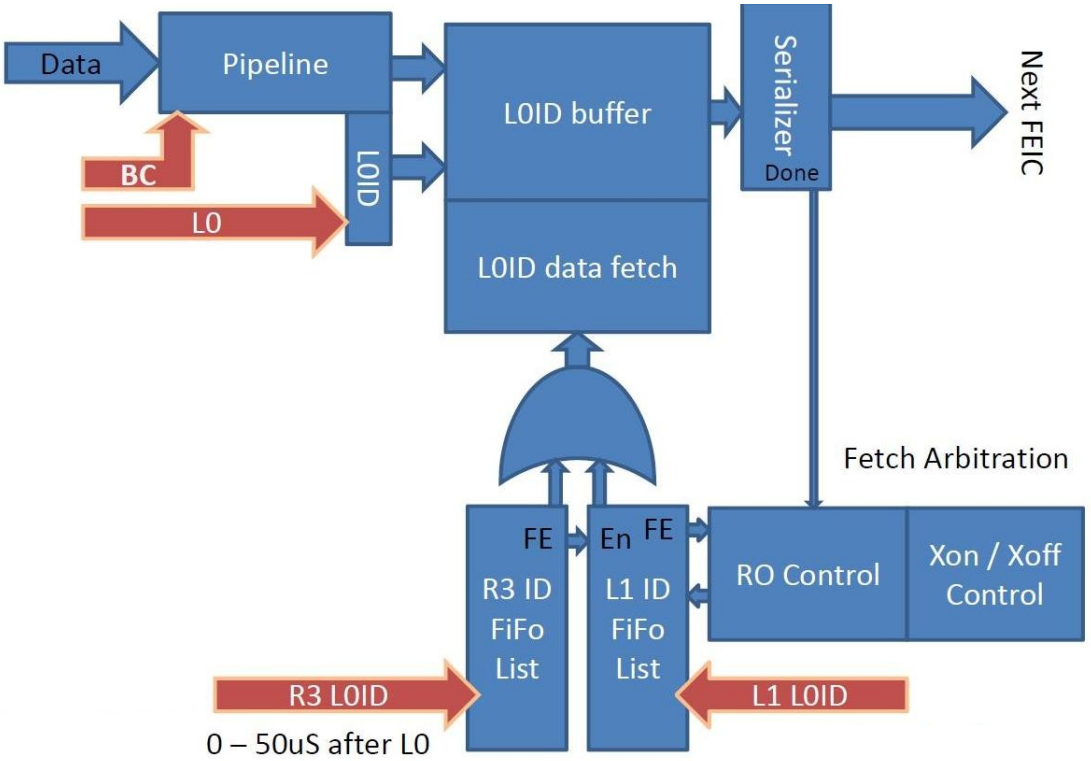
Level-0 + R3 used to reduce rate prior to L1:

- Level-0 (L0) trigger at 200-800kHz
  - Broadcast to all modules, synchronously
  - FEs transfer events from pipeline to a buffer
  - Latency ~6μs (assuming 256 deep pipeline)
- Regional Readout Request (R3)
  - Sent only to modules inside regions of interest
  - Expected that a module is in <10% of RoIs
  - R3 data expected 20-50μs after BC
- Level-1 (L1) trigger at 20-80 kHz
  - Track-finder helps reduce rate
  - Broadcast to all modules
  - Latency ~500μs (assuming 256 deep buffer)



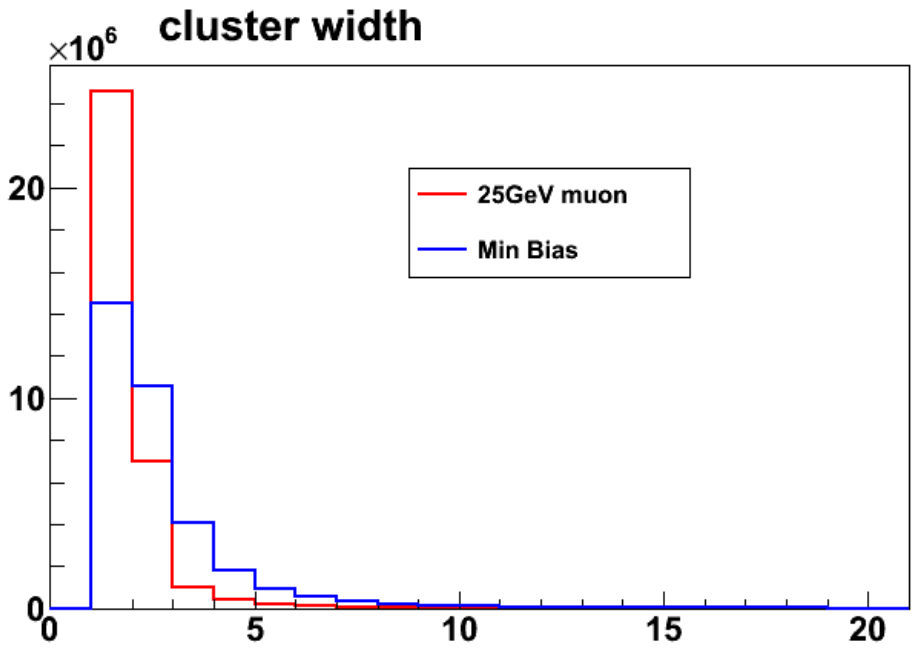
L0/R3 Implementation: ABC130

- New chip, in the design phase (based on ABCN)
- L0 collects event from pipeline, synchronously
- Event tagged/stored by "L0ID" in buffer memory
- R3 and L1 sent asynchronously
  - messages contain an L0ID that addresses event in buffer
- R3-data is prioritised over L1-data (& data-reduced differently)



Tracking data (for strips) need not be full event

- Data reduction prior to sending from module
  - Only using <3 strip clusters (high-pT tracks)
    - Do not, however, suppress fakes from multiple scattering
  - Send central strip only
- Cap number of clusters/chip
  - Send ~2/chip, report total
  - <5% of 'good' hits lost



Challenges for L0/R3 Concept

UCL

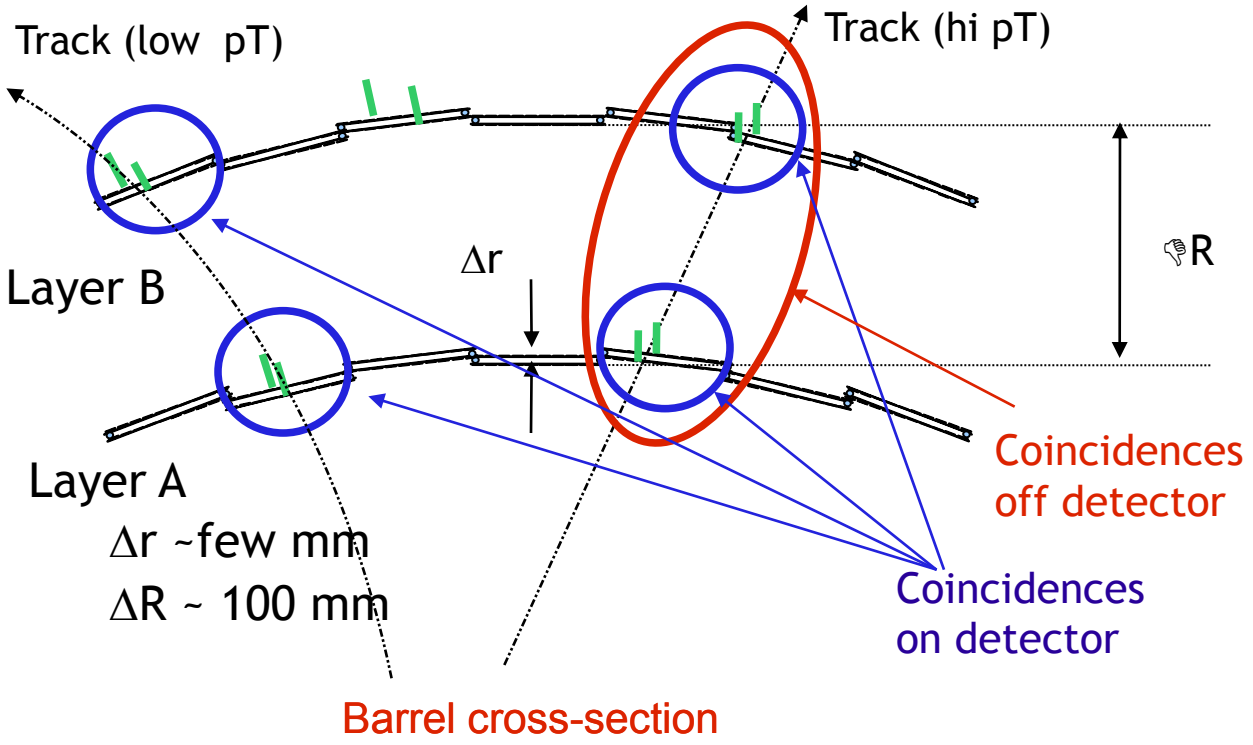
- The current ATLAS design is too restrictive
  - 128 deep pipelines/100m cable = little spare latency
  - High rate triggers (>100kHz) can mostly not be accommodated

= New FE electronics may be needed for entire ATLAS!

  - Many sub-detectors are already planning a change
  - Most are capable

Self-Seeded Track Trigger

- Tracking contributes to the L1 decision without seeding from Calo/Muons.
- A number of strip layers are equipped with trigger functionality to give an efficient trigger with built in redundancy



Self-Seeded Readout

UCL

Bandwidth is the big issue (raw data = ~200Gb/module/BC)

Need to apply multiple bandwidth reduction techniques:

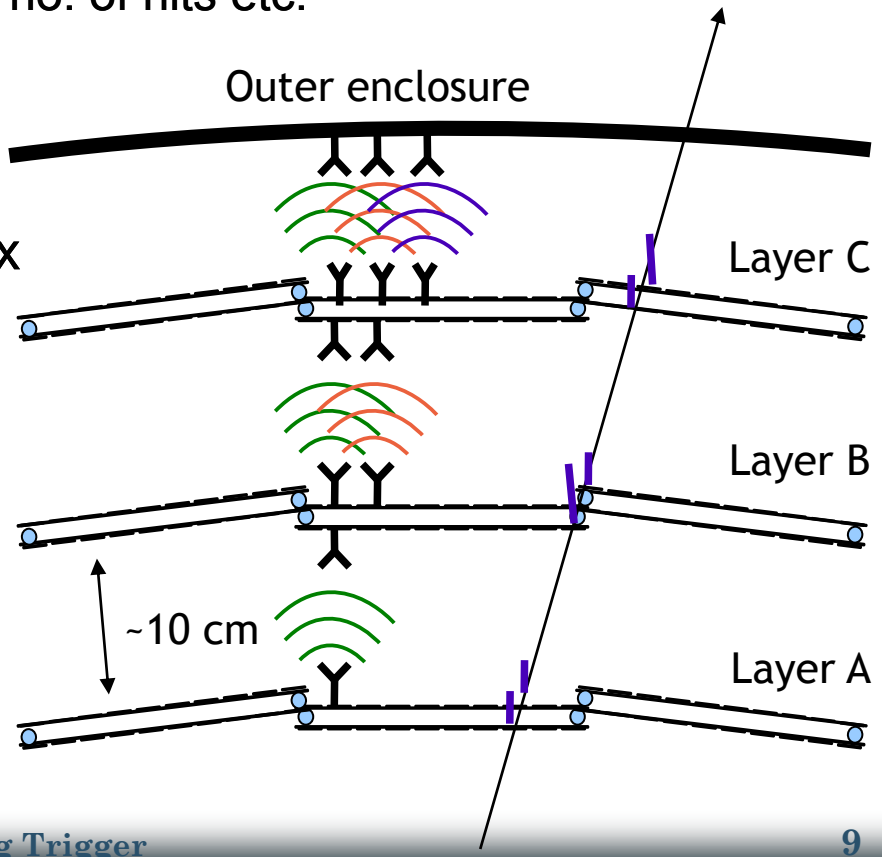
- Co-incidence between module sides reduces rate
  - Needs modified strip modules but only minor impact on material budget
- Compress using similar techniques to regional readout
  - Small clusters only, central strip, max no. of hits etc.
- ~~Local track-finding across layers~~
  - ~~Still need fast links, so no benefit~~

Readout links need to be faster – 10-100x more than current strips design

- Micro-coax?
- Intra-layer optical/wireless

Track-finding performed fast off detector

- Make use of next generation CAMs (commercial or custom)



Challenges for Self-Seeded

UCL

- 3.2 μs trigger latency
  - Cabling + CTP leaves 800ns window
  - Need low latency data links
  - Need largely parallel track-finder
- Readout bandwidth
  - Need very fast data links
  - R&D on low mass, low power link technology required
- Changes to geometry
  - Ideally change module angle and layer spacing
    - Improved pattern matching efficiency
    - Reduce fakes
- Impact on the rest of ATLAS
  - Material
  - Less stereo layers affects offline

Conclusion

UCL

- Regional readout looks to be technically feasible
  - Strips are incorporation a version into their FE design
  - BUT requires changing all FE electronics in ATLAS
  - Unclear how to deal with inaccessible components
- Self-seeding is attractive, but needs more work
  - We can keep existing pipelines, L1 architecture
  - BUT no technical solution for high-BW is yet available

- Background information for Self-Seeded option:

Coping with a trigger latency of 3.2 μs

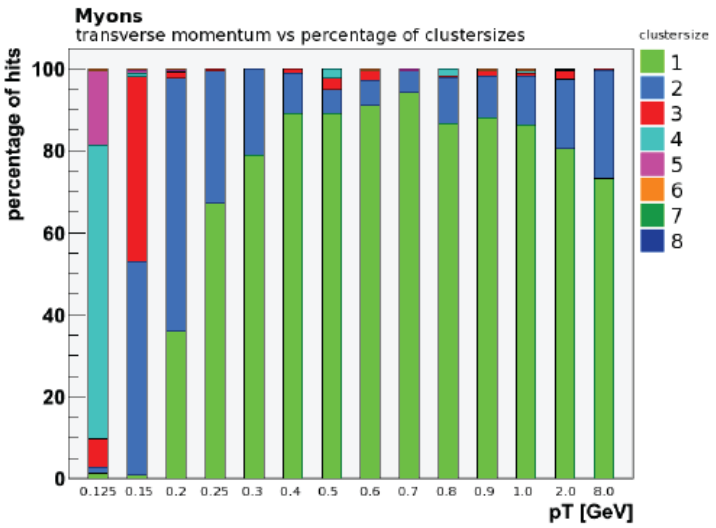
- Main contribution to trigger latency
- On detector data reduction
  - To be done real-time at 40 MHz → 25 ns
- Transfer of on-detector data to off-detector trigger hardware
  - Data to be read out at 40 MHz, link capacity has however to be scaled to data rate → 25 ns
- Pattern matching off-detector using Content Addressable Memory/Associative Memory technology (used in FTK)
  - Input to chip < 100 ns
  - Search and output < 50 ns
  - Interfaces (receiver, driver, demultiplexer, Tag RAM etc) < 150 ns
- Cable/link length between tracker and trigger processors
  - Rough estimate 500 ns

- Cumulative sum so far: **< 850 ns** (+ some relatively small transition delays)
- **Of the 3.2 μs, time need also to be reserved for the CTP and TTC → data from tracker has to be at the CPT within ~1600 ns**

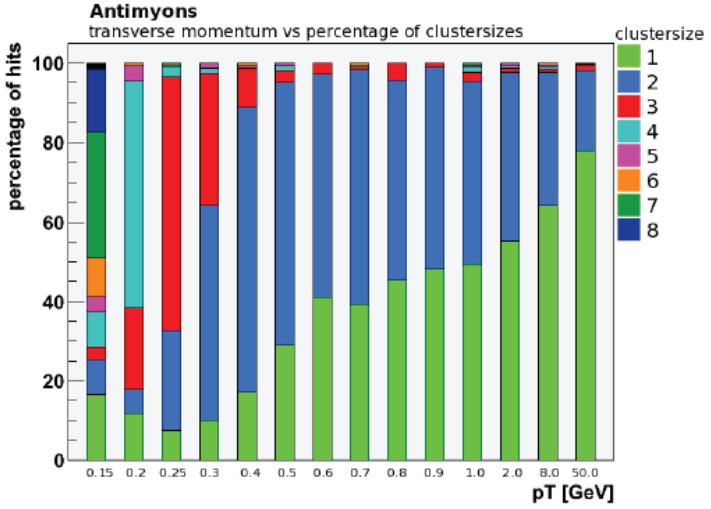
- **A very rough calculation but gives some hope that the latency can be met. The challenge is in technology for signal processing and readout. (more about this later)**

Impact on geometry layout

- Charge symmetry
  - The trigger performance for positive and negative particles should be equal → cluster width should be equal for both charges → present tilt in layout not optimal and change will probably improve offline performance as well

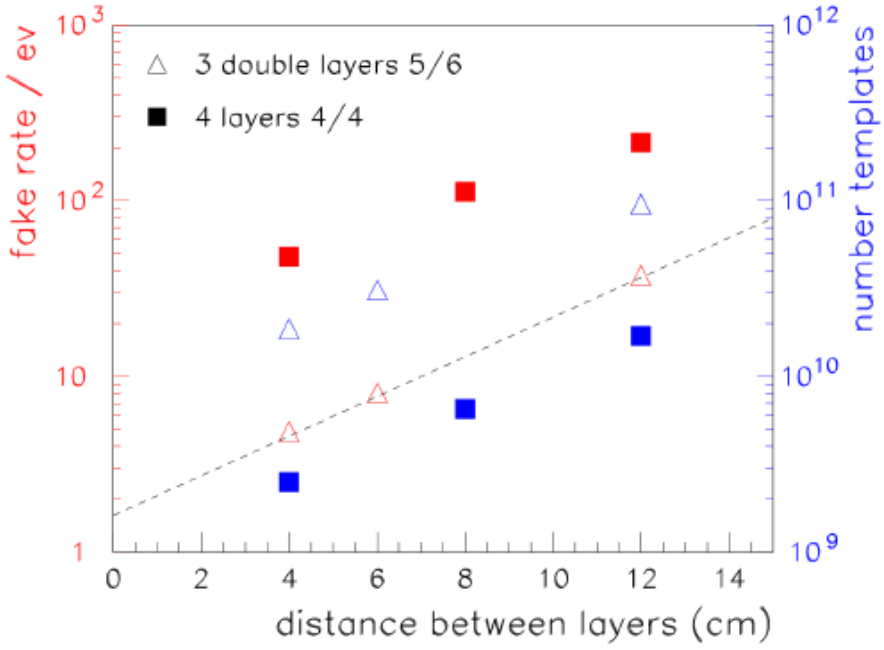


- Removal of z-coordinate in trigger layers
  - If data reduction with doublet layers is done then the z-coordinate will be lost → impact on offline to be studies



Impact on geometry layout (cont)

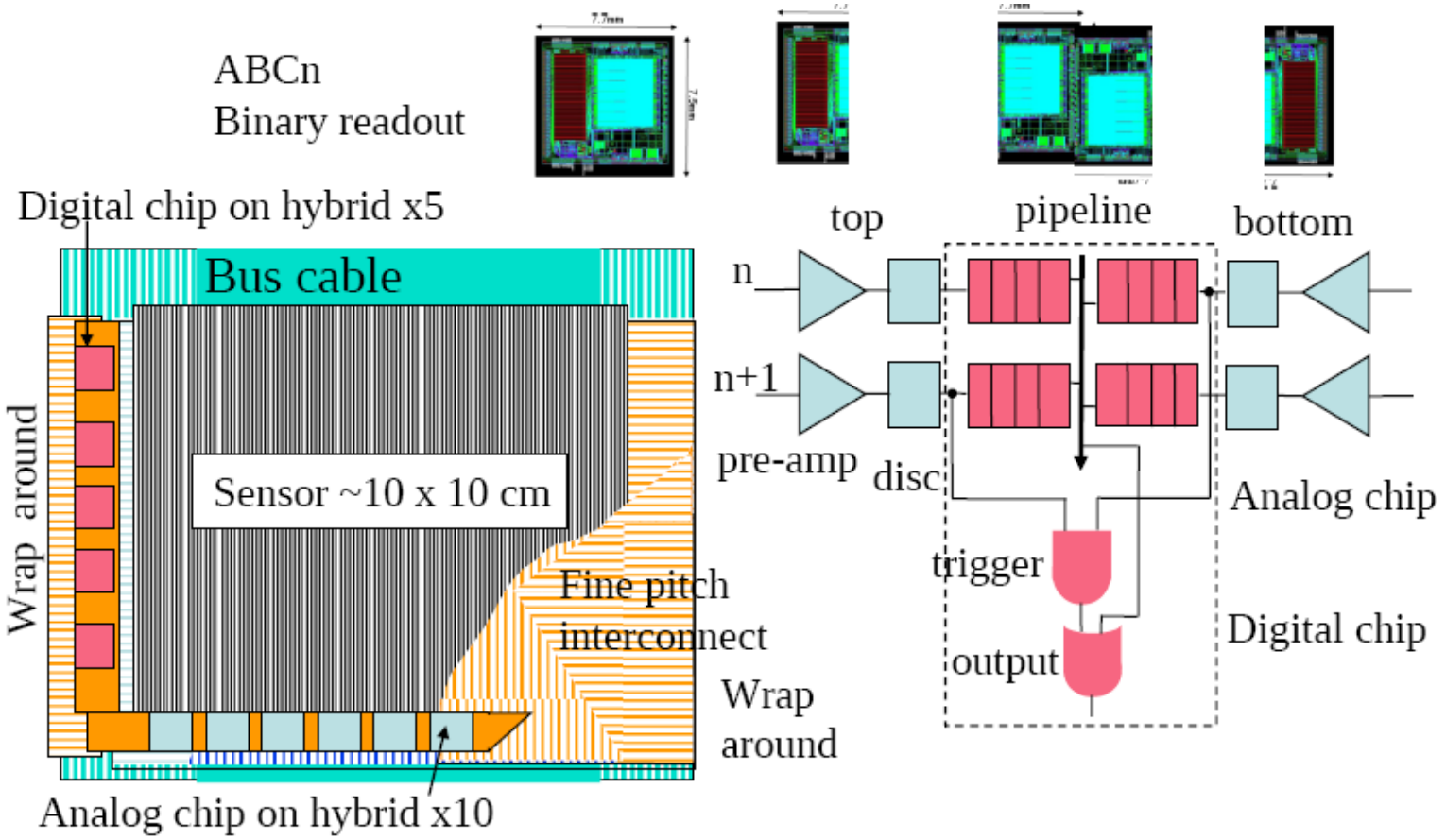
- Distance between trigger layers (short strip) should be made slightly shorter than in present layout to reduce size of pattern bank and to reduce fake rate → study impact on offline (expected to be small)



- Instrumentation of trigger in End-Cap
  - Not studied in ATLAS but we keep on eye on CMS ;-)

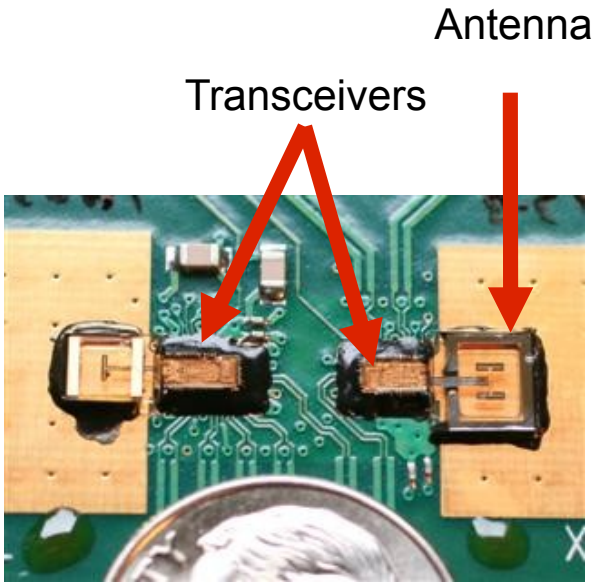
Split chip approach for Triggering

- Split the readout chip and add an embedded fine pitch interconnection. Analogue part near sensor to minimize noise, digital separated and connected top-bottom for coincidence logic.



Readout links

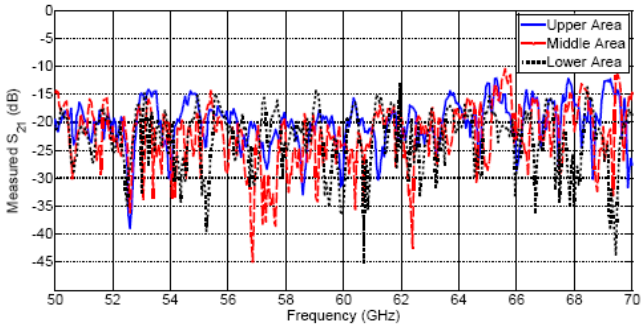
- The ID modules drive data on LVDS at 160 Mbps to the end of barrel/disk and from there data is transferred over Gbps optical links
  - Bandwidth has to increase by x10-20 to accommodate L1 trigger → more links or higher speed
- Wireless data transmission with mm-wave is a rapidly developing technology
  - Low power
  - Cheap components available for prototyping
  - Gbps capacity
  - Passive antennas (no fragile optical components) BUT needs free line of sight



RX/TX chipset (MSK modulation) with antennas with 2 Gbps capability (by IBM)

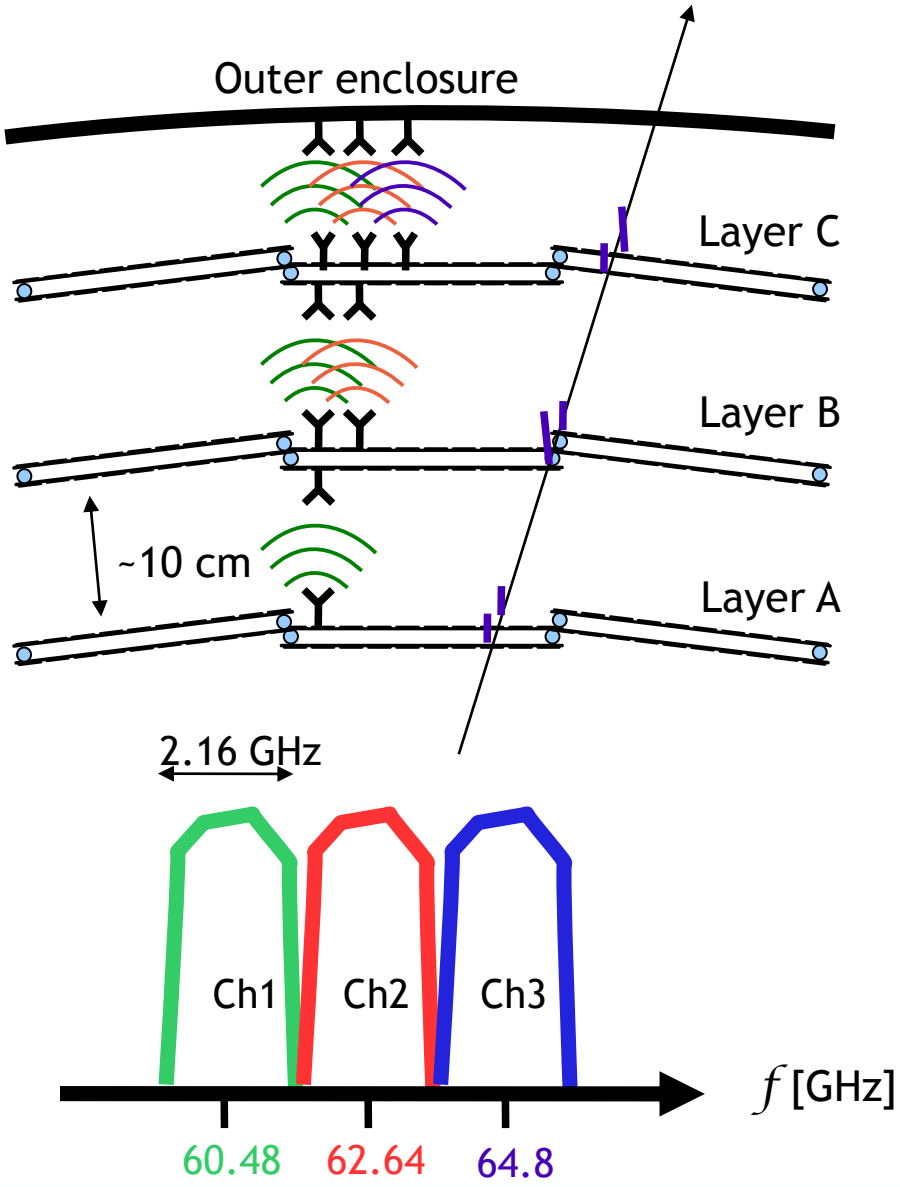
Simplified Wireless Idea

- All complicated trigger/pattern logic moved off-module → simple implementation on module
- Short distances if data transferred radially. It is however not possible to transfer 60GHz radially data trough silicon layers



Transmission test through a silicon module

- Solution: signal from inside is forwarded unchanged through layer by repeater electronics



Network Search Engine (CAM)

Netlite Series (Netlogics)

- Knowledge based processor (like CAM)
- Input Bandwidth ~ 40 Gbits/s (unencoded data)
- about 10000 units needed (bachelor thesis D.Glodeck, Heidelberg)
- timing studies (dipl. student Robert Weiler)

- checked data specs (NL6000, 7000, 9000)
- checked Verilog simulation (NL 9000)
- check soon hardware NL 9000 (delivery this week)

	latency standard speed	high speed	frequency standard speed	high speed	result rate standard speed	high speed	memory size	
NL6000	71 ns	54 ns	266 Mhz	500 Mhz	33 Mhz	62.5 Mhz	512k x 72 bit	32k x 576 bit
NL7000	71 ns	54 ns	266 Mhz	500 Mhz	33 Mhz	62.5 Mhz	1024k x 72 bit	64k x 576 bit
NL9000	156 ns	195 ns	(300/300) Mhz	(400/200) Mhz	75 Mhz	100 Mhz	512k x 80 bit	64k x 640 bit

~100k pattern

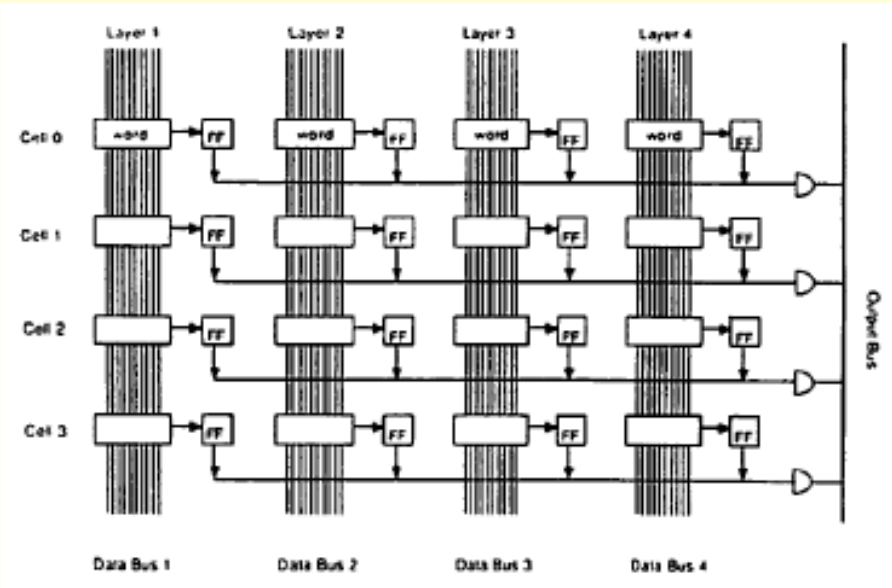
latency of search: ~ 50-150ns
plus interfaces 150 ns (my guess)

New AMchip (FTK)

AMchip 2014-2016 for FTK

- 180 nm → 65 nm
- fewer layers
- full custom cell
- larger chip
- 5000 → 120000 patterns

New! variable pattern size (TSP)
(effectively factor 10!!!)



Clock speed: 50 → 100 MHz (2.5 hits / layer / BC)

- need ~ 4 parallel processing chips

(process up to 10 hits per layer / BC)

Projections:

- year 2016: 2.5D chip (factor ≥2 pattern)
- year 2016: 45nm? (factor 2 patterm)
- 2-4 million effective patterns/chip!
- latency determined by input speed **~150 ns**