LHCb electronics upgrade

Upgrade plan
Architecture
Review of R&D

On behalf of all the LHCb sub-systems

LHCb upgrade plan

At L = 2 x 10^{32} $cm^{-2}s^{-1}$, beyond 5 years running, statistics don't improve

Big statistical improvement if:

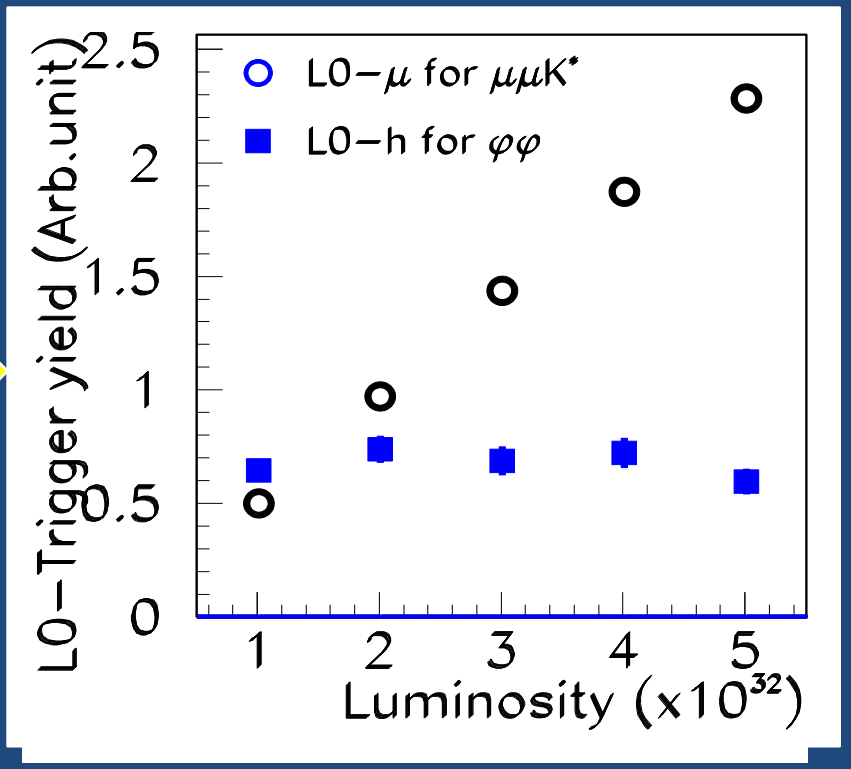
- **increase L to 1 x 10^{33}, AND**
- **improve efficiency of trigger algorithms**

BUT ..... current L0 trigger:

rate & latency limited by electronics

BUT.... efficient trigger decisions require:

- **long latencies**
- **computing power**
- **data from many (all) sub-detectors (momentum, impact parameter .....)**



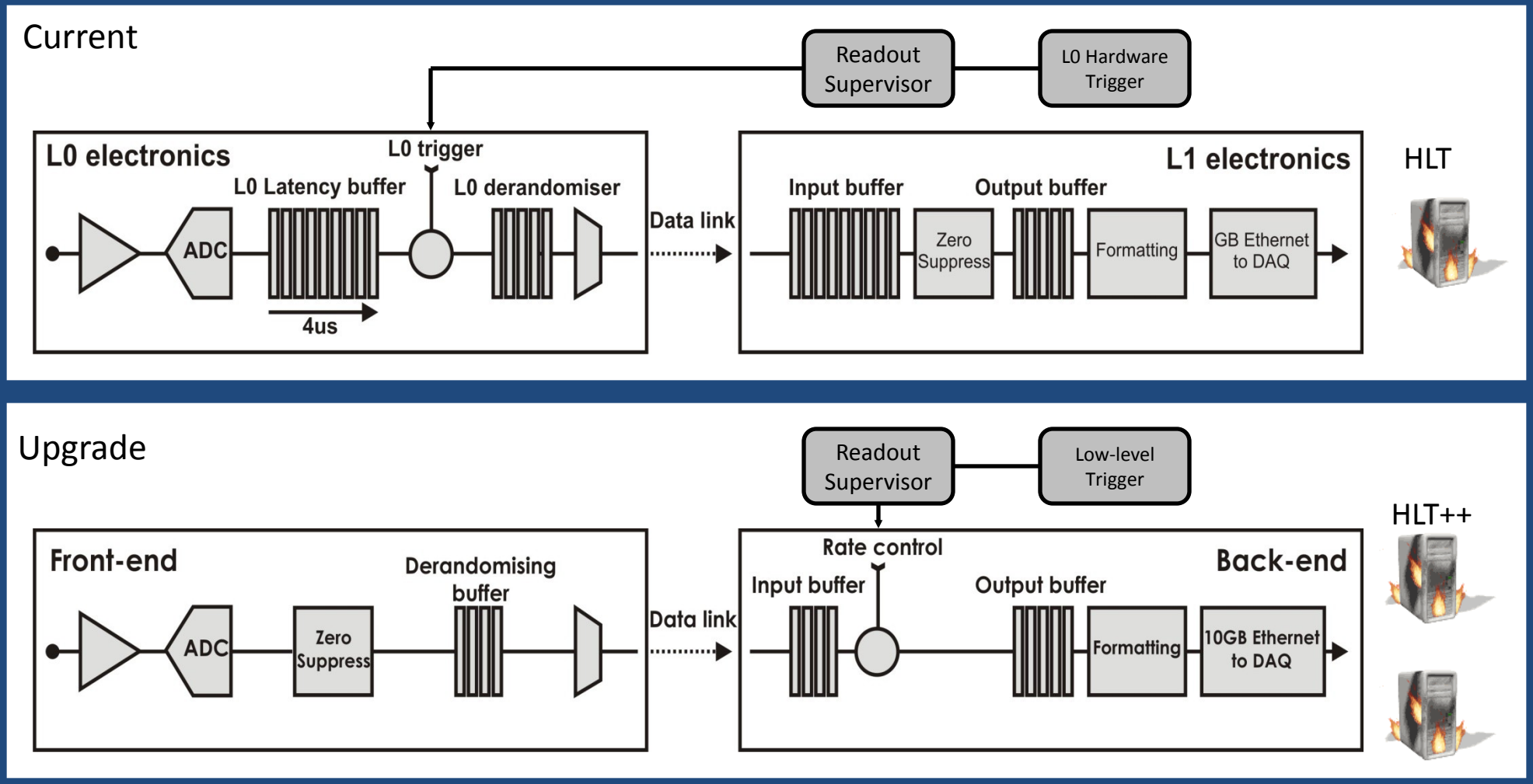
⇒ **upgrade electronics + DAQ architecture ~ 2018**

LHCC-2008-007

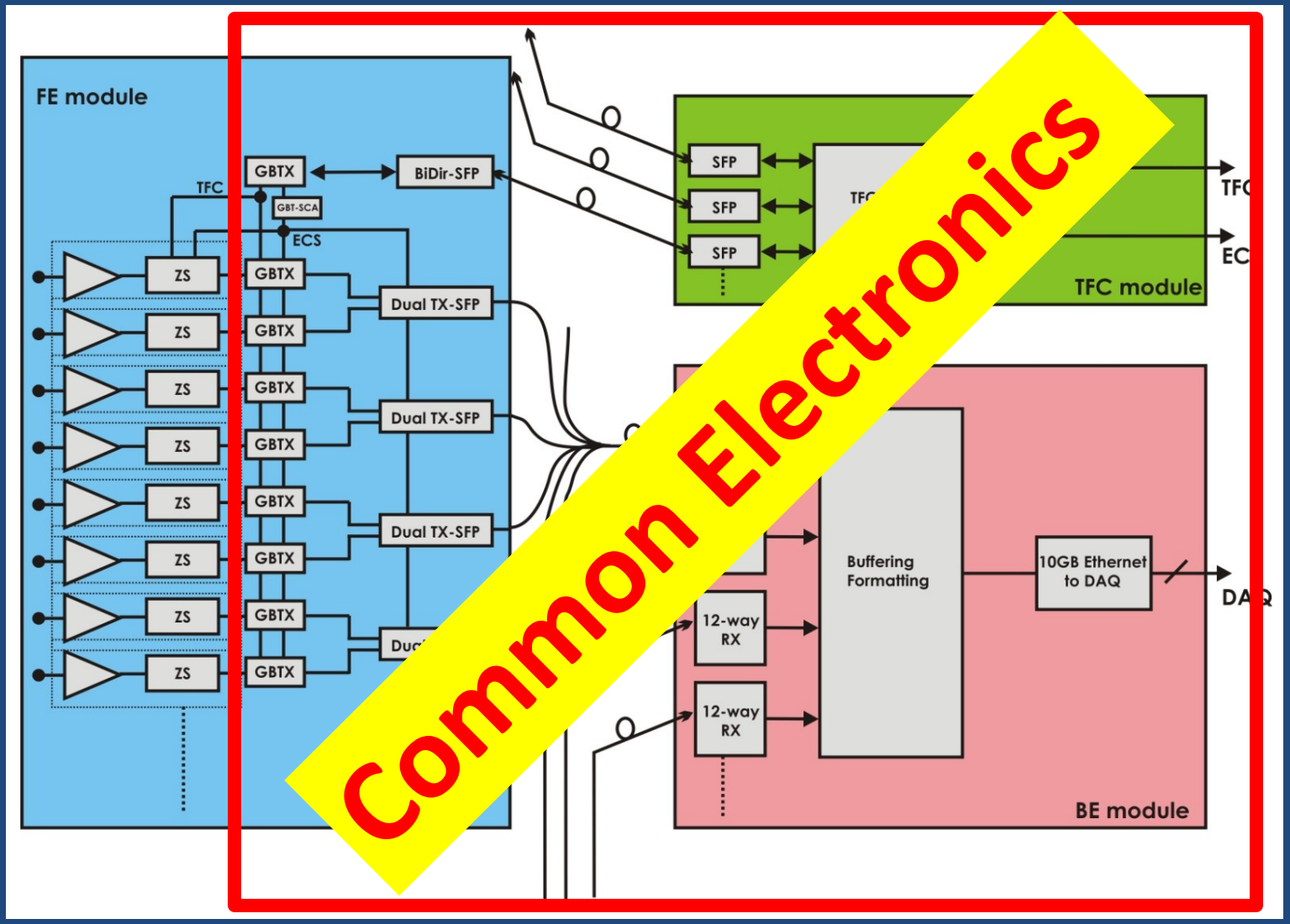
LoI on the way

Electronics architecture

Front-end electronics: transmit data from every 25ns BX



Generic Sub-Detector Readout & Control



Implementation

Try to optimise:

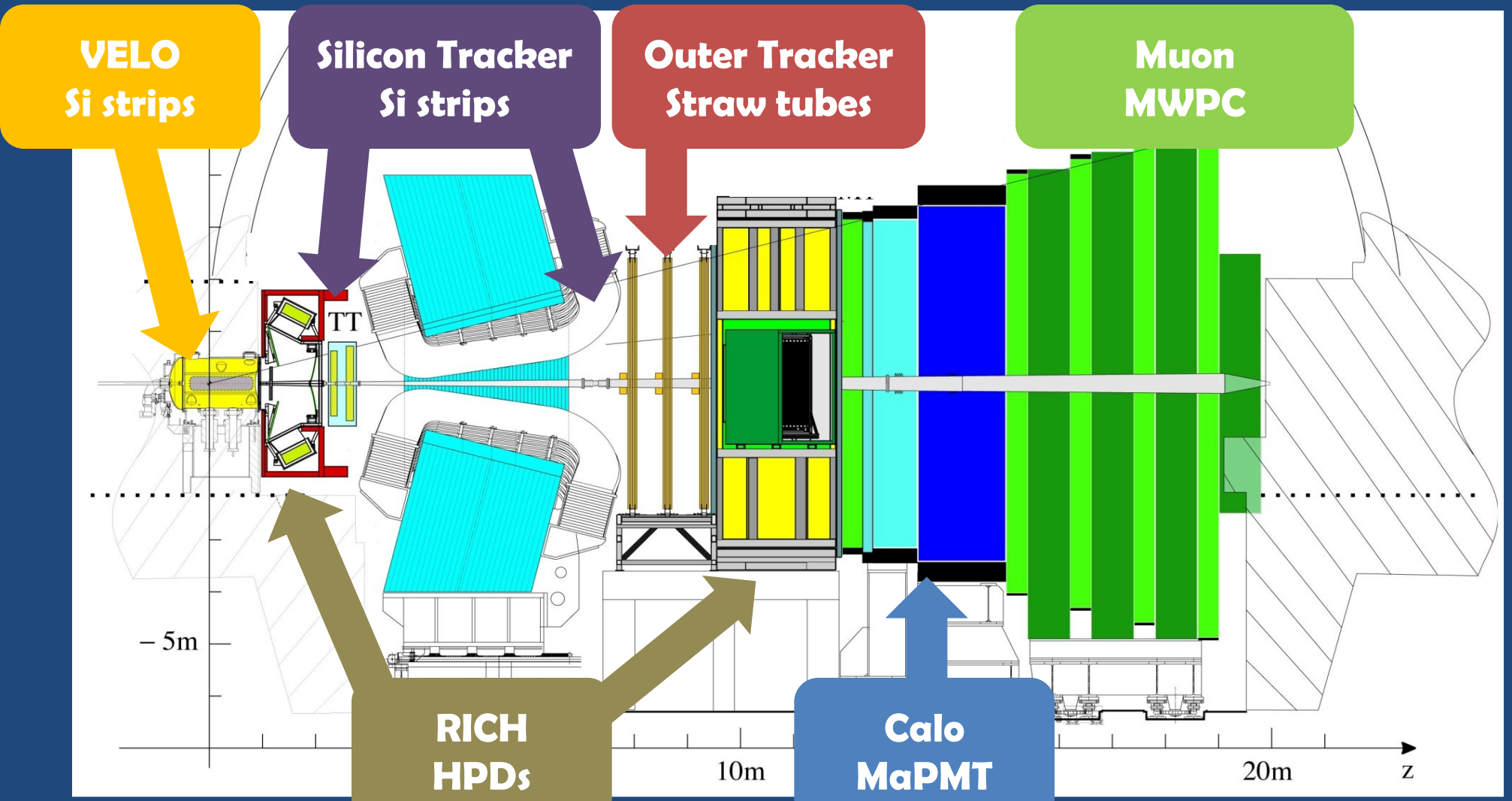
- Cost
- Manpower
- Time (development, production, installation)

1. Re-use existing electronics & infrastructure as much as possible
2. Develop common solutions for use by all sub-detectors

Example: data links

Use GBT @ 4.8 Gbit/s
~ 12,000 links
8,300 optical fibres already installed in LHCb

LHCb sub-systems

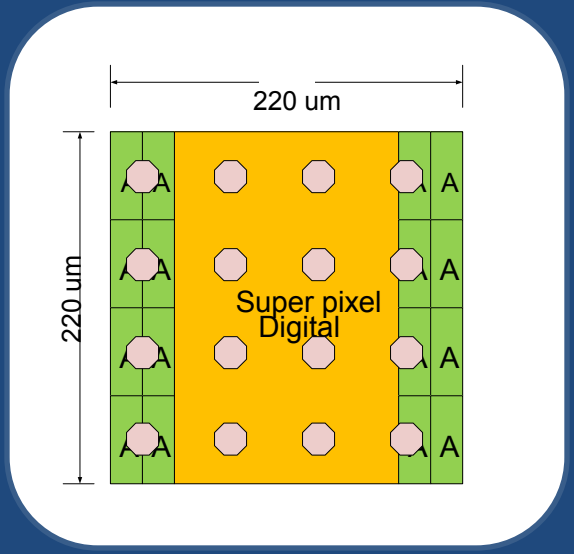


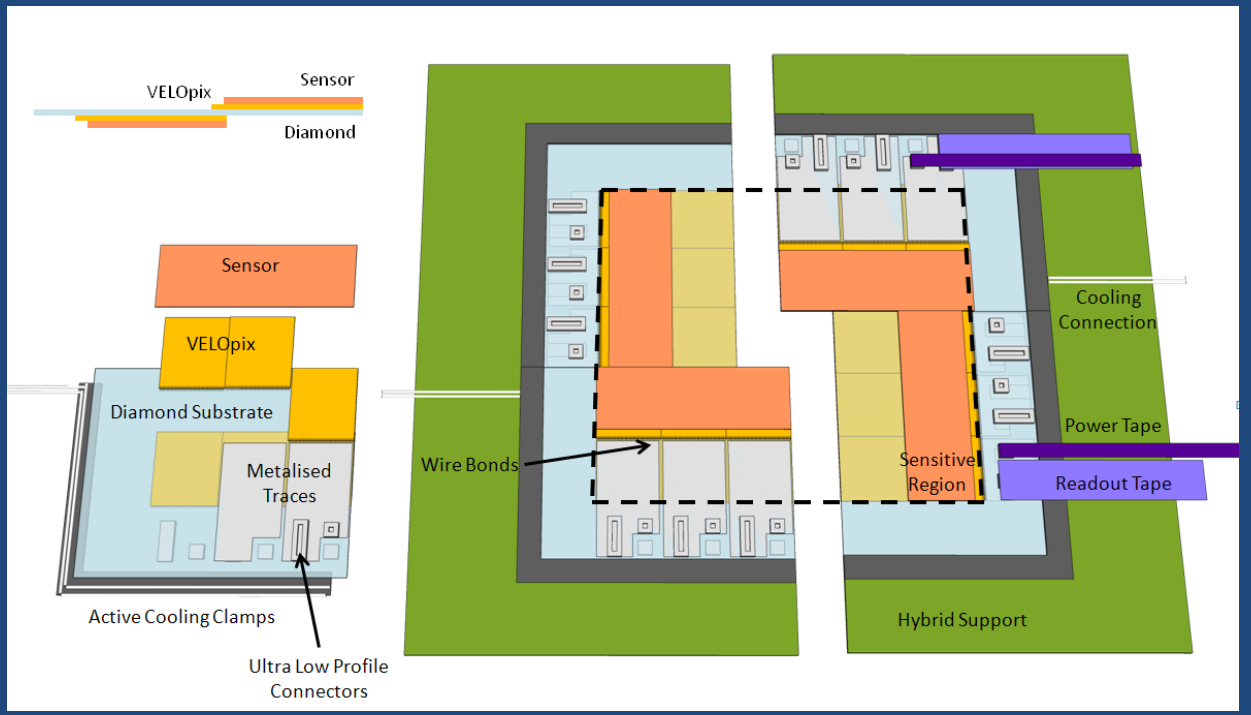
VELO

Pixel (baseline) option

VeloPix chip: 256 x 256 array, 55 x 55 μm pixels

- Strong overlap with TimePix2 (under design)
- 3 or 4 bits TOT
- Architecture to minimise bandwidth (hottest chip = 12 Gbit/s)
- Serial readout





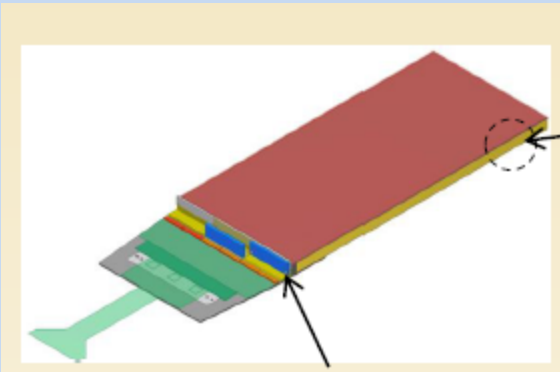
Ken Wyllie, CERN

Tracker

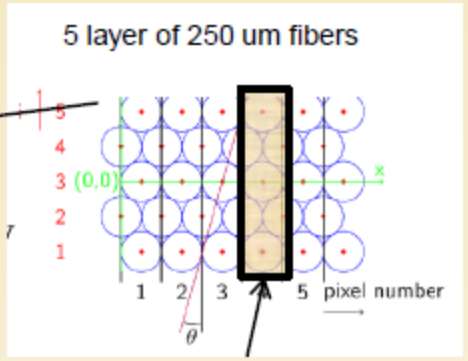
Si tracker -> SciFi tracker ?

Fibres coupled to SiPM
SiPM Radiation tolerance?

ASIC investigation started



SiPM array

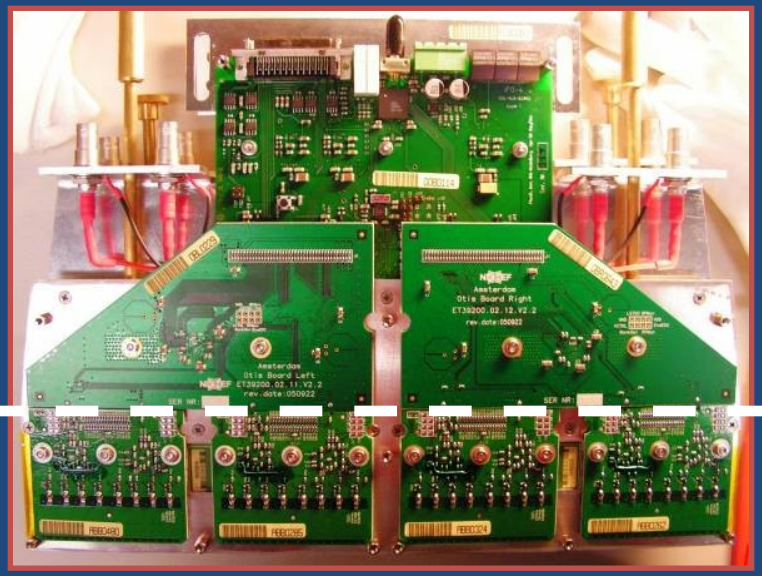


SiPM cell coverage

Outer tracker

Re-use front end

Implement TDC (1ns) in ACTEL ProASIC FPGA: prototype already working

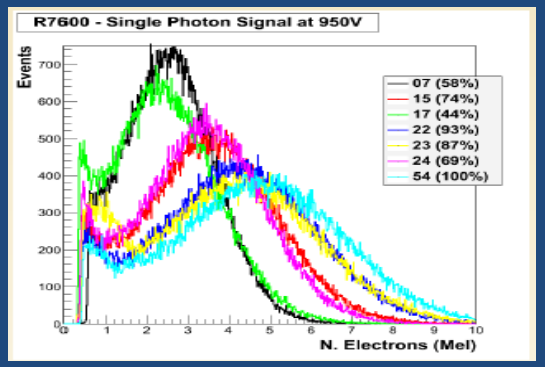


Re-use

Replace

RICH

MaPMT (baseline) option



Prototyping using MAROC3:

- Gain compensation
- Binary output

Digital functions in ACTEL

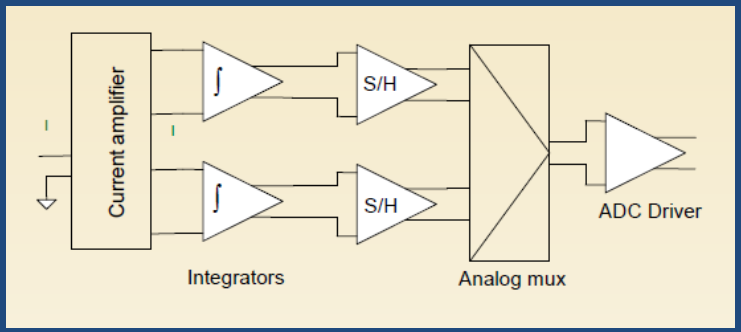
Muons

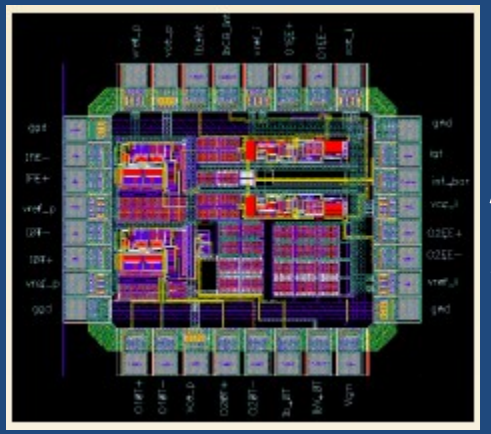
40MHz data transmission already – re-use

Calorimeter

MaPMT gain reduction
⇒Reduce electronics noise
⇒Active termination in ASIC (à la ATLAS LAr)

Interleaved integrators





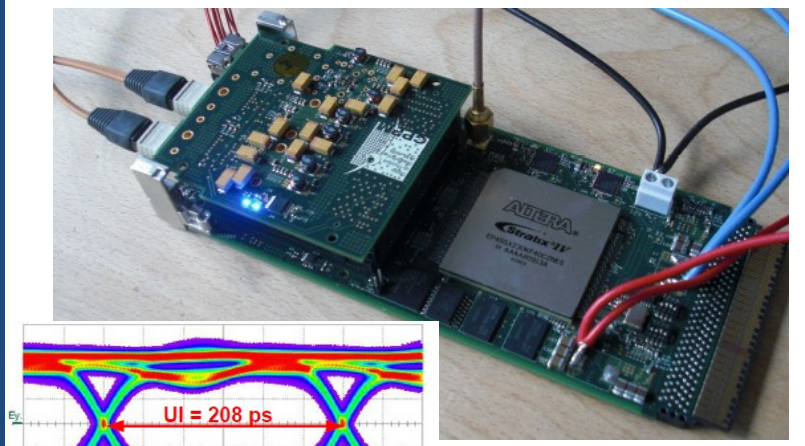
Protoype in AMS 0.35μm SiGe

Common developments

TELL40: Common back-end readout board

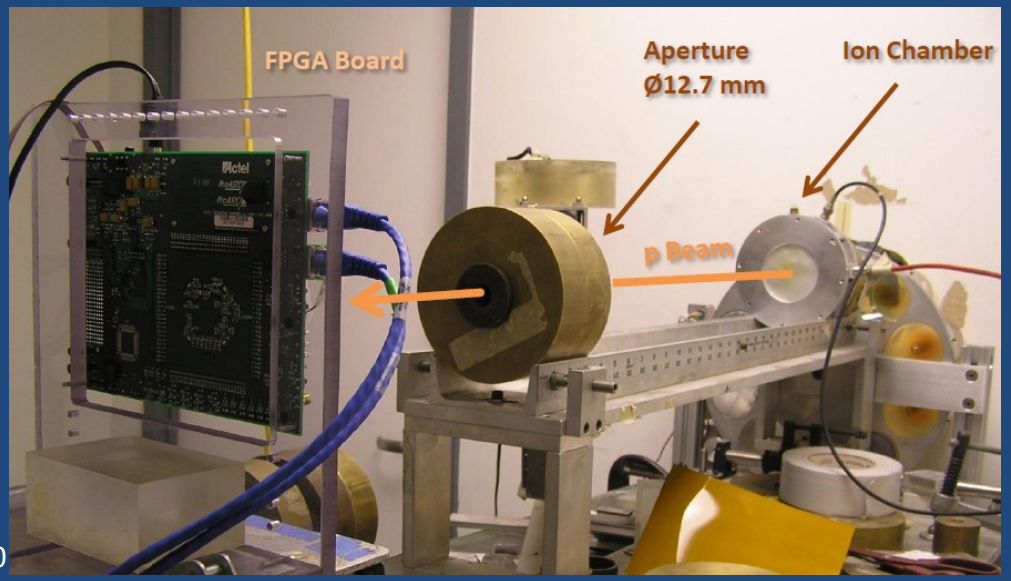
- Tests of high-speed links on proto-board
- Parallel optical I/Os (12 x > 4.8 Gb/s), GBT compatible
- Final aim: ATCA with different mezzanine recipes

See talk from Jean-Pierre Cachemiche tomorrow



ACTEL Flash FPGA for front-end modules

- Advantages over ASICs: re-programmable!!!
- Can they survive the radiation.....?
- Irradiation programme started on A3PE1500



Conclusions

Architecture defined
All sub-detectors actively developing systems
Common items progressing

Re-use a lot of existing system but ……
…… significant R&D still needed