

Status of the DCDC development @ CERN

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CERN - PH/ESE

Outline

- ASIC

- ✦ Technology
- ✦ Design

- Full converter boards

- ✦ Air-core inductor
- ✦ Shielding of EM fields
- ✦ Low-noise board design
- ✦ Integration in detector systems

ASIC technology

- Two adequate technologies offering LDMOS rated above 12V Vds have been selected: 0.25 (IHP) and 0.35um (On Semi) nodes
 - ❖ New experimental LDMOS transistors introduced by IHP in 2010 and used in DCDC prototype are not suitable for our application:
 - * Insufficient radiation tolerance (SEB, displacement damage)
 - * Excessive current injection in the substrate when used in buck DCDC
 - ❖ Prototype DCDC (AMIS2) in the 0.35um passed all radiation tests (including SEB)
- Design has been moved in Sept2010 to the On Semi 0.35um technology for phase1 applications - while working in collaboration with IHP to select and qualify LDMOS compatible with our requirements

ASIC design

	AMIS2	IHP1	IHP2	AMIS3	AMIS4
Full control loop	✓	✓	✓	✓	✓
Dead times' handling	Fixed	Adaptive (QSW)	Adaptive (QSW and CCM, sharp transition)	Fixed	Adaptive (QSW and CCM, smooth transition)
On-chip regulator(s)	No	No	✓	✓	✓
Soft Start	Simple RC	Simple RC with comparators	Full sequence with comparators	Simple RC	State machine
Over-I protection	No	No	✓	No	✓
Over-T protection	No	No	No	No	✓
Under-V disable	No	No	No	No	✓

↕
Used in
system tests

ASIC design

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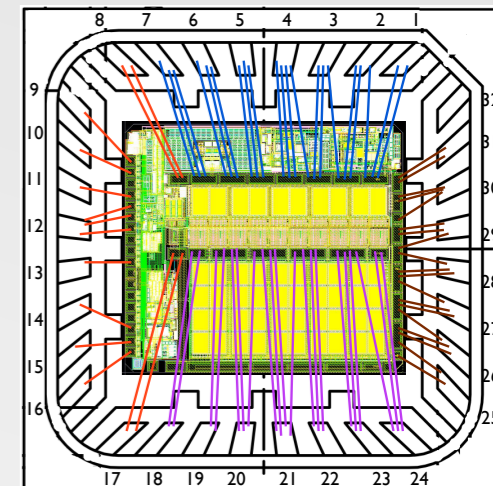
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Used in system tests

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Samples should be available in a few weeks

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Packaged in QFN32



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Used in system tests

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Tape-out Jan2011
Expected May

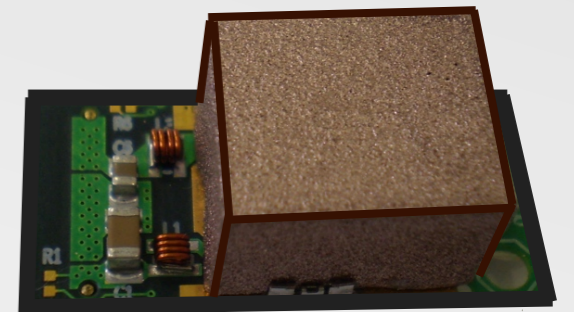
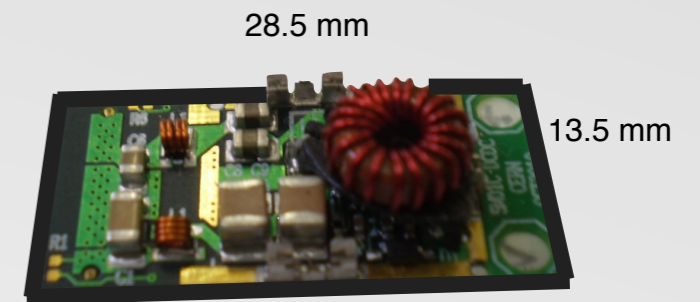
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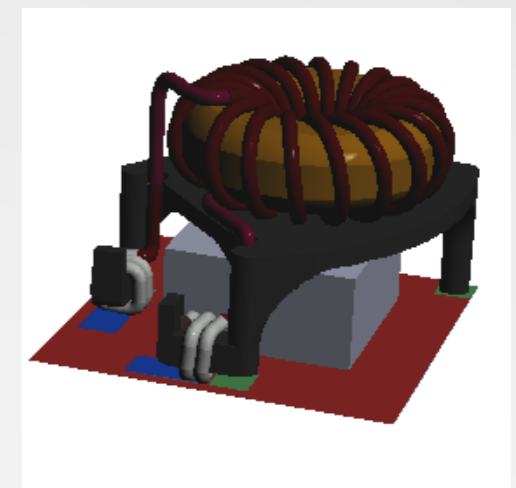
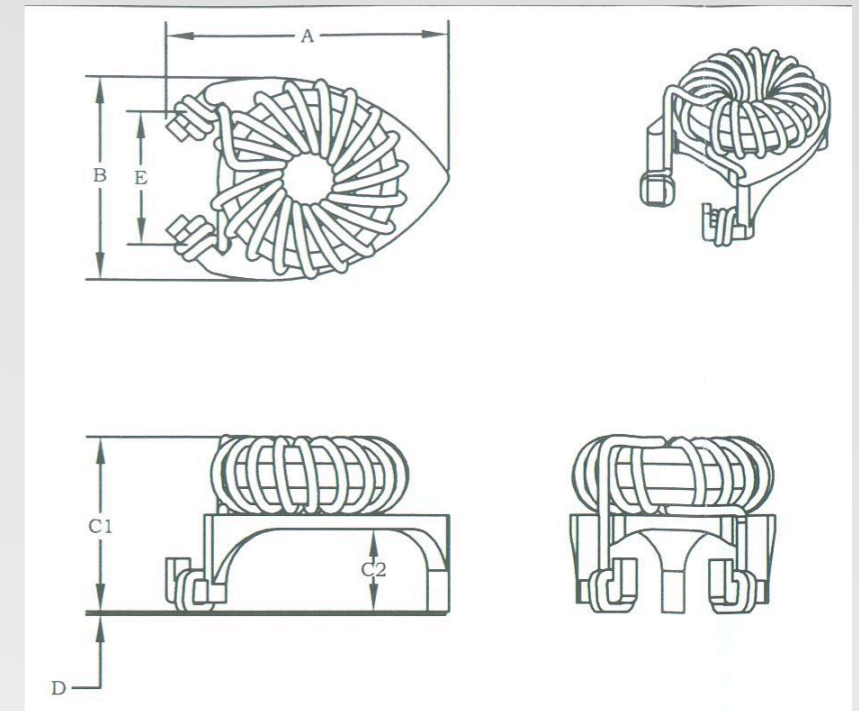
- Full converter boards

- ✦ Air-core inductor
- ✦ Shielding of EM fields
- ✦ Low-noise board design
- ✦ Integration in detector systems



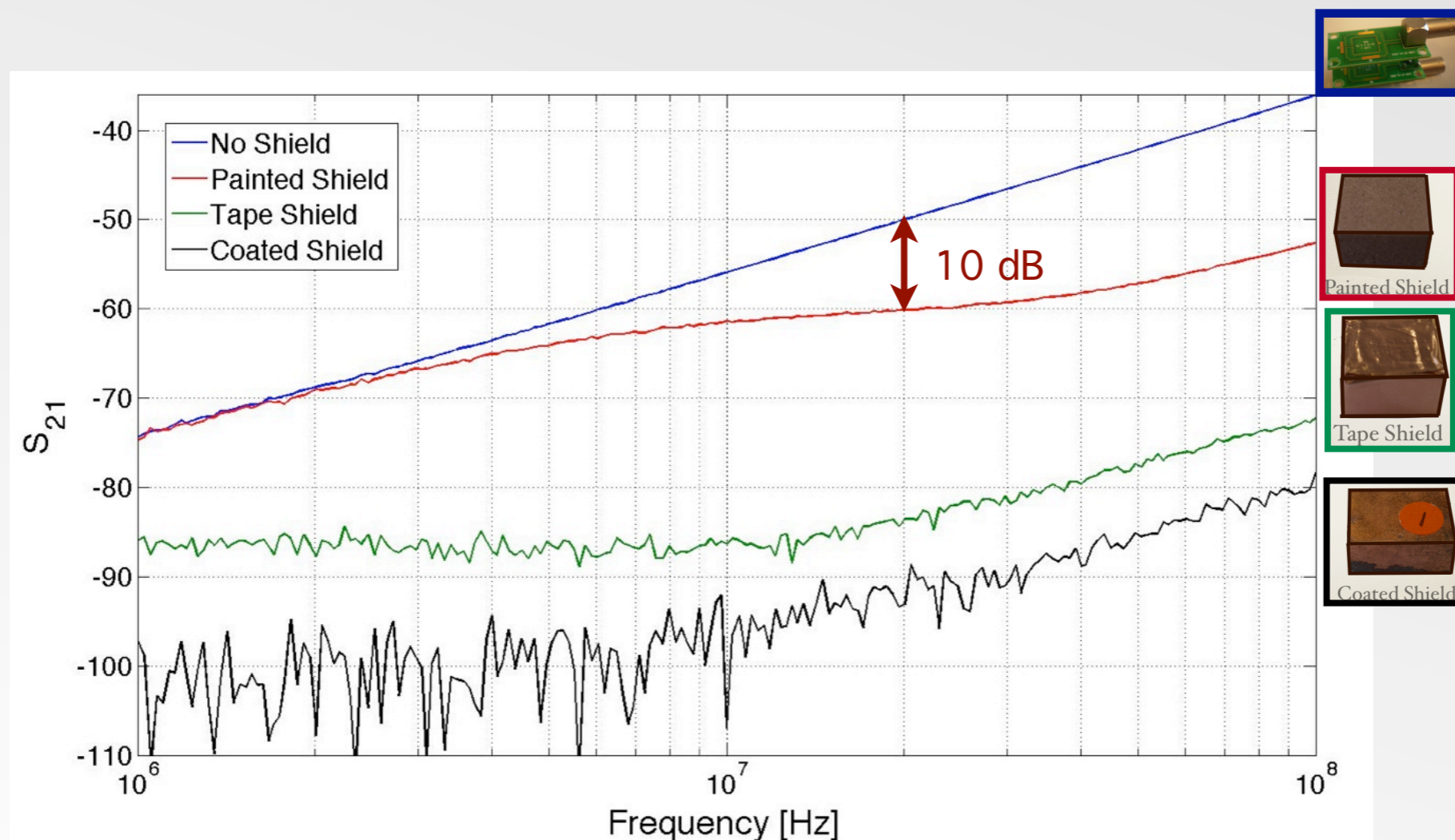
Air-core inductor

- Tolerance to B field imposes air core coils
 - ❖ Air core typical inductance values: 5-700 nH MAX
- Toroidal topology was selected in 2009
 - ❖ Compact geometry
 - ❖ Radiates significantly less magnetic field than other topologies
 - ❖ Air core toroidal inductors not available commercially: custom development for mass production is required
- Development with Coilcraft:
 - ❖ 220nH/30m Ω air core toroid
 - ❖ Coil mounted on plastic stand-off to fit precisely above the converter ASIC
 - ❖ Prototypes delivered in 2010. One sample successfully radiation tested at PS (8E15 p/cm²)

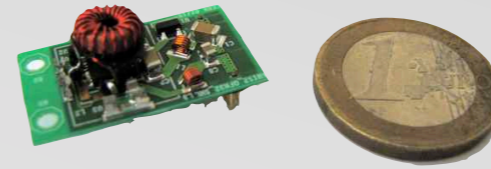


Shielding EM fields

- Shielding EM field is essential to reach minimum noise
- Different approaches to build the shielding box are being explored, and shielding effectiveness measured with dedicated setup

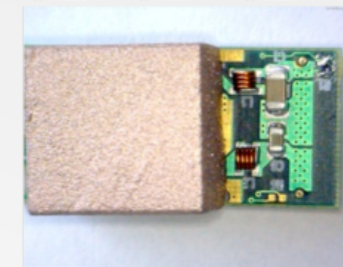
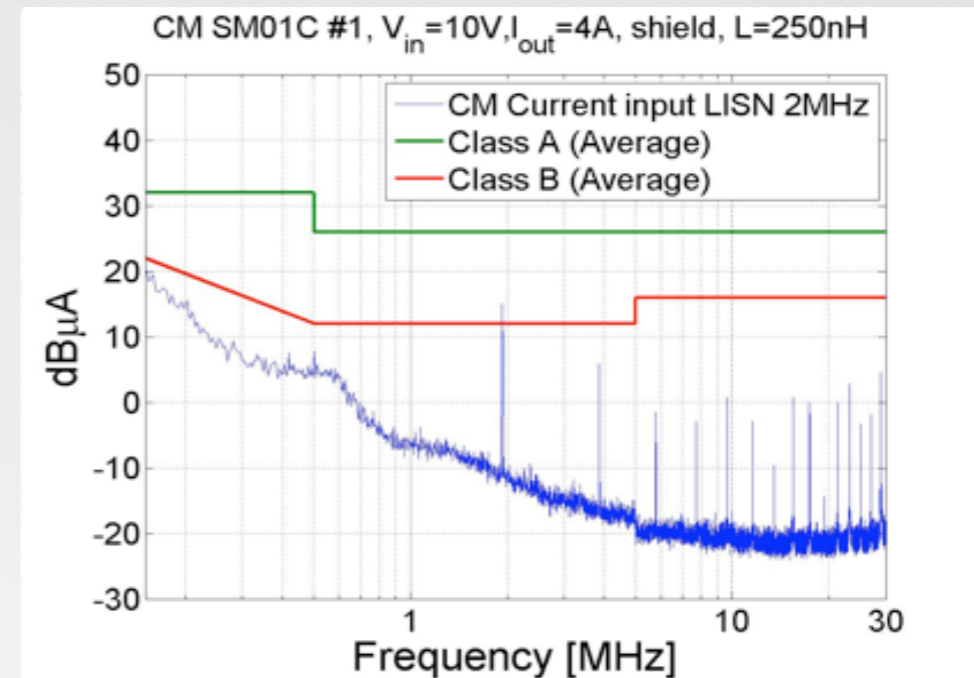
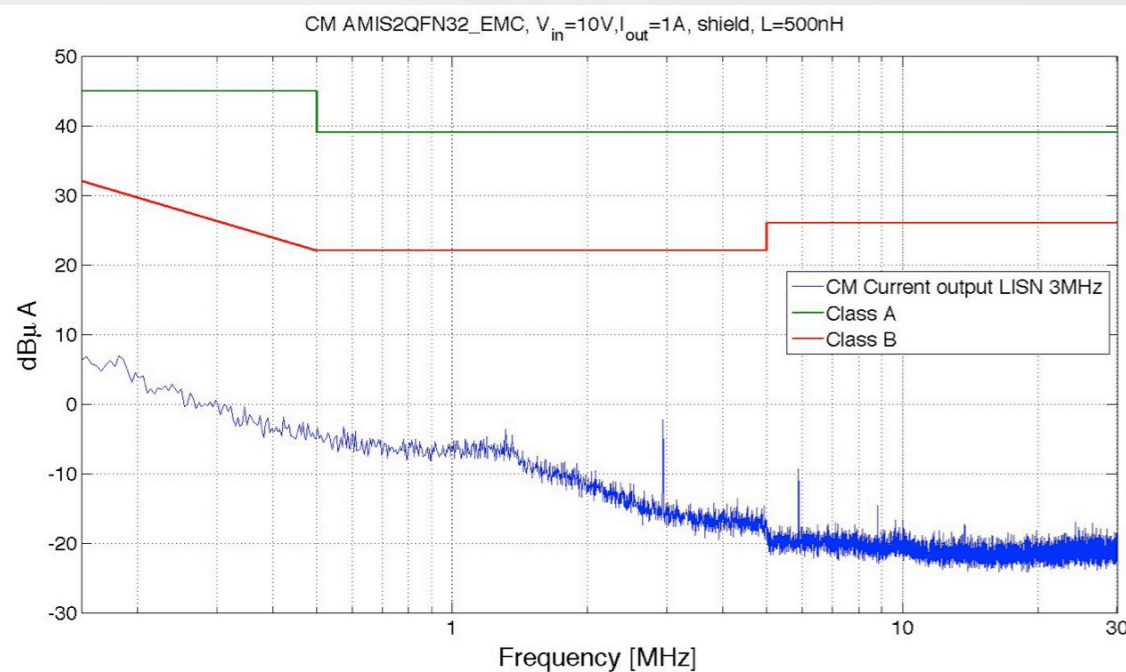


Low-noise board design

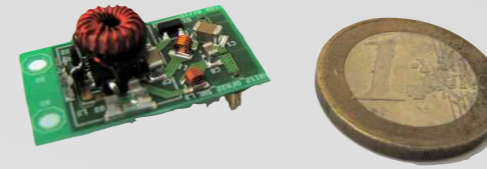


- Using the AMIS2 ASIC
 - ❖ Optimization principles fully applied
 - ❖ Very compact design, need only for few external components

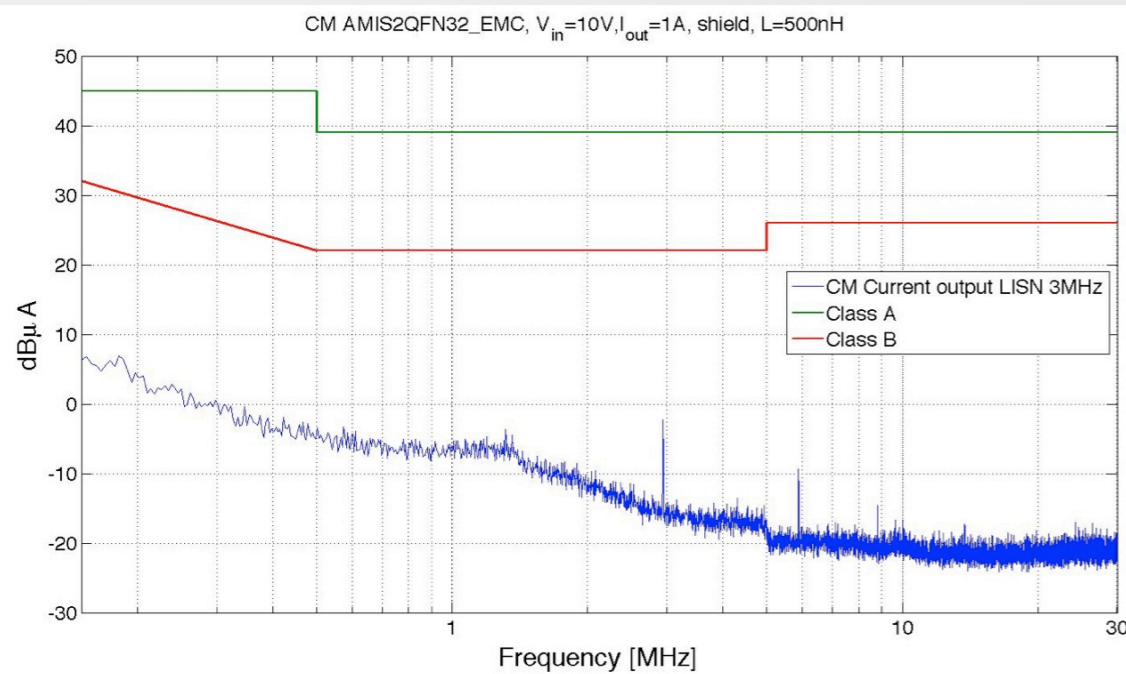
- Using a commercial DCDC circuit (LTC3605) - SM01C
 - ❖ Designed to provide up to 5A to match requirements of ATLAS SCT prototype modules



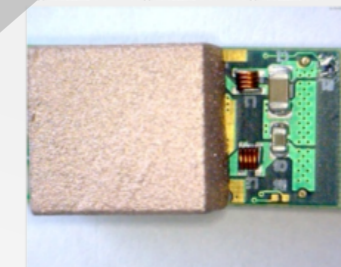
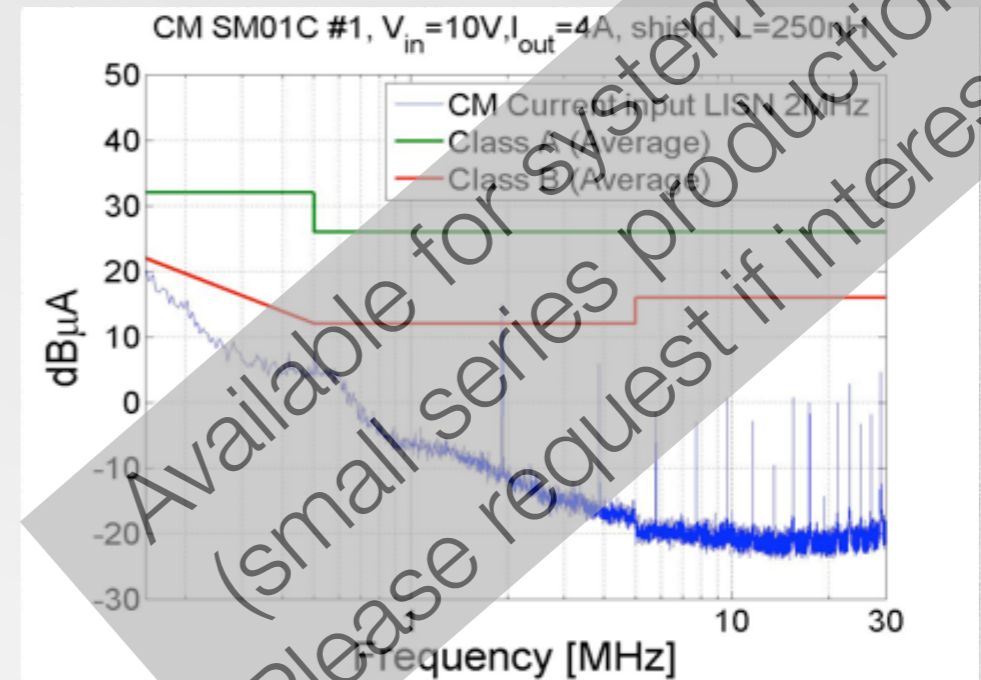
Low-noise board design



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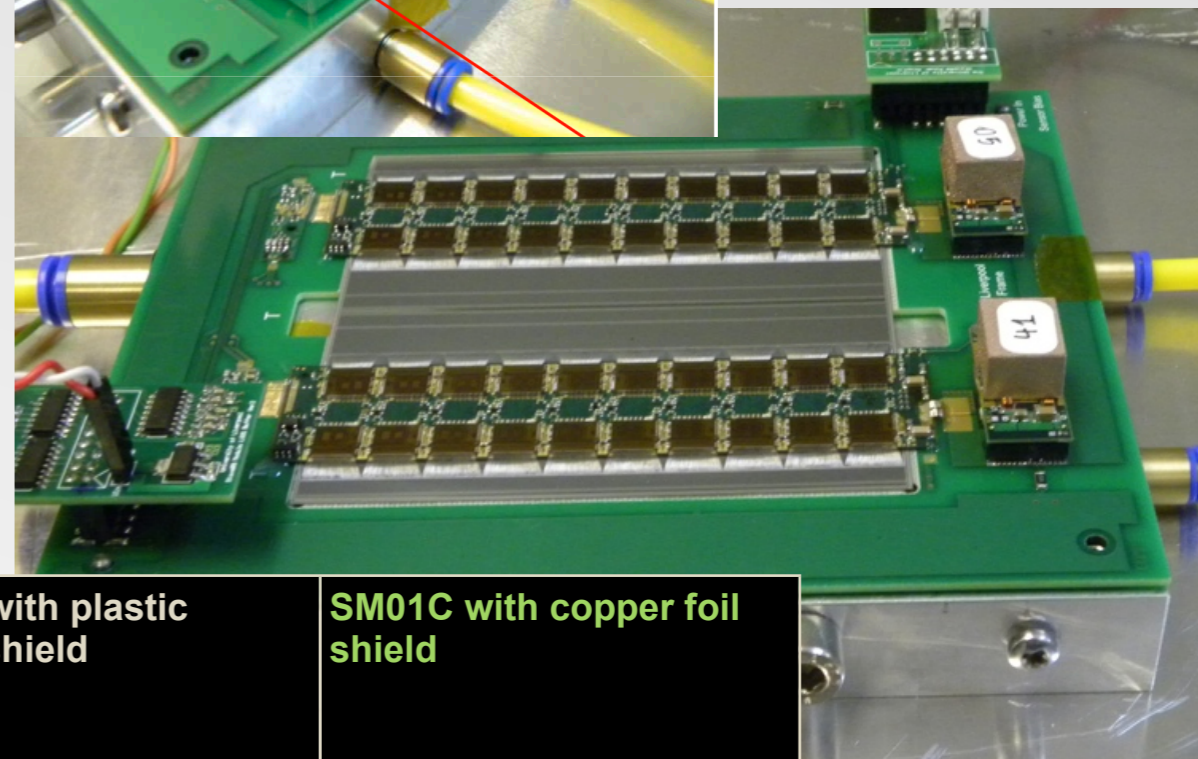
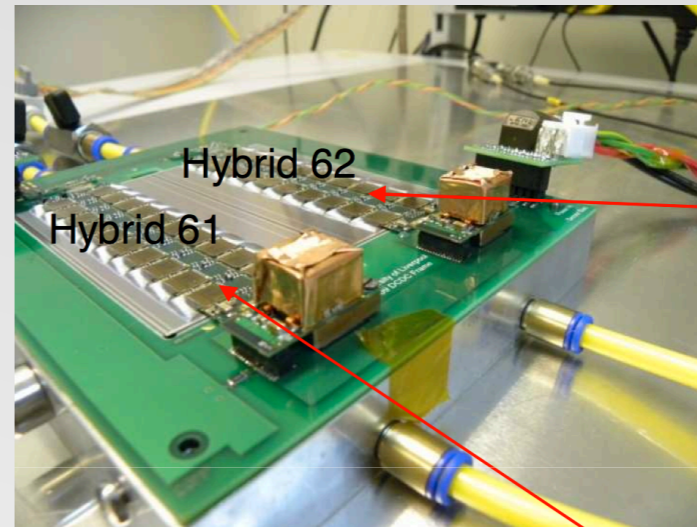


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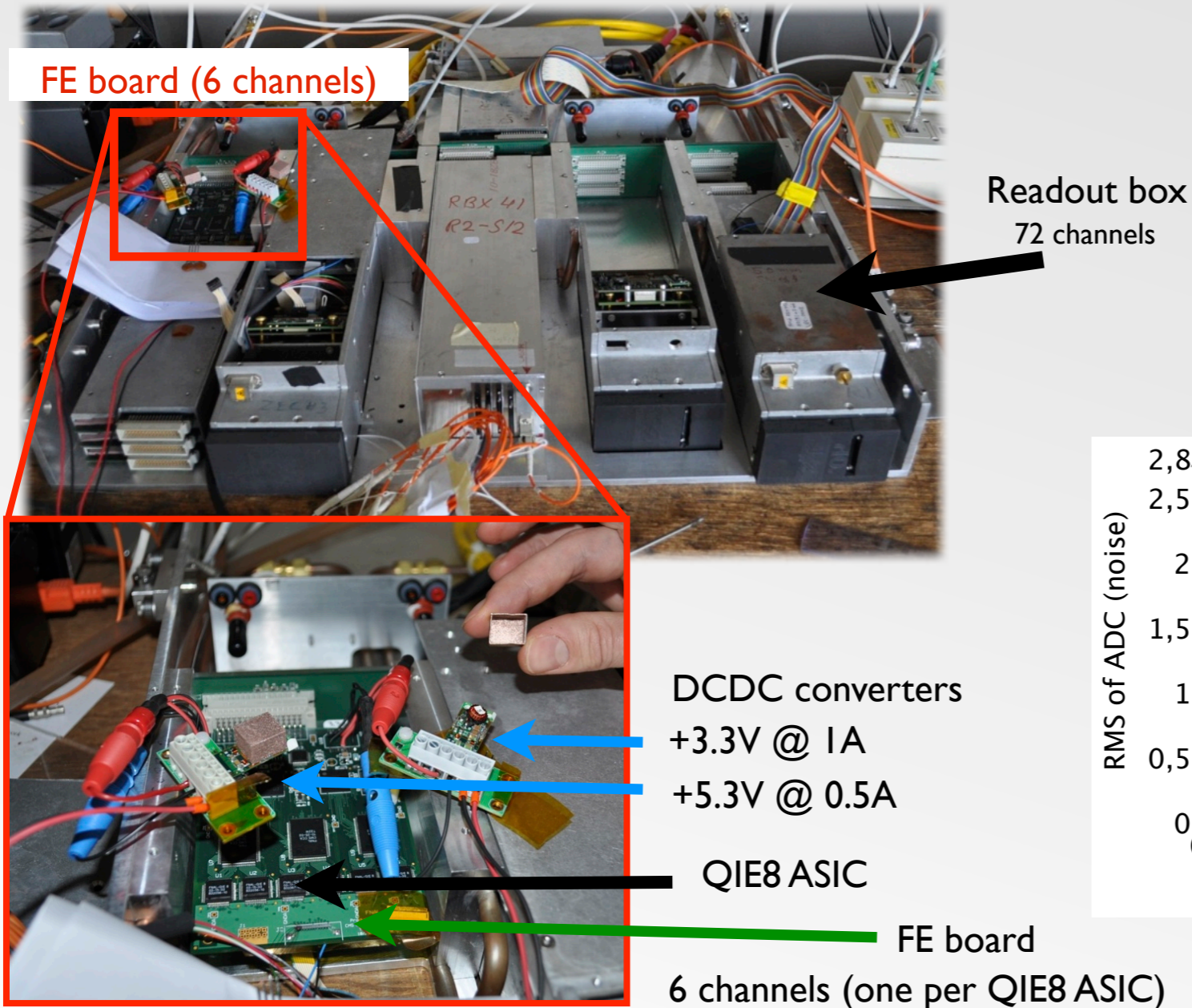
Measurements with ATLAS SCT prototype modules

- A stave module was powered with two SM01C converters and its performance was compared with the one obtained using a linear power supply (test done at Liverpool and at CERN with UniGe module)
- A residual magnetic field emitted from the DCDC board fitted with plastic coated shield raises the noise of the front-end
- When using a copper foil shield instead, the reference noise levels are recovered
- The compatibility between SM01C and the ATLAS stave modules is now achieved, using copper foil shields

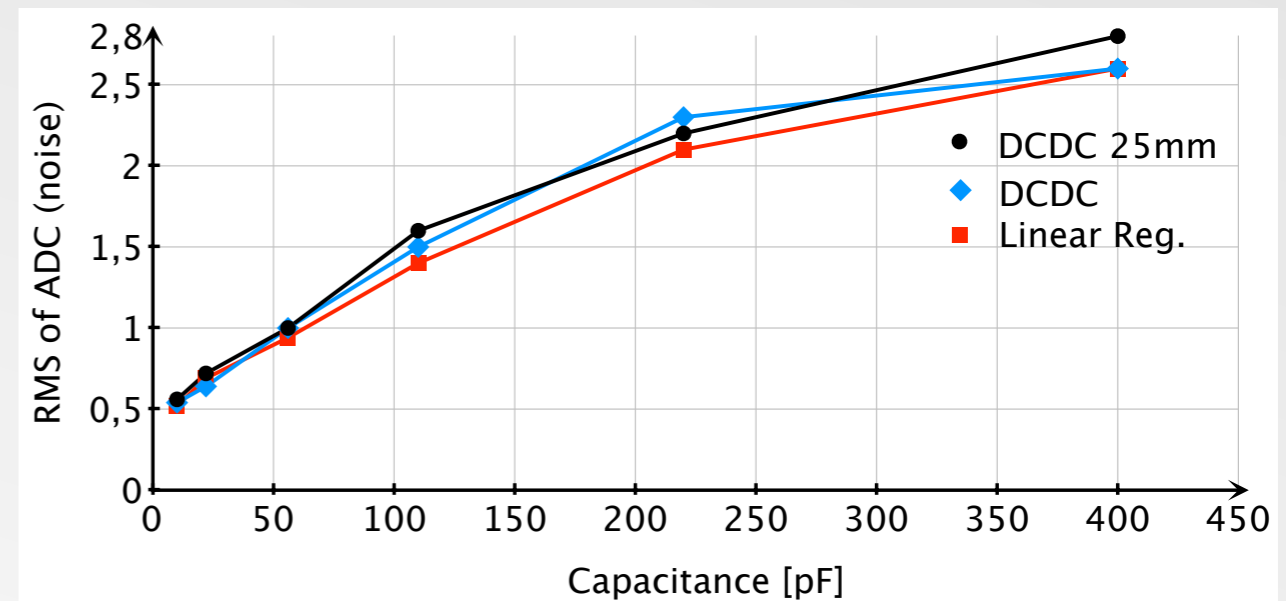


Hybrid	Reference ENC	SM01C with plastic coated shield	SM01C with copper foil shield
61 Row 0	585	645	585
61 Row 1	591	674	591
62 Row 0	570	723	595
62 Row 1	596	716	603

Measurements with CMS HCAL modules (collaboration with HCAL groups, T.Grassi)

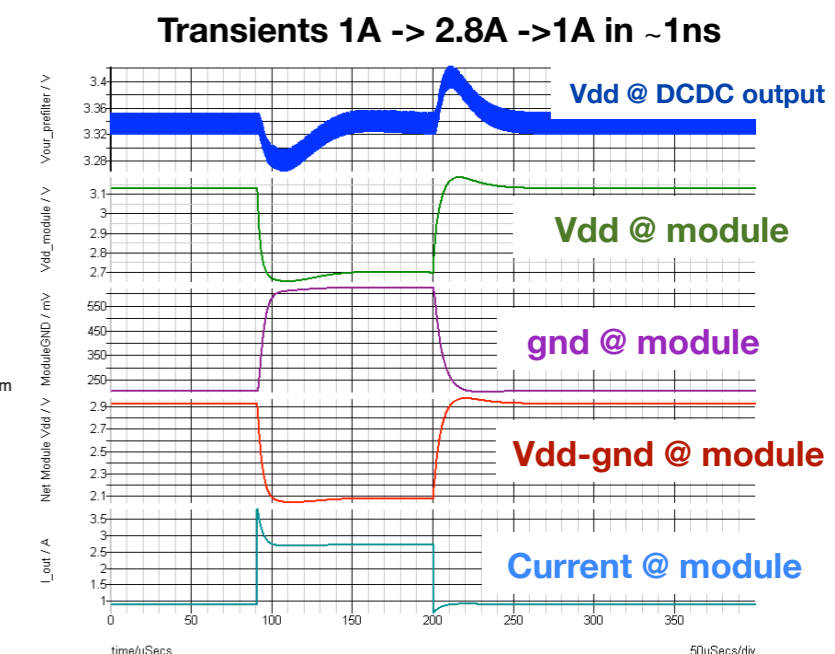
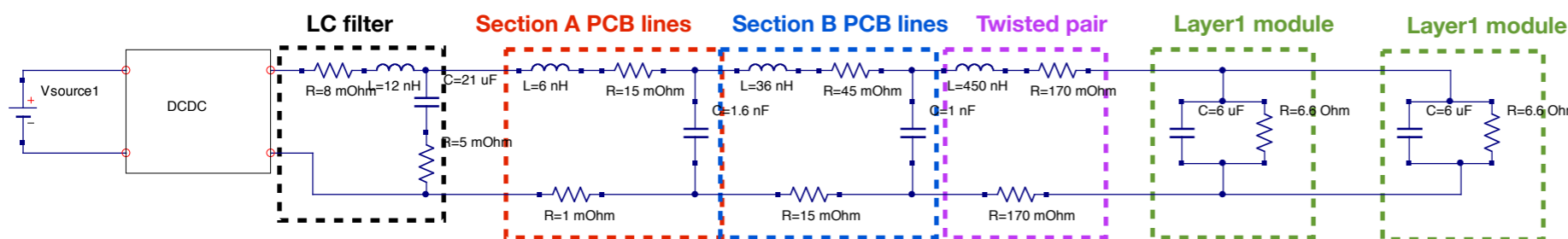
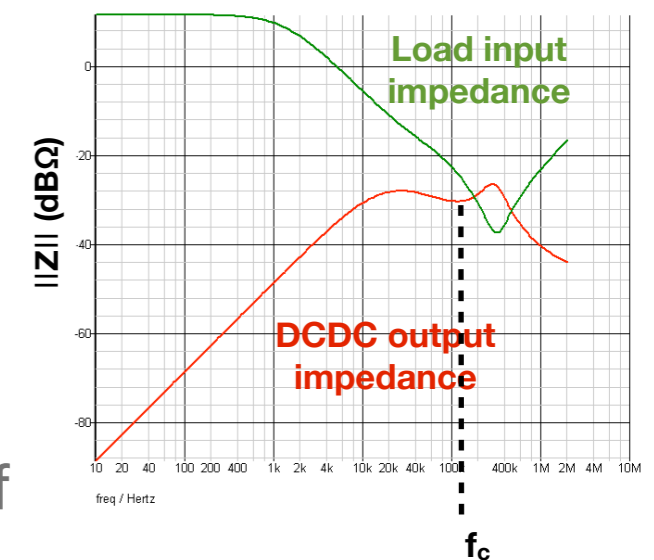


- Measurements performed powering one FE board of a Readout box with DCDC converters
- Converters shielded with painted shield (small EM shielding efficiency) have been placed at different distance from readout ASICs - up to 2.5cm from the ASICs
- Noise performance of the ASICs measured essentially identical to the one obtained with a linear regulator



Simulation of full system stability

- The integration of a POL DCDC buck converter in detector systems requires addressing possible concerns related to stability and voltage oscillations
- A behavioral model for the AMIS4 DCDC ASIC has been developed and used to study with simulations stability issues
 - ❖ In the explored range of parameters for input and output impedances, based on available estimates, no sign of instability or oscillation has been found
- The developed simulation tools, based on the characteristics of the ASMI4 POL buck, can be used to study specific systems during the development phase and help finding and fixing possible problems



Summary

- **ASIC**

- ❖ Technology

- * On-semi 0.35um technology fully validated. Qualification of IHP 0.25um technology LDMOS design in progress

- ❖ Design

- * 2 prototypes in production in On-Semi 0.35um. AMIS4 contains full protection features and is very close to a final design

- **Full converter boards**

- ❖ Special components

- * Inductor design chosen, transferred to industry and in production
 - * Different shielding options studied, prototypes produced and measured

- ❖ Low-noise and compact prototypes available for both rad-tol ASIC and commercial DCDC

- ❖ Integration in detector systems

- * Measurements on different systems (Tracker and HCAL) confirm that power can be provided by DCDC converters without impacting the noise performance
 - * Simulation tools to evaluate system stability have been developed