Summary of the Power WG

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Agenda

Tuesday 08 March 2011

14:00 - 14:05 Introduction 05'
Speakers: Magnus Hansen (CERN) , Philippe Farthouat (CERN)

14:05 - 14:25 Status of the DC-DC ASICs development 20'
Speaker: Stefano Michelis
Material: Slides

14:25 - 14:45 Experience with serial powering on the ATLAS SCT stave 20'
Speakers: Mitch Newcomer (University of Pennsylvania) , Mitchell Franck Newcomer (Departm.of Physics & Astronomy)
Material: Slides

14:45 - 15:05 DC-DC modules development at CERN 20'
Speaker: Cristian Alejandro Fuentes Rojas (Univ. Tecnica Federico Santa Maria (UTFSM)-Unknown-Unknown)
Material: Slides

15:05 - 15:25 Shunt LDO regulator in FEI4 20'
Speaker: Laura Gonella (University of Bonn)
Material: Slides

15:25 - 15:45 Switched capacitors DC-DC in FEI4 20'
Speaker: Yunpeng Lu
Material: Slides

15:45 - 16:05 DC-DC development for the CMS pixel upgrade 20'
Speaker: Katja Klein (I. Physikalisches Institut (B))
Material: Slides

16:05 - 16:25 DC-DC stability studies 20'
Speaker: Federico Faccio (CERN)
Material: Slides

▸ http://indico.cern.ch/conferenceDisplay.py?confId=127662

ACES 2011

Serial power (Mitch Newcomer)

- Stavelet (4 modules, 8 readout hybrids) used with serial power

- Protection scheme with a small hybrid (BNL)
    - Over-voltage, ON/OFF

- Serial Power Protection (SPP) chip development in 130nm
    - Modulation of the main power line to send commands (e.g. ON/OFF)

Stavelet Numerology (@RAL)
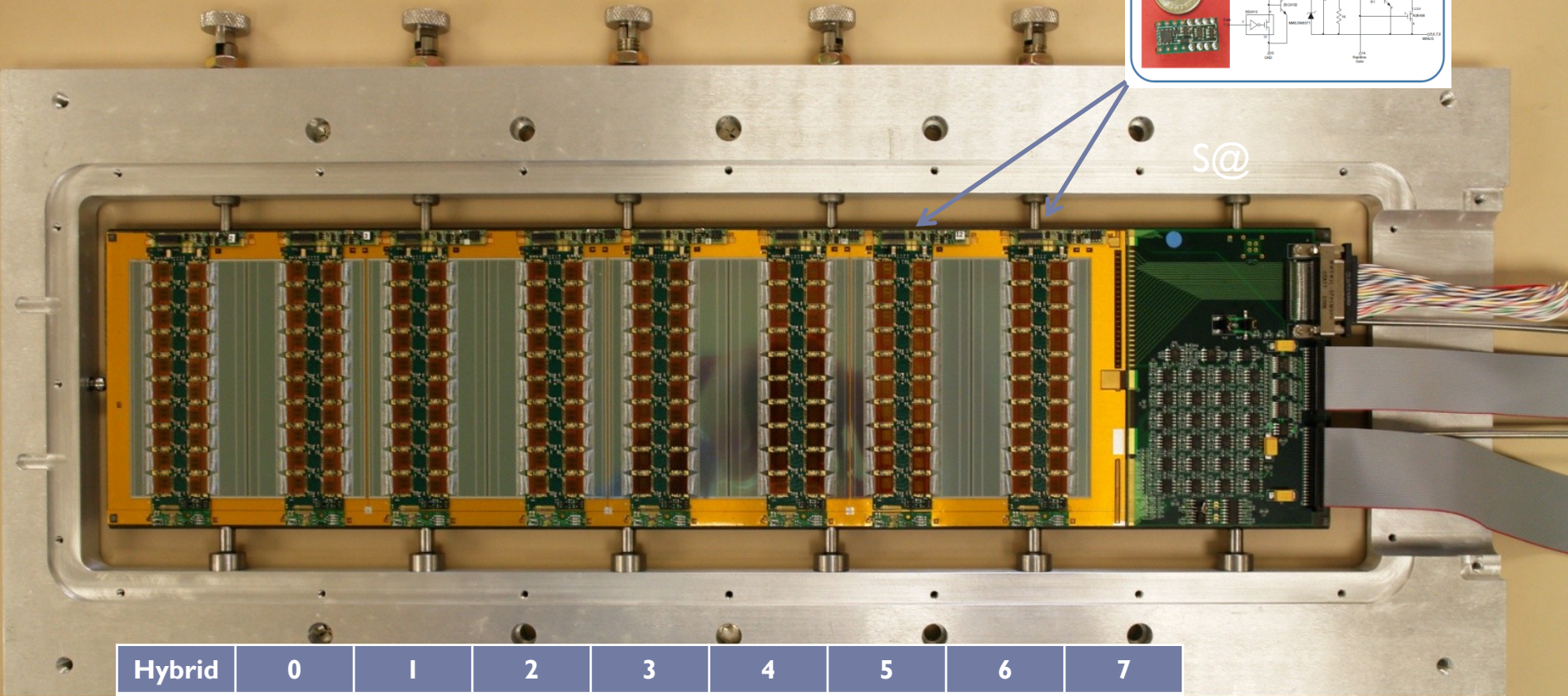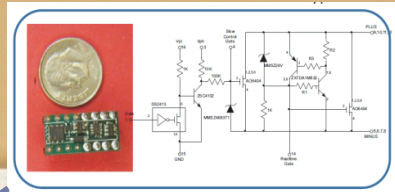
Hybrid	0	1	2	3	4	5	6	7
BCC	62	61	60	59	58	57	56	55
MUX	7	6	5	4	3	2	1	0
DEMUX	14/15	12/13	10/11	8/9	6/7	4/5	2/3	0/1
Coupling	DC	AC	AC	DC	AC	DC	AC	DC
Module	0		1		2		4	
s/n	1		9		3		4	

Thermal Images of the Stavelet in Operation (RAL)
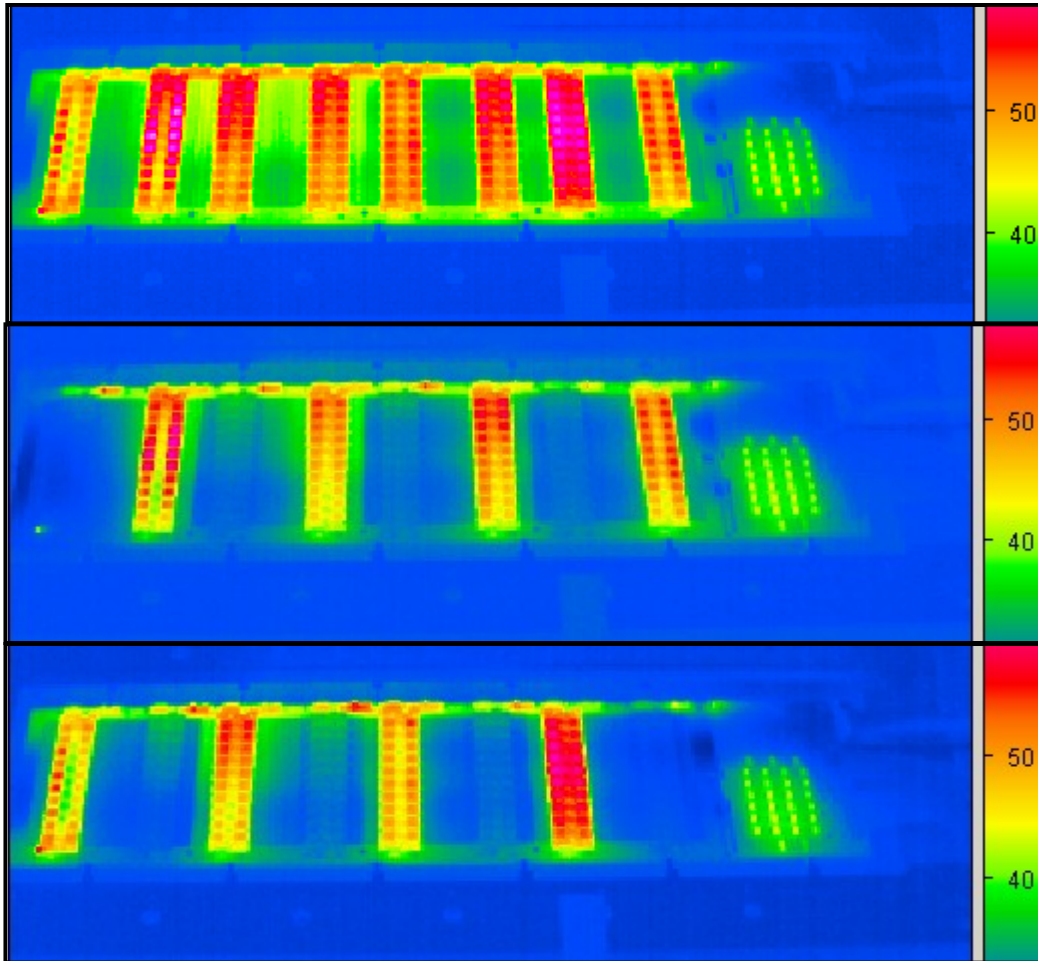
All hybrids on

22.7V
5.09A

Slow control disables odd hybrids

12.7V
5.09A

Slow control disables even hybrids

Each hybrid may be bypassed using the PPB 1-wire operated shunt
Voltage differences consistent with 2.5V per hybrid
2.7V overheads: bus tape, bond wires, PPB PCBs, external cabling

First Prototype of SPP block ready for testing

IBM CMOS8RF 130nm Technology

Analog Control loop includes:

- 1.1 V BandGap .
- SPP 2.3V internal shunt regulator.
- Hybrid Regulation loop suitable for use on hybrids or staves.

Submitted for fab May 2010
Returned   Jan 2011

Chip on board test PCB prepared but due to bond pad size: 60X95um Pad layout needed to be reworked. To be sent out this week.

Test board plug in compatible with ABCn Modules and Stavelets.

Connector Pin compatible with BNL Protectiion board socket on Hybrid

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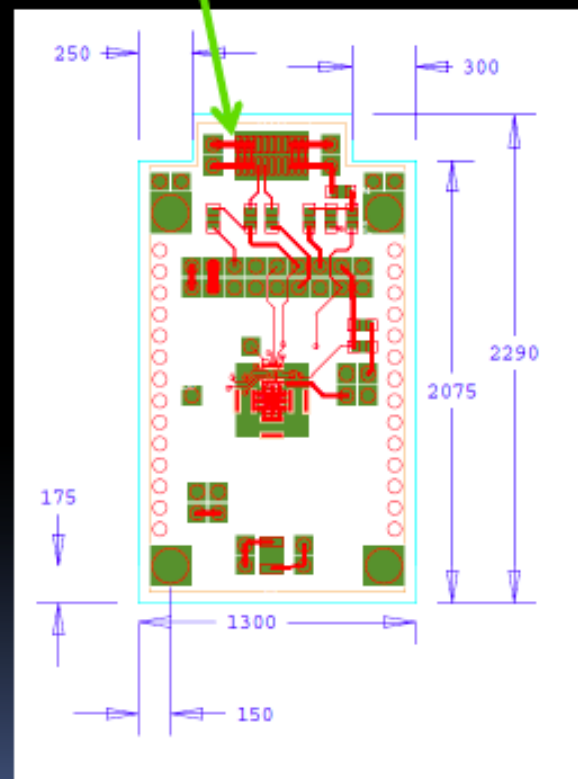
SPP full Prototype Chip Layout (2011 submission)

Shorting Transistors
5cm X ..6um Added
63mV @ 1.6A

SPP chip as in 2010

PENN 3/7/11
SPP CHIP: 2mm x 2mm
Big Shunt: 54000um/600nm

NFET Shunt
Transistors
W=18000u,
L=600n

OPAMP

Small Shunt
Transistor
W=6800um
L= 600nm

CMOS 8RF

SPCONTROL

Serial Power Protection and Control

- Single Global power line supplies each SPP with independent power
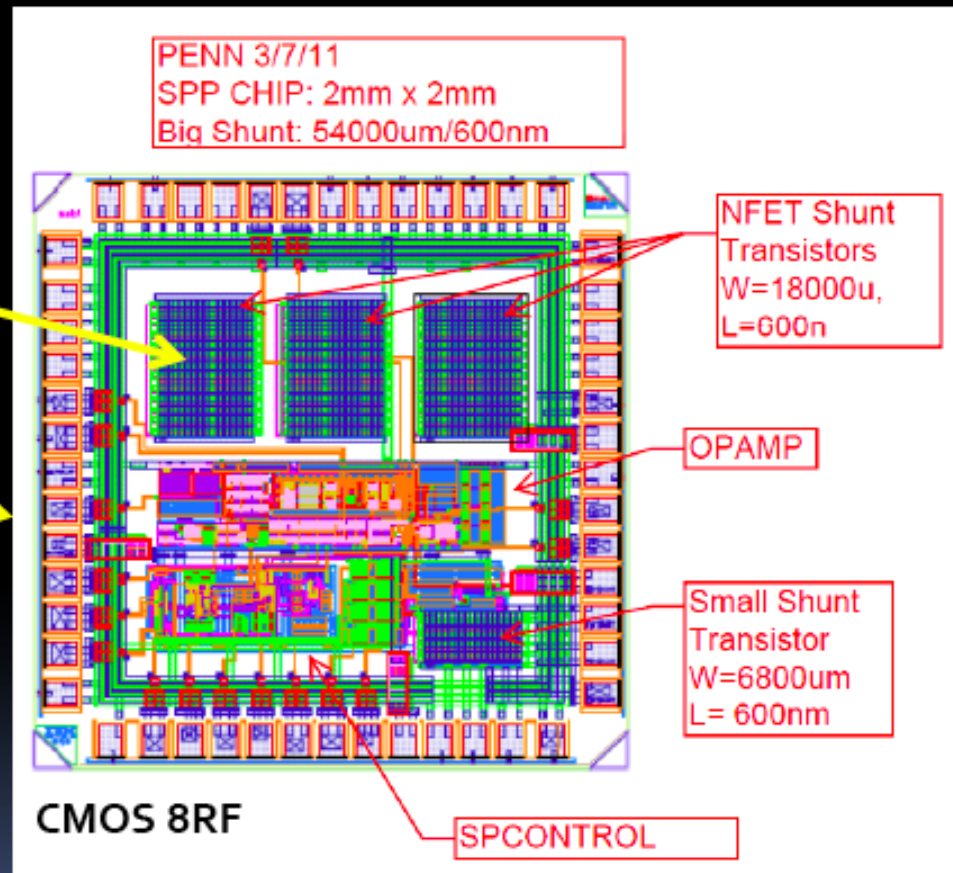- SPP is addressable to turn "on" and "off" a hybrid.
- Built in Transistor capable of shunting hybrid current Independent of ASIC based Shunt Transistors

Global SPP bus Power & addressable communications

1.5K @ 6mA

SP+

SP-
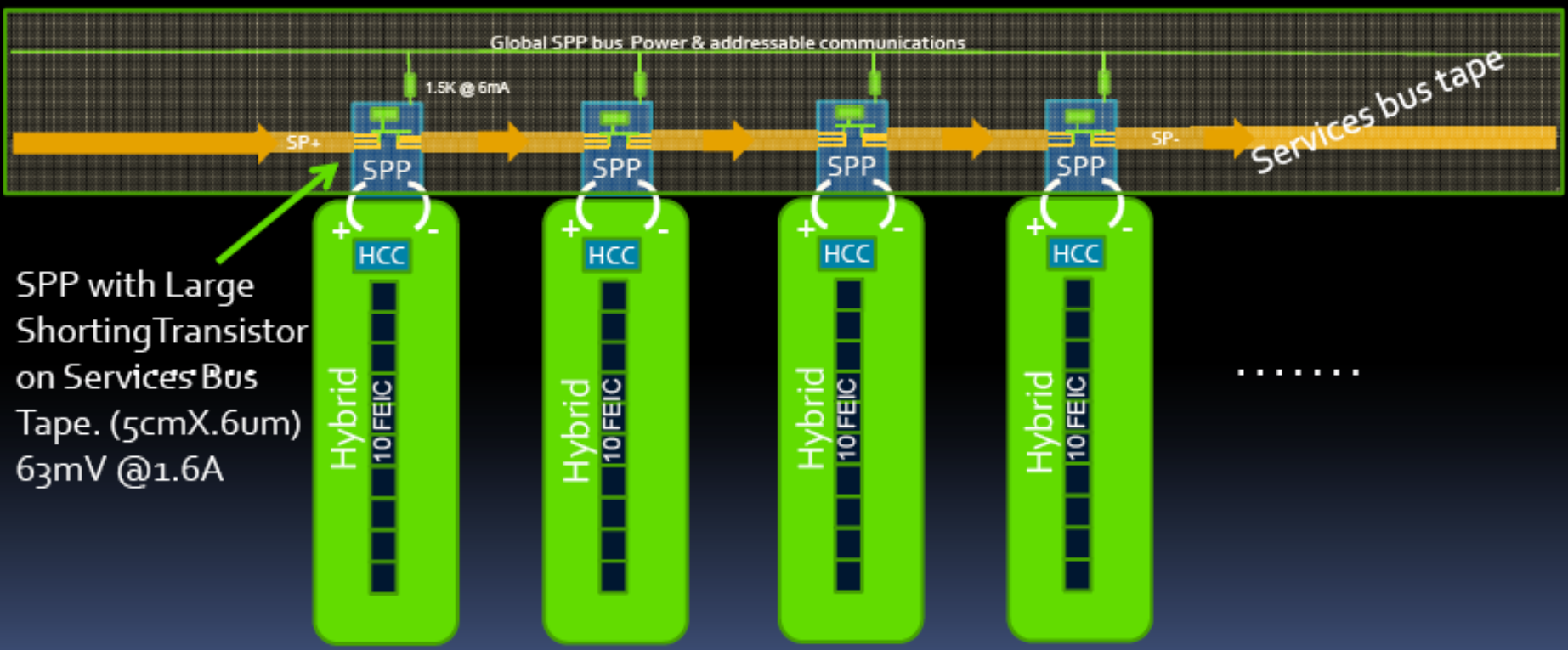
Services bus tape

SPP with Large Shorting Transistor on Services Bus Tape. (5cmX.6um) 63mV @1.6A

SPP   SPP   SPP   SPP

HCC   HCC   HCC   HCC

Hybrid 10 FEIC

. . . .

Summary

- **S**erial Powering shown to be successful at the Module and Stave Level.
- **C**urrent Source operates reliably with a 5A, 2.5V ABCn based Stavelet. (Should be easier to build for a lower current, 1.2V 130nm Chipset.)
- **O**ne wire protection shown to work with Stavelet. Remote addressing works.

- **O**pimization of G&S underway
    1. AC coupled Sensor.
    2. AC coupled signaling.
    3. Need to study coupling of module Reference to EOS reference to minimize common mode.

- Testing of fabricated SPP Control loop including Bandgap, Opamp and hybrid regulation will start in a couple of weeks. Results will feed into submission of first complete SPP ASIC.   Expected in Q2 2011

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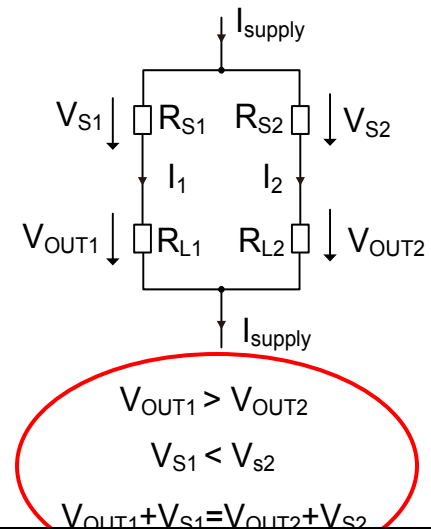# Shunt LDO regulator (Laura Gonella)

- Included in FEI4 and recently tested

- Behaviour well understood

- Good candidate for serial powering of the pixel

Shunt-LDO reminder

Combination of a LDO and a shunt transistor

Shunt-LDO: simplified schematic
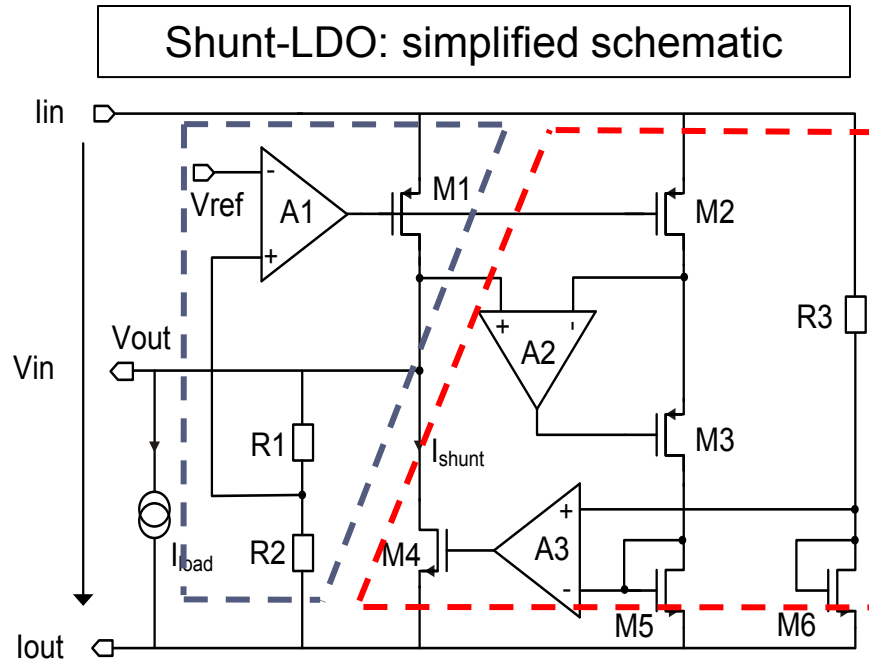
2 Shunt-LDOs in parallel: equivalent circuit

$V_{OUT1} > V_{OUT2}$

$V_{S1} < V_{s2}$

$V_{OUT1}+V_{S1}=V_{OUT2}+V_{S2}$

→ Shunt-LDO can be placed in parallel without problems due to mismatch
→ Shunt-LDO with different V_{out} can be placed in parallel
→ Shunt-LDO can cope with increased I_{in}
→ Normal LDO operation when shunt circuitry is off

Shunt-LDO: voltage generation

Reg2

Reg1
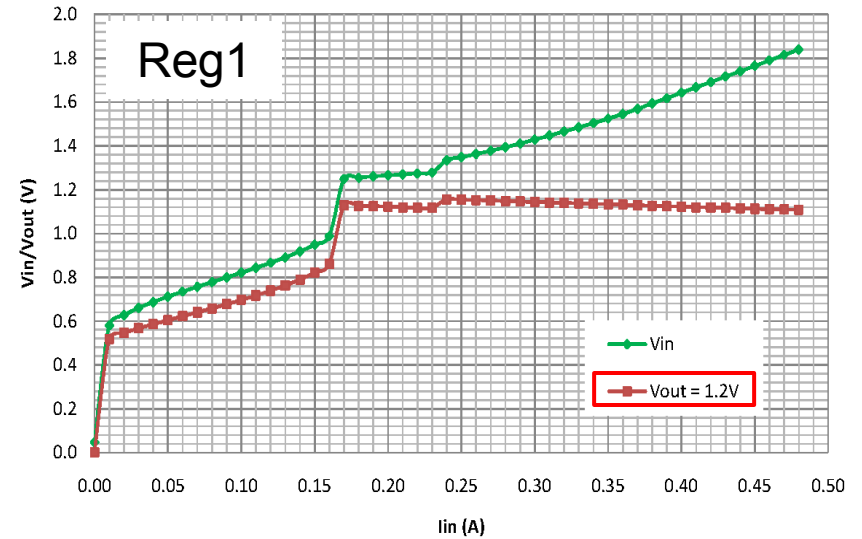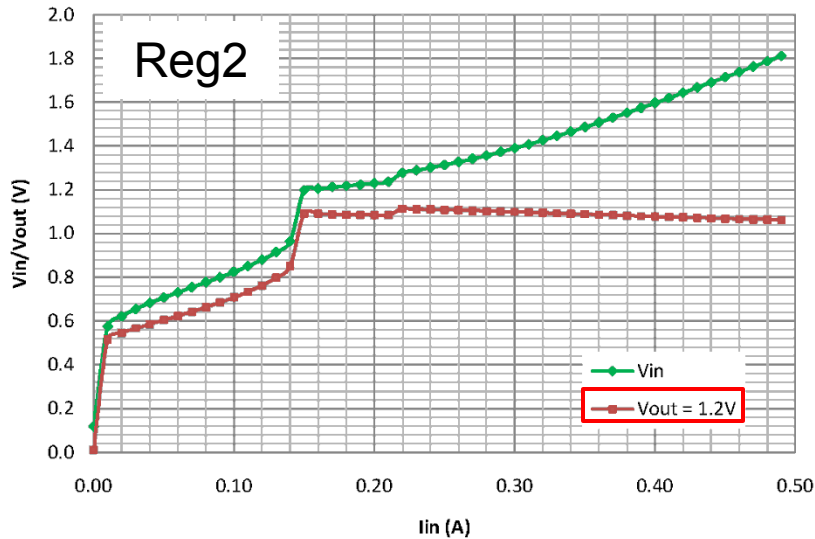
▸ Vout reaches the selected value after saturation of the regulator

▸ Measurement however show differences wrt simulation

  ▸ Abrupt jumps

  ▸ Vout < 2Vref, and decreases with increasing Iin

Simulation[*]
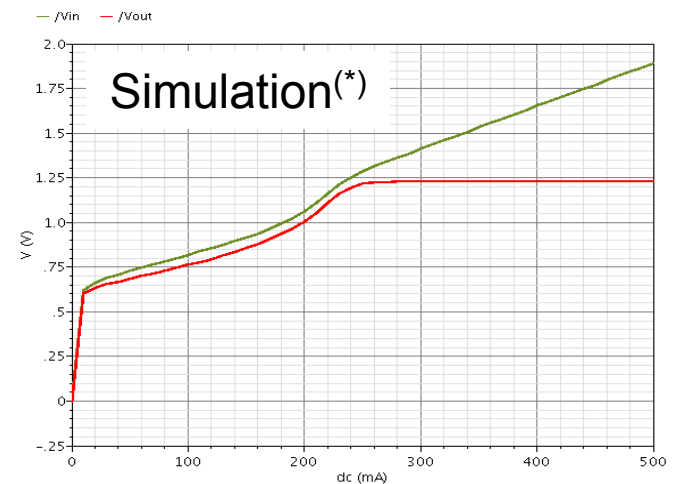
(*) *Shunt-LDO schematics including IO pads*

Conclusion

▸ Both regulators on chip have been operated stand-alone as Shunt-LDO and LDO

▸ Regulator basic functionalities have been asserted

▸ The regulator works fine!

▸ More results to come...

ATLAS-CMS Power Working Group

Switched capacitor DC-DC (Yunpeng Lu)

▸ Included also in the FEI4

▸ Vout / Vin = ½

▸ Some optimisation to be done with respect to noise

Power Options for FE-I4

- Basically the power rail inside FE-I4 are devided into 4 groups and attached to seperate pads:
  - VDDD1/GNGD1, VDDD2/GNDD2, VDDA1/GNDA1, VDDA2/GNDA2
  - In addition dedicated power nets for PLL, EFUSE and T3 isolation as well.
- 3 isolated power modules in the chip.
  - Two linear-shunt LDOs(ShuLDO)-> **Laura's talk.**
  - One switched capacitor DC-DC converter-> **this talk.**
  - Neither is hard-wired inside the chip. Thus Wire connections outside the chip needed.
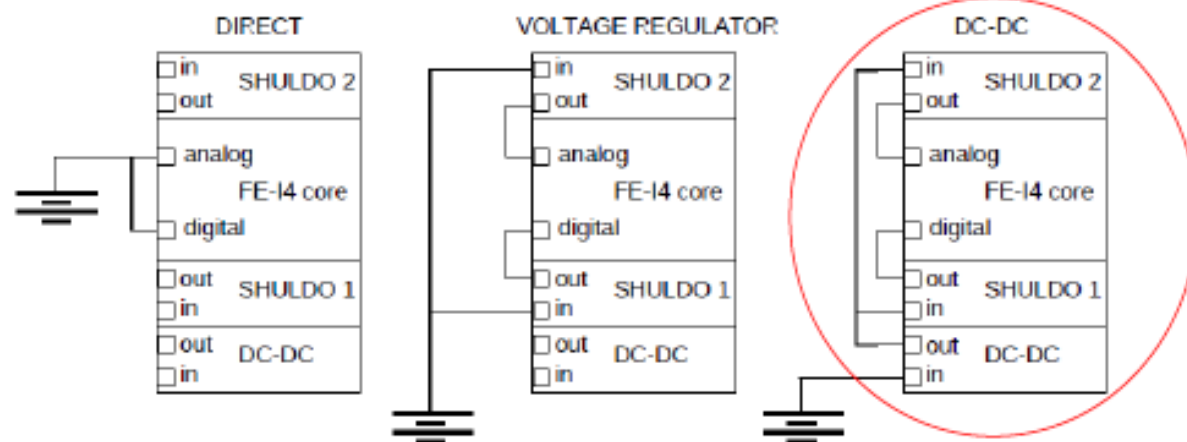
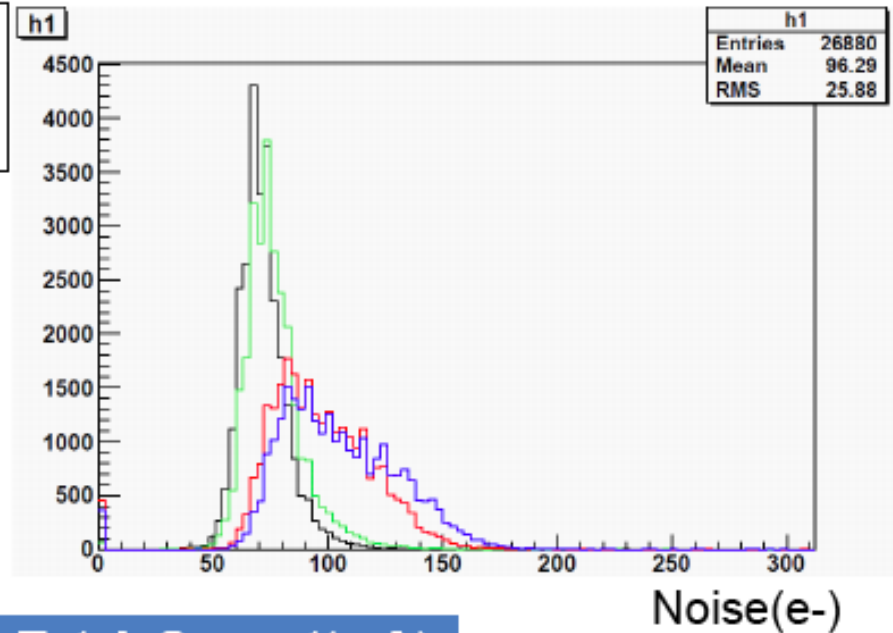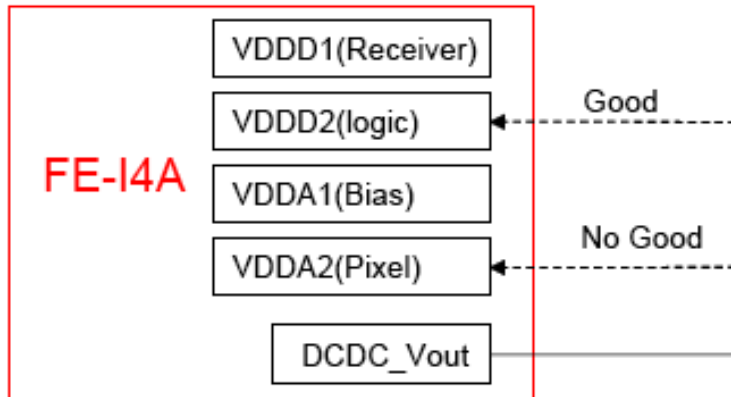(Ground connections not shown)

Efficiency vs Clock frequency

Vin=3.3V, Rload=5Ω
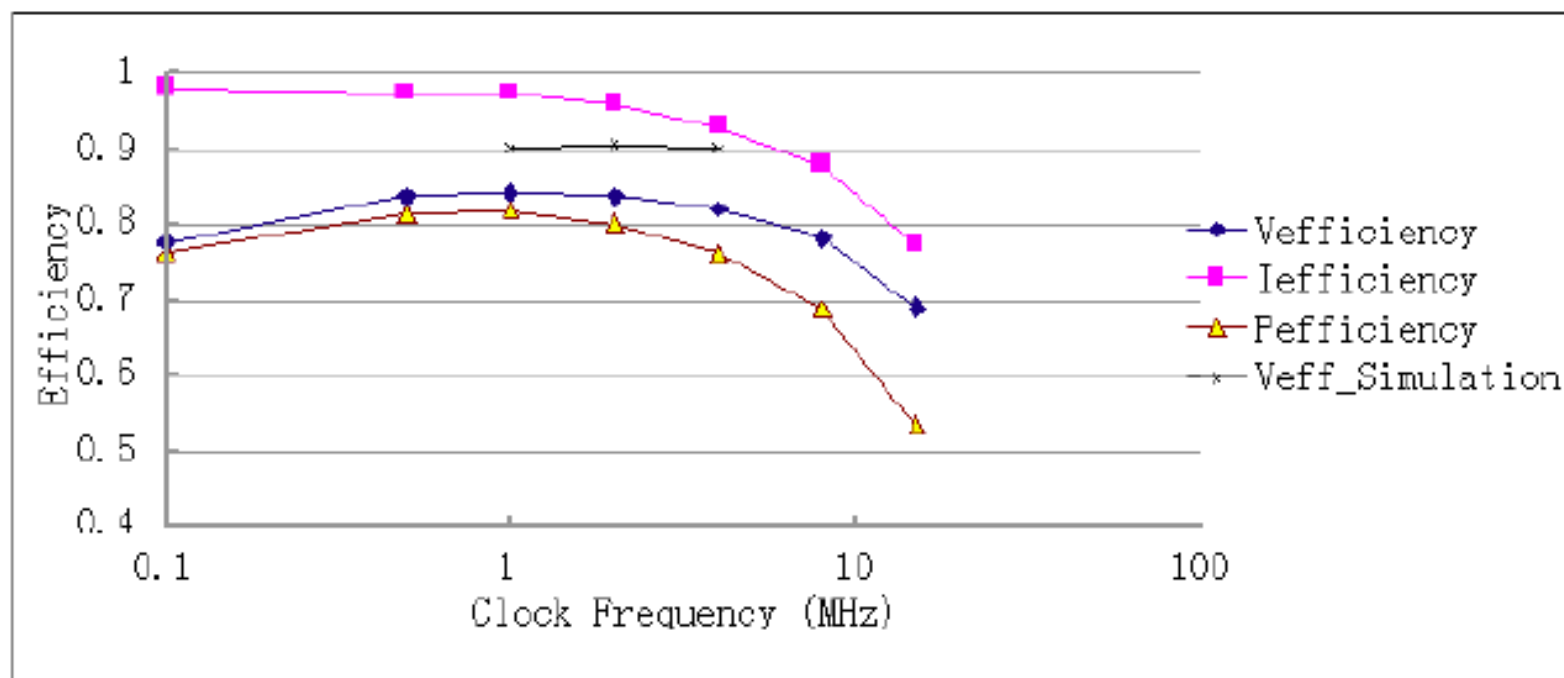
- Simulation result shows Vefficiency around 90%, while the test result shows Vefficiency of about 84%.
- Just take 1MHz as the optimal frequency for the following test.

Noise in Threshold Scan

DC-DC powering analog-->Noise increased; DC-DC powering digtal--> Noise seemed good;

FE-I4A

| VDDD1(Receiver) |
| VDDD2(logic) |
| VDDA1(Bias) |
| VDDA2(Pixel) |
| DCDC_Vout |

Good

No Good

h1	
Entries	26880
Mean	96.29
RMS	25.88

Noise(e-)

Power Scheme	Noise(e−)	Total Current(mA)
External_Power	72	396
DCDC_VDDD2	76	356+27=383
DCDC_VDDA2	96	121+148=269
DCDC_(VDDA2+VDDA1+VDDD2)	104	76+169=245

Is it safe to say: good for digital, but not good for analog?

Well, it depends...

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Conclusion

‣ We have seen that the DC-DC converters are now very much optimised and do not introduce extra noise

‣ We have seen good progress on the serial power side in terms of protection and control

‣ The power working group has only been attended by people from the tracker community

‣ However the work done for getting a radiation hard POL DC-DC converter is in my view very relevant to the calorimeter and muon community