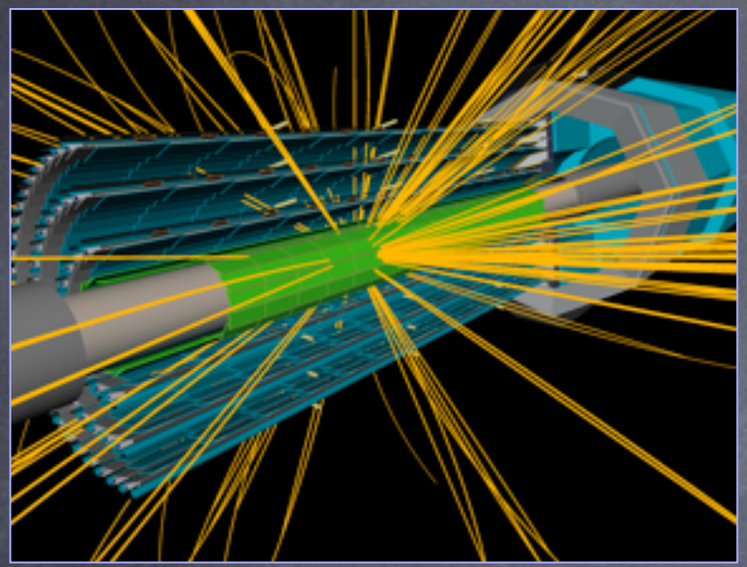
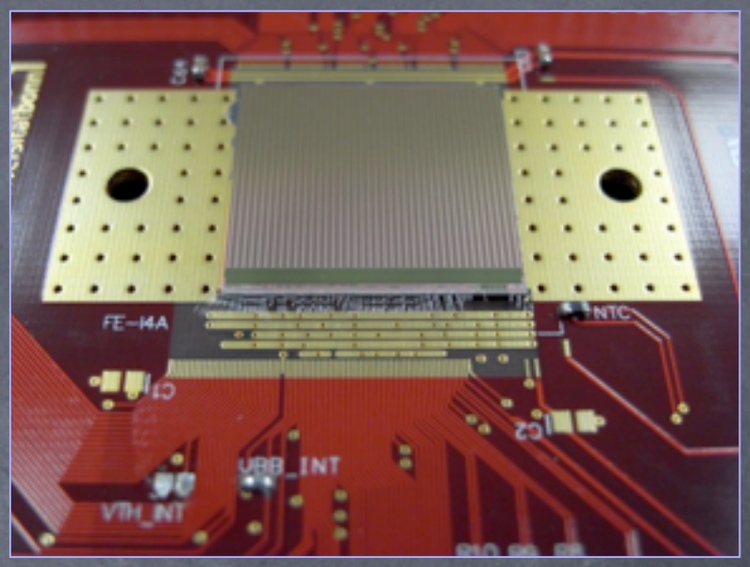




ATLAS - IBL electronics

Roberto Beccherle - INFN Genova

ACES 2011 - 09/11 March

E-mail: Roberto.Beccherle@cern.ch

Insertable B-Layer

- Current plans foresee that in 2013 a fourth Pixel Layer, called Insertable B-Layer (IBL), will be installed in the current Pixel Detector

- Motivations for this project are:

  - Tracking robustness: Adding a new layer compensates for inefficiencies and damages that the present detector will develop in time.

  - Luminosity effects: The current detector copes well up to a peak luminosity of 10^{34} cm^{-2} s^{-1}.
    Higher luminosity (a factor of two is foreseen) will induce pileup and readout inefficiencies potentially affecting the performance of the present detector.

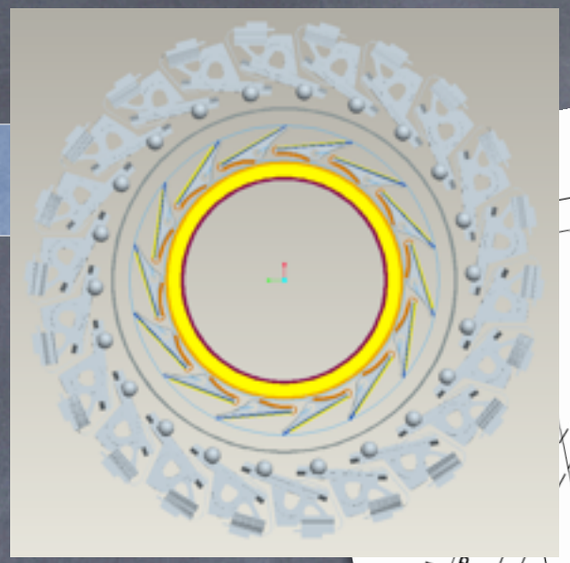
  - Tracking precision: Being closer to the interaction point the quality of impact parameter reconstruction for tracks is improved.

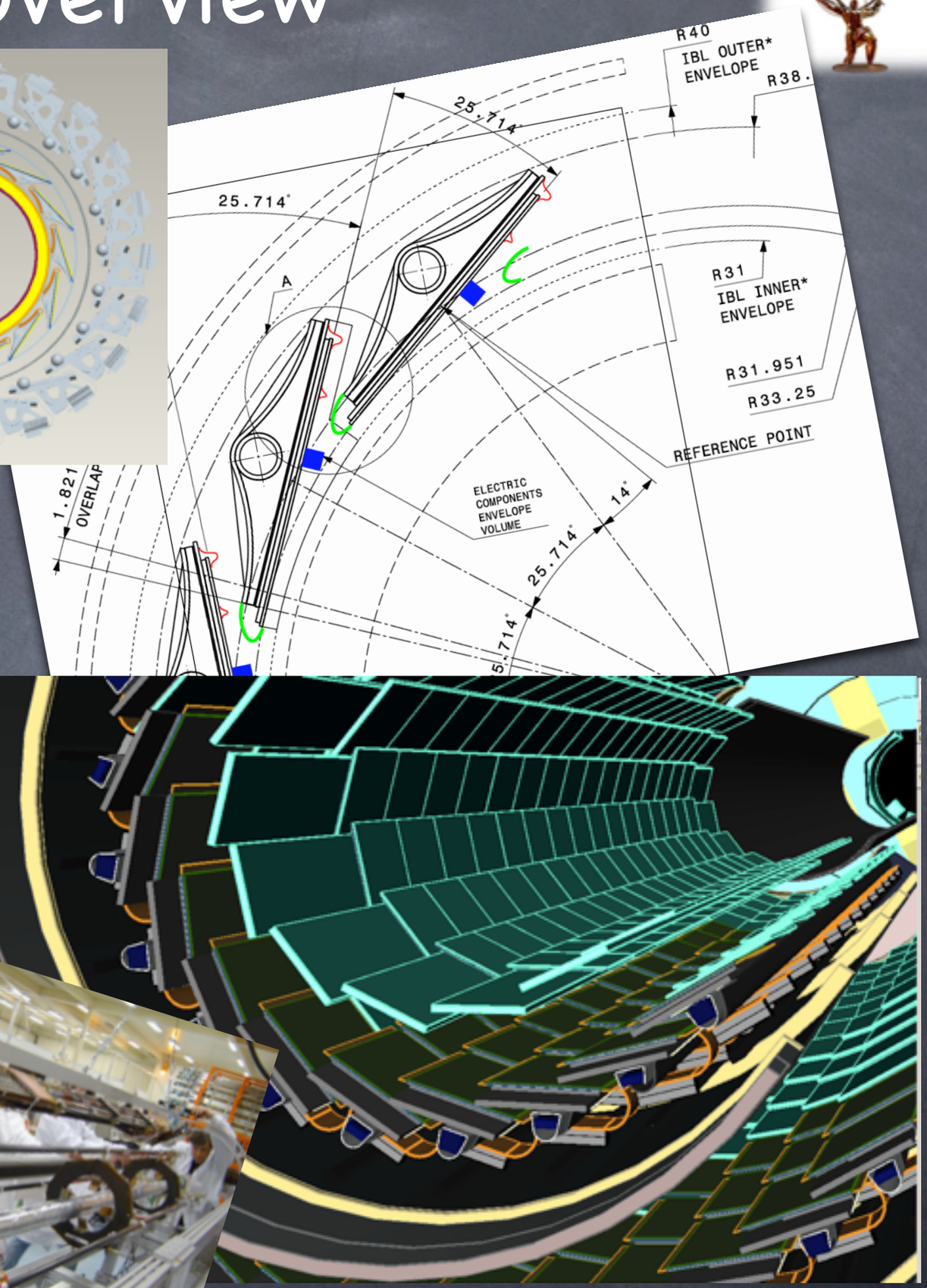
  - Beam pipe replacement: Actual beam pipe is installed together with the detector. The new, smaller beam pipe will only be connected to the IBL, thus allowing faster removal.

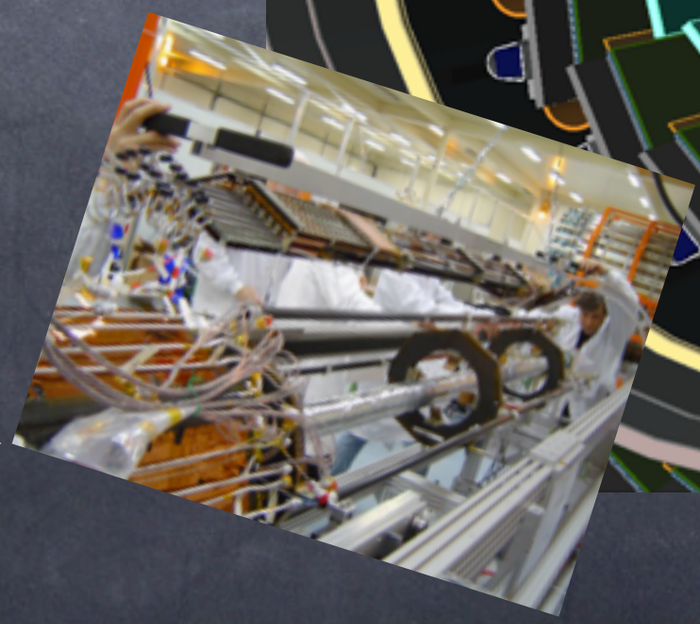
- Being closer to the beam requires new and more rad hard electronics and sensors

System overview

	Value	Units
Number of staves	14	
Stave length	706	mm
Modules per stave	16	
Pixel size (phi, z)	50×250	μm^2
Module active size	40.8×20.4	mm^2
Coverage in η	η < 3.0	degree
IBL nominal radius	33.25	mm
IBL outer envelope	38.3	mm
IBL inner envelope	31.0	mm
Stave tilt angle	14	degree
Sensor thickness:		
Planar silicon	150÷250	μm
3D silicon	230	μm
Diamond	400÷600	μm
Radiation length at z=0	1.54	% of X_0

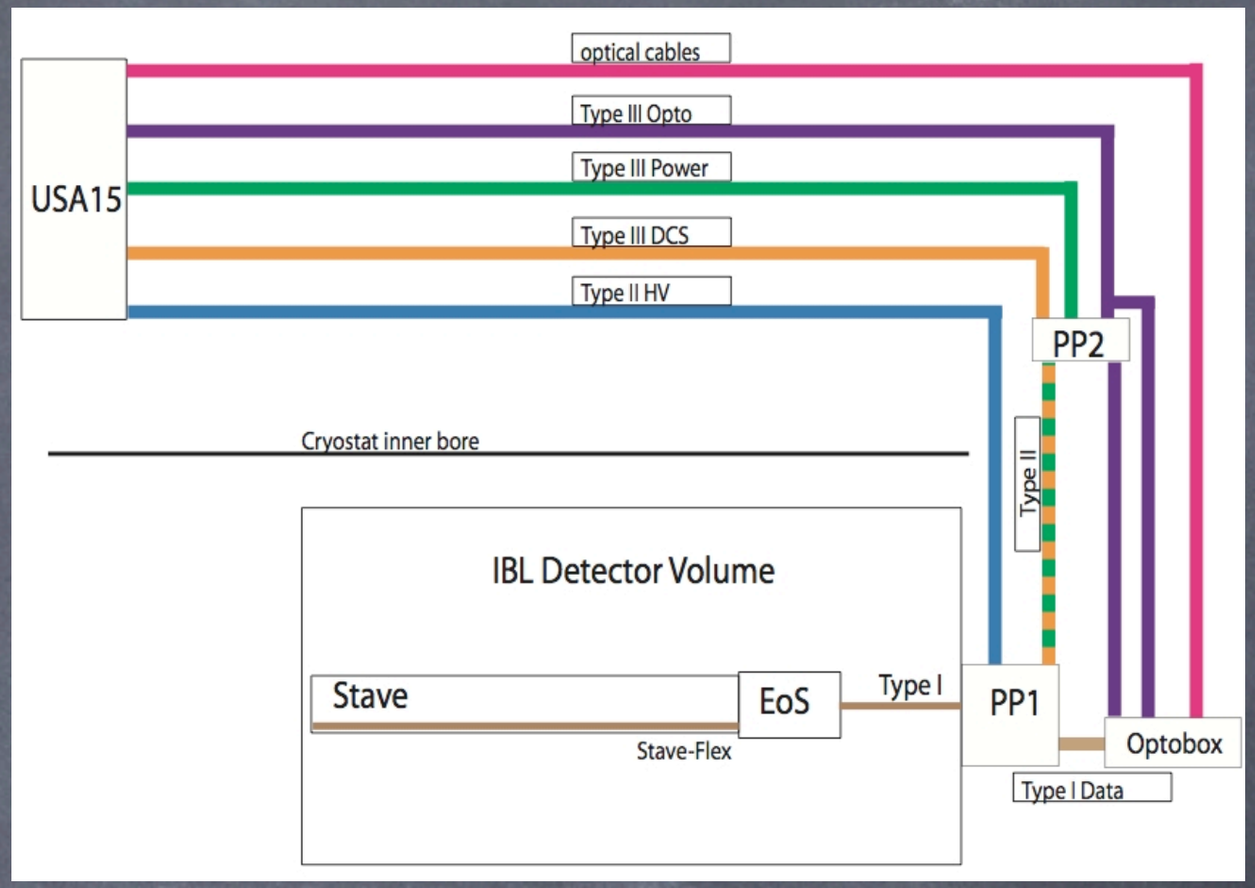






Services

- Rather complicated services and not a lot of space available for routing
- Optical links (data transmission):
  - Baseline foresees VDC and DORIC (inside the optobox) as in the present detector but they are at z=6m.
  - Back Of Crate (BOC) card is located inside USA15.
- High voltage:
  - Operating voltage depends on sensor choice. 1kV foreseen in order to cope with all options.
- Low voltage:
  - Baseline foresees direct, parallel, power supply (small detector, more compatible with present services).
  - Linear regulators or DC-DC converters inside the FE chip are possible options.
- Voltage drops:
  - The design of the cable chain of the IBL is driven by the maximum safe voltage operation of the FE chip, which is designed in 0.13 μm technology.



Service lengths: LV from IP to PP2 ≈ 12 m
Data from IP to Optobox ≈ 8m

Electrical element	Counts (half stave)	Packing form	Rad. length [%]
LV wire	2 x 16	power bundle	1.30
LV sensing	2	power bundle	3.40
Signal data	2 x 17	twisted pairs	0.31
Clock + Command	2 x 17	twisted pairs	0.46
DCS and Env.	2 x 9	twisted pairs	4.00
High Voltage	8	twisted pairs	1.33

Type II cable: (one possible solution)

IBL Type II Cable: Braid Power Return and AWG12 LV

1. Four twisted and jacketed quads of wires XT 2807 CUSN
   - Conductor AWG28
     - Material: tin plated copper
     - Construction: 7 x 0.127 mm nom.
     - Diameter: 0.381 mm nom.
   - Insulation
     - Material: Extruded Poliax
     - Diameter: 0.7 mm nom.
   - Jacket
     - Material: Extruded Poliax
     - Diameter: ~1.9 mm
   - Voltage rating: 250 V AC

2. Four single wires :
   - Conductor AWG12
     - Material: tin plated copper
     - Construction: 91 x 0.203 mm nom.
     - Diameter: 2.15 mm nom.
   - Insulation
     - Material: Extruded Poliax
     - Diameter: 2.9 mm nom.
   - Voltage rating: 600 V AC

3. Five single wires:
   - Conductor:AWG24
     - Material: tin plated copper
     - Construction: 10 x 0.16 mm nom.
     - Diameter: 0.61 mm nom.
   - Insulation: Extruded Poliax
     - Diameter: ~1.48 mm nom.
   - Voltage rating: 1200 V AC

4. Maintaining tape

5. Drain wire AWG28 for external isolated foil shield
   - Details: see Item 1

6. Braided shield and power return
   - Conductor: 17.6 mm^2 (6 x AWG12)
   - Material: tin plated copper

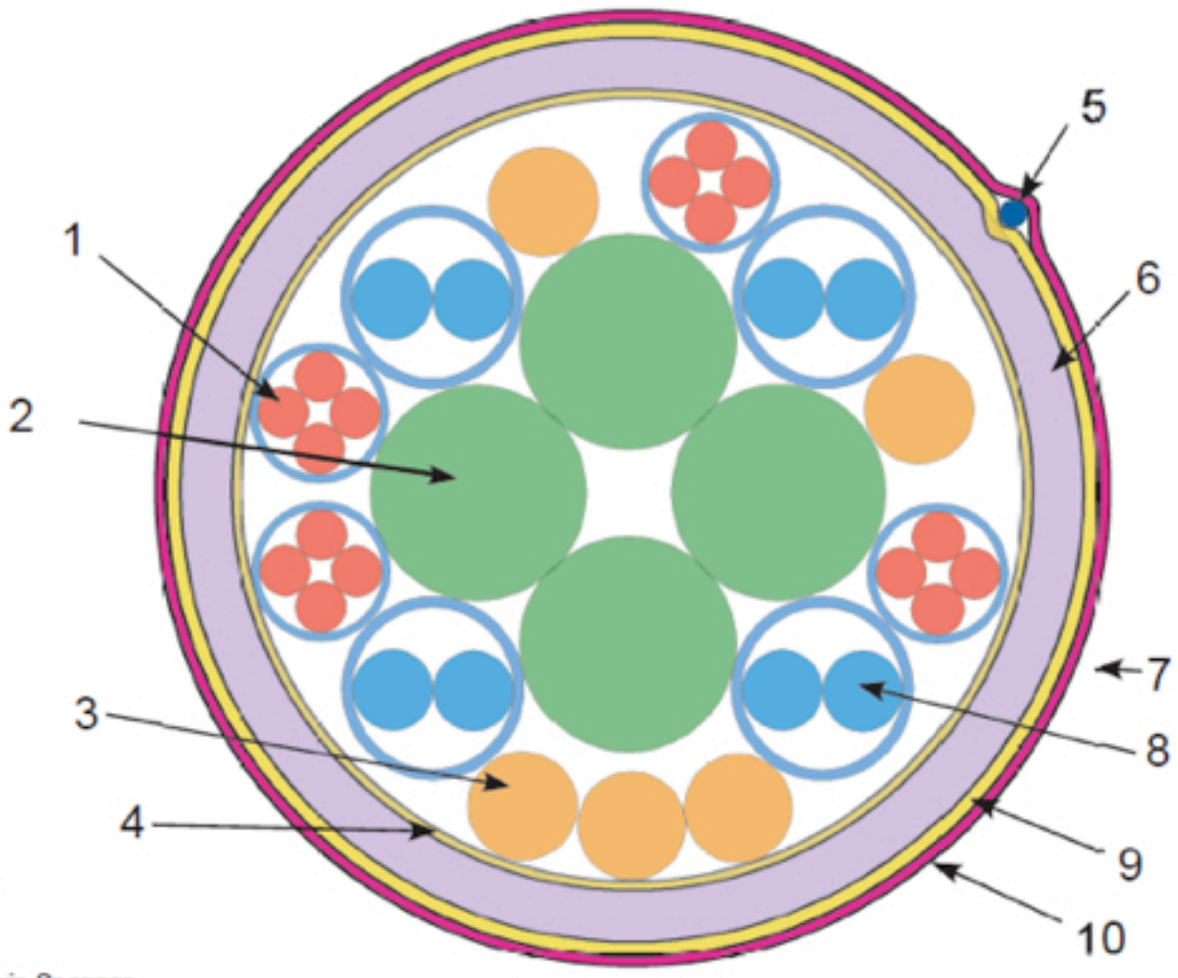
7. Outer Jacket not shown

8. Four twisted and jacketed pairs of wires XT 2807 CUSN:
   - Conductor AWG22
   - Insulation diameter: 0.7 mm nom.
   - Jacket diameter: ~1.9 mm
   - Voltage rating: 250 V AC

9. Isolation wrap for foil shield

10. Foil shield isolated from braid, 50 μm Al thickness

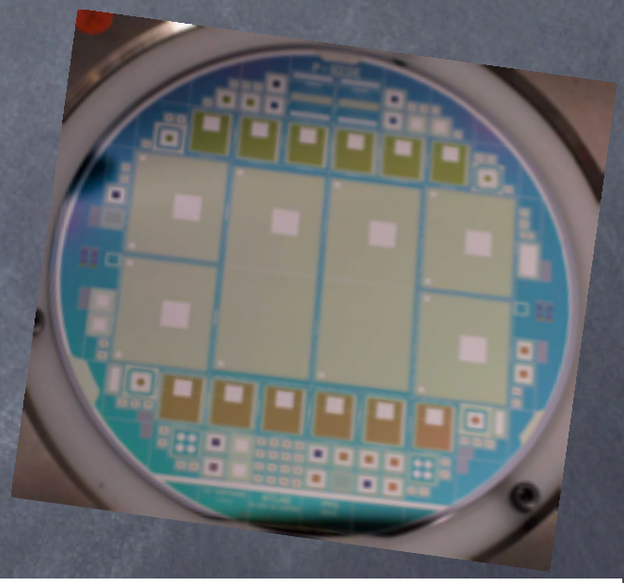
OVERALL diameter with 1 mm jacket: ~13 mm + 2 mm= ~15 mm

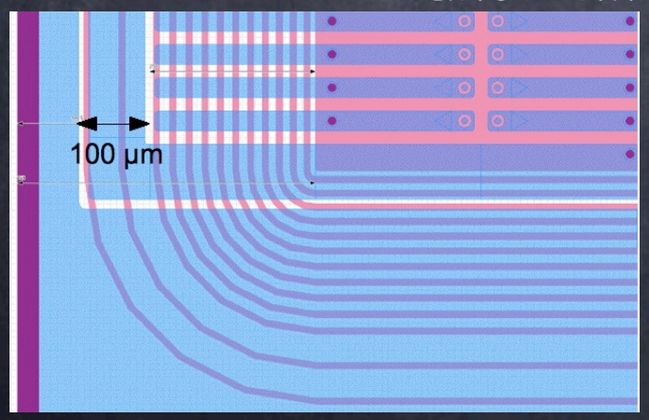


Edwin Spencer
UC Santa Cruz, February 8, 2011

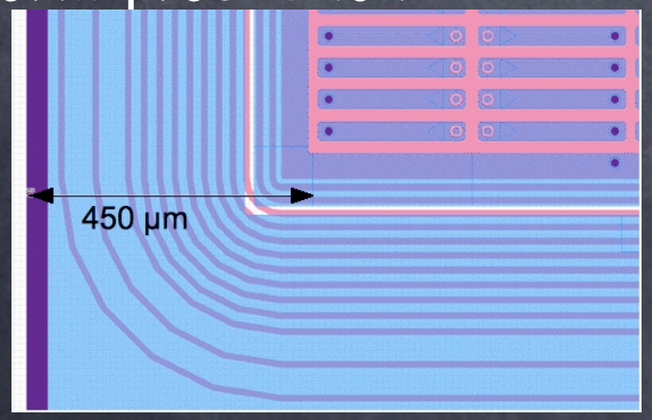
Sensors

- IBL staves do not allow for shielding in z, so geometrical acceptance changes with 1 chip (98.8%) or 2 chip (97.4%) assemblies.
- A critical point for choosing the sensor will be electrical performance with FE-I4 chips.
- Charge collection efficiency with highly irradiated sensors is a critical parameter.
- Three different sensor options are possible for the IBL (Planar, 3D, Diamond)
- Main concerns with all possible candidates:
  - Planar: Radiation tolerances with limited bias voltage, the width of the inactive edge, low operating temperature to avoid termal runaway.
  - 3D: Manufacturability and uniformity on a production run.
  - Diamond: Signal size, cost and uniform production.

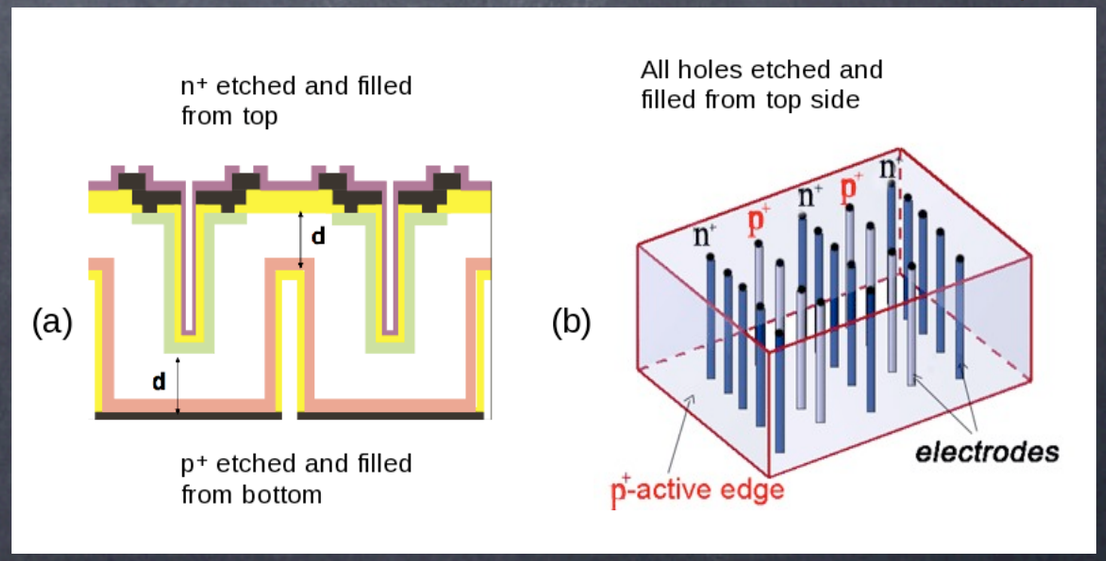




Slim edge n-in-n planar sensor



Conservative n-in-n planar sensor



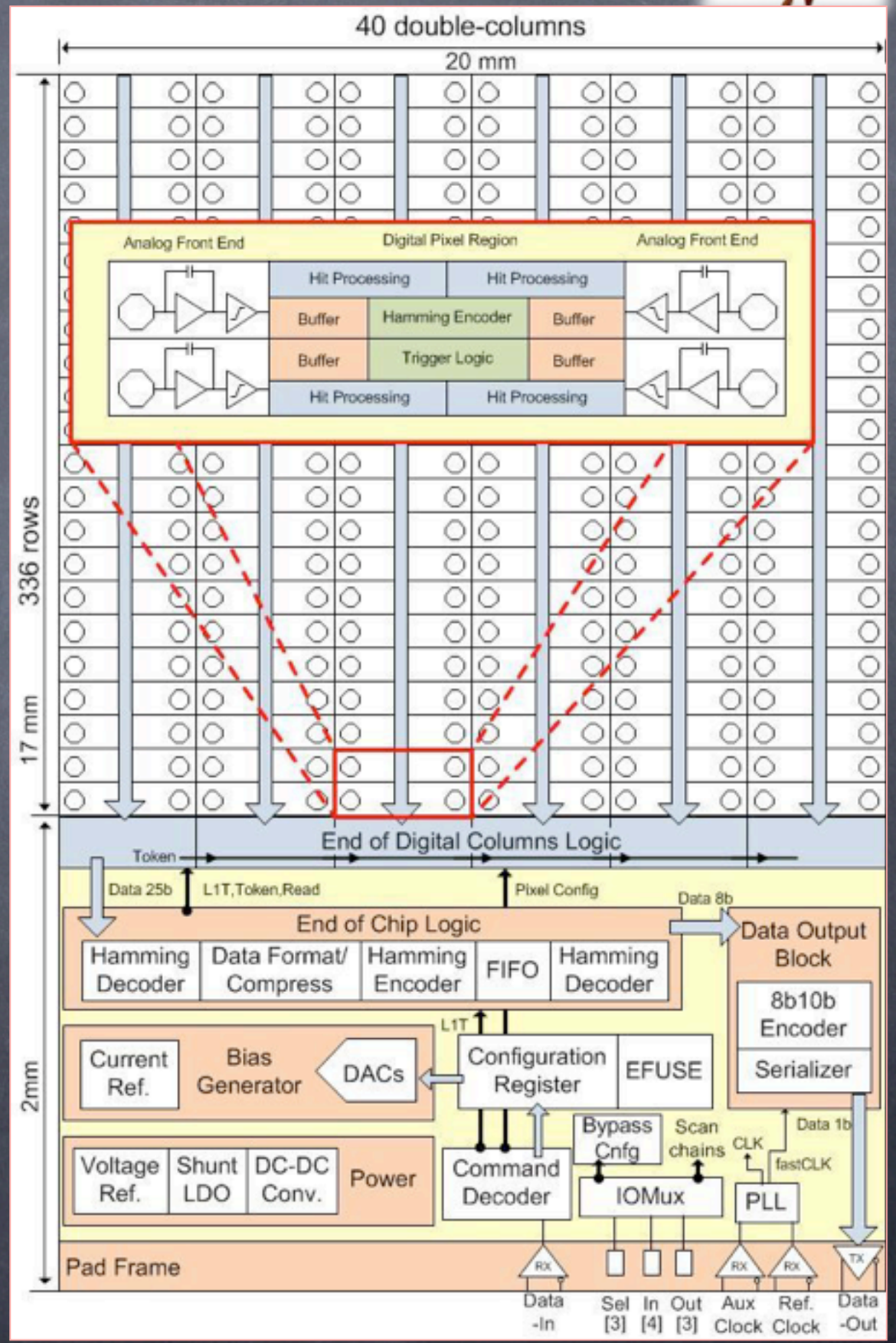
Double sided process (a) and full 3D with active edges (b)

FE-I4: specs and architecture

Basic FE-I4 specs	Value	Units
Pixel size	50 x 250	μm^2
Bump spacing	50	μm
Pixel array size	80 x 336	ColxRow
DC leakage current tolerance	100	nA
Pixel input capacitance (normal/edge)	100÷500/150÷700	fF
Tuned threshold dispersion	< 100	e^-
Charge resolution (ADC method is ToT)	4	bits
Radiation tolerance (with specs met)	250	Mrad
Pixel analog power (with specs met)	15	μW
Pixel digital power (above hit rate)	< 15	μW
Single serial data input (CK + Data)	40	Mb/s
Single serial data output (8b/10b enc.)	160	Mb/s

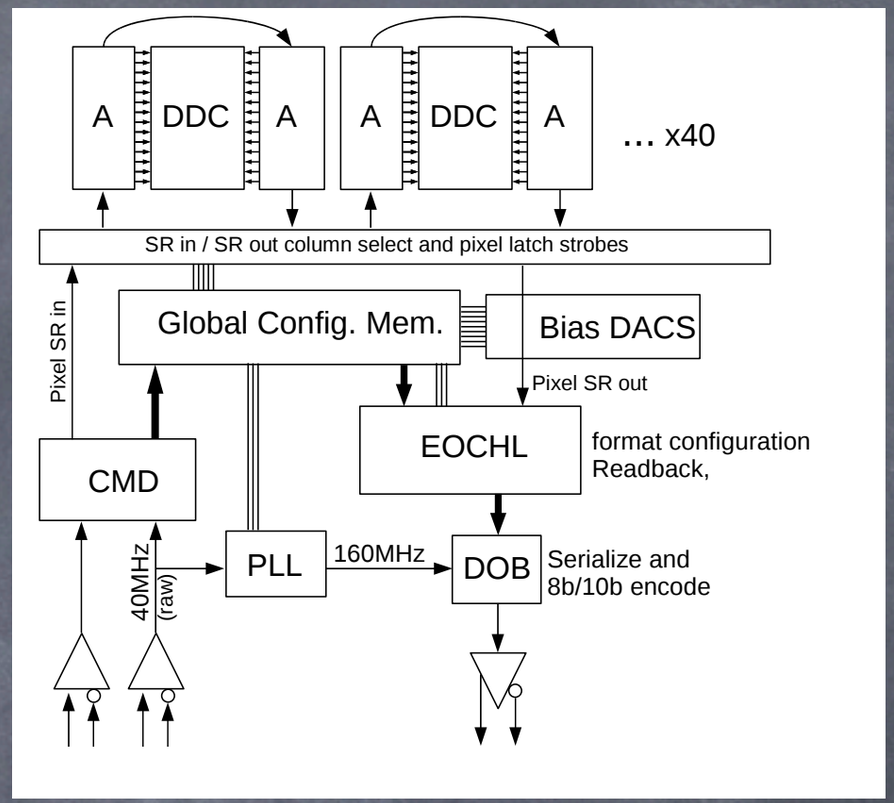
	Value	Linear regulators	DC-DC converter	Units
Min. operating voltage	1.20	1.30	1.30	V
Max. operating voltage	1.50	1.65	3.40	V
Nominal operating current	0.60	0.60	0.31	A
Max. current @ max. V	0.90	0.90	0.46	A
Peak transients allowed	1.75	2.00	4.00	V
Max. V @ power supply	2.10	2.50	4.73	V
Drop allowed in cables	0.60	0.85	1.33	V

Voltage ratings and current consumption of FE-I4



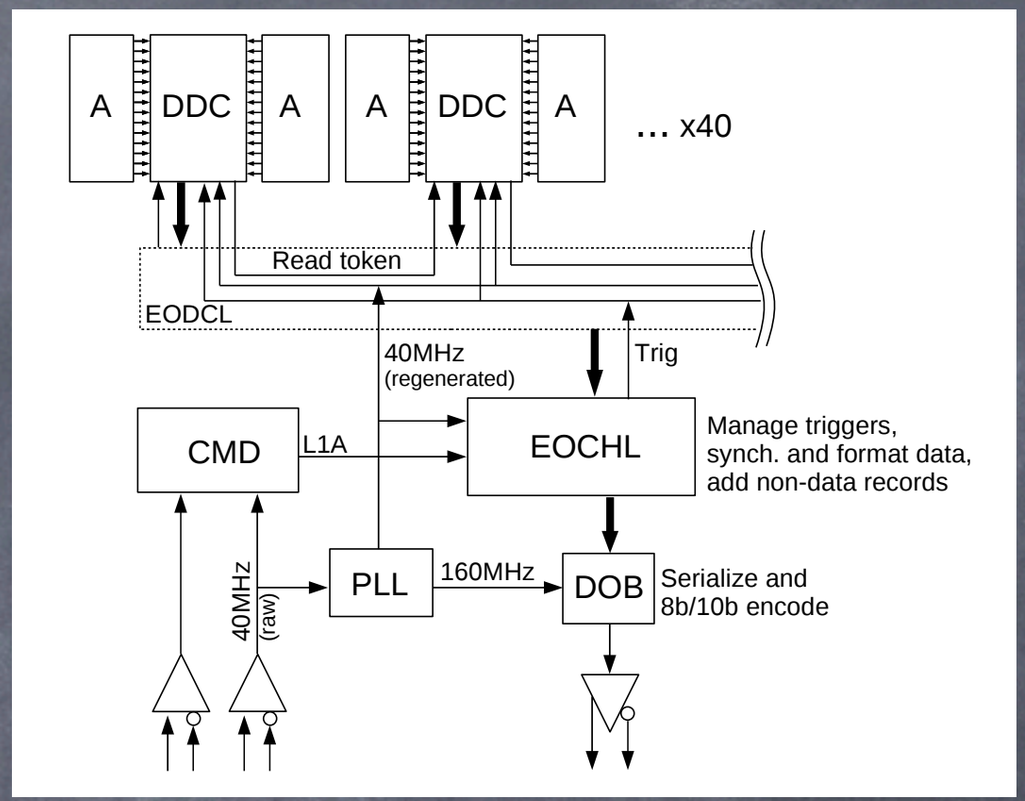
FE-I4: Configuration

- Like present electronics FE-I4 has two different operating modes: Configuration and Data Taking.
- Configuration Mode:
  - The FE is initialized to a low current mode.
  - Global configuration memory is written.
  - Pixels are configured/tuned using shift registers that address any of the 40 double columns.



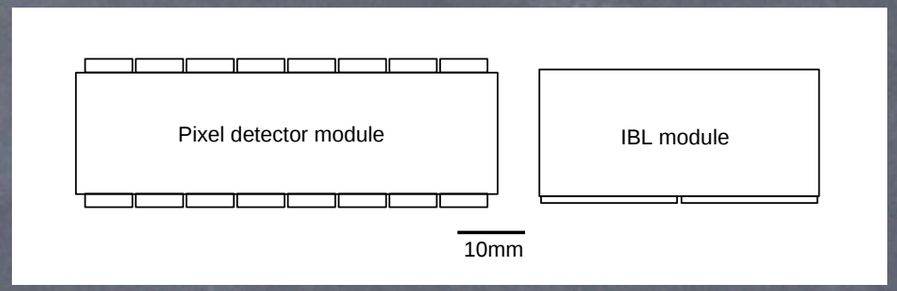
FE-I4: Configuration and RunMode

- Like present electronics FE-I4 has two different operating modes: Configuration and Data Taking.
- Configuration Mode:
  - The FE is initialized to a low current mode.
  - Global configuration memory is written.
  - Pixels are configured/tuned using shift registers that address any of the 40 double columns.
- Run Mode:
  - The FE responds to Trigger and Fast (ECR, BCR and CAL) commands.
  - Data is fetched from the double columns via a Read token.
    All hits matching the time stamp of the Trigger are red out.
  - Data is sent to the Data Formatter, encoded and sent out on a 160 Mb/s data link.
    System messages and/or errors are encoded together with detector data.
  - An internal PLL multiplies the system clock up to 160 MHz.

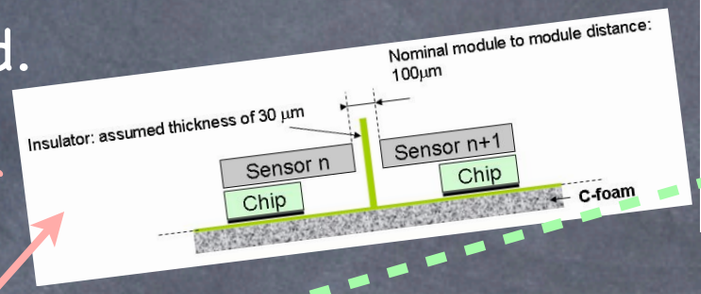


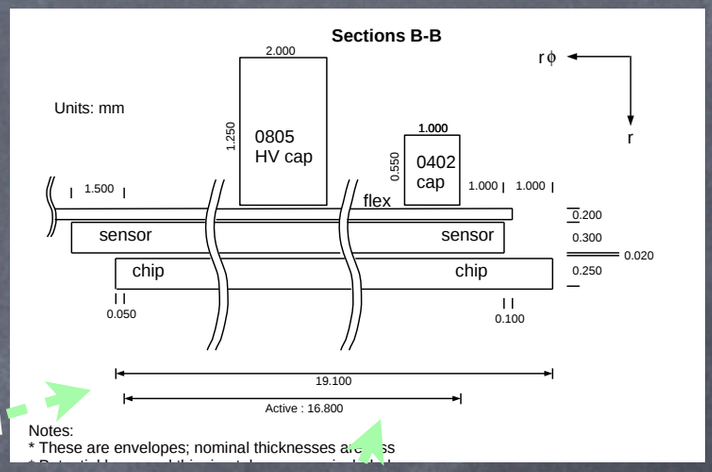
Modules

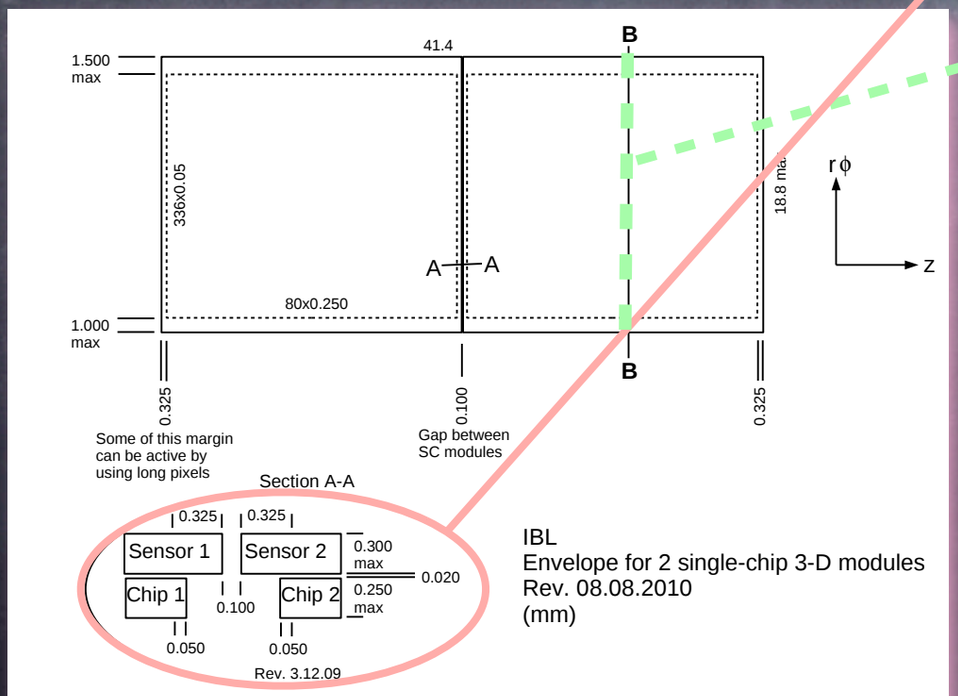
- Depending on the chosen sensor there are two possible modules:
  - Single chip assemblies: One sensor for each FE chip.
  - Double chip assemblies: Two FE chips for each sensor.



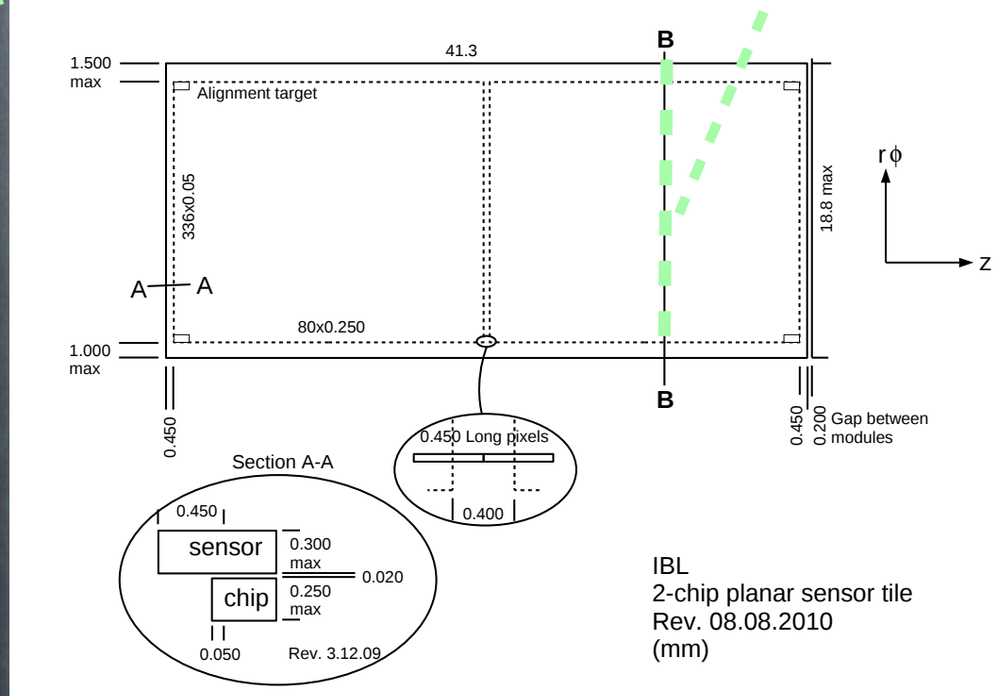
- An electric insulator will be placed in the gap between two adjacent sensors (200 μm for planar and 100 μm for 3D).
- LV supply is organized in groups of 4 FE's. Copper-clad aluminium wires are used.
- HV supply is segmented in one copper wire per two modules.





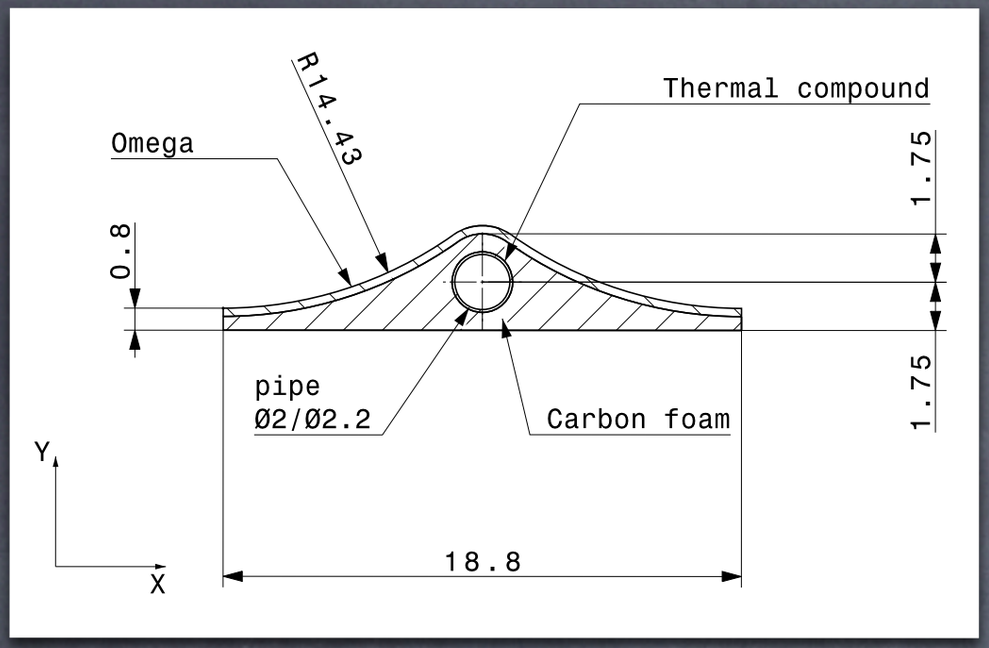


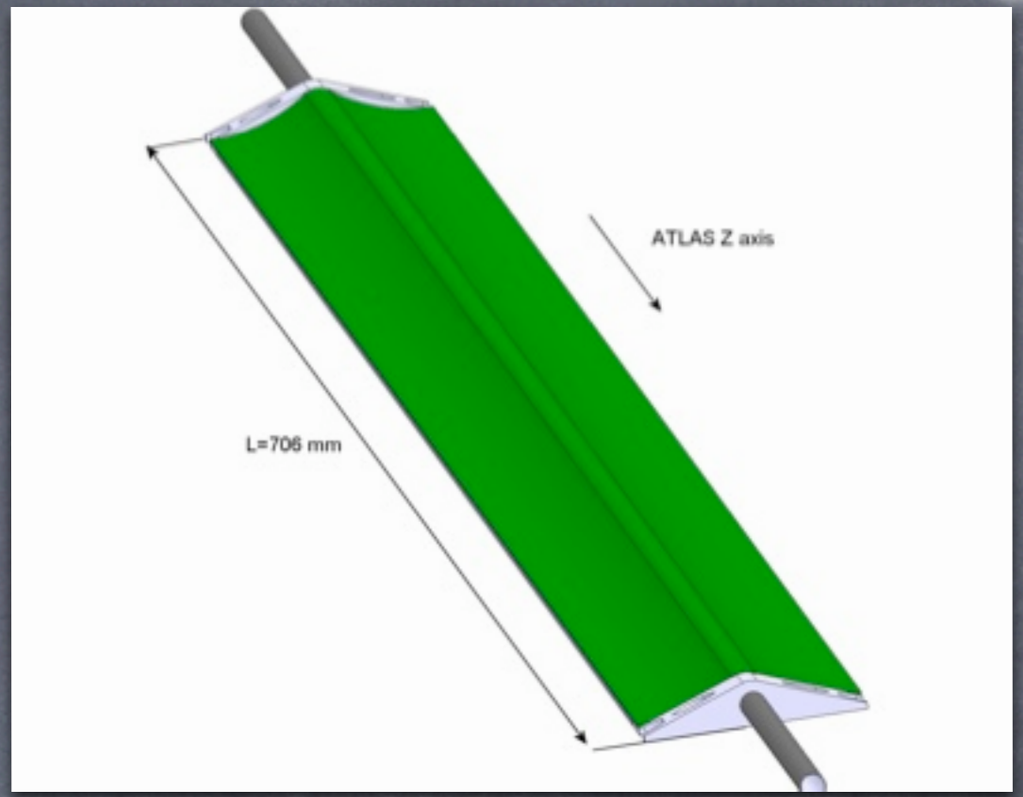
IBL
Envelope for 2 single-chip 3-D modules
Rev. 08.08.2010
(mm)



IBL
2-chip planar sensor tile
Rev. 08.08.2010
(mm)

Staves

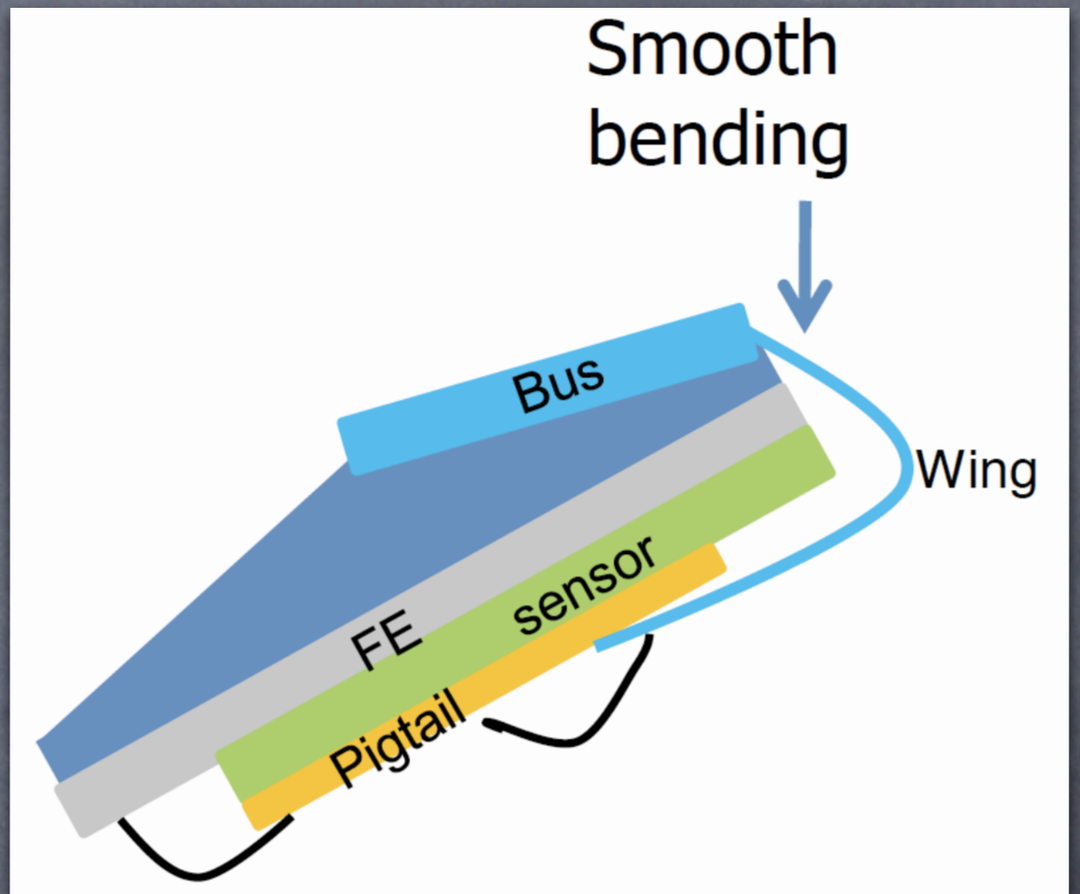


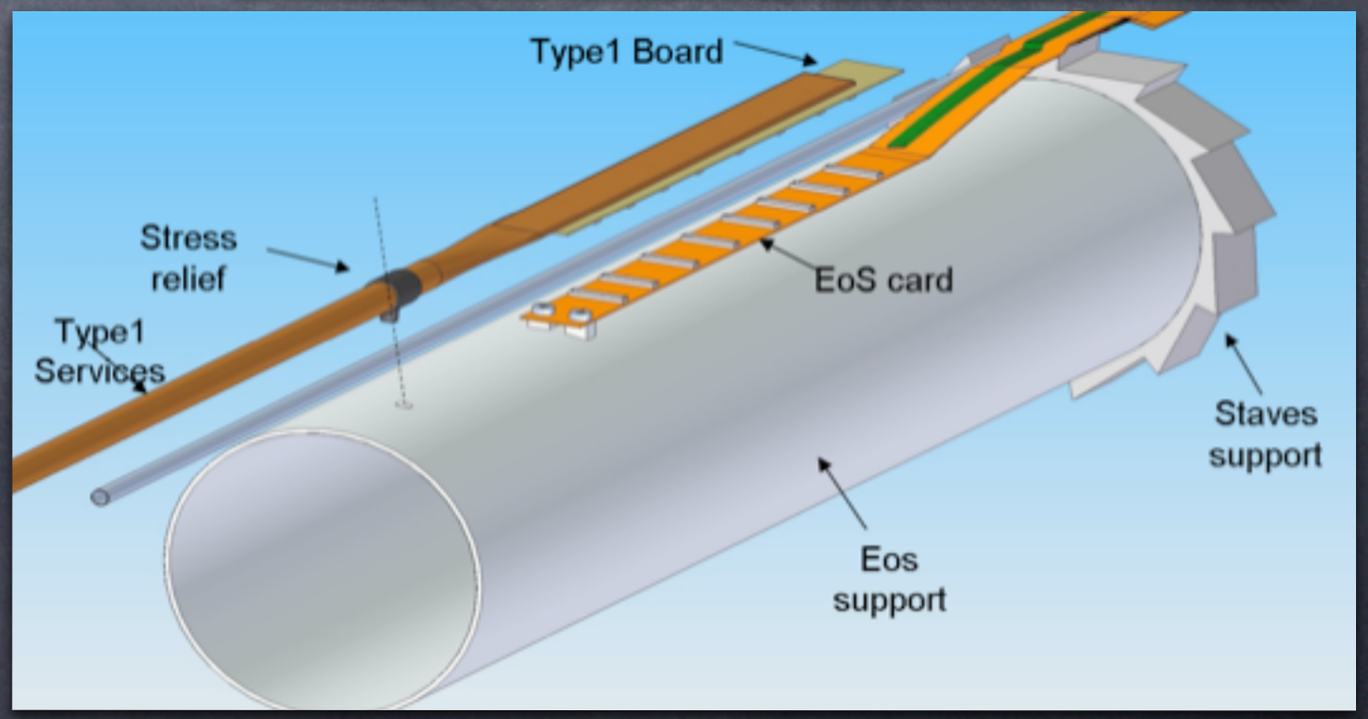


- There will be 14, seven meter long, staves:
  - Made of Carbon Foam (provides termal path between electronics and cooling pipe).
  - CO_2 cooling (74 bara @ 31 ^{0}C, maximum design pressure is 100 bara)
  - Stiffness provided by a carbon laminate Omega
  - Pipe options:
    - 100 μm Titanium pipe --> 300 μm thick Ω
    - 300 μm Epoxy carbon fiber --> 150 μm thick Ω

Type 0 services

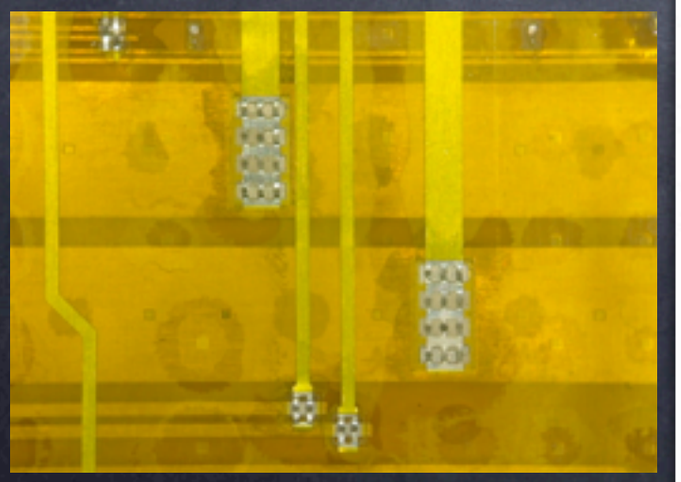
- Due to the material budget and space constraints the services have to be tightly integrated with the stave itself
- Services run on the back side of the stave
- All electrical connections are made from one half stave to the end of the stave
- Flex is connected to the services via a wing which is bent around the stave edge, glued on the module pigtail and wire bonded to it after module loading
- One big challenge is keeping the low voltage drop within FE-I4 budget:
  - LV lines are in Al.
- On the electrical side, data has to be transmitted at 160 Mb/s across the stave to the EoS and then 6 m onwards to the Optoboards at PP1.



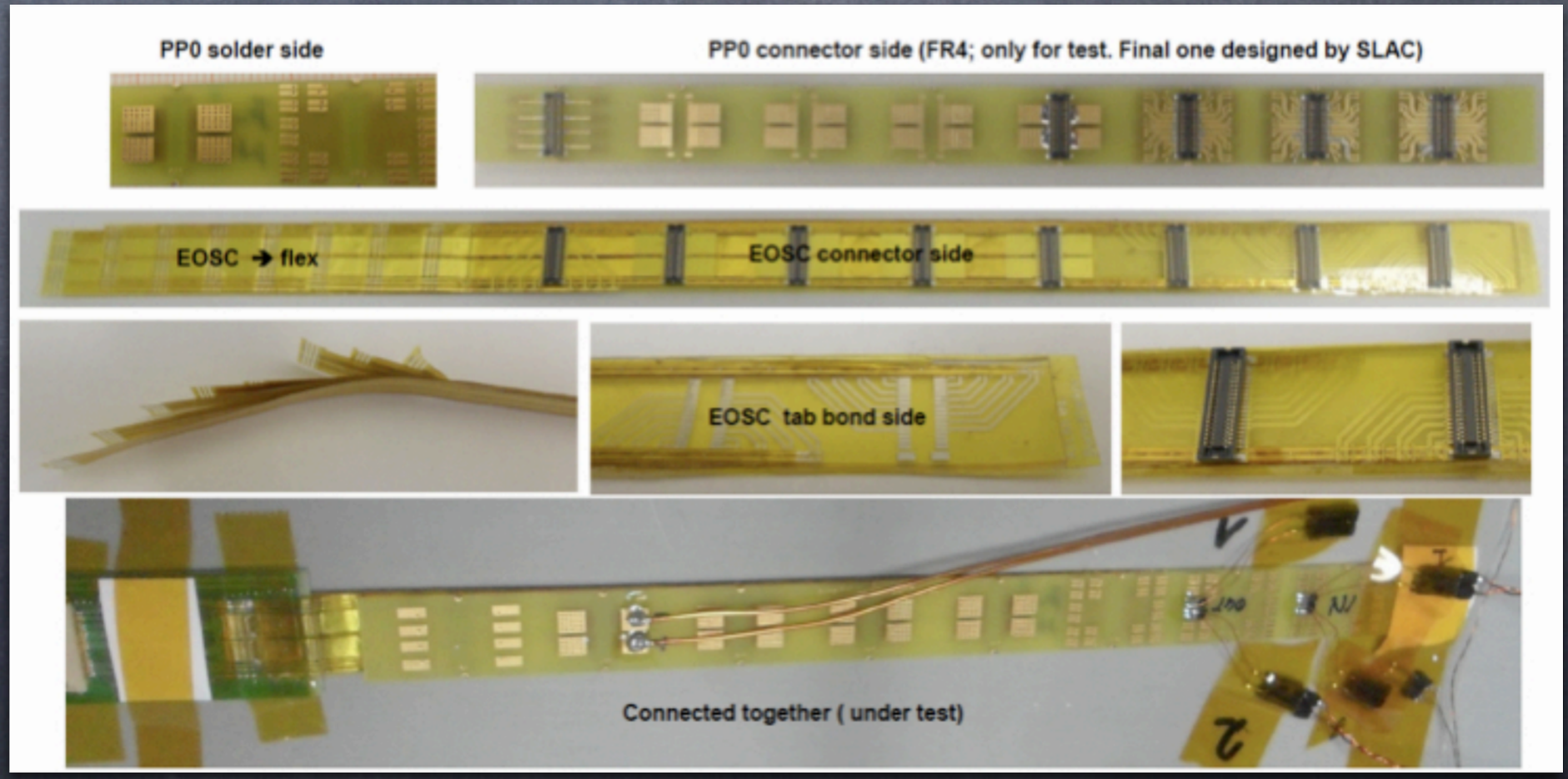


Type 0 services: Bonn option

- Currently there are two different versions of the Type 0 services, based on different technologies in order to solve common issues in different ways...
  - Stack of 8 single layers Al flex FDI 50 (20 µm kapton, 30 µm Al 99.9%)
  - Connection to flex via Tab bonding --> NO vias used !
  - Connector soldered on top --> Tab bond connection on bottom side
  - Need mechanical support for EOSC to open and close

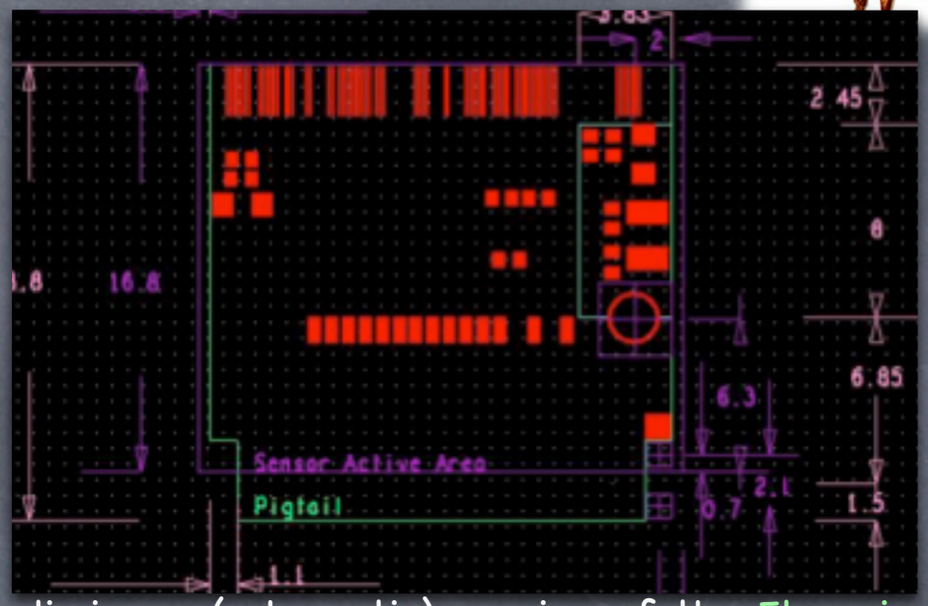


Tab bonding

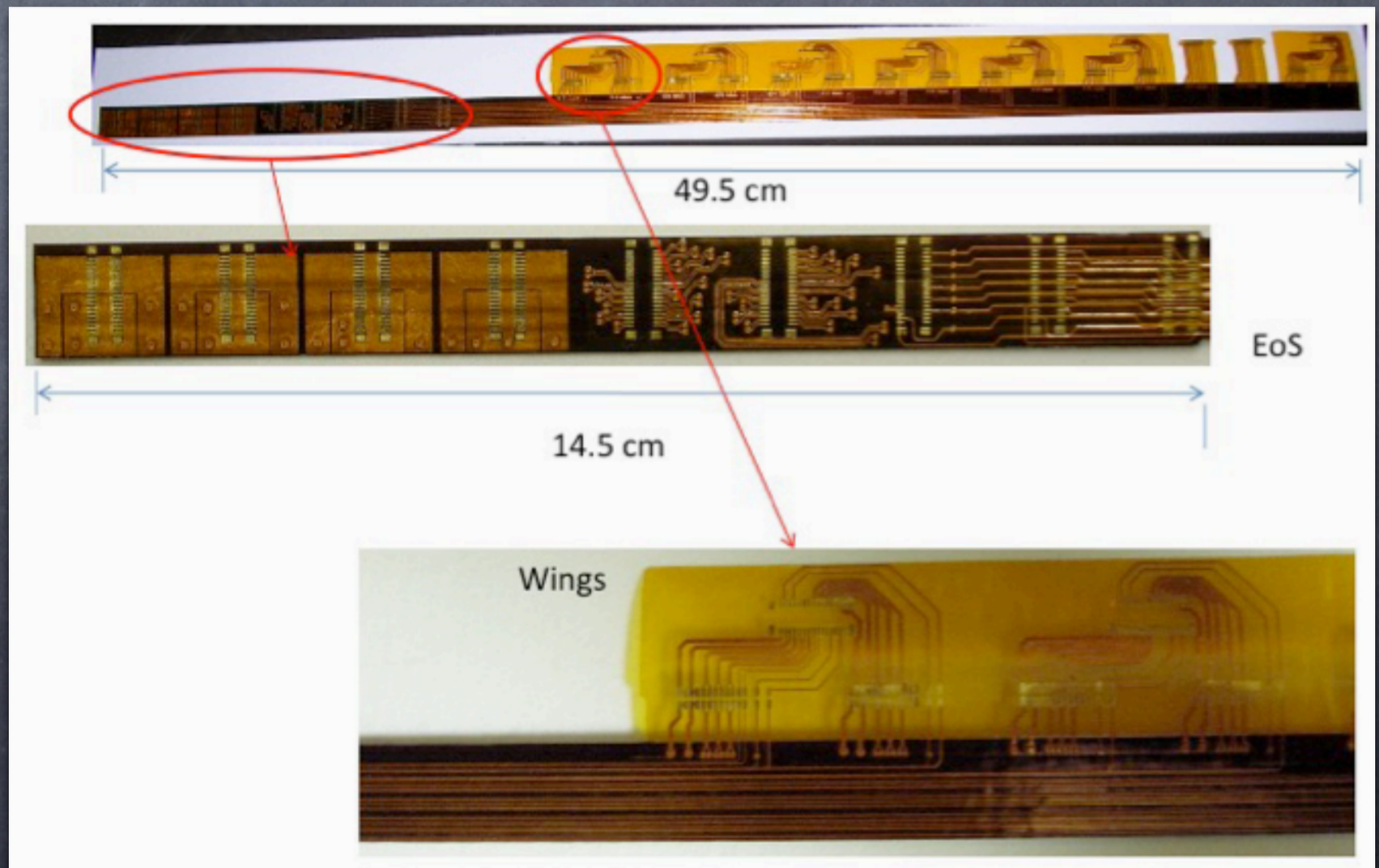


Type 0 services: Genova option

- 2 Al (LV power) and 6 Cu (signals, NTC, HV)
- bottom plane only Power vias–no tracks
- No components foreseen on the flex or the wings
- Design impedance = 80 Ohm
- Total thickness = 470 μm
- x/X0 ≈ 0.3 %



Preliminary (schematic) version of the Flex circuit



- Common interface for the multi-layer and the single layer approaches
- Both options have the same connectors at the EoS

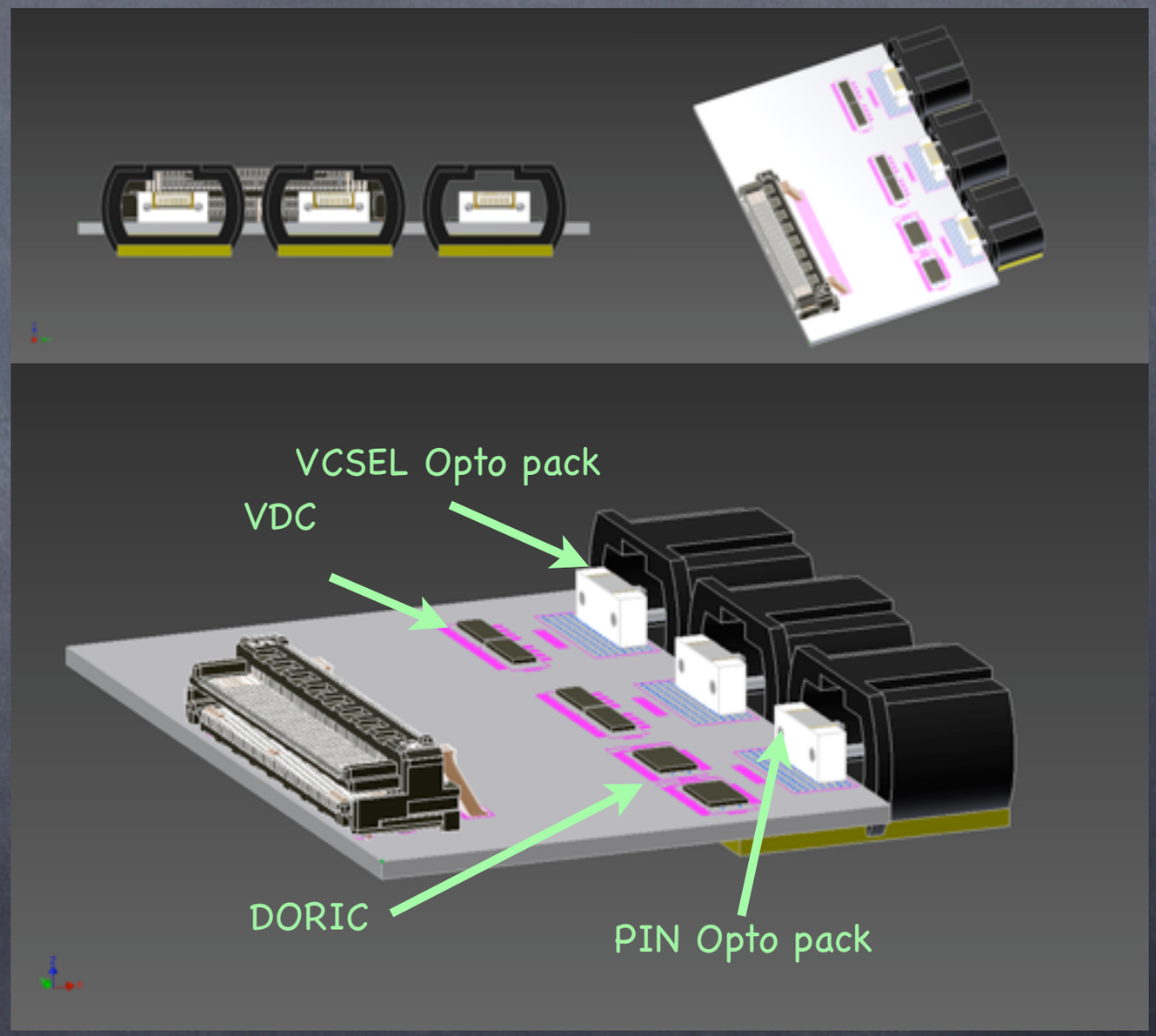
Opto boards

- new Service Quartel Panels (nSQP) project implies to rebuild the current Opto-boards. The project is developed to address possible ageing problem detected for the light emitting VCSEL'S used for data transport. The most probable cause is humidity.
  - This drives also development of the new Opto-boards for IBL.

- nSQP opto-boards have 7 links:
  - use 80 pin connector just like current pixel opto-board

- IBL opto-boards have 8 links:
  - use 100 pin connector

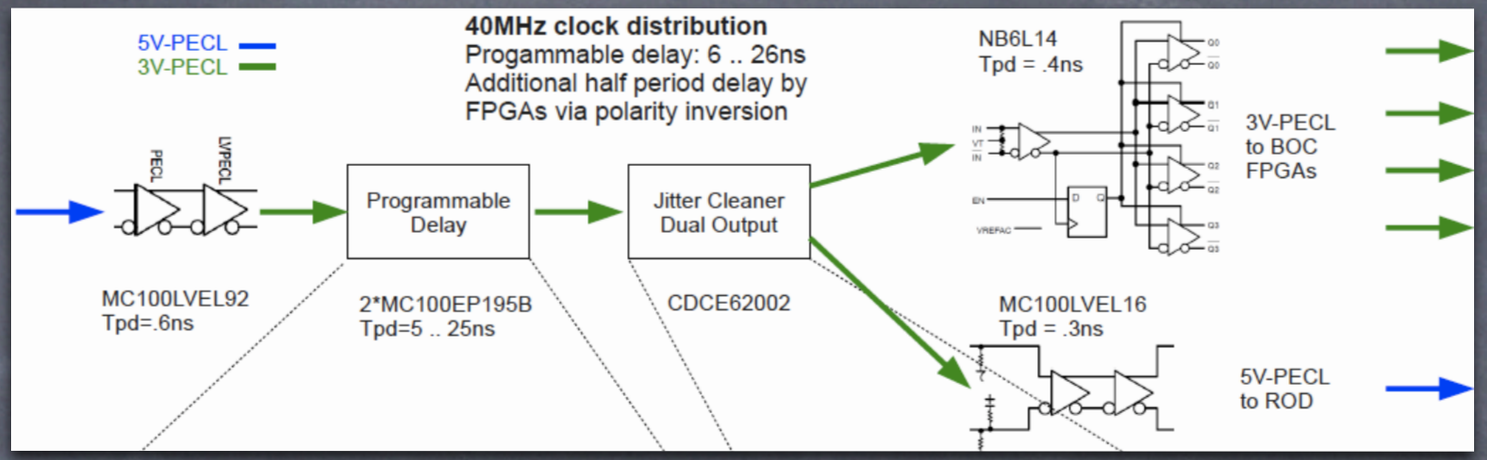
- The connection between the on-detector optical components, (opto-boards), and the off-detector components, (TX- and RX-plugins), will be done by optical fibers.



- Downlink is BPM encoded ck/data at 40 Mb/s, uplink is 160Mb/s with 8b/10b encoding.

BOC

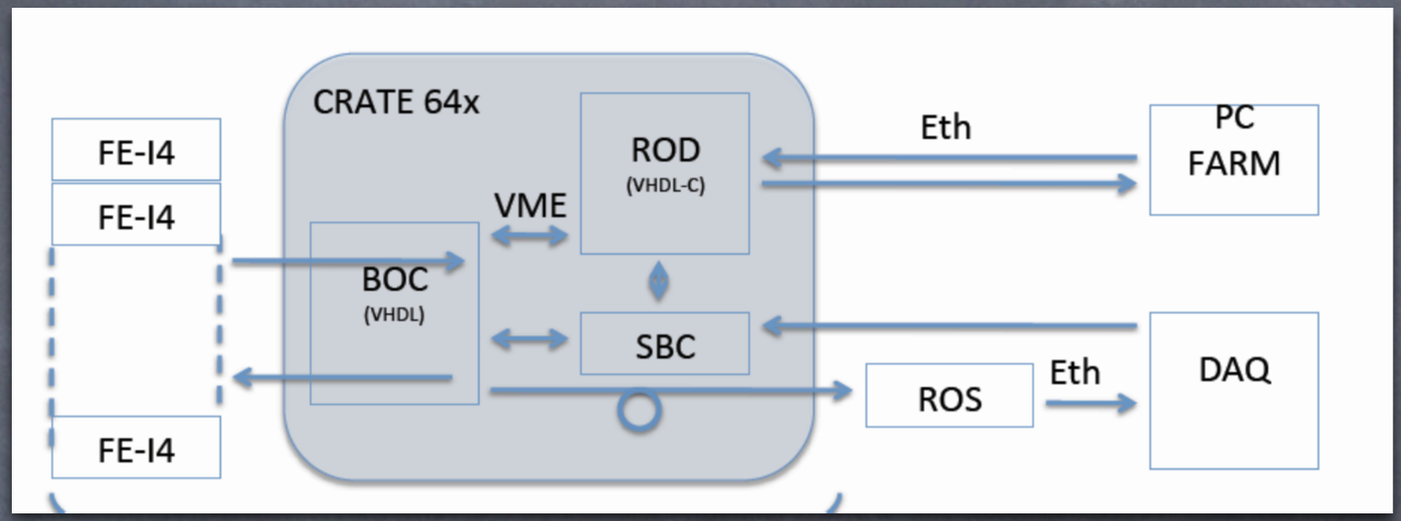
- Back of Crate card plugs to the Read Out Driver (ROD) and has to fulfill some important tasks:
  - Clock distribution (programmable delay + Jitter Cleaner).
  - Tx timing: Bi Phase Mark (BPM) encoding and Mark Space Ratio (MSP) adjustment will be moved inside the new BOC [new Spartans have 300 ps delay elements].



  - Rx side: Clock alignment, decode 8b/10b data, multiplex one 160 Mb/s data stream into 4 parallel 40 Mb/s streams to be fed to the ROD.
  - Provide 2 S-Links [now supported by Spartan FPGA's] @ 2 Gb/s.
  - Dual HOLA for FastTrack (FTK) support.
  - There will be an analog ELMB on the BOC to measure currents and voltages and monitor the temperature.
- First Verilog models of the board are being developed in order to allow full simulation of ROD/BOC system

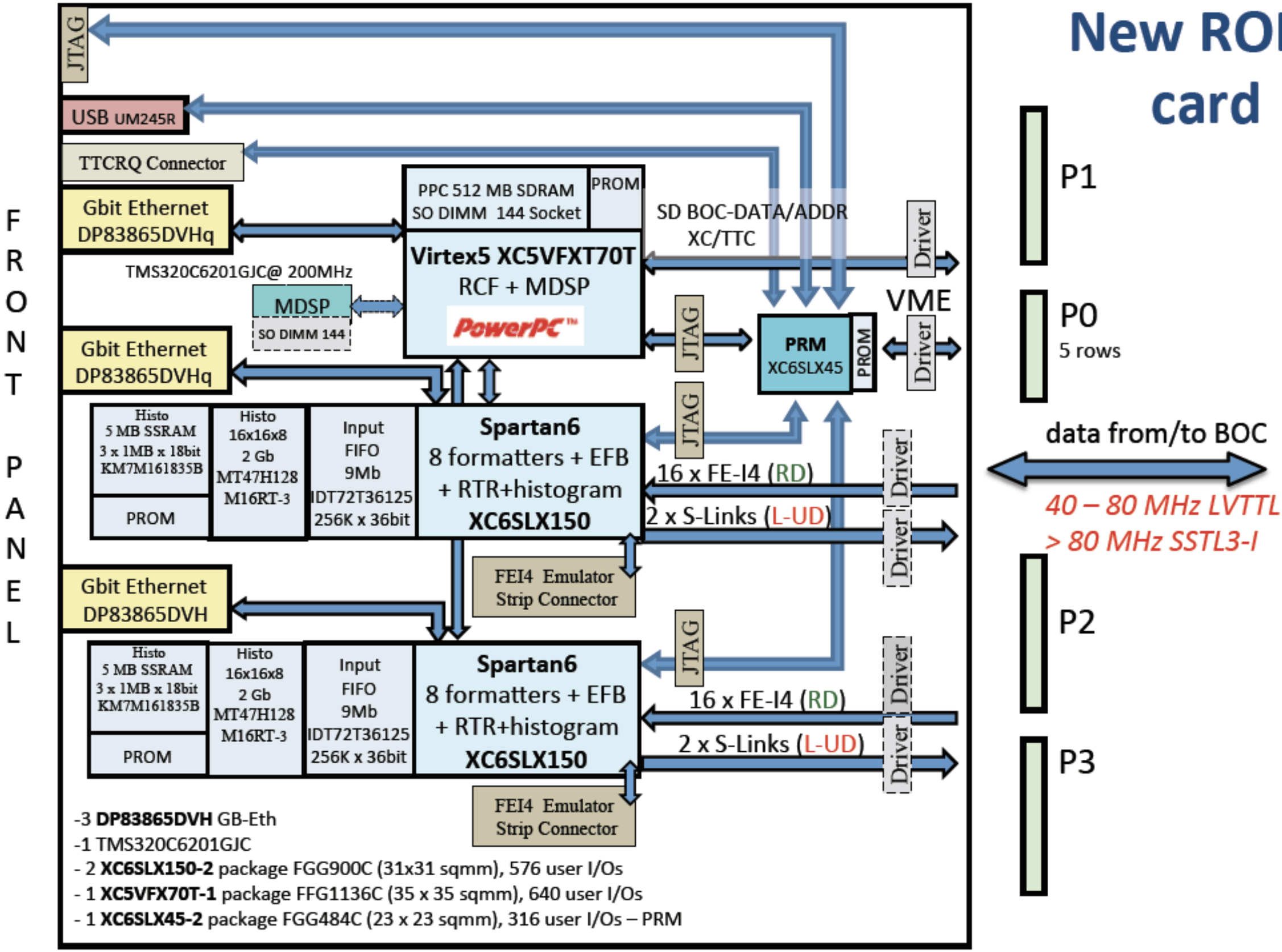
ROD

- A new Read Out Driver (ROD) VME card is being developed for the IBL:
  - New hardware allows, in principle, a simpler design as FPGA's have evolved a lot.
  - No need for the Master DSP! FPGA + PowerPC core will do.

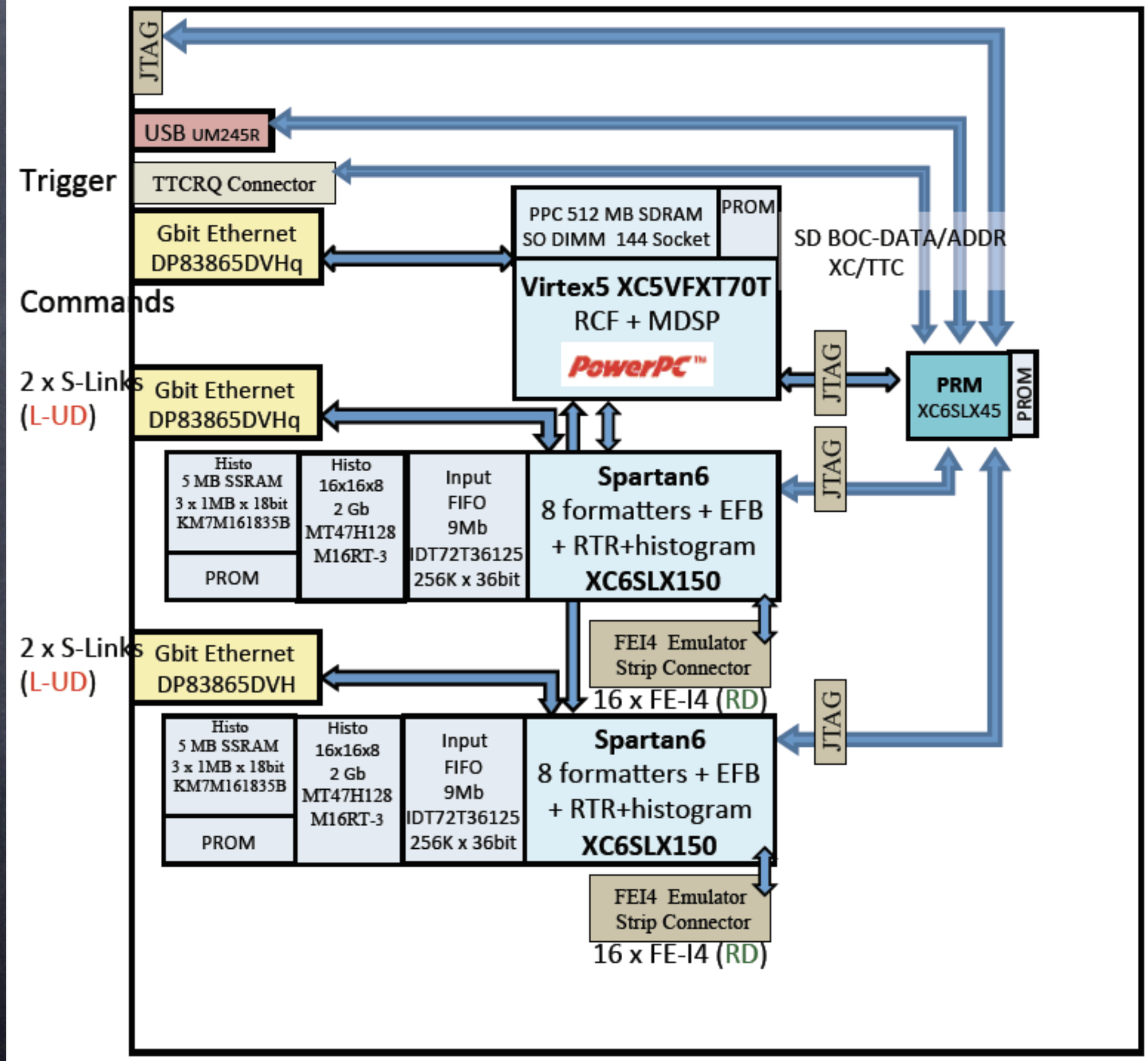


  - This has the huge advantage that, in principle, all blocks (also all FE chips and BOC) can be simulated with a single simulation environment (ModelSim©) allowing a much better understanding of the whole system.
  - Being part of an existing project, one would like backward compatibility with present system to ease development and to reuse as much as possible existing code.
    - Histogram fitting and calibration runs are the peculiarity of our Detector.
    - Lots of code (is being) ported from DSP to c-code inside the PowerPC.
- The result is a rather complicated card that has many different "operating modes"...

ROD: All components



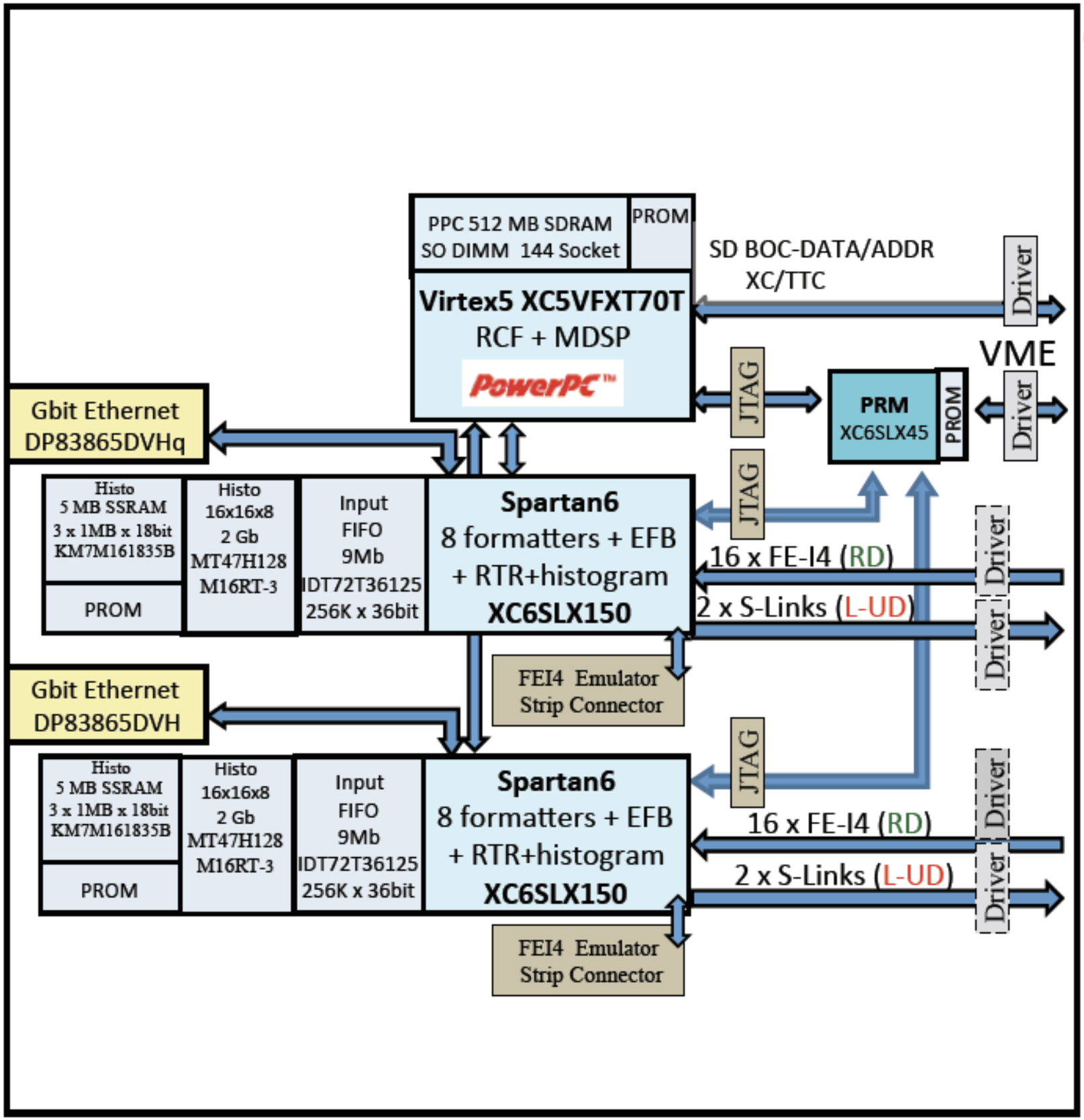
ROD: Test Mode



No crate

Test Mode

ROD: Configuration Mode



Configuration Mode

P1

P0
5 rows

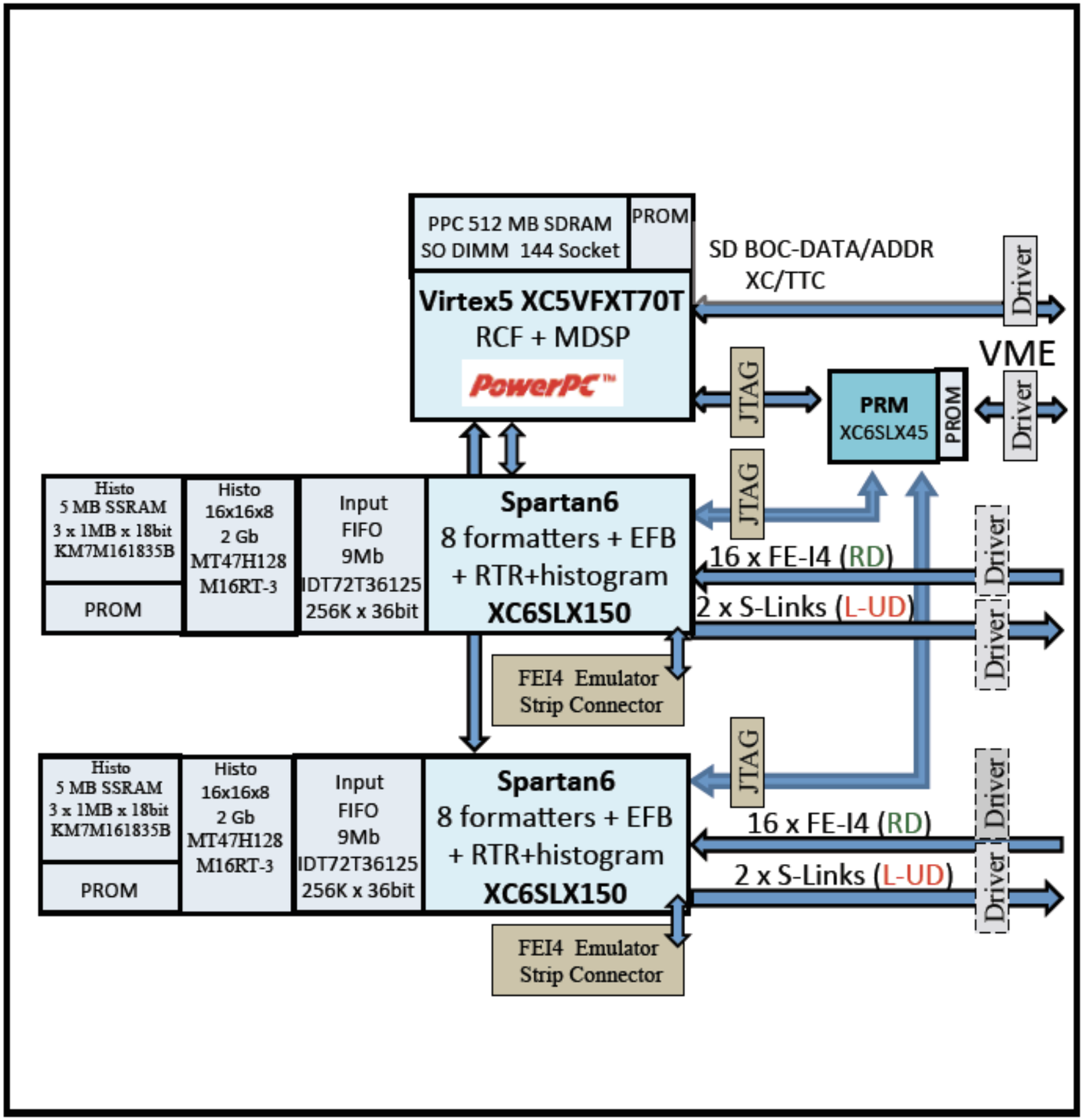
data from/to BOC

40 – 80 MHz LVTTL
> 80 MHz SSTL3-I

P2

P3

ROD: Data taking Mode



Data Taking Mode

P1

P0
5 rows

data from/to BOC

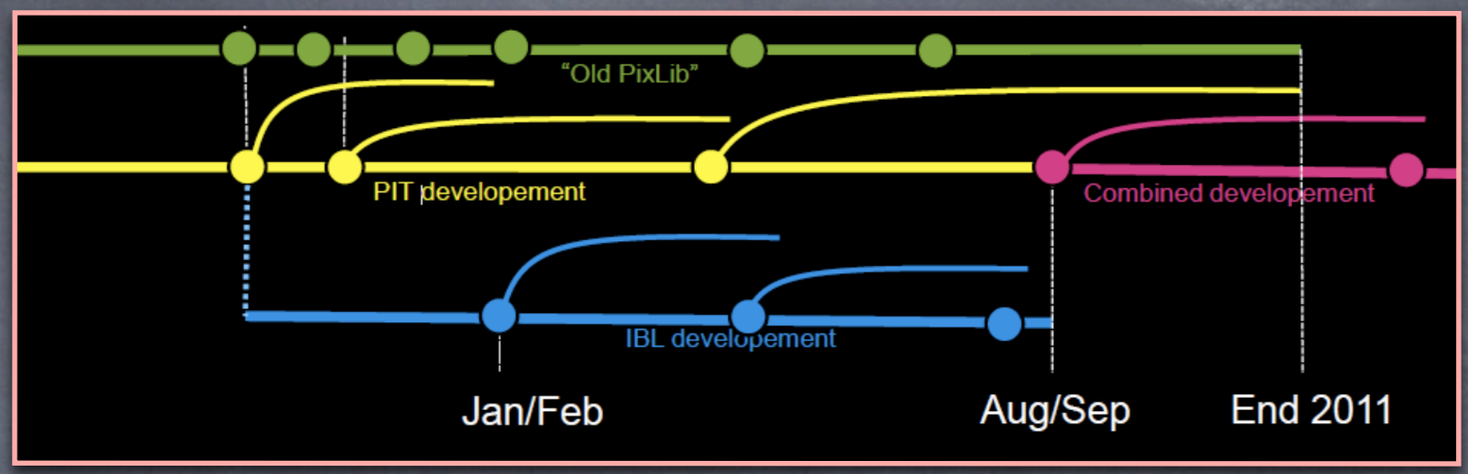
40 – 80 MHz LVTTL
> 80 MHz SSTL3-I

P2

P3

DAQ

- Once installed in the pit, IBL will be part of the current Pixel Detector (a new layer)

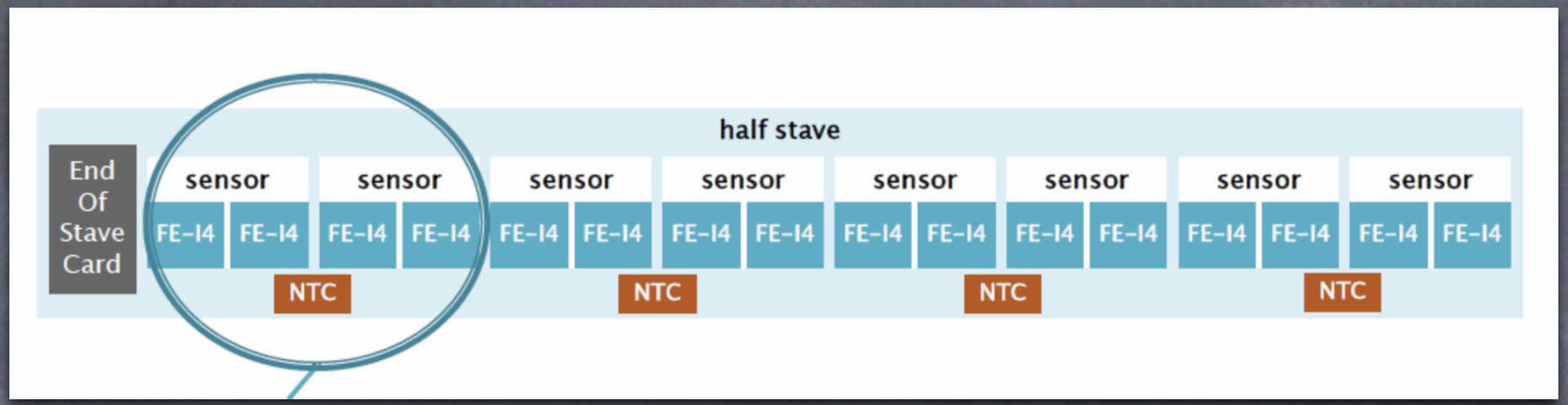


- A key point is the ability to develop a stable and robust version of the DAQ software that has to support both present Pixel Detector and the new IBL with minimal debugging and development time. --> It has to work "out of the box"

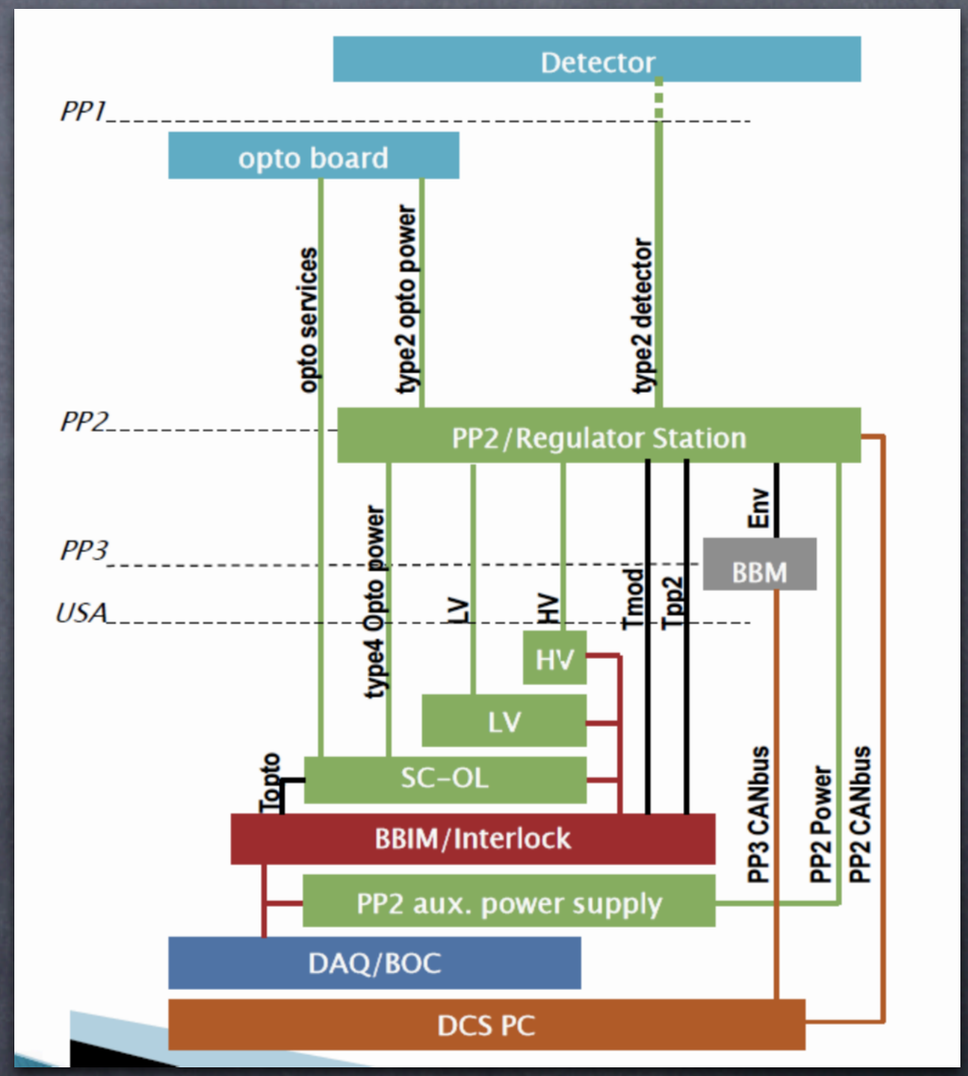
- DAQ is still evolving and many people are working on it.
- A new branch in the software will start (from the Pixel production software) to implement support for both the new ROD/BOC and FE-I4 hardware:
  - Multi-module-type and multi-ROD-type support needs to be included since the beginning (not all the work, but the software must allow easy extensions).
  - ROD/BOC prototypes are expected by summer 2010.
- At a certain point there has to be a merging of the code in order to fully support the new detector (actual Pixel Detector + IBL).

DCS

- 1 half stave:
  - 1 opto board
  - 4 bi-modules
  - 8 detector modules



- 1 DCS bi-module:
  - 1 HV for depletion of 2 (4) sensors
  - 1 LV for 4 front ends
  - 1 NTC for temperature monitoring
  - 4 HV channels every half stave
  - 16 channel for each iseg HV module
  - 14 staves x 8: a total of 112 channels
  - 16 channel/HV module
  - 1 Redel connector every HV module



- separate services for A and C side

Conclusions & Outlook

- Even a "small" detector is rather complicated to build and finalize...
- The new Pixel layer presents many challenges being so close to the beam and having to fit inside a working detector
- Although the project is in an advanced phase there are still many options available. The new 2013 schedule does not allow for contingency
  - Forthcoming months will allow us to decide based on results with real components.
- 2013 installation schedule is very tight, but seems feasible if there are no major component failures and no major delays (like unforeseen R&D steps).
- Simulation of the whole system, from ROD/BOC down to FE chips within a single environment, will (hopefully) provide a key component to the successful completion of the project

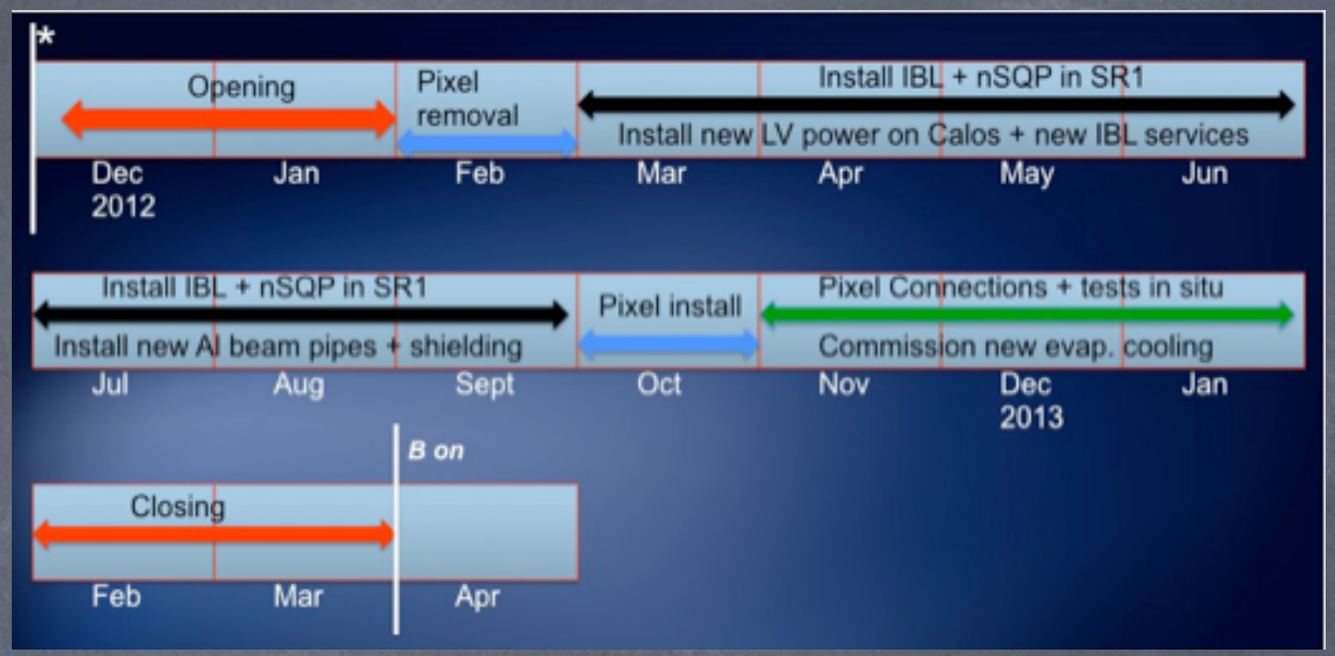
Many thanks to all the people to whom i have stolen slides, pictures, etc...

Spare slides

- IBL installation in 2013
- Type 0 Services: Electrical tests
  - Type 0 Services: Clk/Cmd tests
  - Type 0 Services: Data out tests
- CO2 cooling

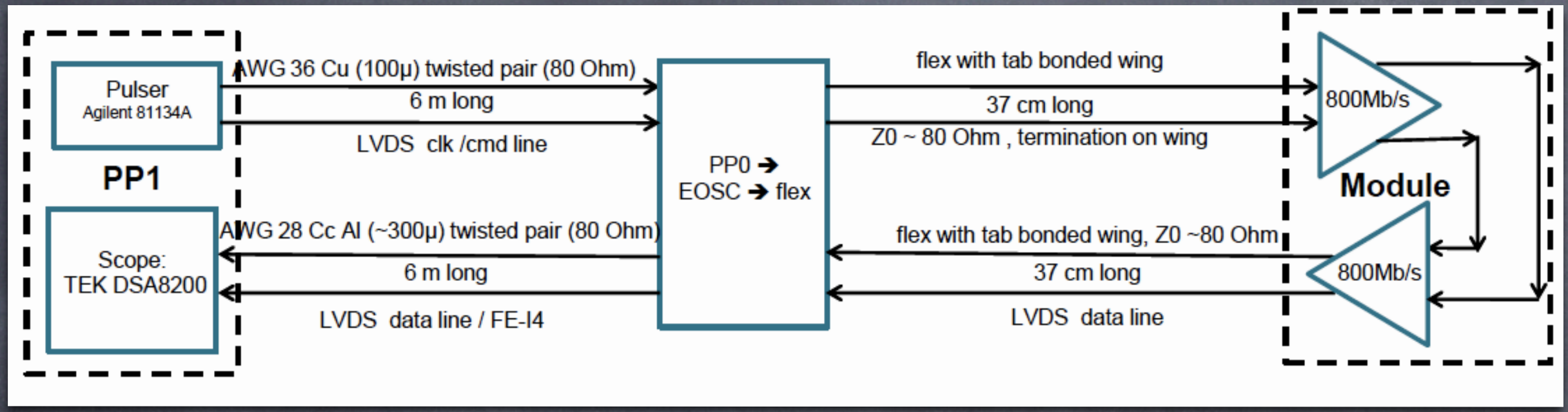
IBL installation in 2013

- Assumptions for installation in 2013:
  - Official project start: 1. March 2011
  - Ready for installation : 1. July 2013
  - Construction time is shortened by:
    remove explicit contingency (2x3mo) +
    parallelizing operations +
    early start for sensor pre-production (6-8 mo) +
    FE-I4 Version 2 direct production run (5 mo)



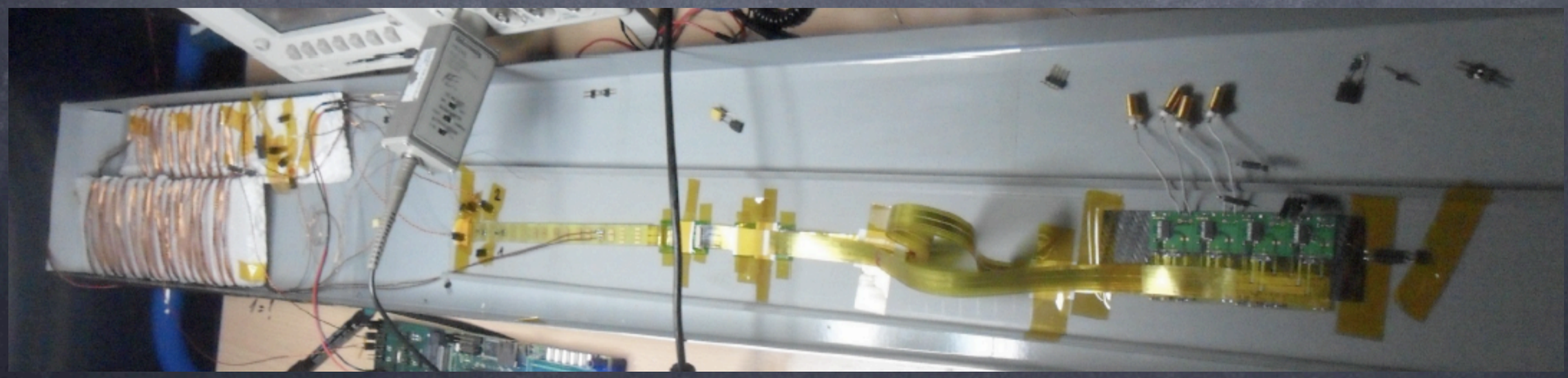
  - Main construction duration of components not changed (e.g. BB, stave loading, integration...)
  - Treated as construction schedule with qualification steps of components (sensor, chip, module, stave, integration)
  - The schedule is aggressive but achievable if there are no major component failures and no major delays (e.g. due to extended RD steps)
- Time critical items:
  - Sensor pre-production run (start Feb) and sensor review/decision (June)
  - FE-I4 Version 2 submission (June 2011)
  - Bump bonding of thin modules (work plan in preparation with IZM, aim to get first thin modules in ≈ 3 months)
  - Stave 0 program to qualify full stave mechanically and electrically (requires rapid advancement on stave flex and module loading) (mechanical stave April-May, loaded August, tested October)
  - Beam pipe qualification of split flange and order of beam pipe

Type 0 Services: Electrical tests



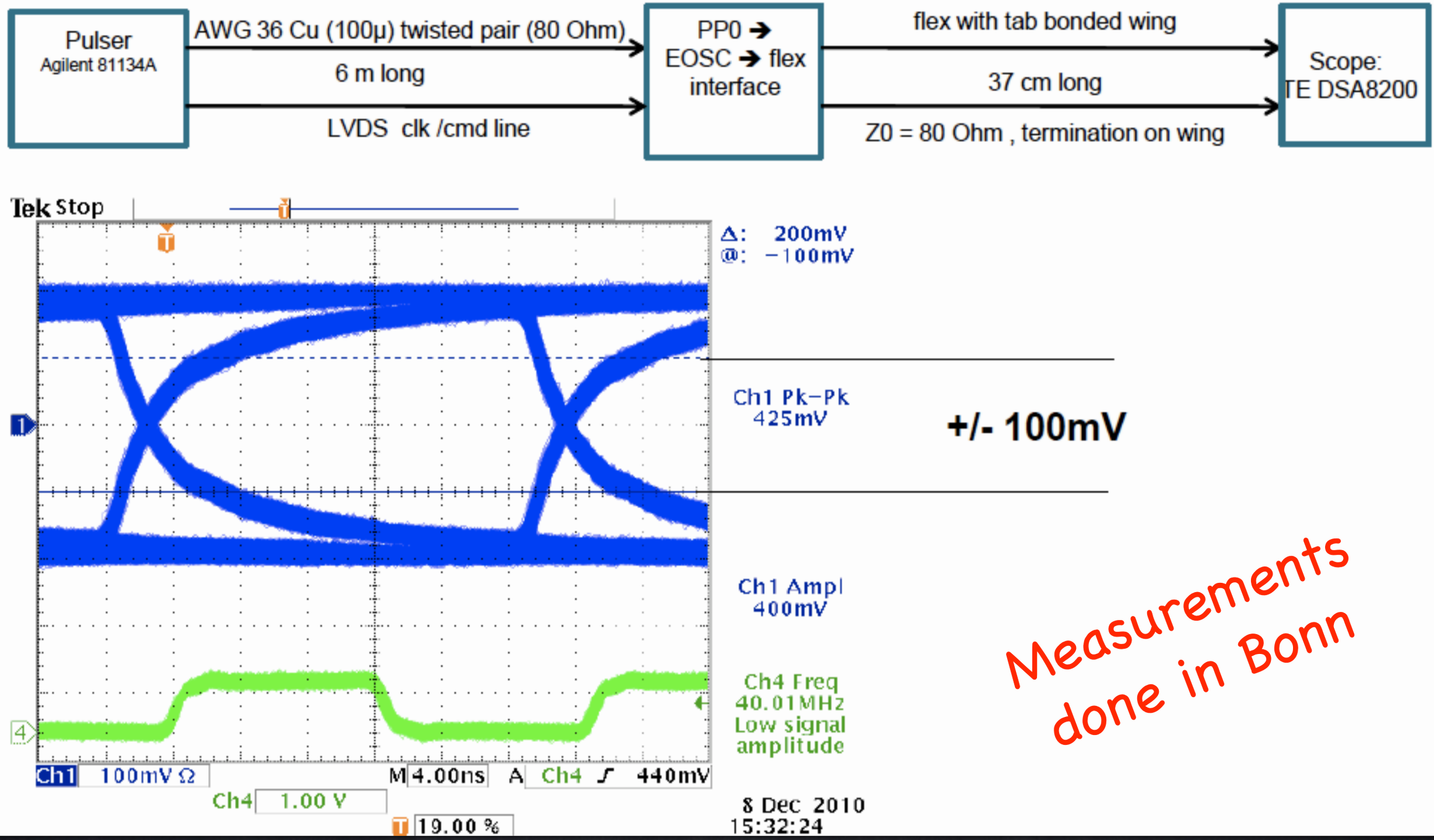
The Bonn Type 0 services: Test setup

BERT Test: 28 hour --> 1.6 x 10^{13} bits sent;
8b/10b encoded PRBS8 as we will use --> with open shielding



The Bonn Type 0 services: connected together

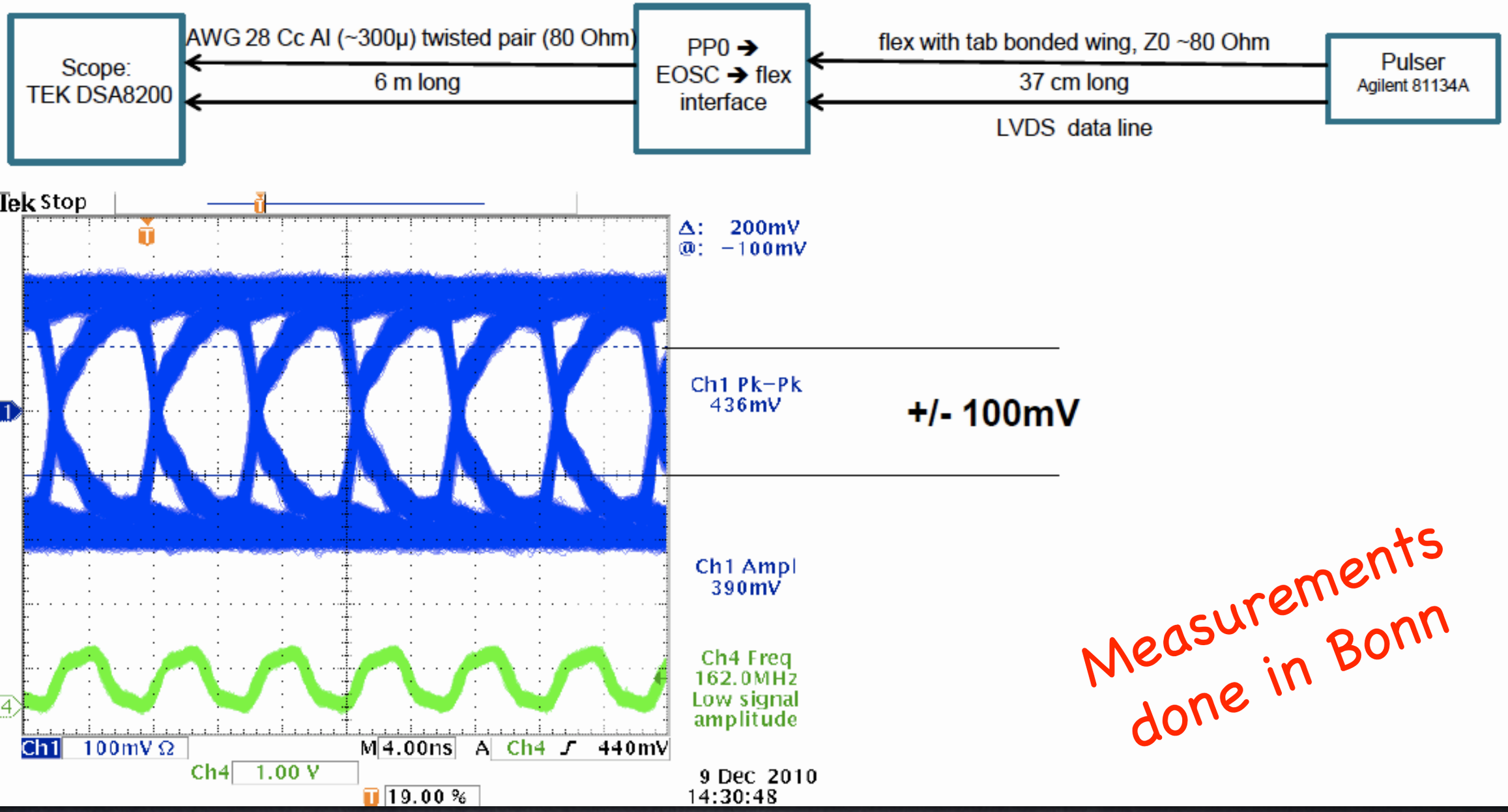
Type 0 Services: Clk/Cmd tests



CLK Signal: measured after the whole services; wire Ø ≈ 100µm

Input: PRBS10; ± 240 mV (3 mA x 80 Ω)

Type 0 Services: Data out tests

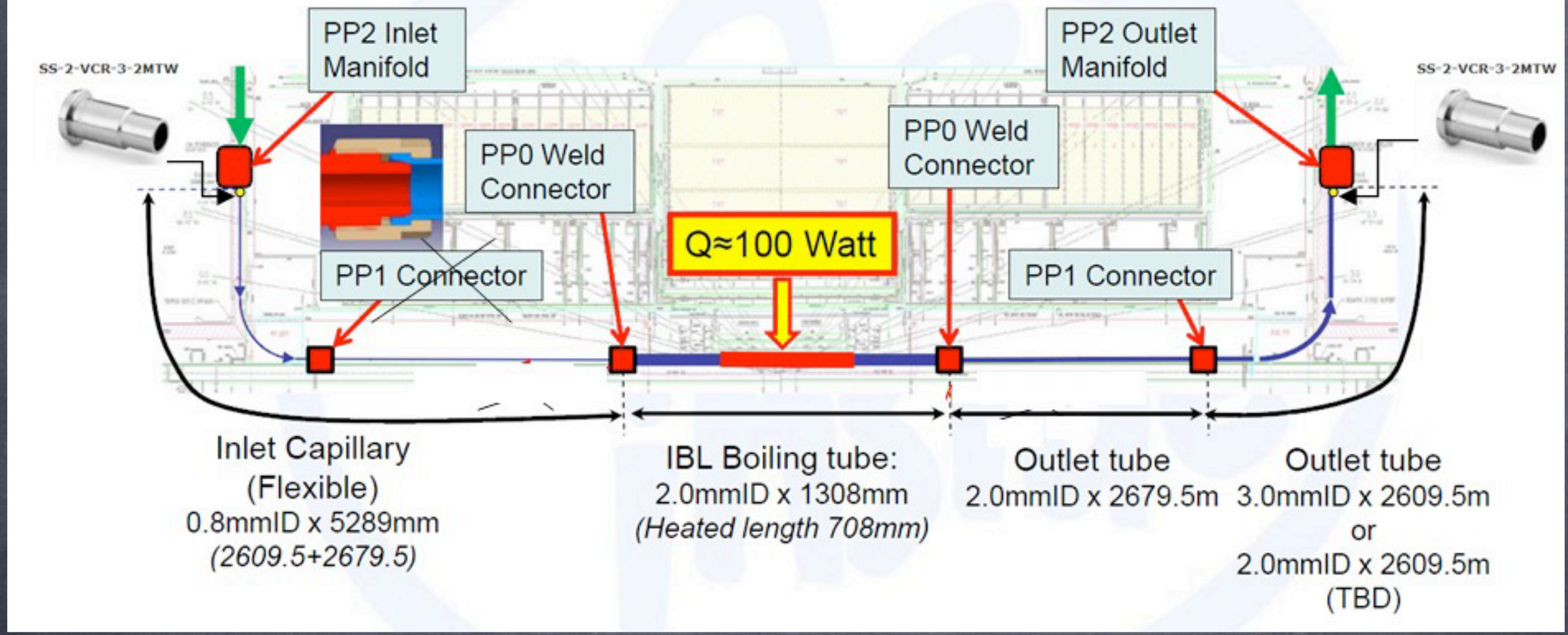


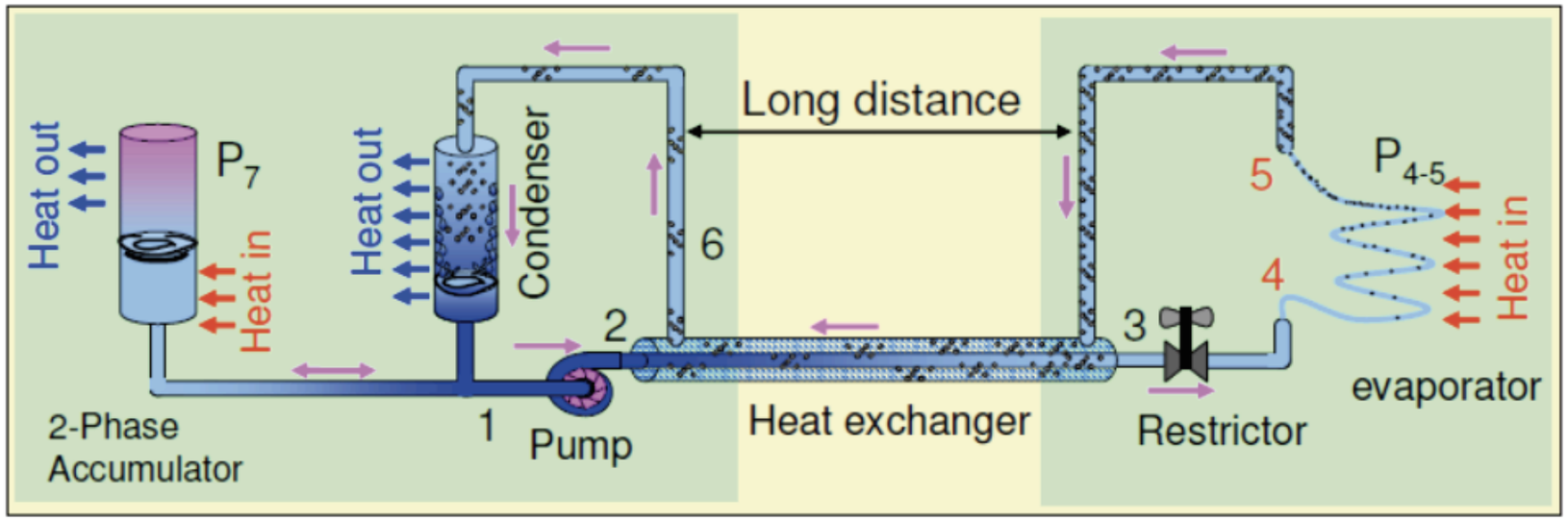
Data out Signal: measured after the whole services

wire Ø ≈ 300 µm

Input: PRBS10; ± 240 mV (3 mA x 80 Ω)

CO_2 cooling


PP2 Inlet Manifold
PP2 Outlet Manifold
SS-2-VCR-3-2MTW
SS-2-VCR-3-2MTW
PP0 Weld Connector
PP0 Weld Connector
Q≈100 Watt
PP1 Connector
PP1 Connector
Inlet Capillary
(Flexible)
0.8mmID x 5289mm
(2609.5+2679.5)
IBL Boiling tube:
2.0mmID x 1308mm
(Heated length 708mm)
Outlet tube
2.0mmID x 2679.5m
Outlet tube
3.0mmID x 2609.5m
or
2.0mmID x 2609.5m
(TBD)


Heat out
P_7
Heat in
Heat out
Condenser
Long distance
6
5
P_{4-5}
Heat in
4
2
3
2-Phase
Accumulator
1
Pump
Heat exchanger
Restrictor
evaporator