



# From analog coded digital to digital coded analog. Changes to the CMS pixel ROC

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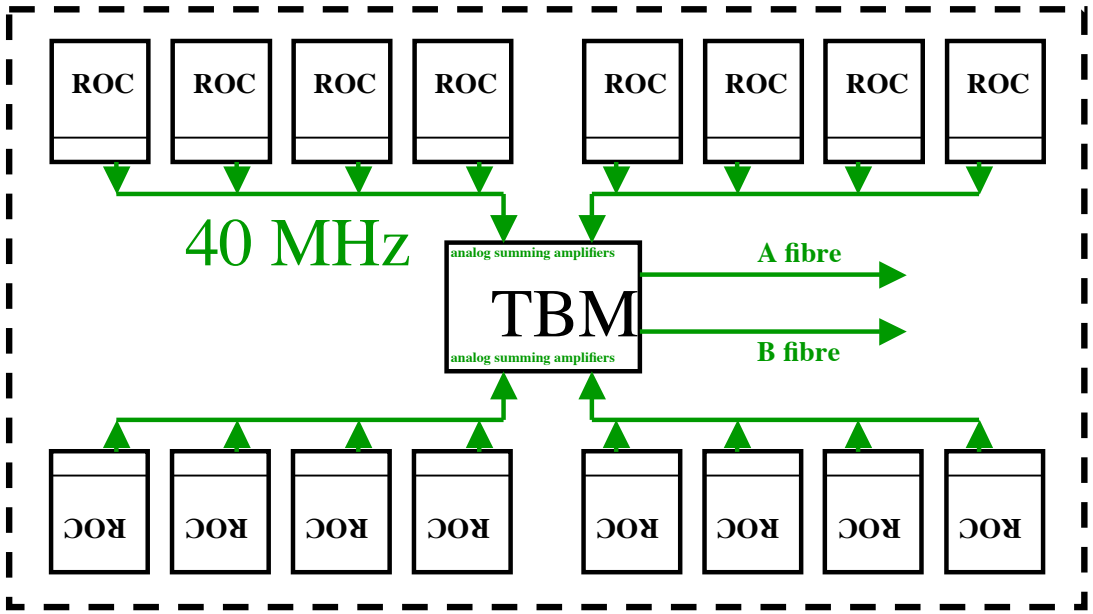
# Content

- Present analog links. What means analog coded digital?
- Why changing the readout ?
- What are the implications?
- Other changes to the ROC
- Conclusion

# Present module readout

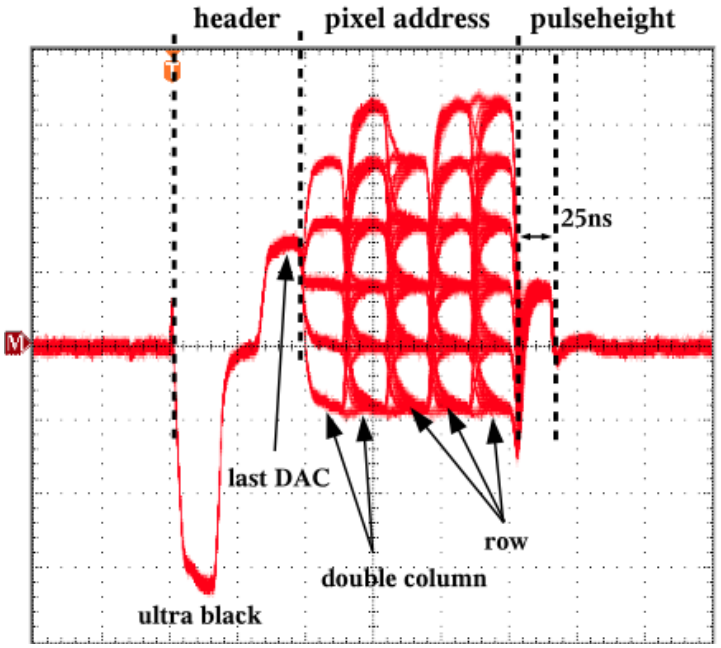
ROC → TBM (module controller) : 40 MHz analog readout
TBM → pxFED (off detector DAQ) : 40 MHz analog readout
8 or 16 ROCs are daisy chained




Layer 1& 2 → 2 fibres A & B
Layer 3 → 1 fibre A

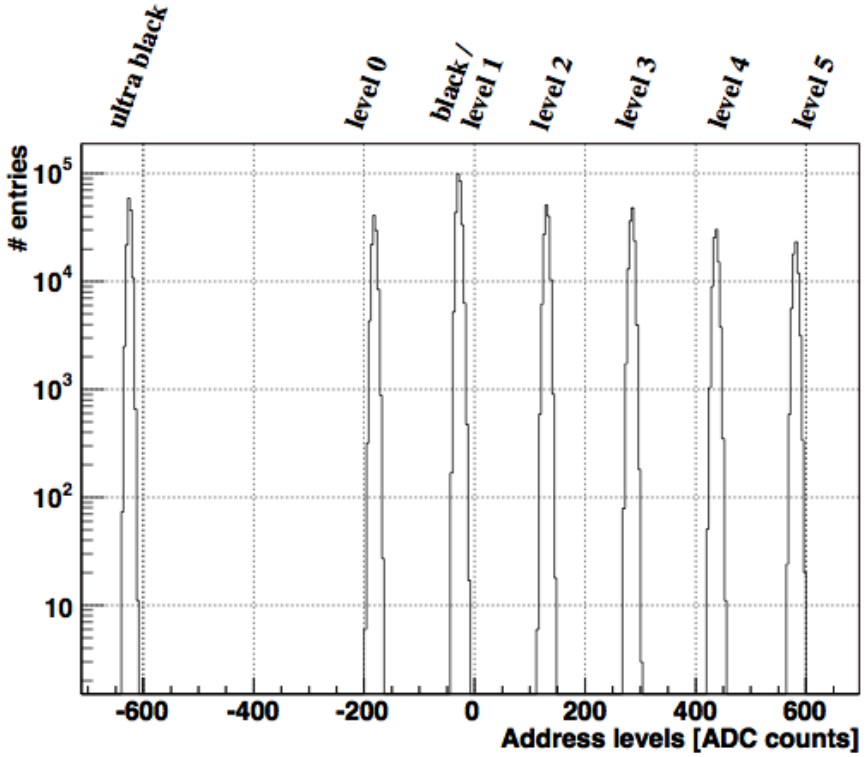
# Present analog readout

Overlay of all single pixel readouts of one ROC, 40MHz




•Ultra black = chip separator in data stream
•ADC converts digital address to 6 discrete levels (analog coded digital)
•Analog transmission of pulse hight information

Address level scan




•Need to adjust level separator after digital conversion
•Online correction for baseline drift
•Works well

# Data Rate Estimations, 25ns

- Full 4 layer phase I geometry
- Assuming 24 bits per hit, 100kHz L1A
- Peak lumi=$2x10^{34}cm^{-2}s^{-1}$, $\sigma_{tot}$=80mb, $\sigma_{signal}$=1.5mb
- Data rate includes headers/trailers
- Bandwidth of present analog links ≈ 100 Mbit/sec peak

| Layer | 1 | 2 | 3 | 4 |
|---|---|---|---|---|
| Pixel fluence [MHz/cm$^2$] | 251 | 108 | 48 | 27 |
| Hits / trigger / module | 70 | 35 | 16 | 8.4 |
| MBit/link/sec | 204 | 107 | 61 | 40.0 |
| # links | 128 | 224 | 352 | 512 |

# Data Rate Estimations, 50ns

- Full 4 layer phase I geometry
- Assuming 24 bits per hit, 100kHz L1A
- Peak lumi=$2x10^{34}cm^{-2}s^{-1}$, $\sigma_{tot}$=80mb, $\sigma_{signal}$=1.5mb
- Data rate includes headers/trailers
- One link per module
- 50ns LHC bunch structure - 100 pile up events!

| Layer | 1 | 2 | 3 | 4 |
|---|---|---|---|---|
| Pixel fluence [MHz/cm$^2$] | 234 | 99 | 44 | 21 |
| Hits / trigger / module | 139 | 63 | 28 | 13.4 |
| MBit/link/sec | 365 | 176 | 90 | 55 |
| # links | 128 | 224 | 352 | 512 |

# Readout Chip for Phase I

- Based on present readout chip
- Limitations of present ROC at Phase1:

1. Buffers sizes for L1 latency (dominating)

   → **Increase number of buffers** → **done**

2. Higher module count / same number of fibres

   → **Digital readout**

   – On chip ADC → done
   – New fast digital readout links → done
   – PLL to provide higher frequencies → done
   – Modification to control logic → ongoing

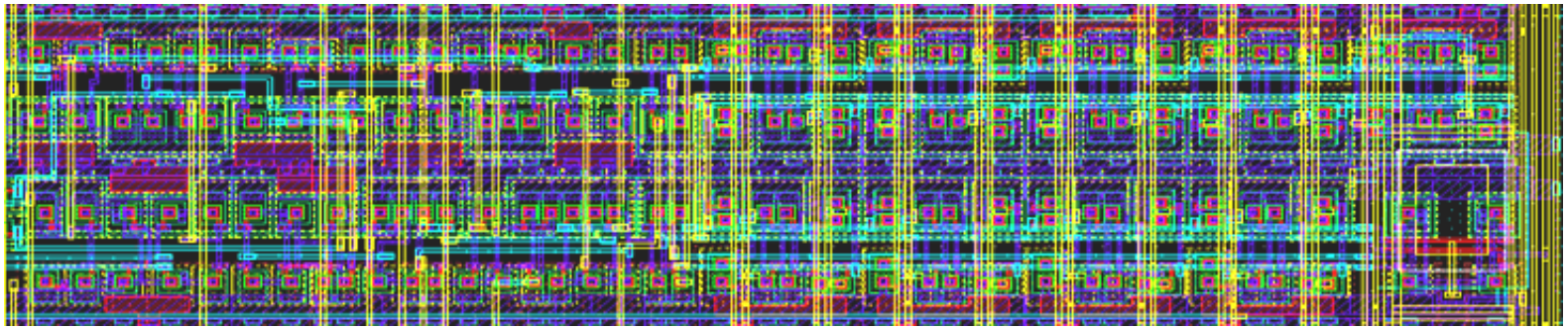
3. Readout related dead-time at higher data volumes

   → **Additional readout buffer stage** → **ongoing work**

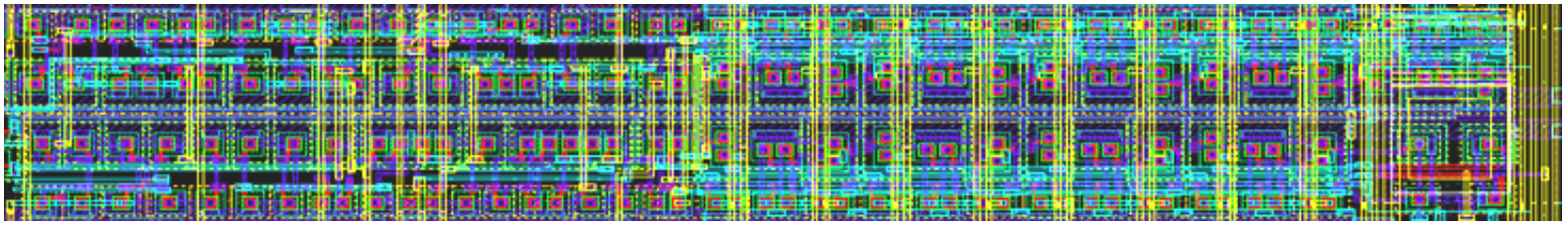
   – Modification to control logic → ongoing

# 1. Data Buffer Redesign

existing data buffer cell

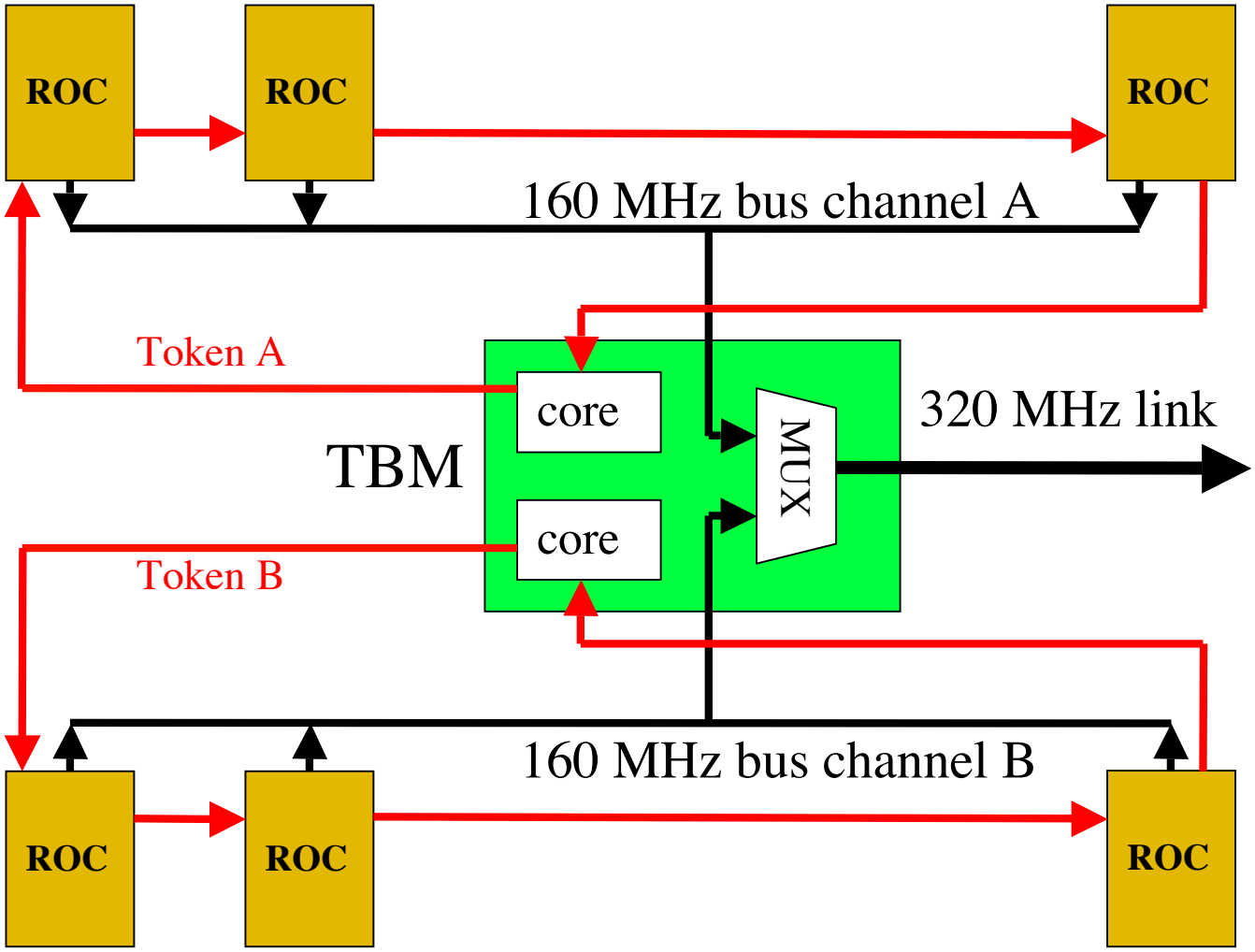



new data buffer cell



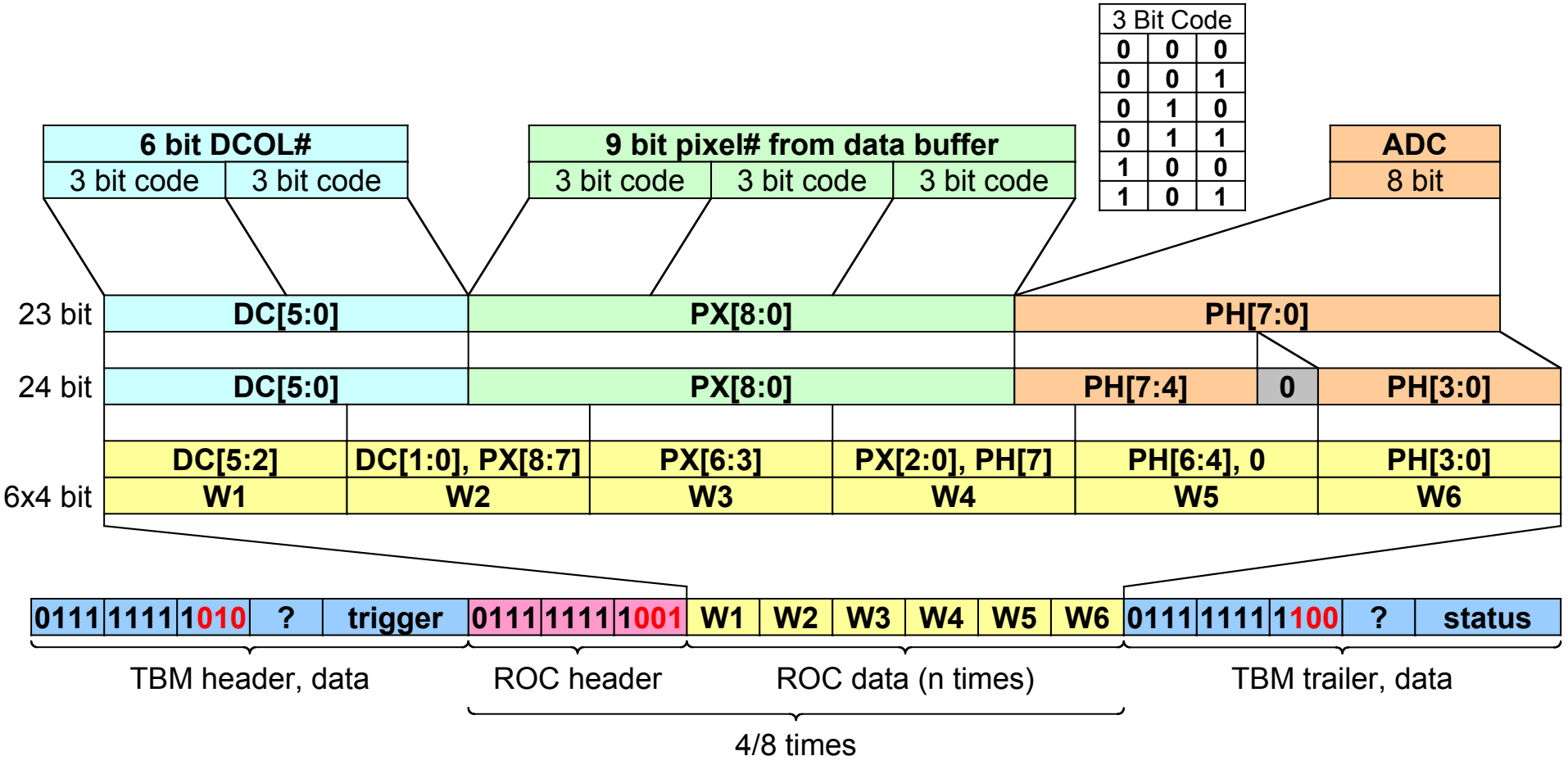

- No change in schematic (except number of cells)
- Extremely dense design. Minimal spacings reached in metal layers
- Size for 80/32 buffers 1.53mm (before 32/12 buffers in 1.18mm)

# 2. Basic Idea of digital module



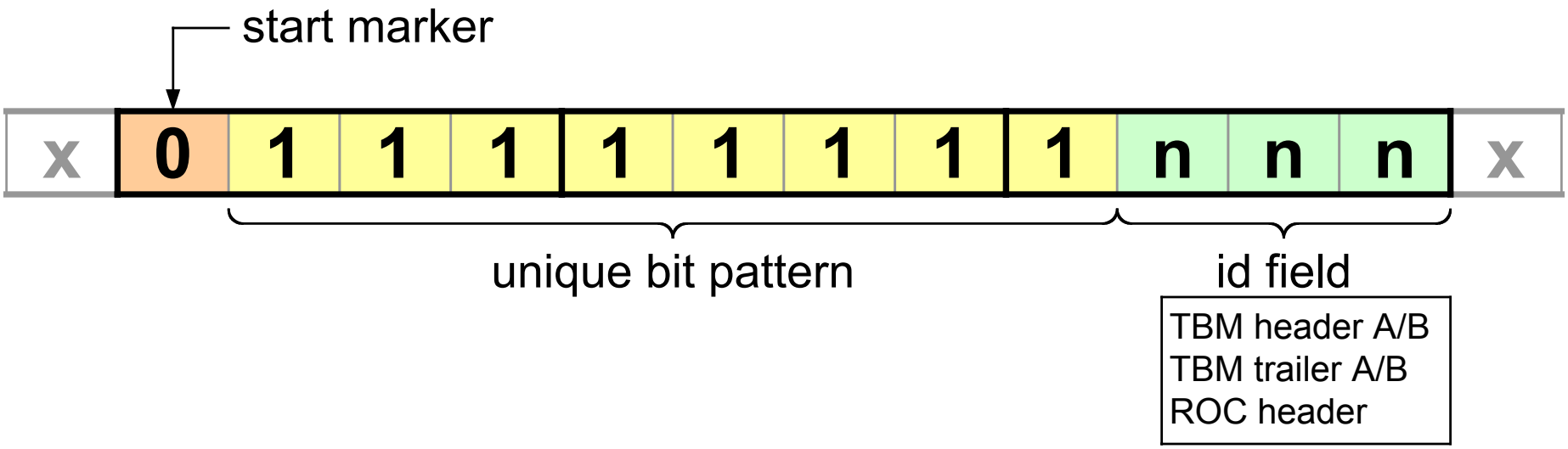

- 2x8 ROCs daisy chained
- Need new separator between ROCs (no ultra black)
- Need ADC on chip

# Digital Data Format



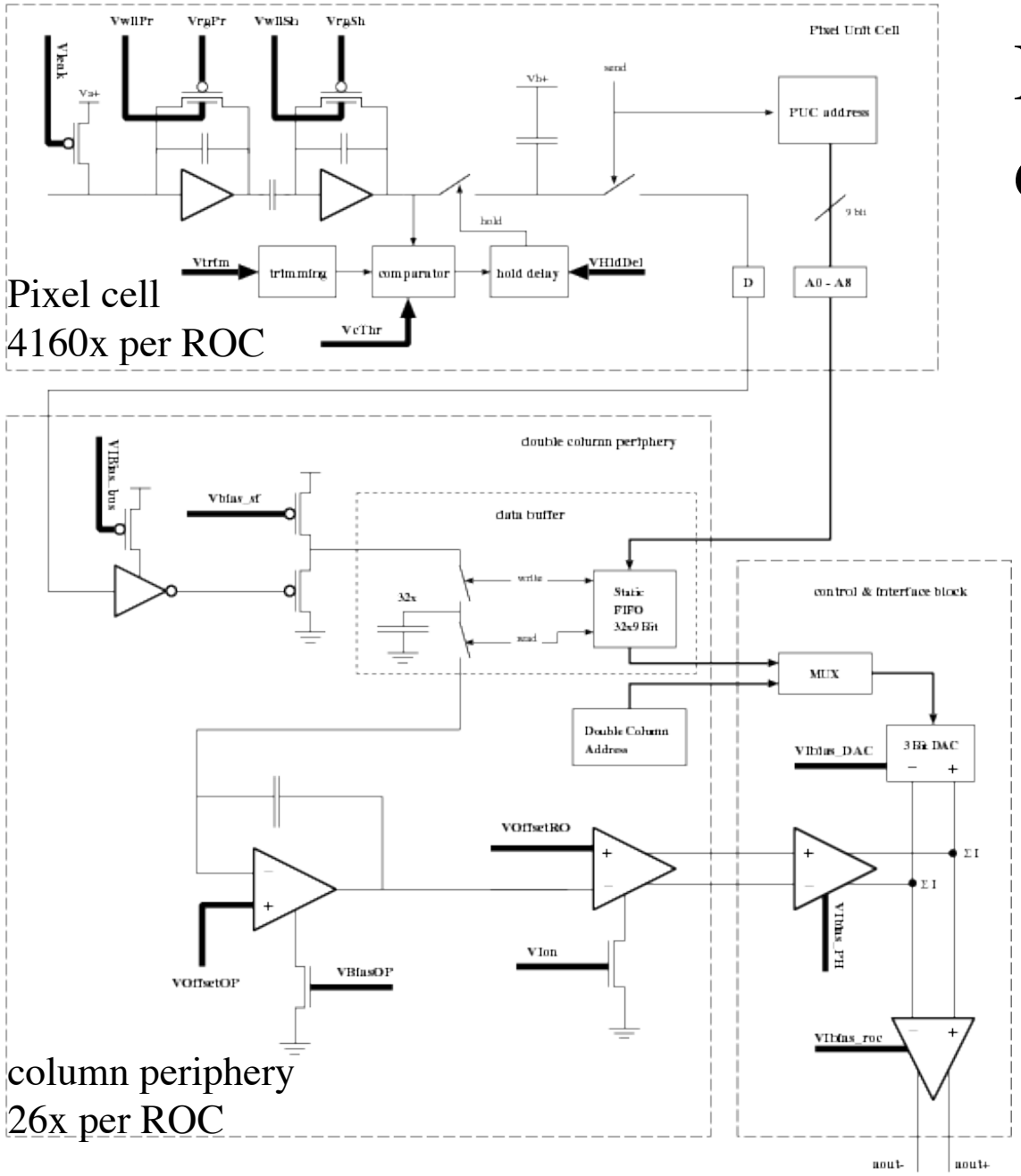

- 8 unused bits in TBM header and trailer

# Header Format




- No ultra black level
- 1111‘1111 not in data stream
- 0 → 1 transition for synchronization
- Same format for all header/trailer → easy decoding
- Id field for TBM header A/B, trailer A/B, ROC header
- Adjusted with 40 MHz clock (320 to 40 MHz clock crossing in FED)

# From analog to digital readout



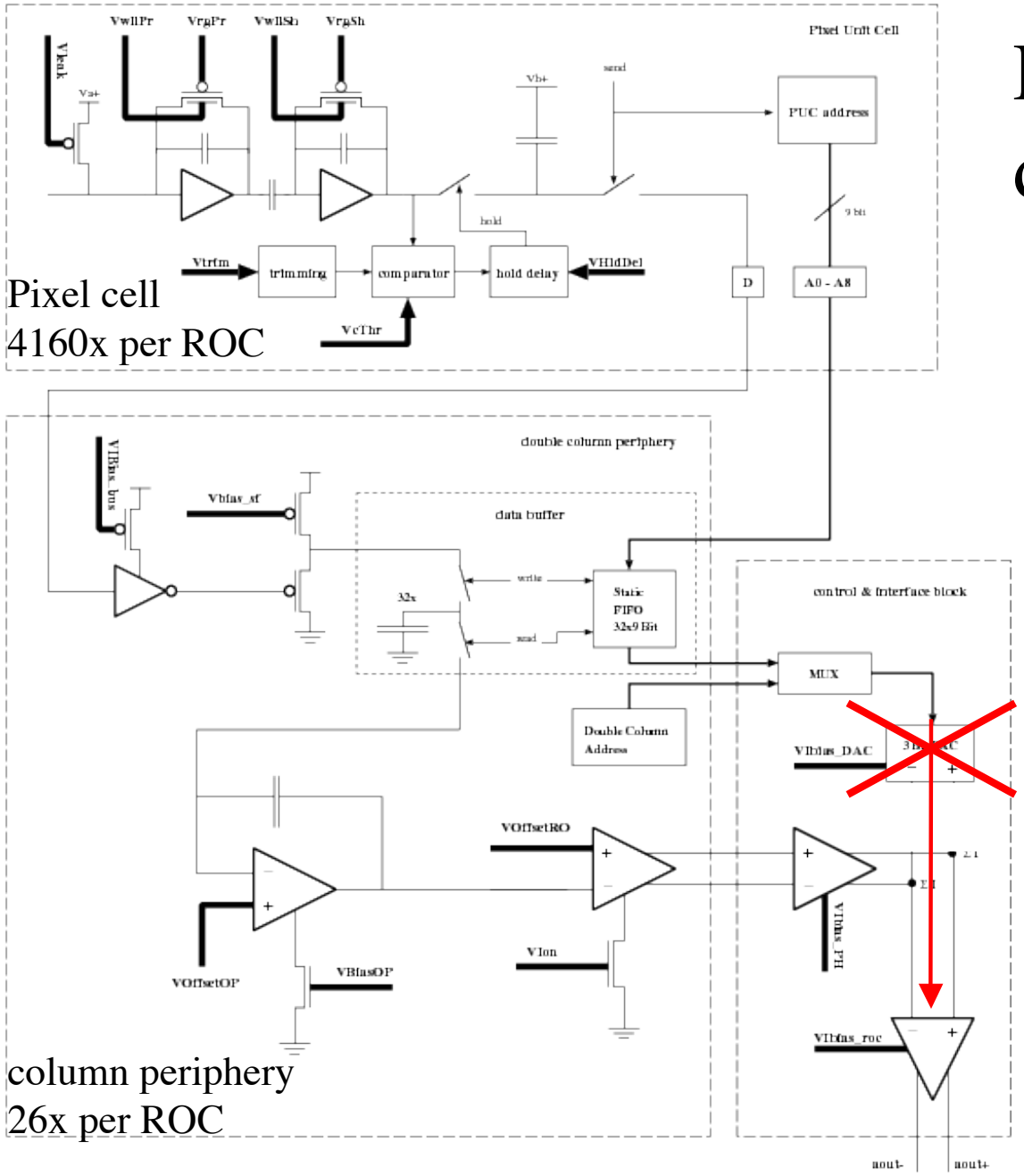

Pixel cell
4160x per ROC

column periphery
26x per ROC

Signal chain in present ROC psi46V2

Chip periphery
1x per ROC

# From analog to digital readout

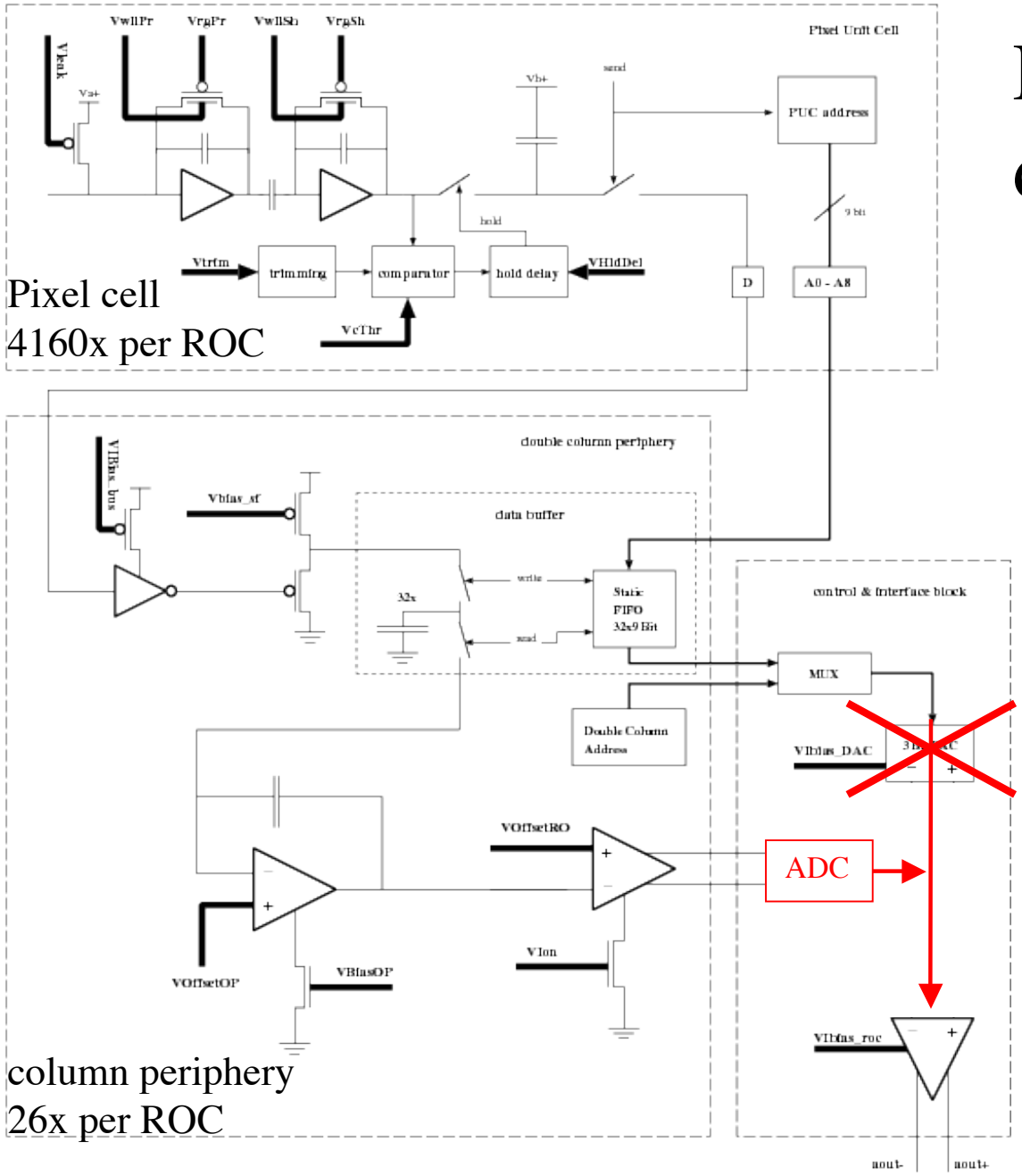



Pixel cell
4160x per ROC

column periphery
26x per ROC

Address internally already digital
→Remove DAC
→trivial

# From analog to digital readout

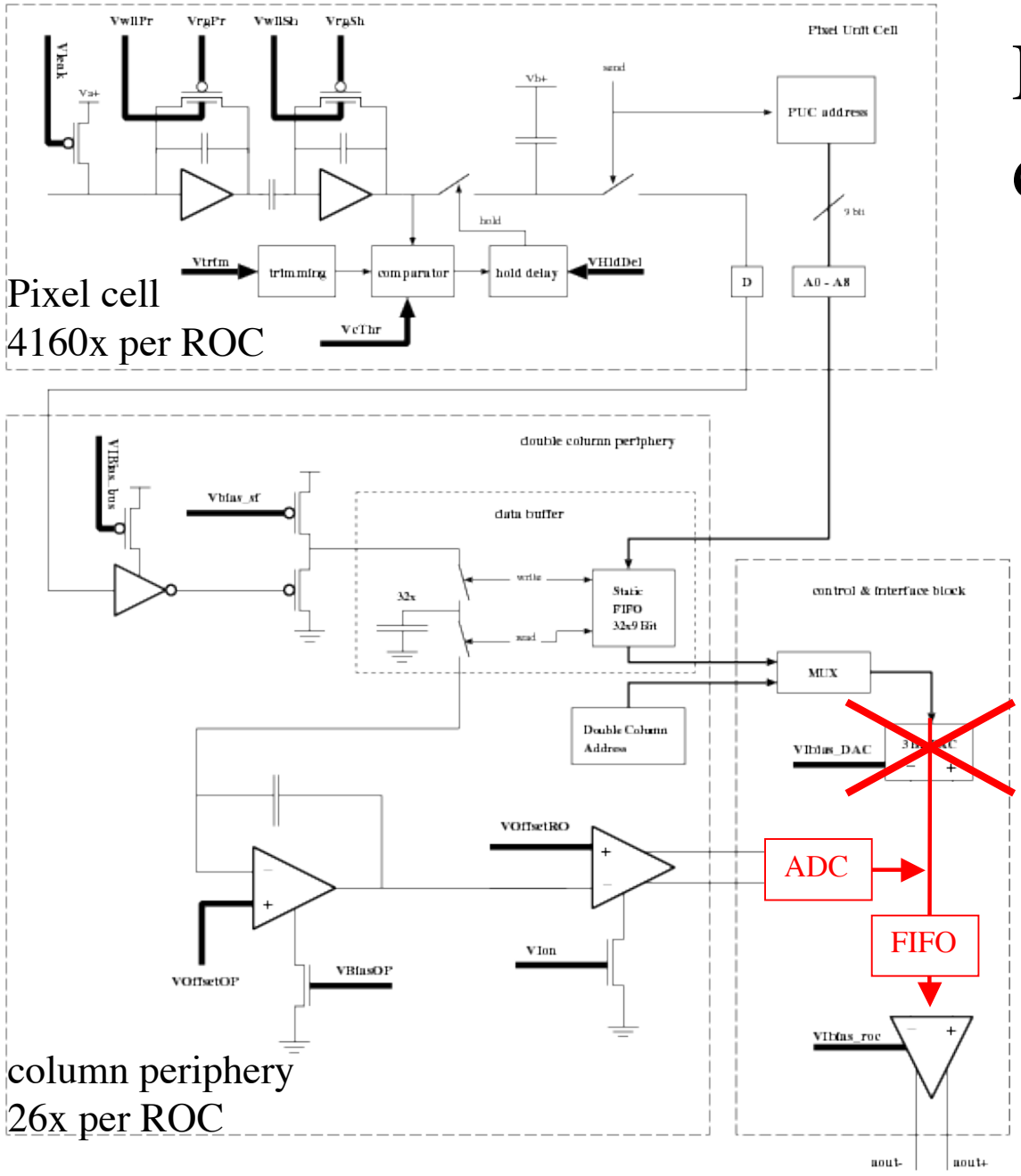



Pixel cell
4160x per ROC

column periphery
26x per ROC

Need to digitize pulse height information
→Need fast 8 bit ADC

# From analog to digital readout

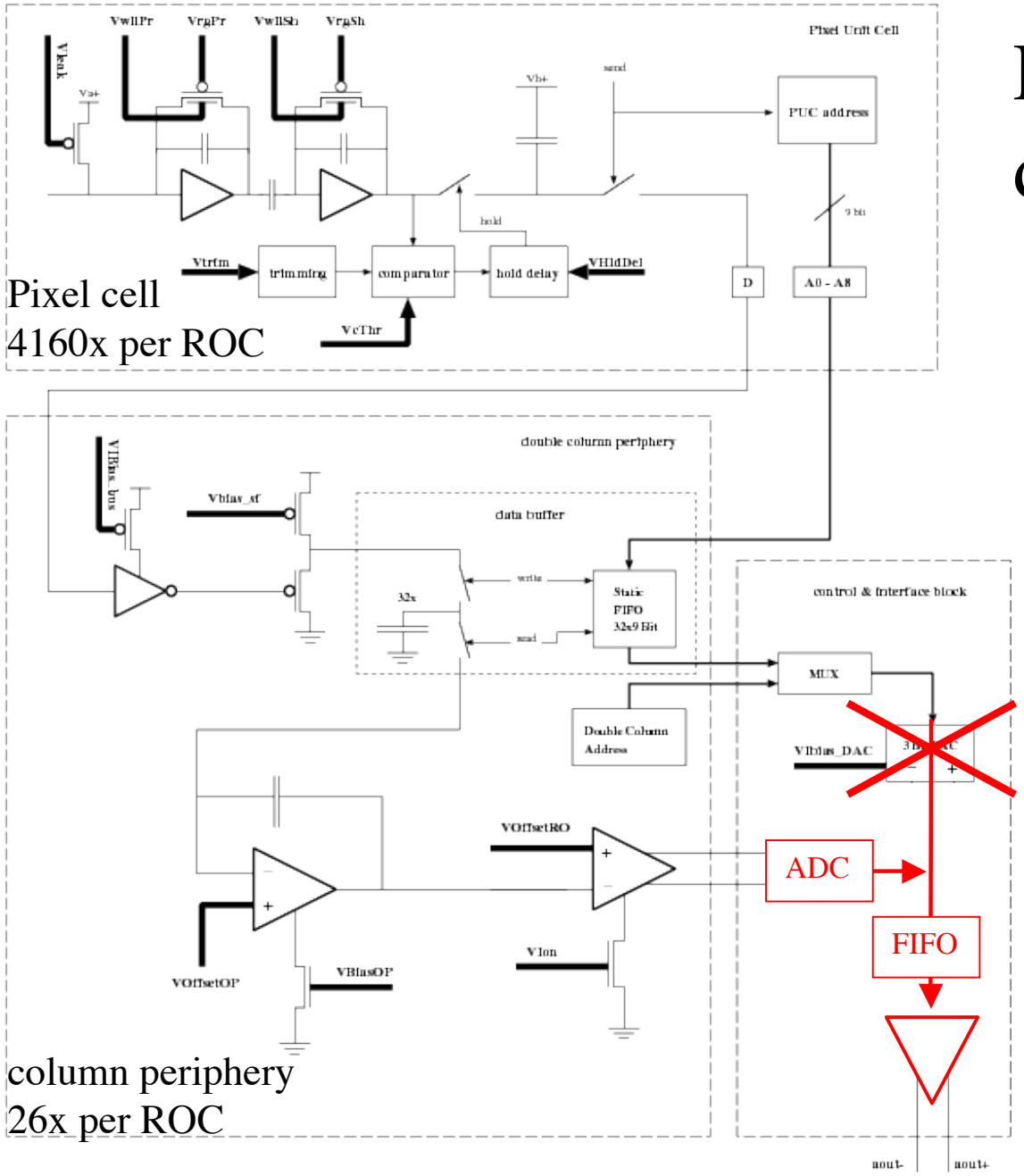



Pixel cell
4160x per ROC

column periphery
26x per ROC

Extra readout buffer stage to reduce dead time
Digital FIFO, 23 bits wide, 80-100 words deep

# From analog to digital readout

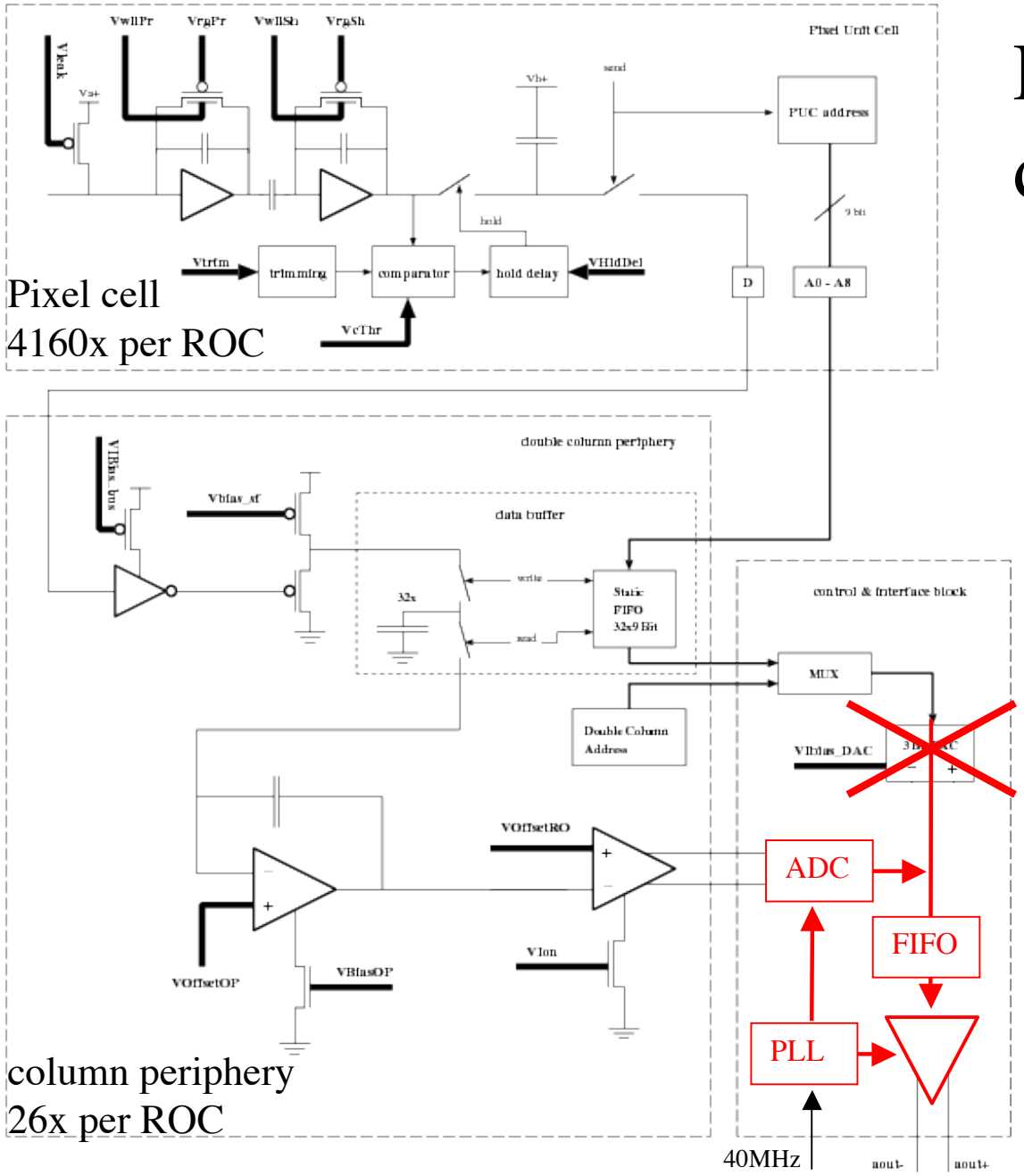



Pixel cell
4160x per ROC

column periphery
26x per ROC

New fast and low power output driver

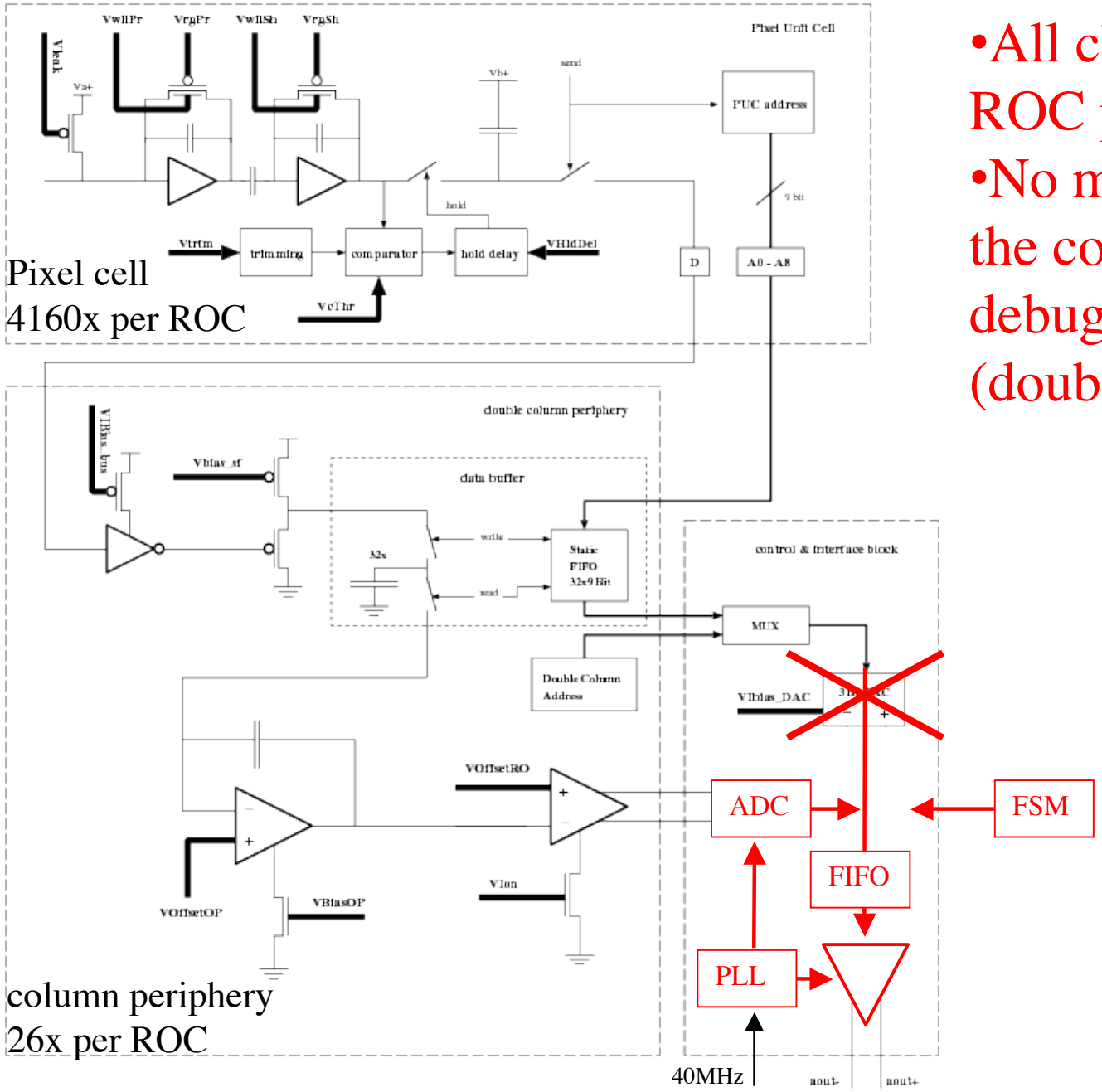
# From analog to digital readout




Pixel cell
4160x per ROC

column periphery
26x per ROC

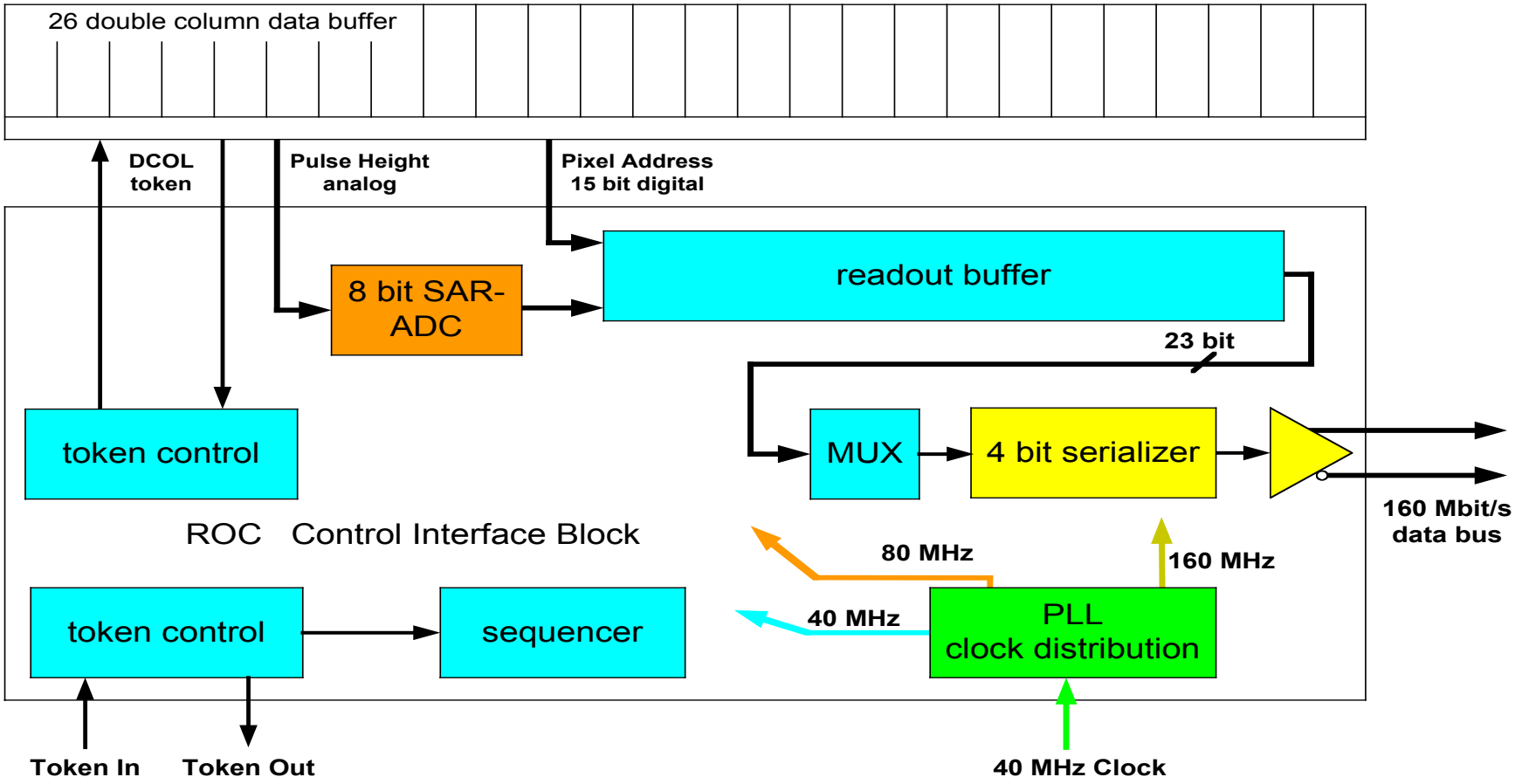
Output at 160MHz
→Clock multiplier with PLL




- All changes in the ROC periphery
- No modification of the complex and well debugged chip core (double columns)!

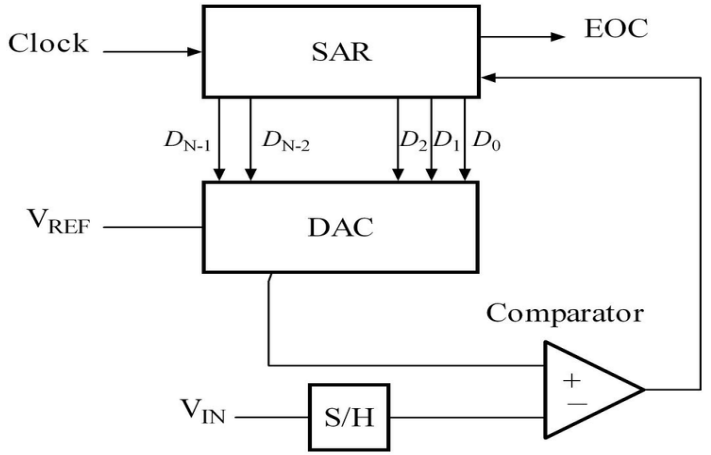
Modified logic

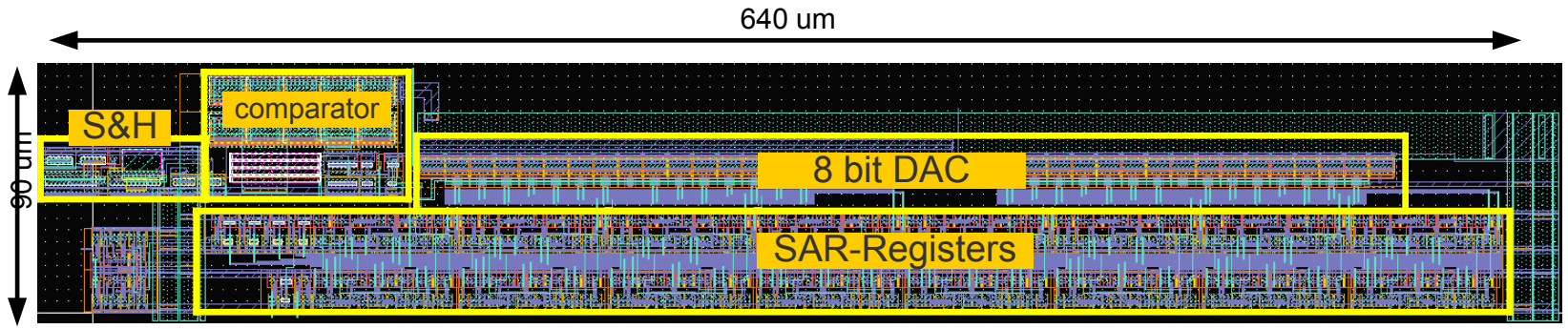
# ROC Periphery Upgrade to Digital Readout



# 8-bit ADC

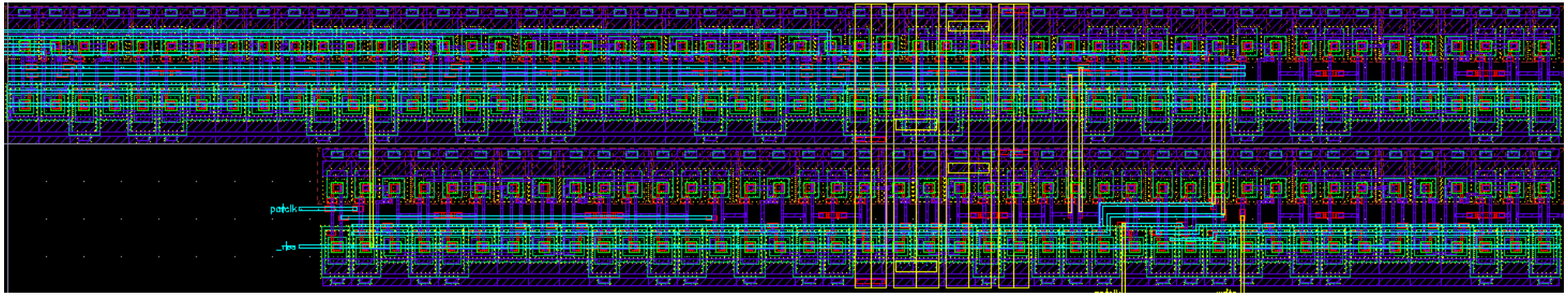
- Successive approximation 8 bit ADC with S&H
- Clock frequency: 80 MHz
- Conversions time: 8 clock cycles
- Test Results
- Non linearity within 1 digit
- Supply current 1 mA (2% of ROC power)
- Speed problem at 80 MHz. Needs redesign of comparator



# 4 bit Serializer

- 4 bit parallel in @ 40 MHz → 160 Mb/s serial output
- Only block running at 160 MHz clock
- Clock domain crossing 40 MHz ↔ 160 MHz
- Phase margin between 40 and 160 MHz depends on this block
- Placed near the PLL clock generator
- Size: 200 µm x 38 µm



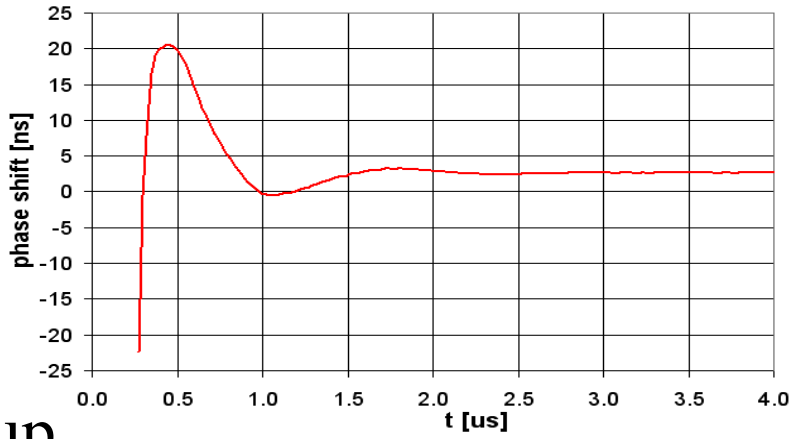
- ☑ Schematic, Layout
- ☐ Simulation with parasitic capacitances, setup/hold time
- ☐ Insertion in ROC

# Frequency Multiplier PLL

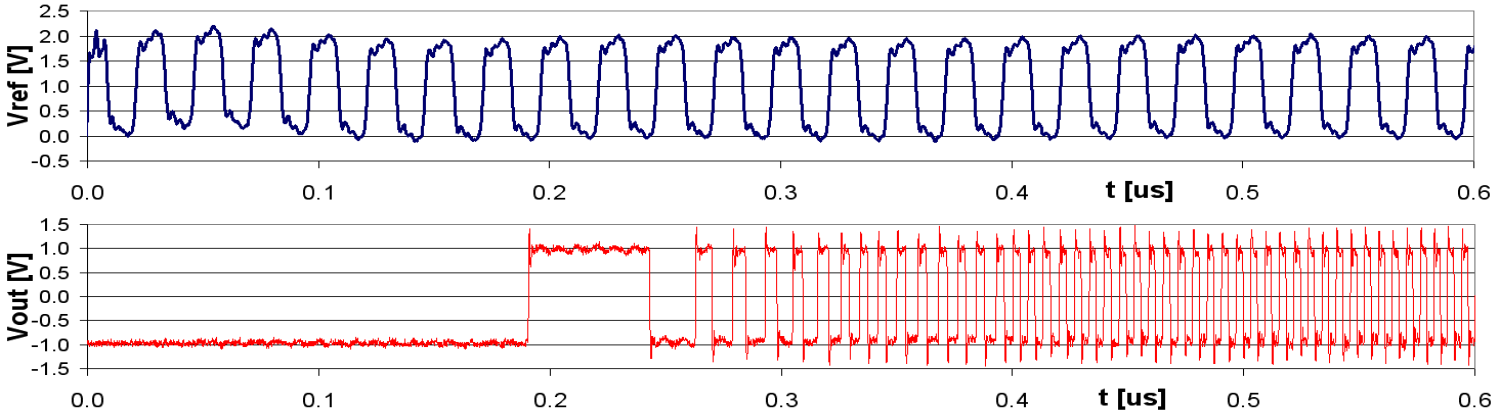
## Results

- Test results:
- PLL locks for 10 … 75 MHz reference frequency
- Supply current: 720 µA
- Lock time: 3 us
- Jitter < 30 ps

start up phase vs time




reference and output signal at start up



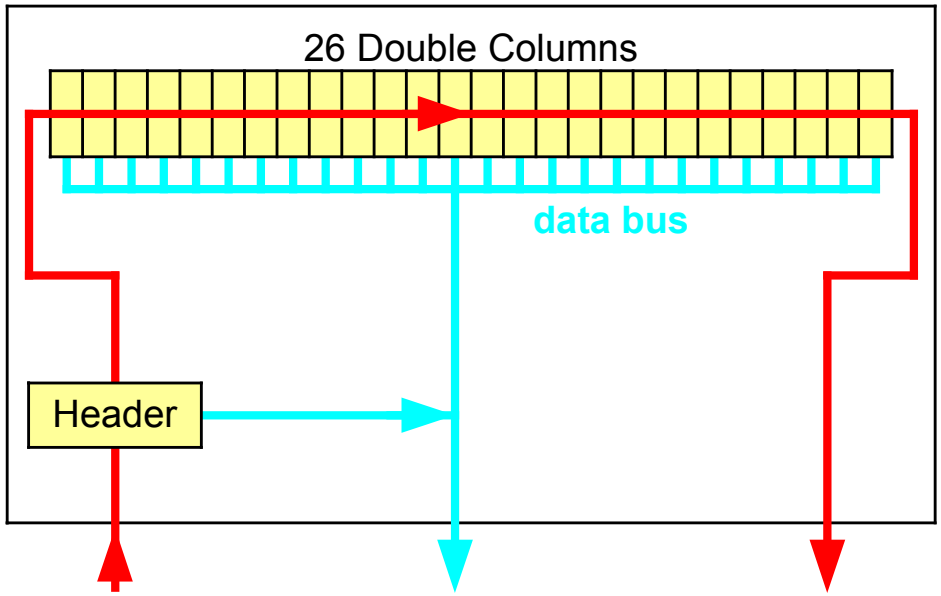
# PLL Frequency Multiplier, Clock Generator: irradiation tests

- Initial design for UMC, now converted to IBM
- Critical blocks exists in IBM design (VCO, PFC)
- Irradiation test of VCO (ring oscillator), 3 samples, IBM
- First results up to 15 Mrad (20 Mrad in work), γ from $^{60}$Co

| Total Dose | 0 | 5 Mrad | 10 Mrad | 15 Mrad |
|---|---|---|---|---|
| Center Frequency | 176 MHz | 173 MHz (-1.7%) | 163 MHz (-7.3%) | 164 MHz (-7.0%) |
| Max Frequency | 474 MHz | 467 MHz (-1.3%) | 461 MHz (-2.7%) | 458 MHz (-3.3%) |

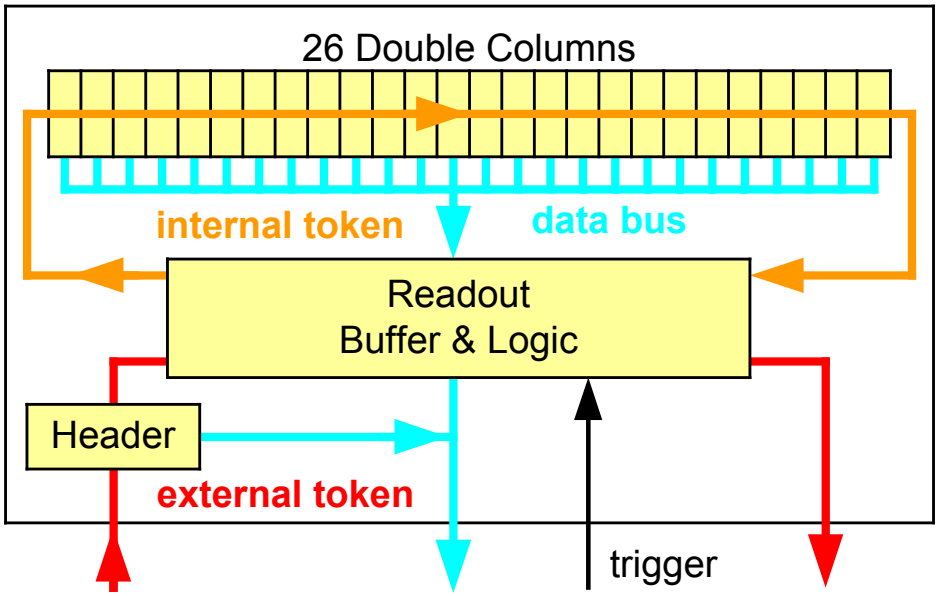
# 3. Buffered Readout

## present ROC



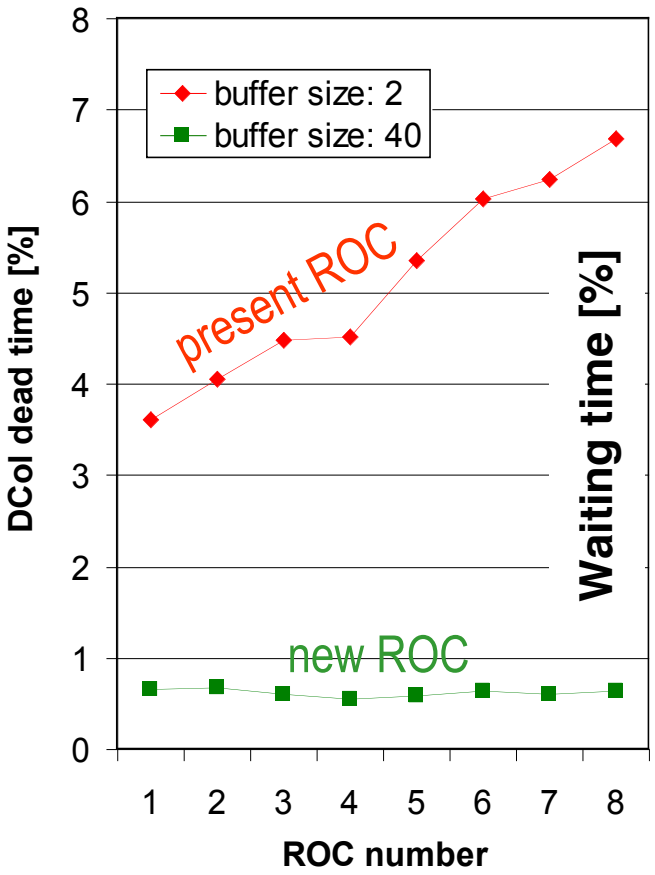

- Double columns with verified data stops → no more events accepted
- Double columns have to wait for external token → long dead time
- Sequential readout of of 8/16 ROCs → high token delay

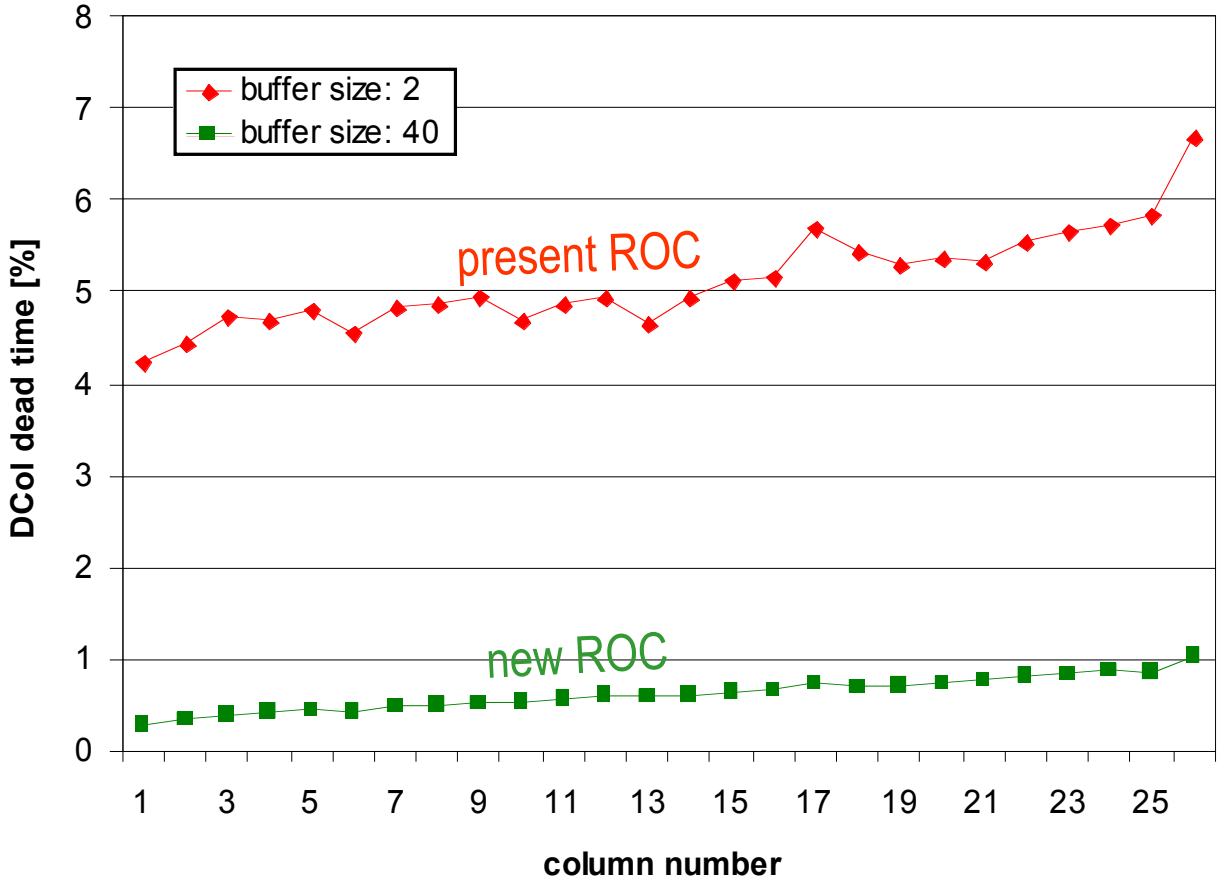
## new ROC




- DCol readout parallel in all ROCs after trigger → reduced waiting time
- ROC readout buffer: read/write simultaneous; data with different time stamps
- Easy implementation in separate buffer on ROC → keep present DCol logic

# Data Buffer Waiting Time



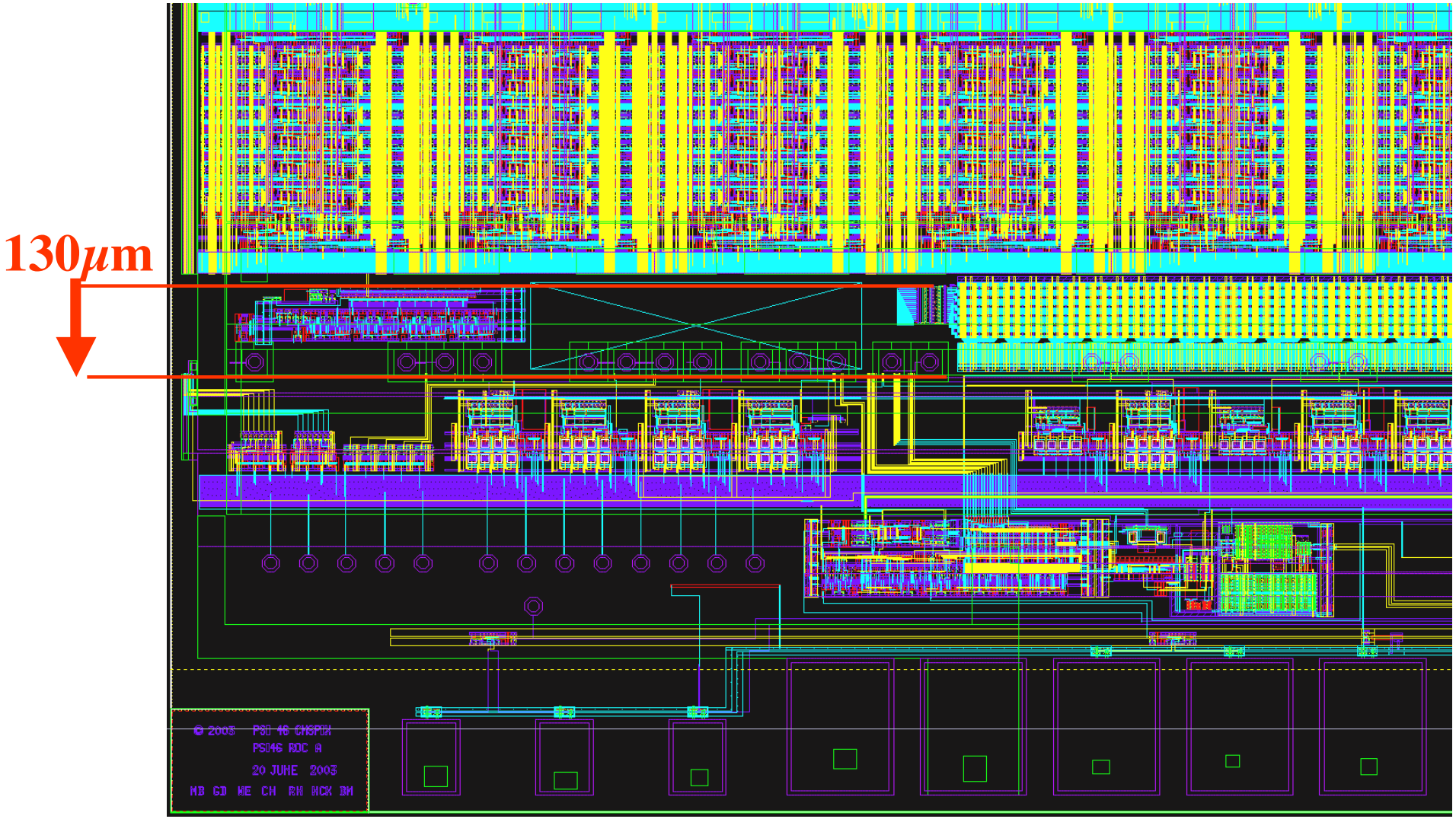

- Data verified by trigger and ready for readout
- DCol data acquisition blocked
- Waiting for readout
- (Not direct translation into inefficiency)

# Readout Buffer

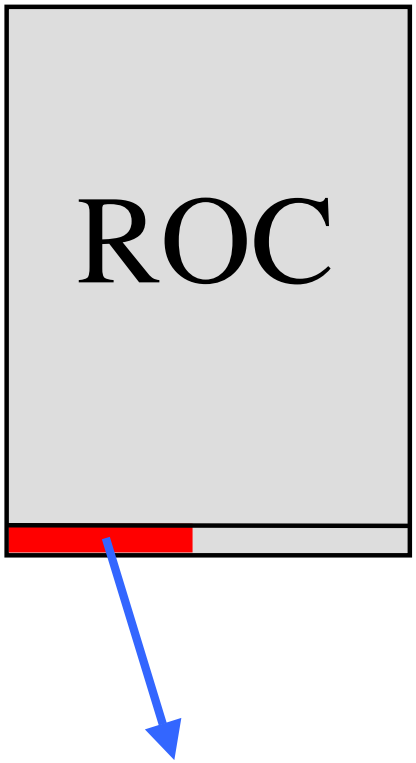
- 64 x 24 bit static RAM with address decoder in each cell
- Simultaneous read and write (synchronous to clock)
- Two 6 bit counters for read and write pointer, IO buffer
- 24 bit cell size: 57.56 $\mu$m x 124 $\mu$m
- 64 cell & control logic: 3800 $\mu$m x 124 $\mu$m (L x W)
- Space for 64 + 32 = 96 cells (5640 $\mu$m)
- Integration in ROC easy to do

☑ Schematic, Layout of RAM
☐ Control logic with counters
☐ Simulation with parasitic R and C (long busses)
☐ Insertion in ROC (insertion study done)

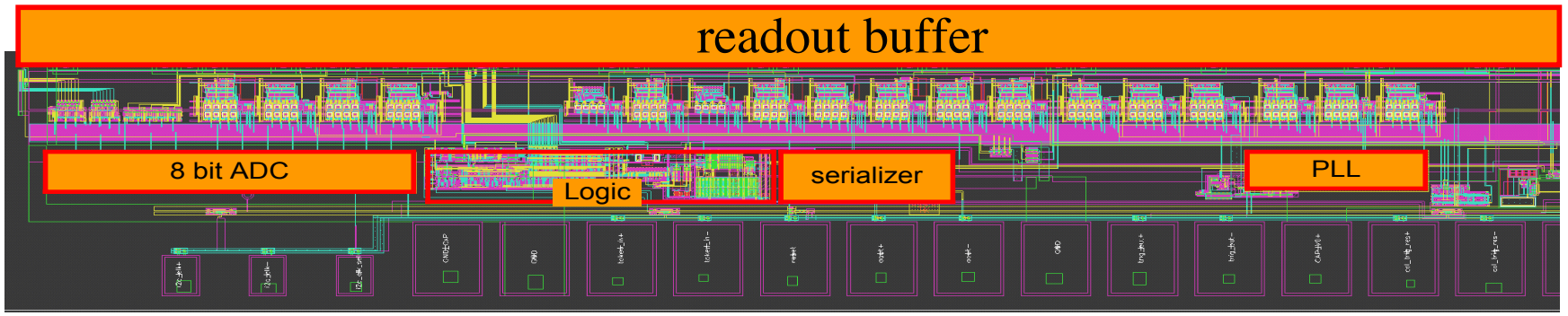
# Insertion in Digital ROC



# Overview of the Digital ROC




- No pixel cell modifications
- Increase double column buffers
- Extra space for readout buffer
- Additional and replaced components in CIB
- Same interface to double column periphery
- Same wire bond pads



# Conclusion

- A readout chip for the Phase I upgrade of the CMS pixel detector is under design
- It is based on the present ROC, changes are made only in the chip periphery
- Due to higher data rates/ROCs per link a change to high(er) speed digital links is needed
- A buffered readout scheme is introduced to reduce readout related deadtime
- Design mostly finished. Critical blocks have been submitted and tested
- Full chip to be submitted in fall 2011