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Digital Readout for the CMS Pixel Phase I Upgrade

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for the CMS Pixel Group

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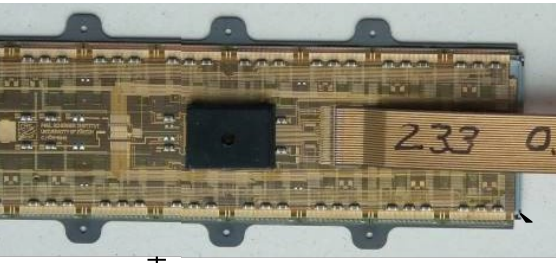
Introduction – Boundary Conditions

CMS Pixel Phase I Upgrade

- Performance improvement
  - More layers for robust pattern recognition
  - Reduction of material in tracking region
  - Higher rate capability, reduce readout deadtime
- Minimal disruption of data taking
  - Interface to CMS (DAQ, control)
- Re-use existing services (power cables, readout fibers, cooling tubes)
  - 3 layers + 2 disks → 4 layers + 3 disks factor 1.6 increase of channels
  - Readout: analog coded 40 MHz → digital coded 320 MHz
    ~ factor 2 bandwidth increase

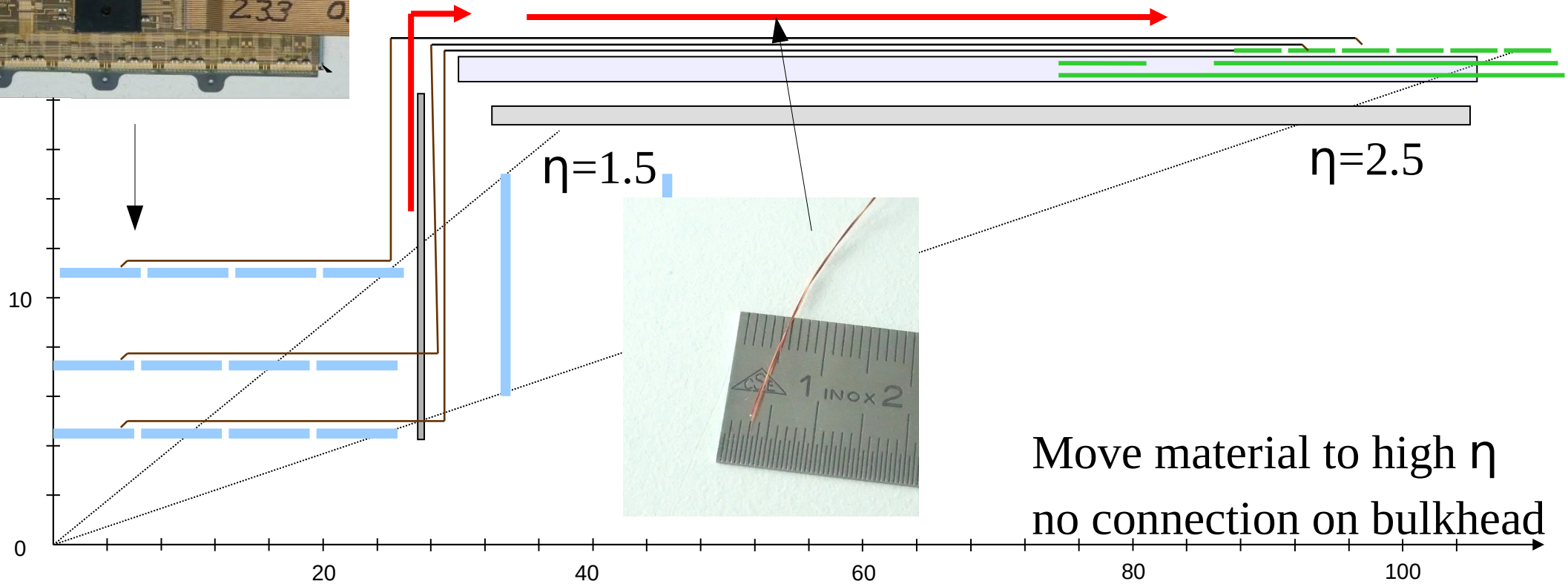
Readout overview (1)

Module



Low mass twisted pair

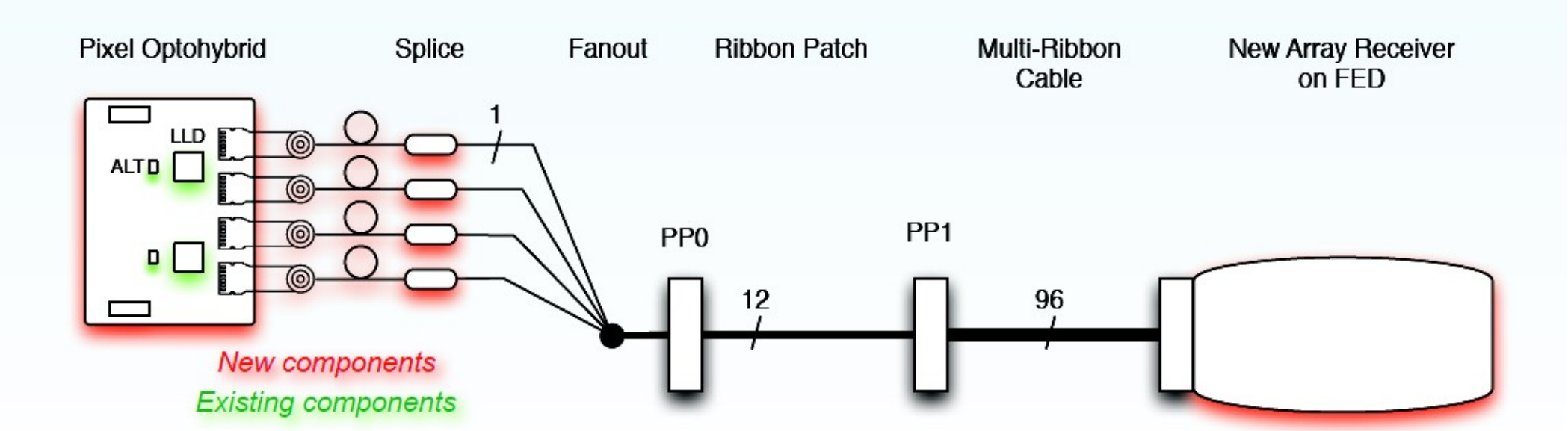
Electrical to optical



Move material to high η

no connection on bulkhead

Readout overview (2)

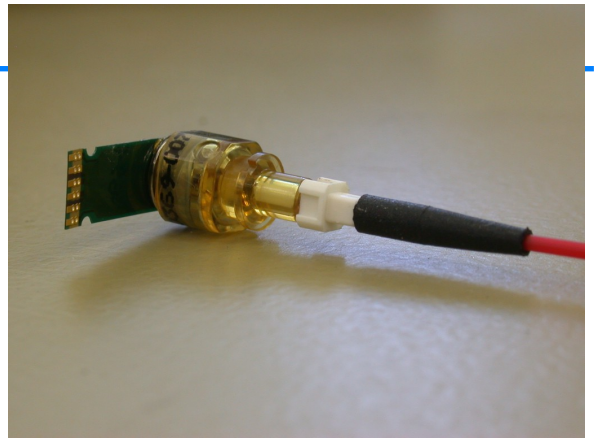


New optical hybrids, existing laser driver and level adapter chips, new lasers

re-use exiting fibers

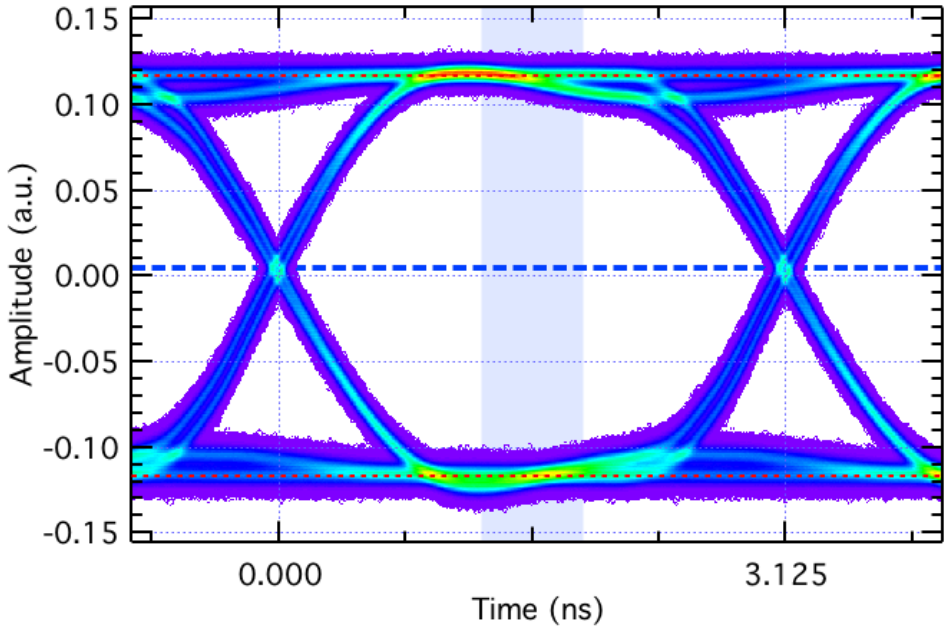
New daughtercards with receiver arrays (Zarlink)

Optical hybrid tests



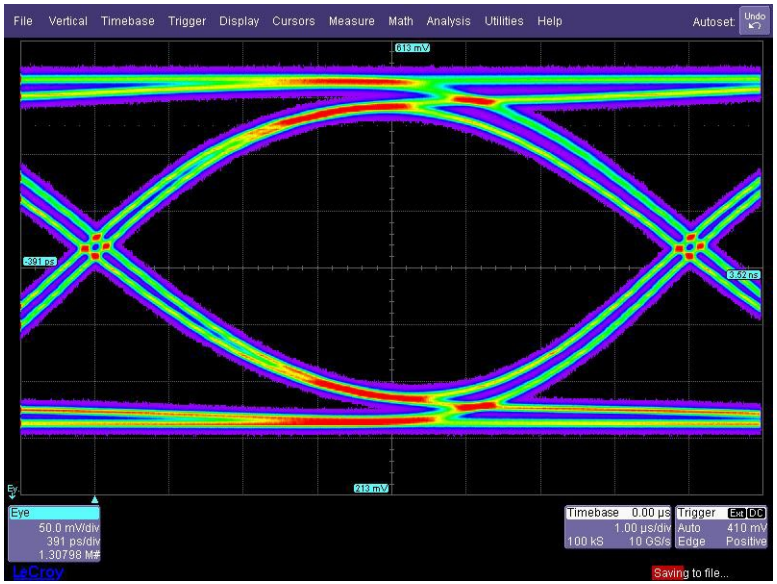
Existing laser driver (LLD) + Laser

320 MHz

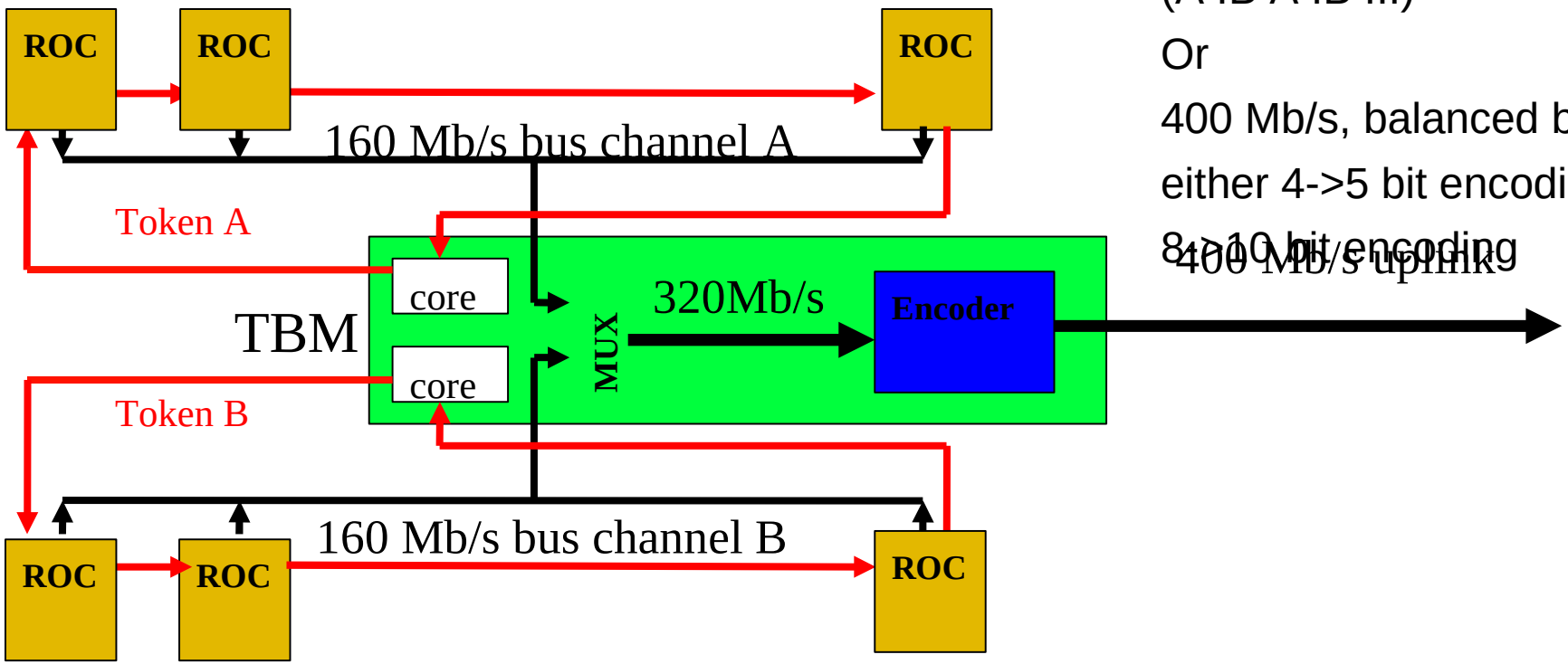


J. Troska

With level adapter (ALT)



Barrel TBM architecture



320 MHz pseudo-balanced
(A !B A !B ...)
Or
400 Mb/s, balanced by
either 4->5 bit encoding or
8->10 bit encoding

Forward detector has one fiber per two modules: separate MUX

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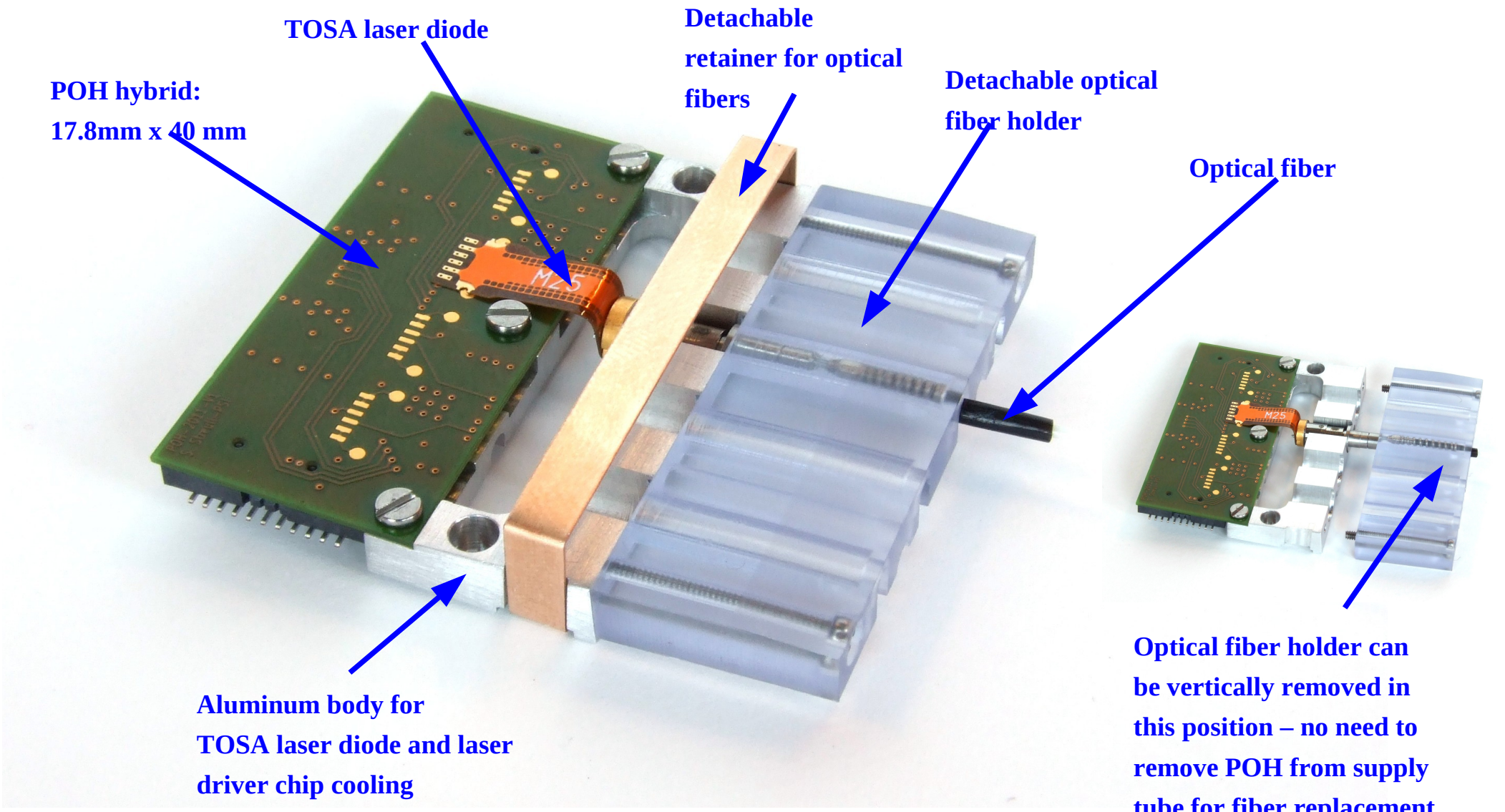
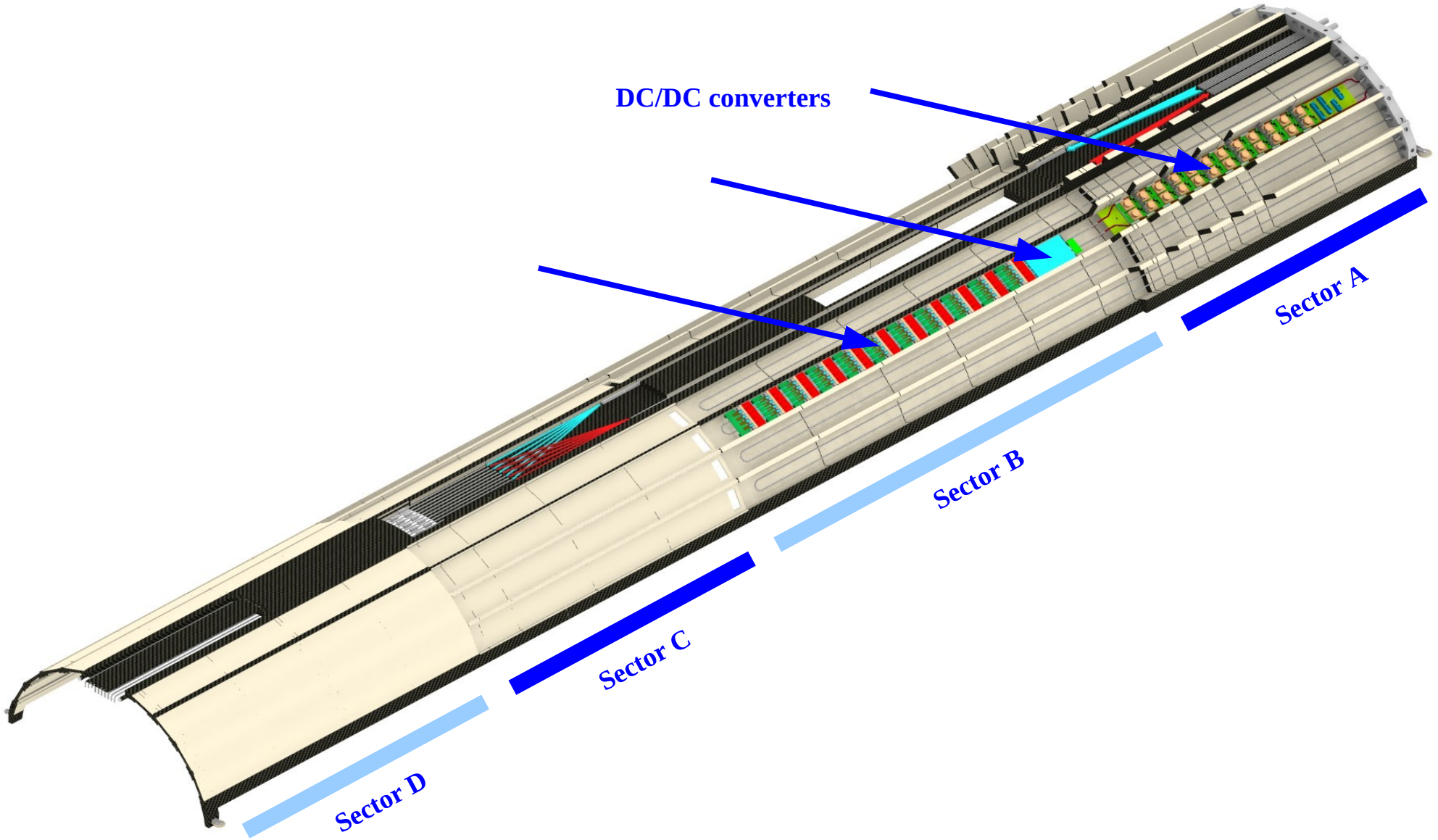
Optical Hybrid



Supply tube with opto hybrids & DC/DC converters



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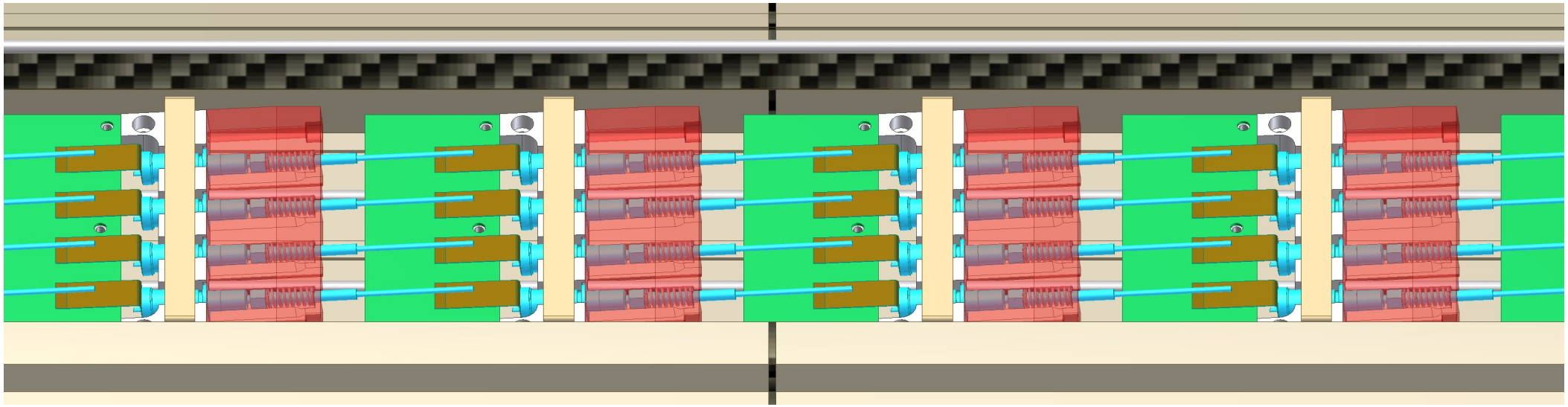
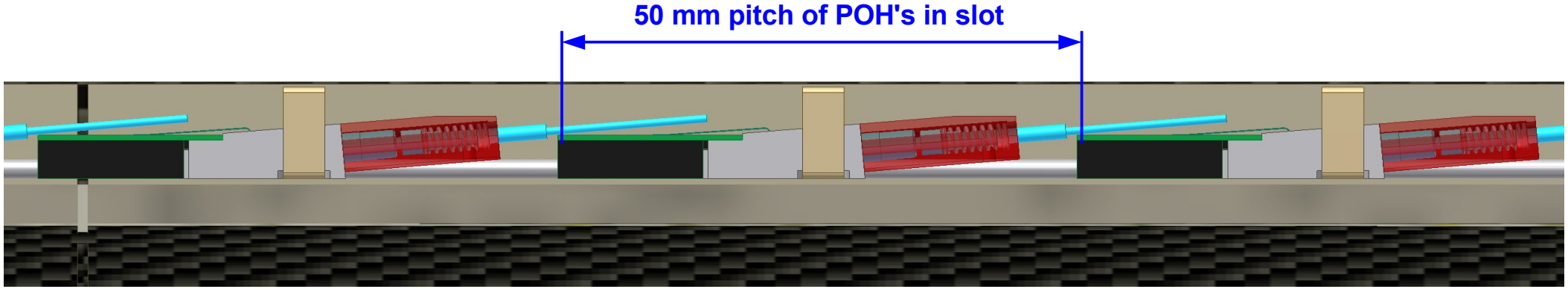
POH opto hybrids in supply tube slot



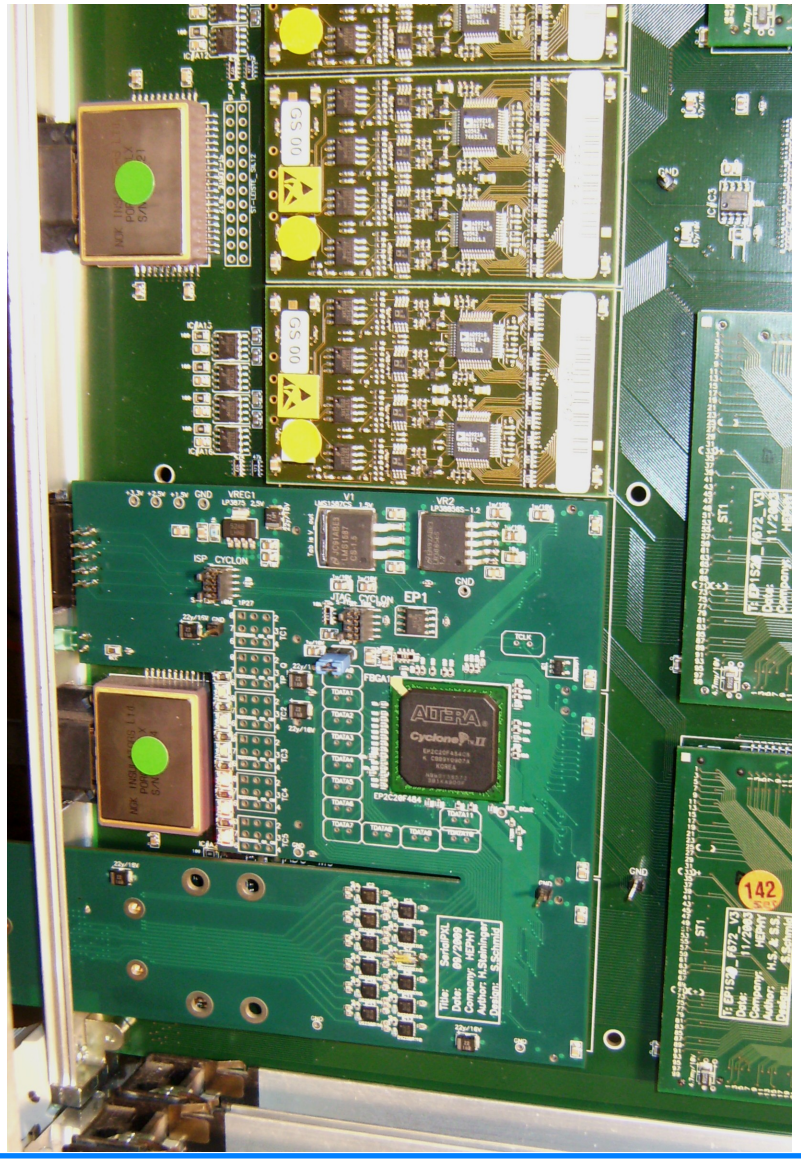
- Cross section of one slot on supply tube



FED / Optical receivers (HEPHY)

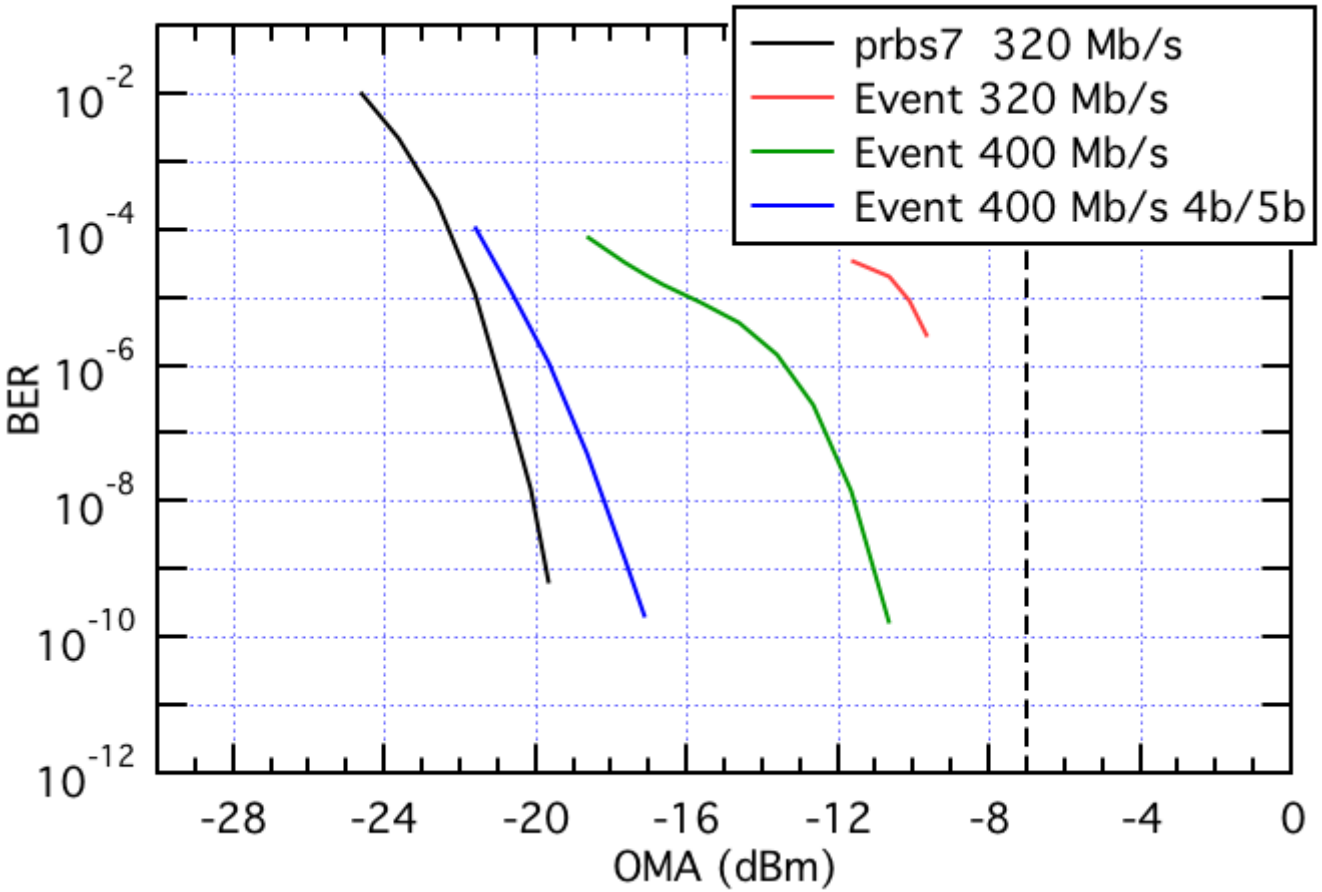
- FED
  - Interface to CMS DAQ
  - Optical receivers on daughter-cards
  - 12 PIN array (ZARLINK)
    + de-serializer in FPGA
  - Tests with simulated data patterns
    - Unacceptable bit errors observed
    - Deterministic, errors occur at sequence segments with largest 0/1 imbalance
    - Pseudo-balancing not sufficient
    - much better with balanced code

H. Steininger



Link tests (CERN)

Similar conclusion from CERN test,
although less severe (different RX version)



RX designed for GHz

balanced encoding preferred

TBM: 320 -> 400 MHz

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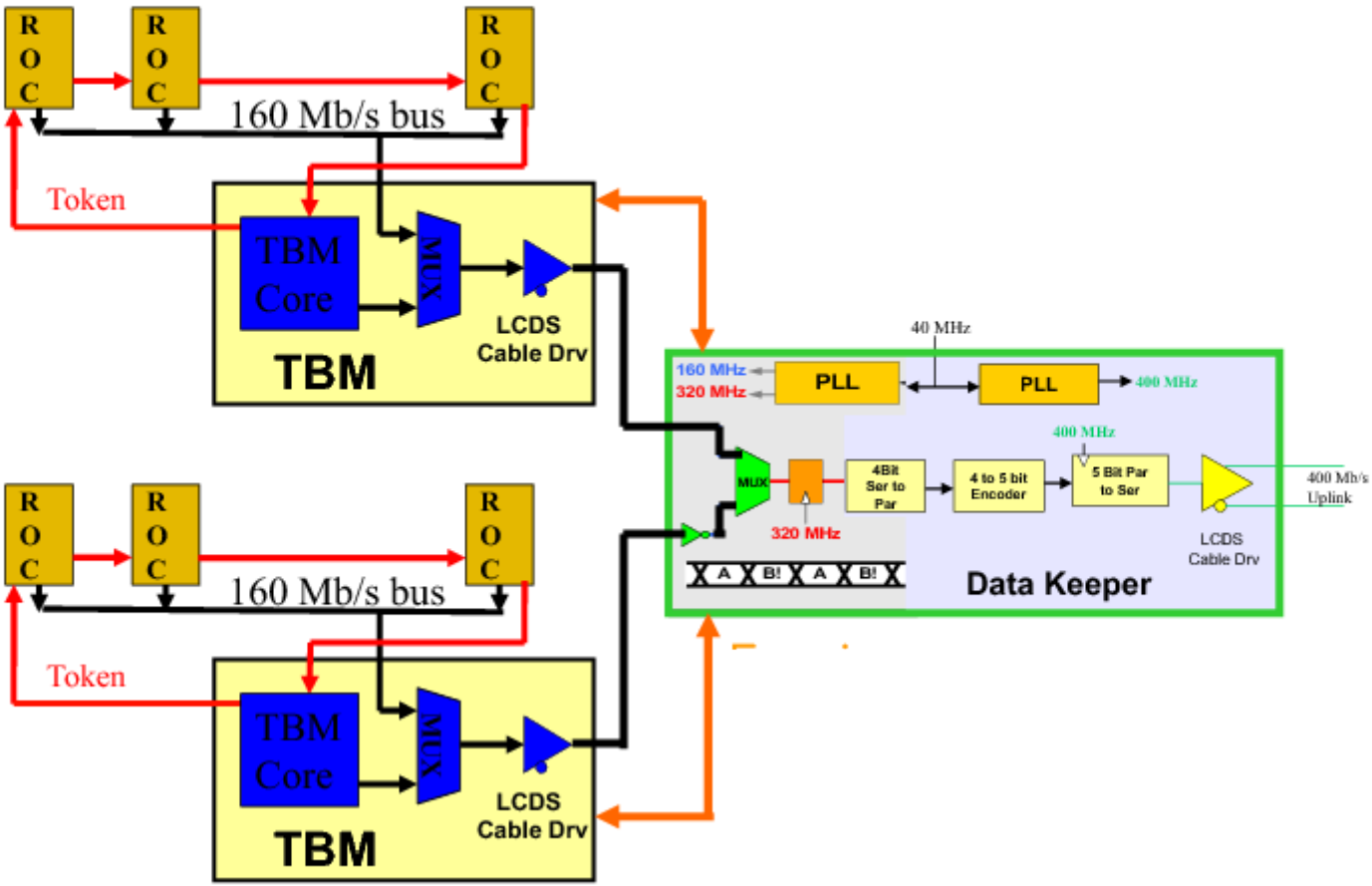
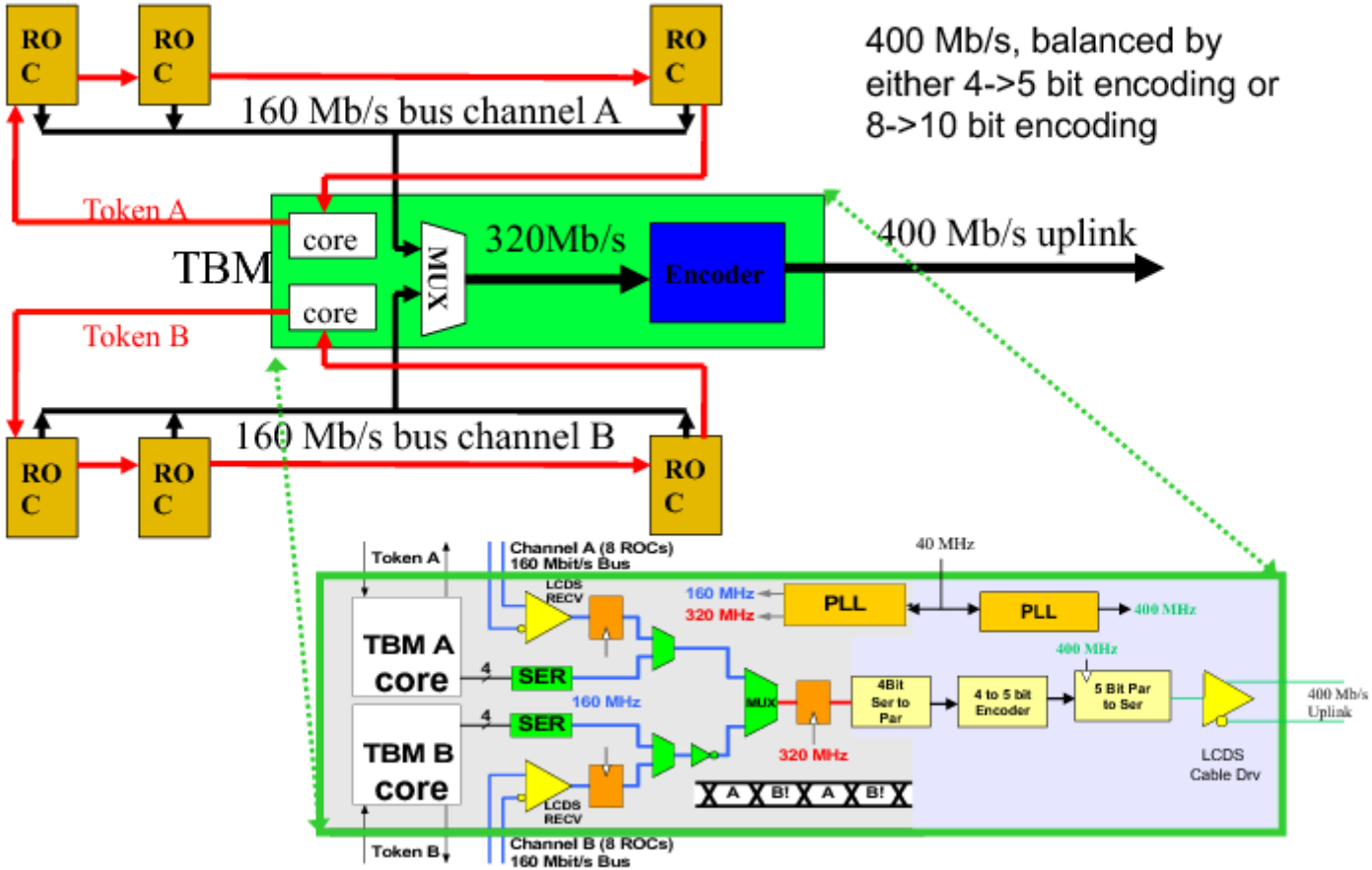
Summary

- The phase I upgrade of the CMS pixel detector must re-use exsting fibers, the bandwidth per fiber must be doubled
- A digital 320 (400) MHz link will replace the analog data transmission
- Tests with possible components and prototypes are underway

Forward TBM Architecture



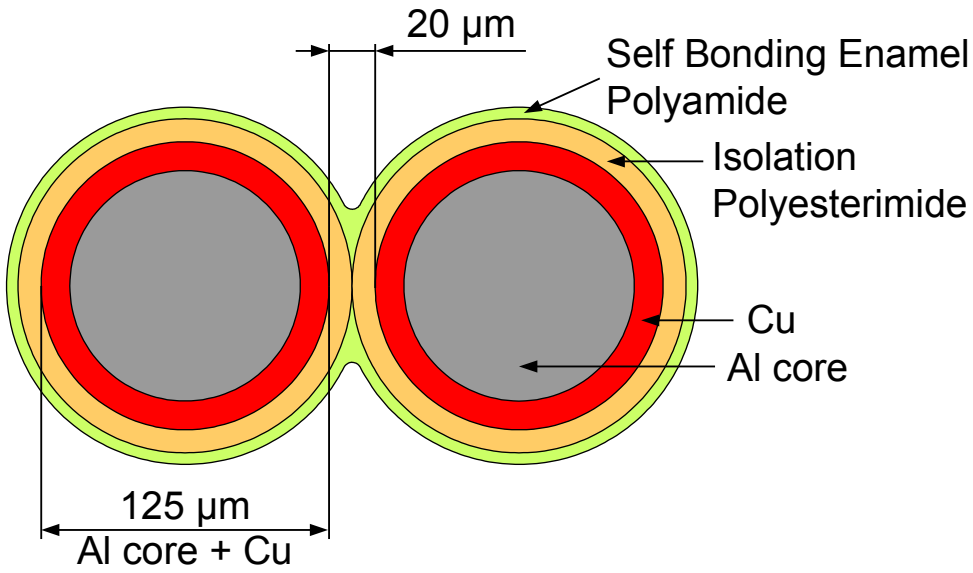
Barrel TBM Architecture

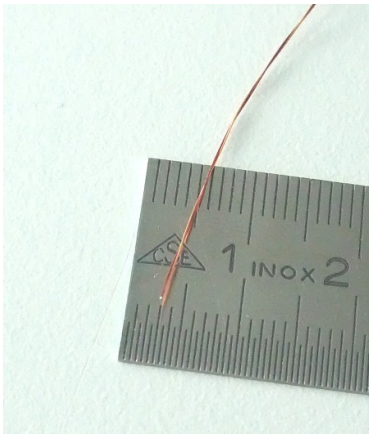


E. Bartz / B.Meier

Micro Twisted Pair Cable

cross section





First Choice:

- twisted pair self bonding wire
- 125 µm wire diameter (4um Cu)

Electrical characteristics:

- Impedance: 50 Ohms diff. (low)
- v = 2/3 c_0 (5 ns/m)
- C = 100 pF/m, L=250 nH/m

Verilog Simulation of Readout Logic

Full module digital functional simulation includes:

- 16 ROCs: DCOL Readout, Readout Buffer, ROC Readout, data mux & serializer
- Dual TBM: 2 TBM5 cores, digital readout logic, serializer (no programming logic I2C)
- 320 MBit/s serial data output
- FED decoder
- Simulation speed: 60 µs/sec