2011

Advanced Packaging in LETI

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CEA-LETI-Minatec

ACES 2011 – CERN – 10-03-2011

General outline

1. Introduction
2. Wafer Level Packaging
   - Key processes & technologies
   - Applications examples
3. 3D Integration
   - Key processes & technologies
   - Applications examples
4. Conclusion and perspectives

Leti at a Glance

→ Founded in 1967 as part of CEA
Leti is ISO2001 standard certified

CEO Dr. Laurent Malier

1,600 researchers

190 PhD students + 34 post PhD

227 M€ budget

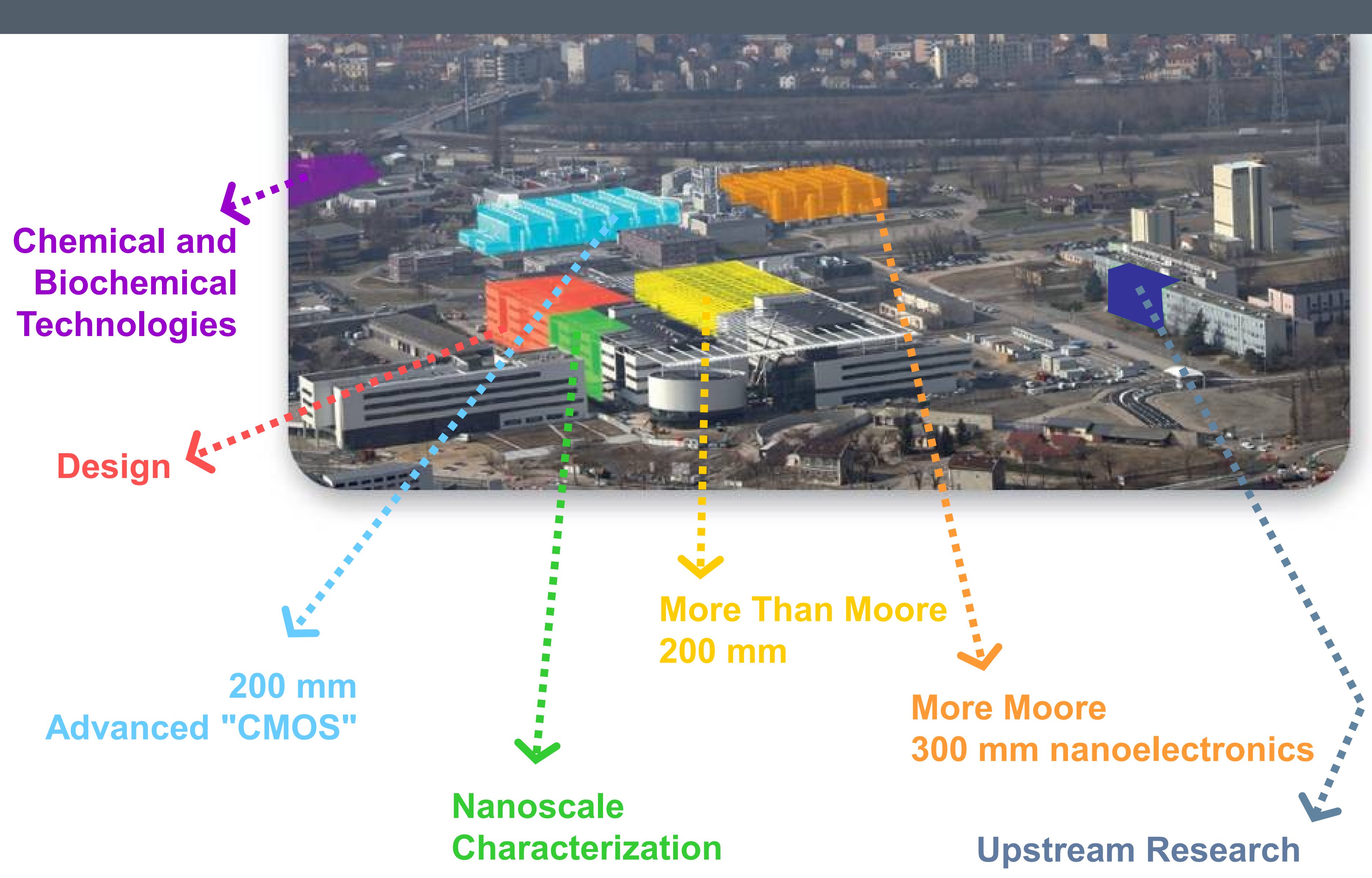
> 75% from contract
~ 30M€ CapEx

Over 1,700 patents

284 in 2009
40% under license

37 start-ups & 23 common labs

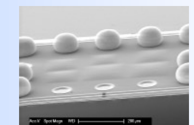
Leti's Research Infrastructures

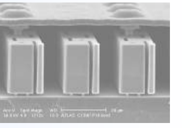


Advanced packaging in LETI : two research axes

Packaging & integration team in LETI : ~ 60 people involved in :

Wafer Level Packaging





Manage functions at wafer level :
- Mechanical protection
- Hermeticity
- Controlled atmosphere / Vacuum
- Cost decrease

Package

Silicon 3

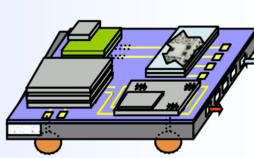
Silicon 2

Silicon 1

Electronic component

3D Integration

To assembly more than one dies in one package :
- Electrical links between strata
- Electrical links with external world
- Thermal management
- Form factor reduction
- Cost decrease



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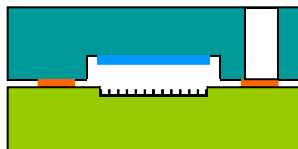
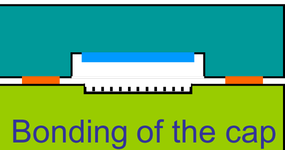
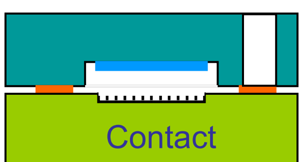
Wafer level packaging approaches

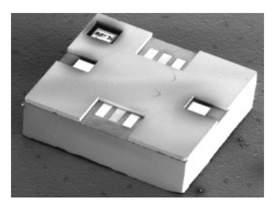
Two integration schemes :

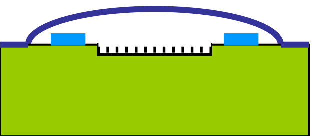
Bonding cap



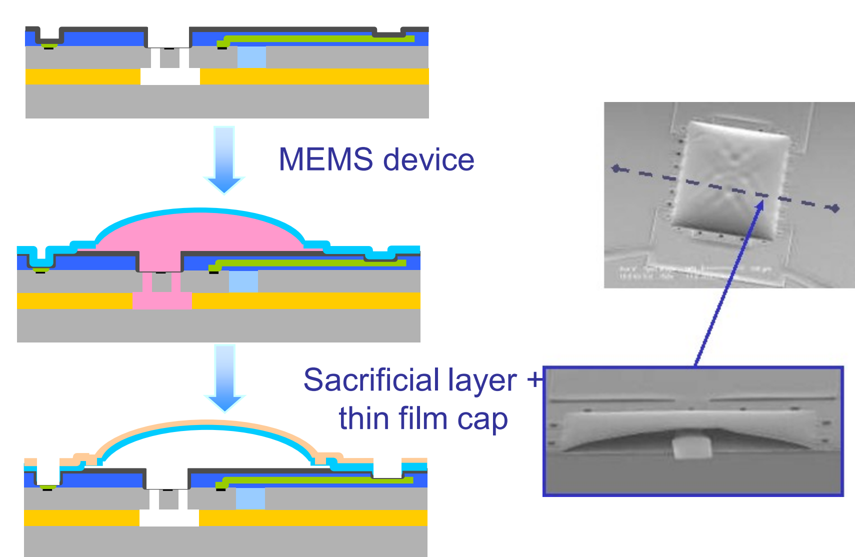








An ultra compact solution, compatible with IC fabs

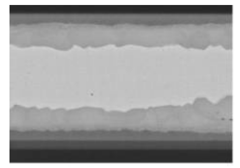


Holes sealing

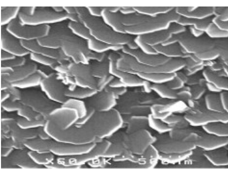
Wafer level packaging approaches

- Requires to develop Generic technologies :

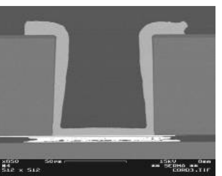
Bonding



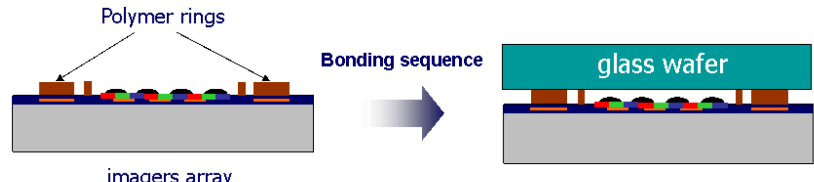
Getters



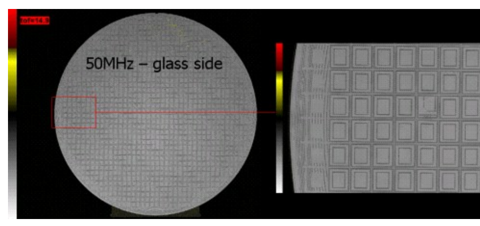
Contact

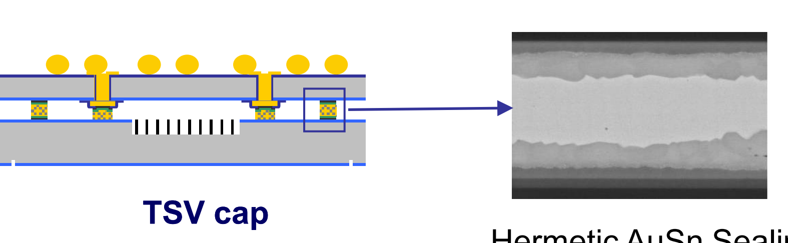


- **Bonding :**
  - Polymer solution for prototyping and low cost applications
  - Eutectic bonding : An hermetic solution, compatible with high vacuum, and flip chip



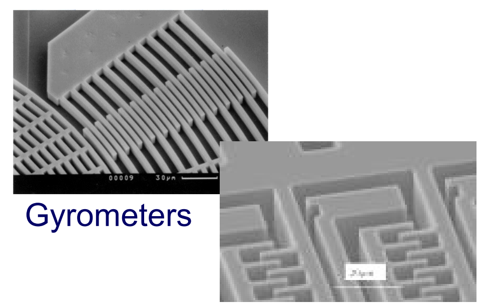
CIS application





TSV cap

Hermetic AuSn Sealing

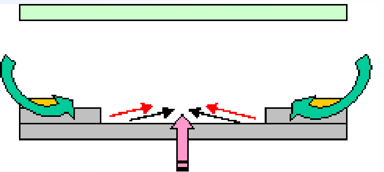


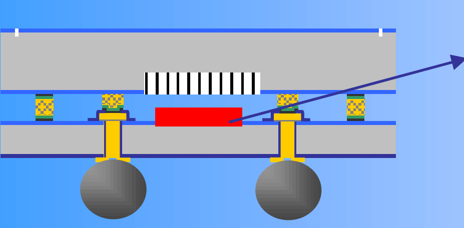
Gyrometers

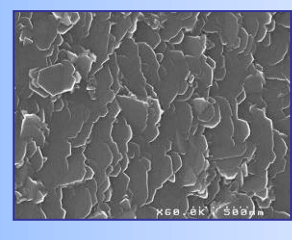
Accelerometers

Generic technologies : getters

- **Why do we need getters in cavities :**
  - Controlled and Low pressure (< 10-2 mbar) required in micro-cavities
  - Outgassing sources : sealing / MEMS / µleaks / permeation
  - Outgassing sources could become critical for the pressure

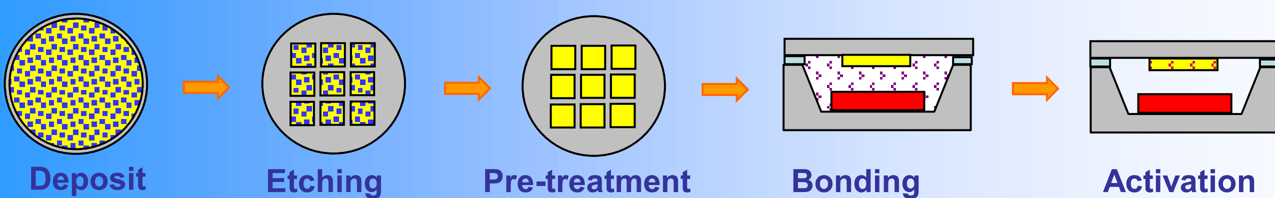






Getter material is able to pump residual gases

- Deposited and patterned as a standard layer (no outsourcing)
- Tunable activation temperature (to fit with sealing process)
- Compatible with both wafer bonding and thin film packaging



Generic technologies : contact by TSV

- **Electrical contact to outside world :**
  - Hermetic metallic sealing (AuSn Wafer to wafer bonding)
  - TSV (Through Silicon Vias) in the cap wafer
  - Direct available for flip-chip

Electrical lift: Via Last TSV

MEMS Wafer

Hermetic AuSn Sealing

Available on 200 mm wafers

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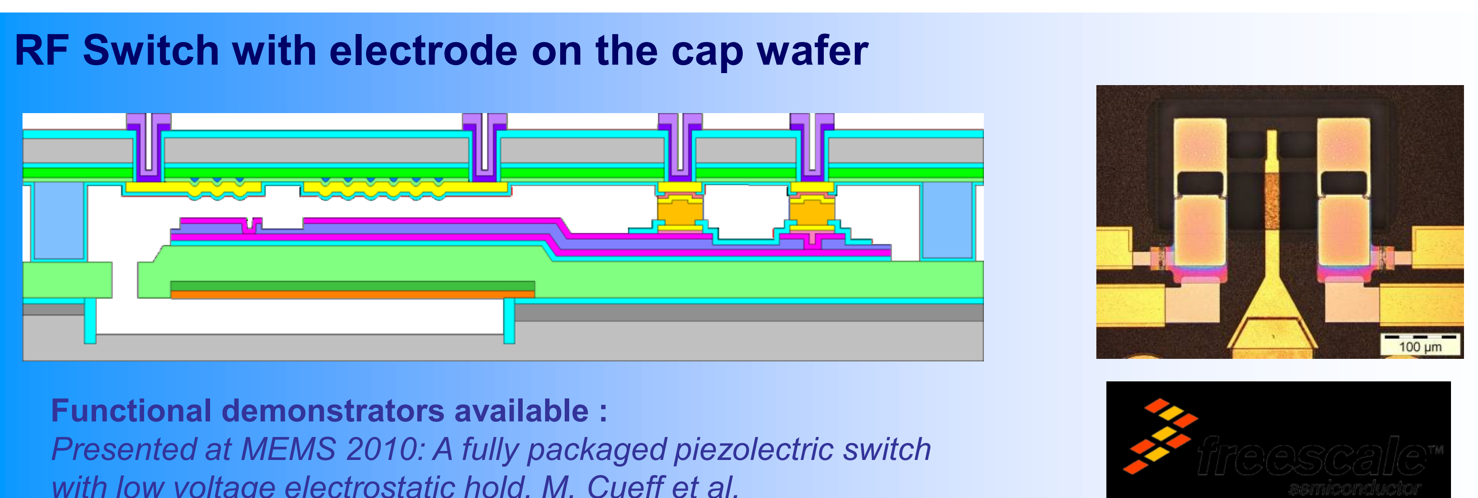
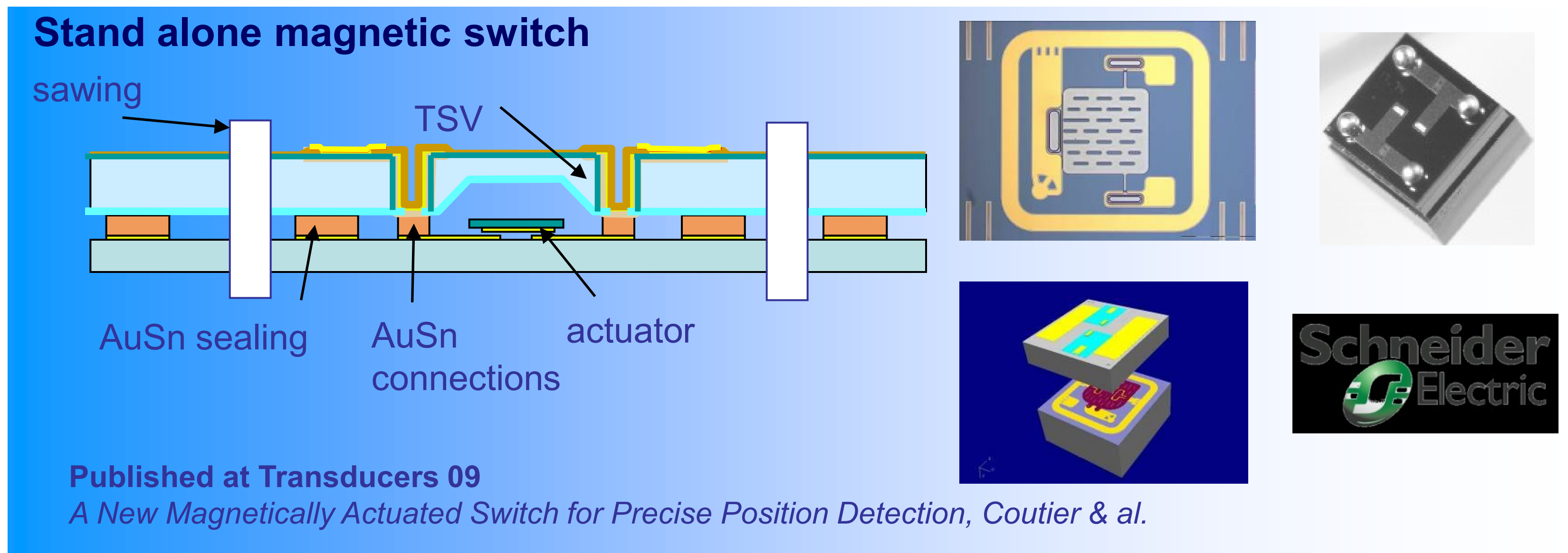
Applications for Bonding cap

RF Switch with electrode on the cap wafer



Functional demonstrators available :
Presented at MEMS 2010: A fully packaged piezolectric switch with low voltage electrostatic hold, M. Cueff et al.

Stand alone magnetic switch



Published at Transducers 09
A New Magnetically Actuated Switch for Precise Position Detection, Coutier & al.

Application for bonding cap: BAW protection

BAW manufacturing

Cap manufacturing & release

Closing

Bumping

Flip chip on BGA

BAW

Stacked on IC

Molding

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What is 3D Integration ?

It's the way to achieve an electronic system or a component by using the third dimension (Z) instead of only the two first dimensions (X & Y)

- **3D Integration key drivers :**
  - **Form factor decrease**
    - Miniaturization of final device (X,Y,Z)
  - **Performances improvement**

    - Decrease R, C, signal delay
    - Increase device bandwidth
    - Decrease power consumption
  - **Cost decrease**
    - Si surface decrease
    - Reuse of existing Packaging, BEOL & FEOL lines

Memory
passive
Substrate
Logic

One Chip
SetTopBox (STM)

128 GB SSD, Toshiba

LETI approach for 3D Integration

- Based on a tool box, including :

Modeling
- Thermo mechanical & thermal Modeling
- Electrical Modeling

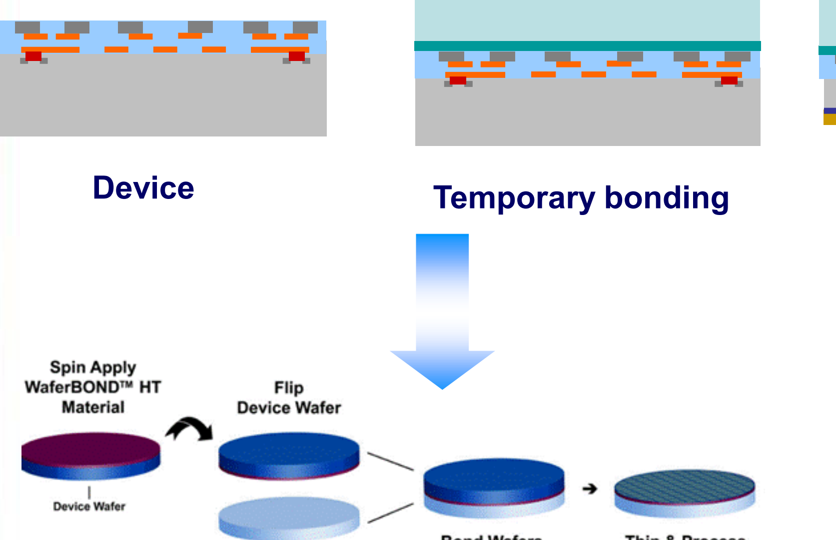
Design layout
- 3D implementation & partitionning
- Standard Design rules manuel & Design kit
- Layout & masks

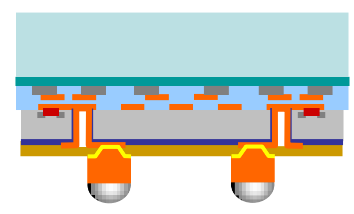
Focus on today's presentation

Indust. / Mfg
- Reliability
- Test strategy
- Cost analysis

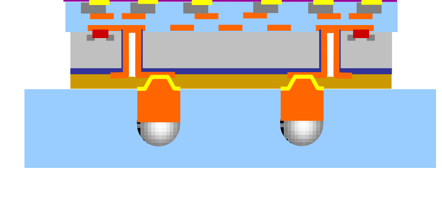
Temporary bonding / Thinning/handling Toolbox

Temporary bonding / thinning / handling

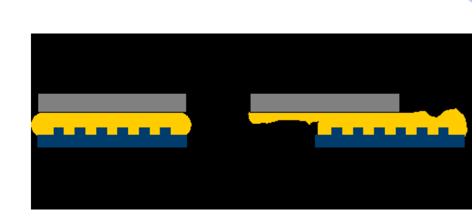




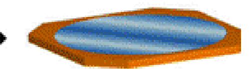
3D techno



Debonding / handling / Stacking

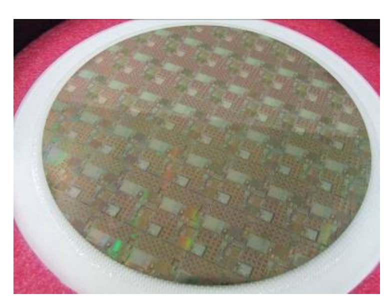


Source : A. Jouve / Brewer Science / 3D IC 2009



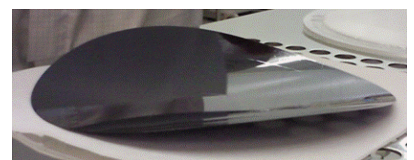
Mount to Film Frame for Transport

EVG 520 bonder



Wafer bonded with temp. glue

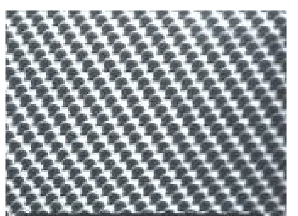
Debonder EVG 805

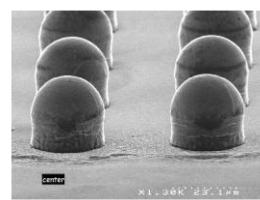


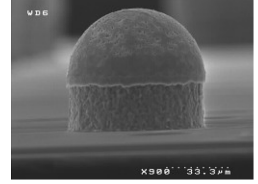
Debonded wafer (70 µm)

Interconnections toolbox

Face to face connections

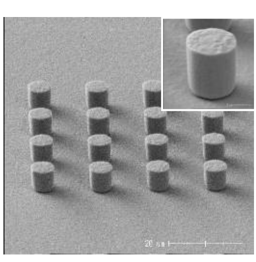




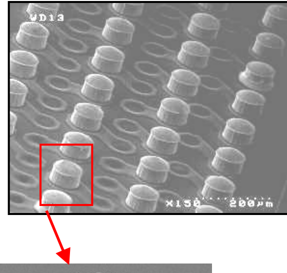


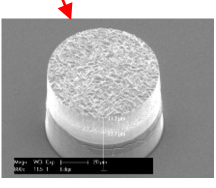
C2C pillars
SLID / TLP

Classic Flip chip
(Ball or stud bump)

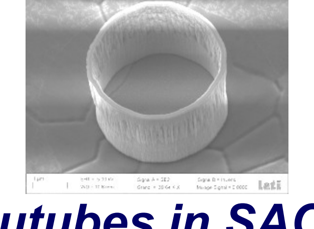


Solder-free µinserts

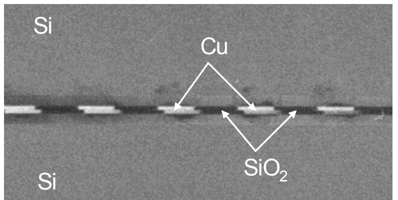




C2S pillars



µtubes in SAC



Cu-Cu Direct bonding

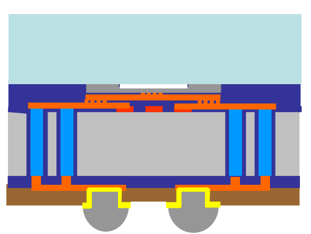
> 100 µm — *100-30 µm range* — *30-10 µm range* — *Down to 5 µm*

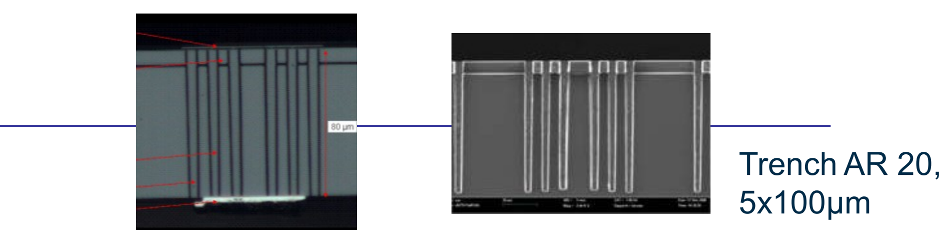
Pitch reduction

TSV Toolbox

Through Silicon Via (TSV)

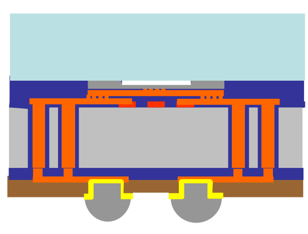
Via First TSV (Polysilicon filled)

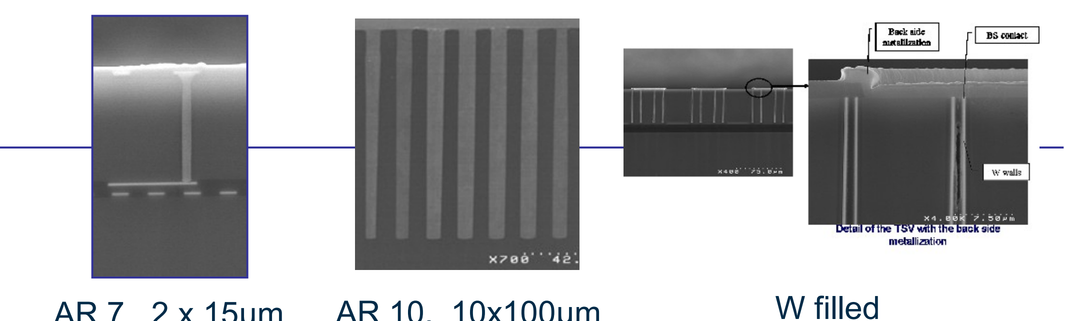




Trench AR 20, 5x100µm

Via Middle TSV (Copper or W filled)



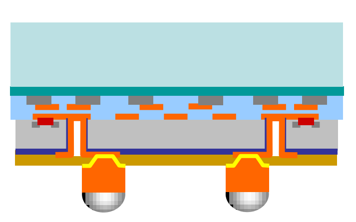


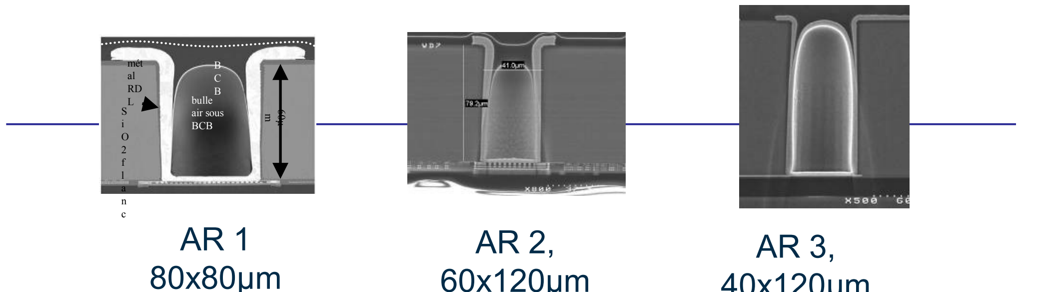
AR 7 , 2 x 15µm

AR 10, 10x100µm

W filled

Via Last TSV (Copper liner)





AR 1 80x80µm

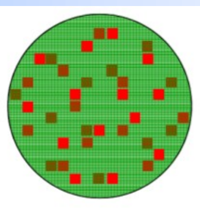
AR 2, 60x120µm

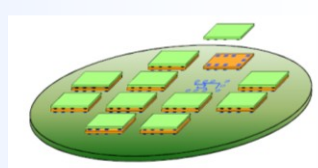
AR 3, 40x120µm

TSV Toolbox

Components placement

- 2 approaches for components stacking
  - Wafer to wafer (W2W)
  - Chips to wafer (C2W)
    - High speed
    - High accuracy

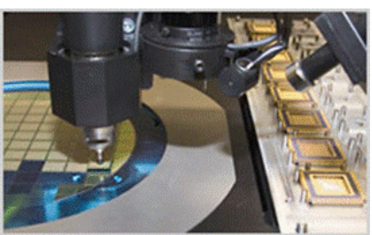




Datacon

SET FC 300

EVG 560



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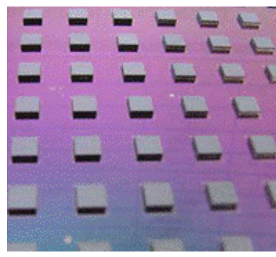

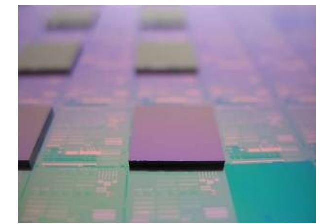

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Assembling the bricks as a LEGO…

1 active layer | Face to Face | Face to back | 3 level stack

Die/die	Die/substrate	TSV	Handling	Die placement & die molding	
Solder balls	Wire Bonding	TSV First	Temp. Bonding +slide off	High throuput P&P	Thick Polymer molding
Copper Pillars	Solder balls	TSV Middle & BS AR10	Temp Bonding + zonebond	High precision P&P	Thin Polymer molding
µinserts	Copper pillar	TSV Last AR1	Permanent bonding	Self Assembly	Thin Oxyde planarisation
µtubes		TSV Last AR2		Wafer To Wafer	WLUF
Cu-Cu		TSV Last AR3			Classic Underfill
DTW Cu-Cu		TSV Last High density			

Assembling the bricks…

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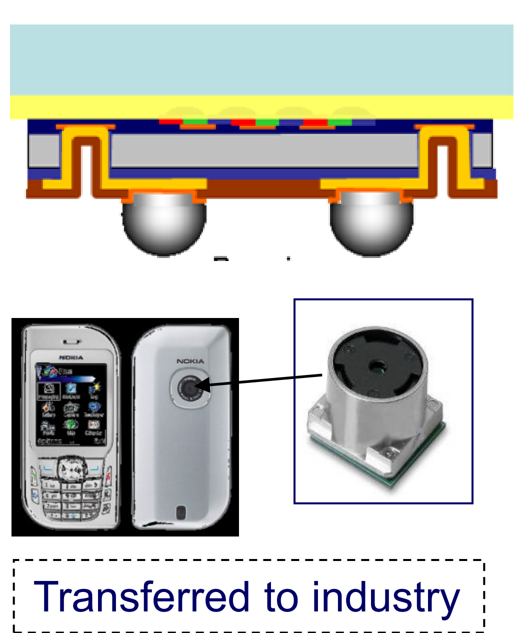
TSV for CMOS image Sensors



Transferred to industry

1 active layer	Face to Face	Face to back	3 level stack		
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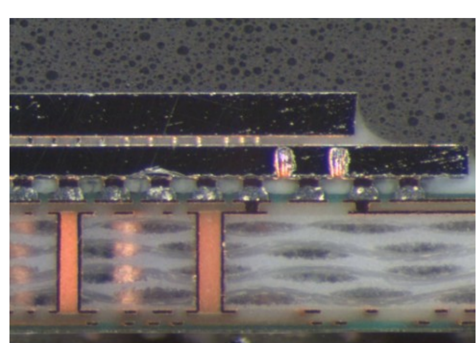
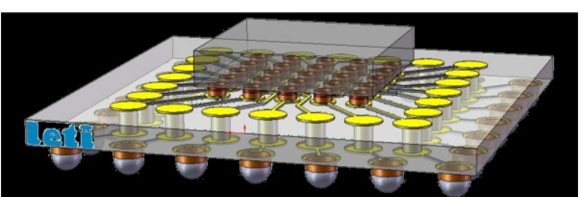
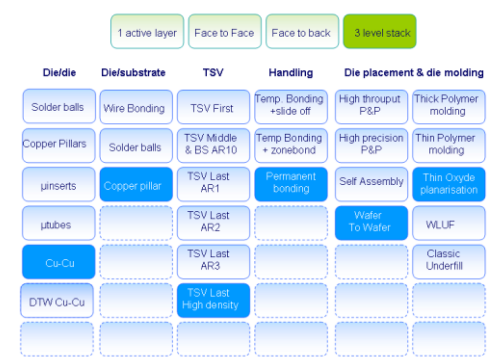
Silicon interposer







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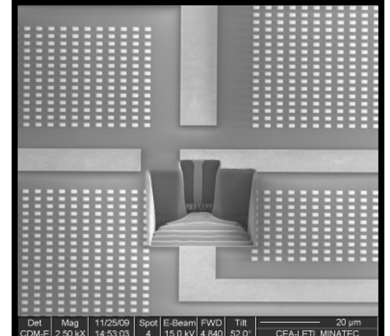
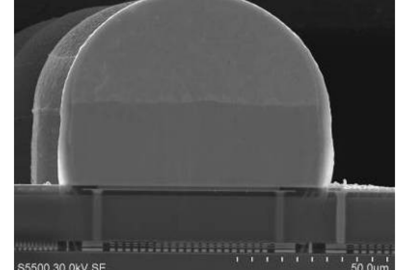
Die/die	**Die/substrate**	**TSV**	**Handling**	**Die placement & die molding**	
Solder balls	Wire Bonding	TSV First	Temp. Bonding +slide off	High throuput P&P	Thick Polymer molding
Copper Pillars	Solder balls	TSV Middle & BS AR10	Temp Bonding + zonebond	High precision P&P	Thin Polymer molding
µinserts	Copper pillar	TSV Last AR1	Permanent bonding	Self Assembly	Thin Oxyde planarisation
µtubes		TSV Last AR2		Wafer To Wafer	WLUF
Cu-Cu		TSV Last AR3			Classic Underfill
DTW Cu-Cu		TSV Last High density			

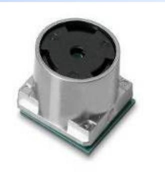
High density stack

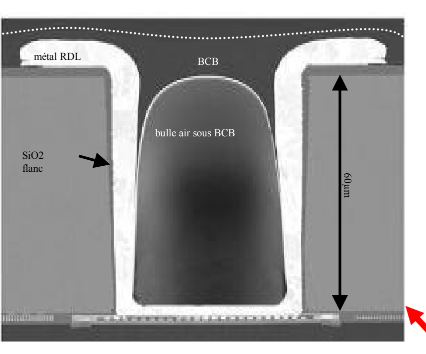


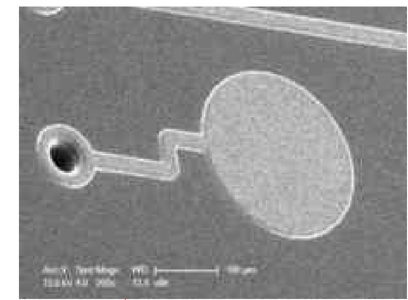


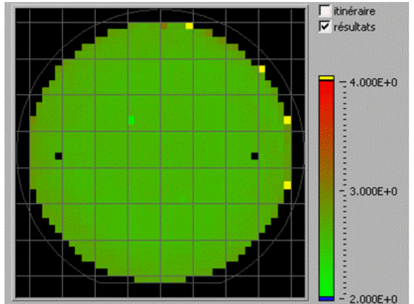
Examples of Applications with partners

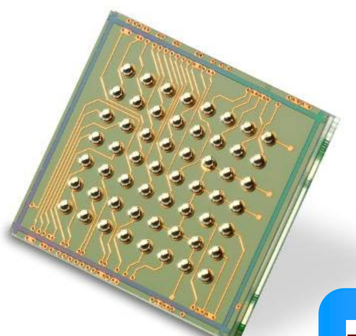
- **ST Micro / CEA-LETI**
  - CIS application for mobile phone
  - TSV AR 1 : 1

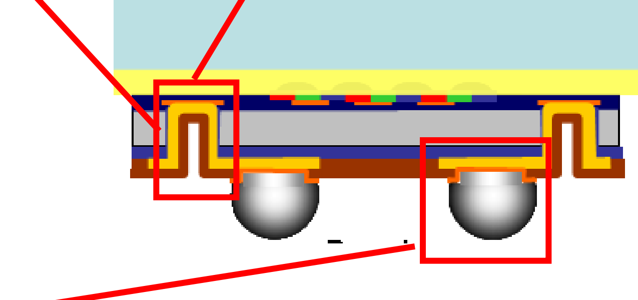












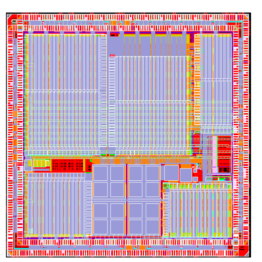
- Production mode since 2009
- 300 mm production line @ STM Crolles (FR)

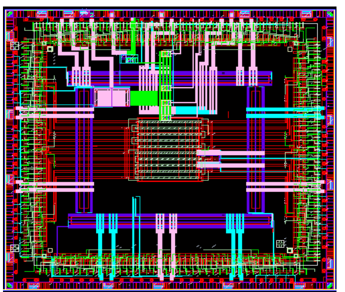
Examples of Applications with partners

- ST Micro / CEA-LETI
  - Partitioning for Set Top Box application
  - 45nm technology stacked on 130nm interposer (Mature + advanced)

Advanced CMOS (45nm)

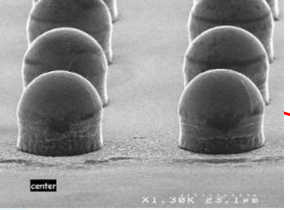
Top Chip





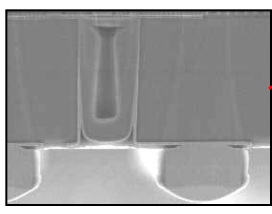
130 nm chip

Interposer

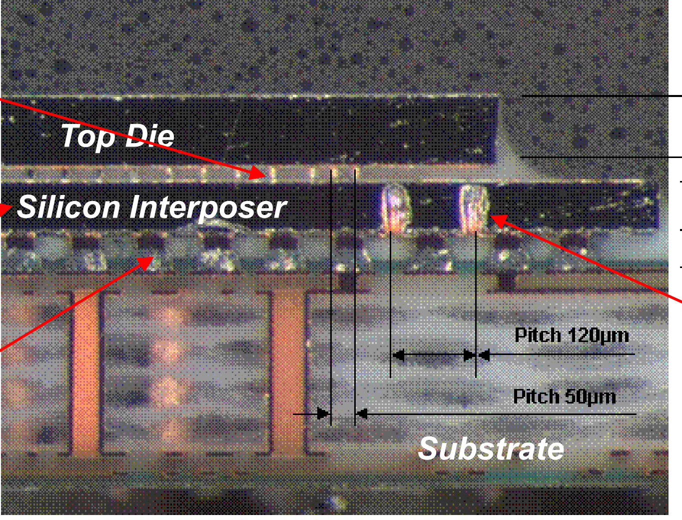


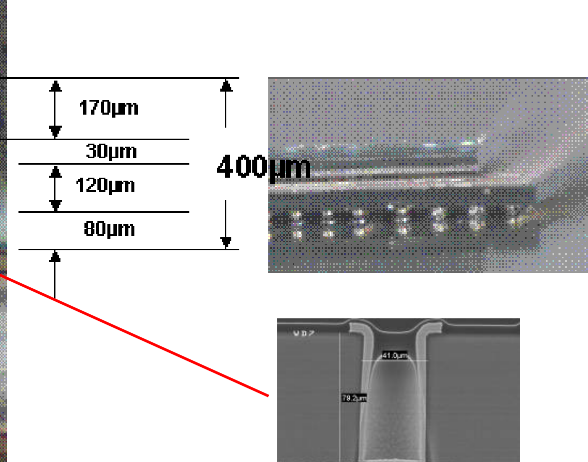
C2C Cu Pillars

Thinned wafer (120 µm)



Chip to substrate copper pillars





TSV AR 2, 60x120µm

Examples of Applications with partners

- **IPDIA / CEA-LETI**
  - Decoupling capacitance
  - RF Integrated passives
  - Integrated protection devices

ipdia
The 3D Silicon Leader

UBM

Metal 2

Metal 1

Thin silicon interposer mechanical and electrical caracterization

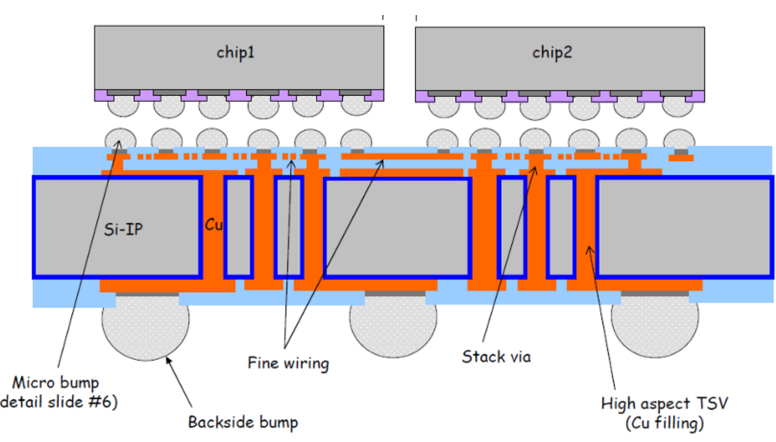
High density 3D interconnections:

Cu Pillars fabrication and analysis

Conformal insulation of TSV

Examples of Applications with partners

- **Shinko / CEA-LETI**
  - High end applications ➔ Logic stack
  - 300 mm wafers



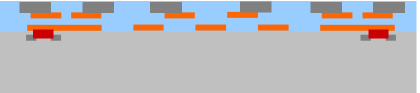
Common lab started January 2011
Nagano Engineers assigned to Leti

The next step of the toolbox : Open 3D initiative

Open 3D Initiative objectives

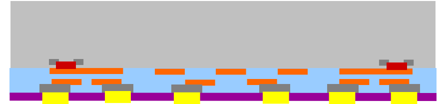
- Need of 3D technologies for a lot of applications / products: medical, bio, imaging, space, energy, …
- A complete 3D development is long and costly (techno development, specific design,…).
- OPEN 3D initiative : to offer a 3D integration solutions for demonstrators & prototyping based on existing technologies

Open 3D philosophy :

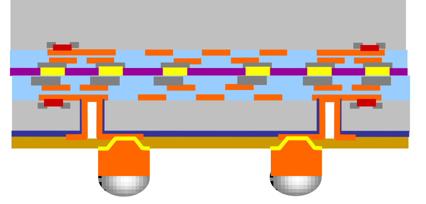


Bottom component coming from IC Foundry or customer

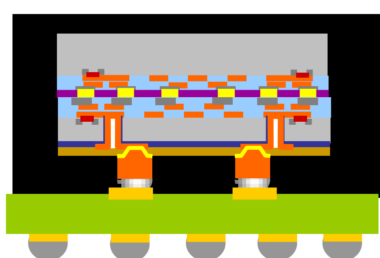
Top component coming from IC Foundry or customer



Open 3D offer
3D technologies service



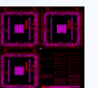
Final assy possible with packaging partners



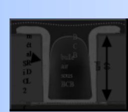
The next step of the toolbox : Open 3D initiative

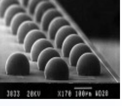
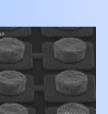
- Open 3D technological offer :

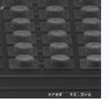
- DRM / Layout & masques

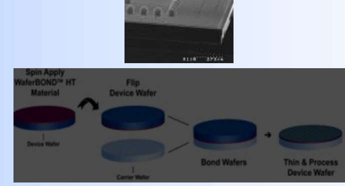


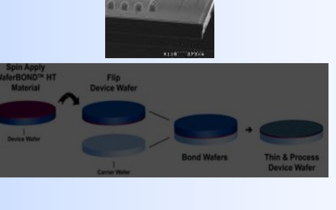
- Six elementary bricks
  - TSV Last (AR 1:1 & 2:1)
  - Interconnections C2C : Cu pillars
  - Interconnections C2C Cu post
  - Interconnections C2S : Cu pillars
  - Temporary bonding / Thinning / Debonding
  - Stacking & underfilling









General outline

1. Introduction
2. Wafer Level Packaging
   - Key processes & technologies
   - Applications examples
3. 3D Integration
   - Key processes & technologies
   - Applications examples
4. Conclusion and perspectives

General outline

Conclusions

- Wafer level packaging and 3D Integration are the best candidates of packaging & integration approaches for the next generations of devices.
- LETI has developed a technological toolbox for Wafer level packaging and 3D Integration
- A part of this toolbox is now mature and ready for using at prototype level

Perspectives / Collaboration models

- To develop new technologies to fill the toolbox and to meet our customers requirements.
- Collaboration models :
  - Classical R&D projects for new technologies developments / EU, local or bilateral funding.
  - Prototyping Via open 3D initiative

Thank you for your attention
Questions ?

Loyauté
Envie d'entreprendre
Travail en équipe
Innovation