CSC Endcap Muon ME1/1 Upgrade Status

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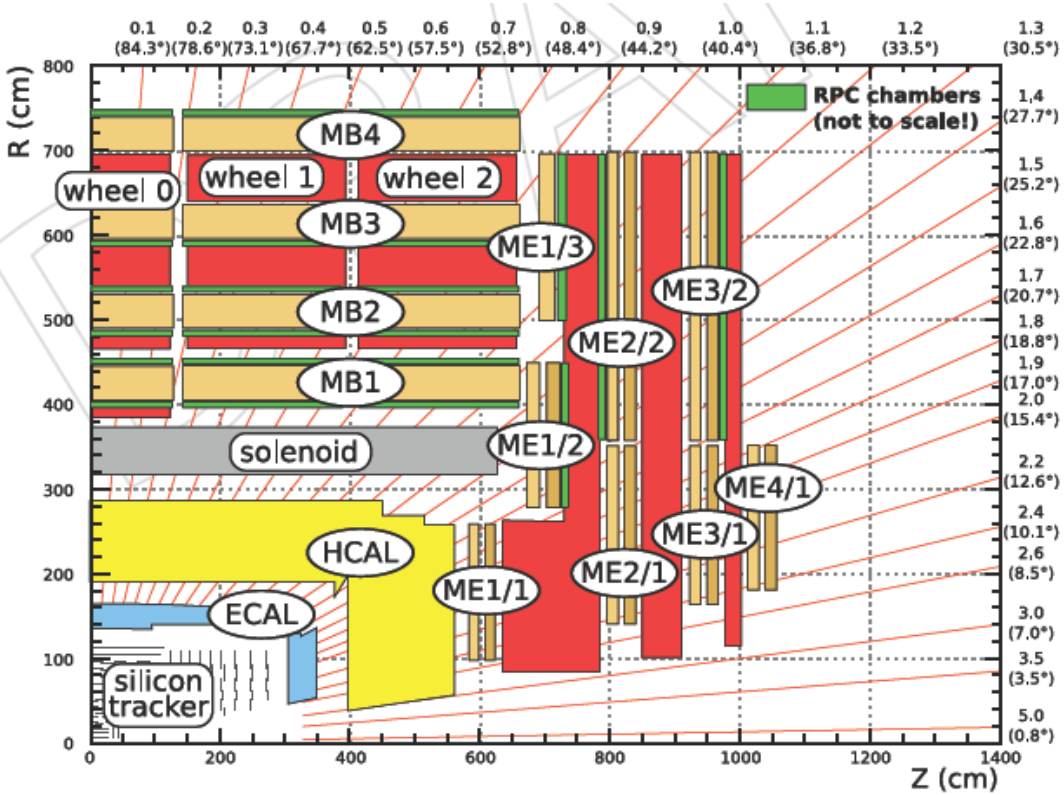
ME1/1 Cathode Strip Chambers



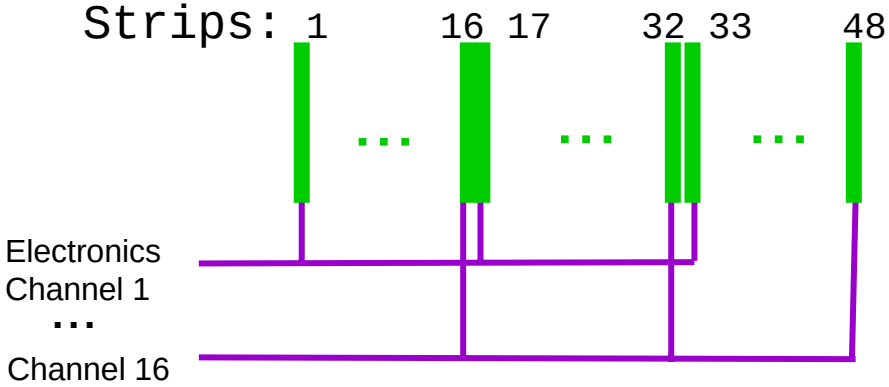
- 72 innermost chambers
- Built by JINR group (Dubna)
- Reside inside the solenoid

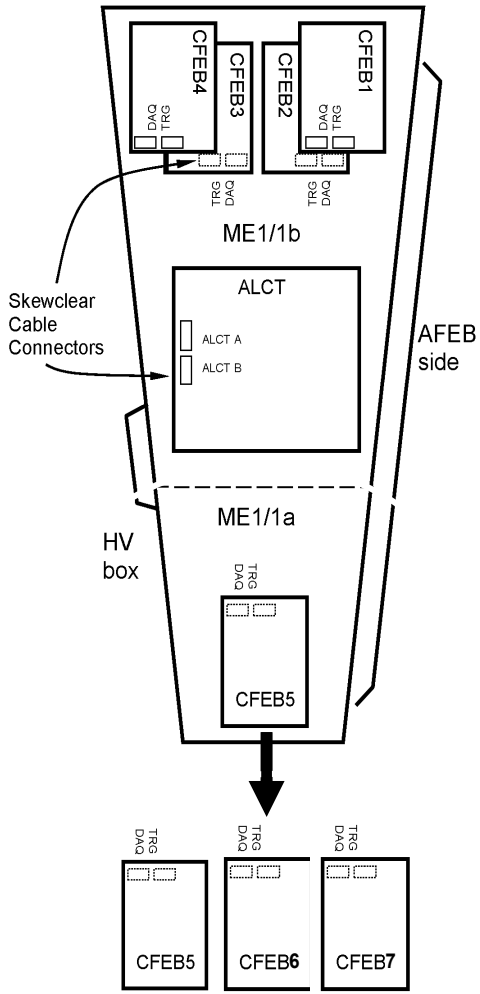
ME1/1 Cathode Strip Chambers are divided into two halves:

- ME1/1a (inner) with 48 strips, covering region $2.1 < |\eta| < 2.4$

- ME1/1b (outer) with 64 strips, covering region $1.6 < |\eta| < 2.1$

Strip Ganging in ME1/1a





48 strips of ME1/1a are ganged 3:1 into 16 readout channels:

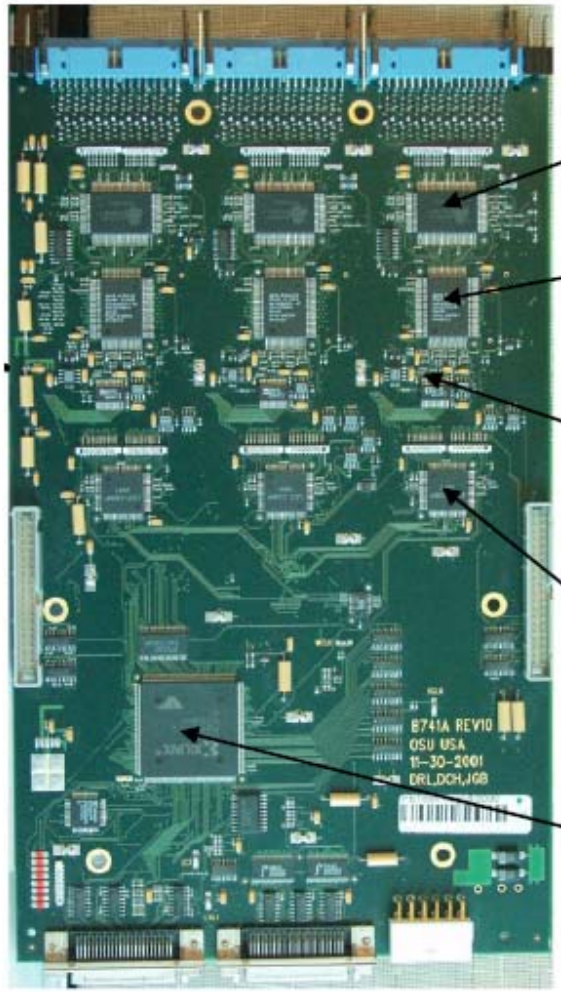
1+17+33 strips into the 1st channel

2+18+34 strips into the 2nd channel etc

This feature leads to triple ambiguity (ghost segments) and compromises trigger efficiency at high rates

Solution: use of 3 CFEB boards instead of one for ME1/1a

Present Cathode Front-End Board



BUCKEYE (ASIC) - amplifies and shapes input pulse

SCA (ASIC) - analog storage for 20 MHz sampled input pulse

ADC - events with LVL1ACC digitized and sent to DAQ Motherboard (25 nsec/word)

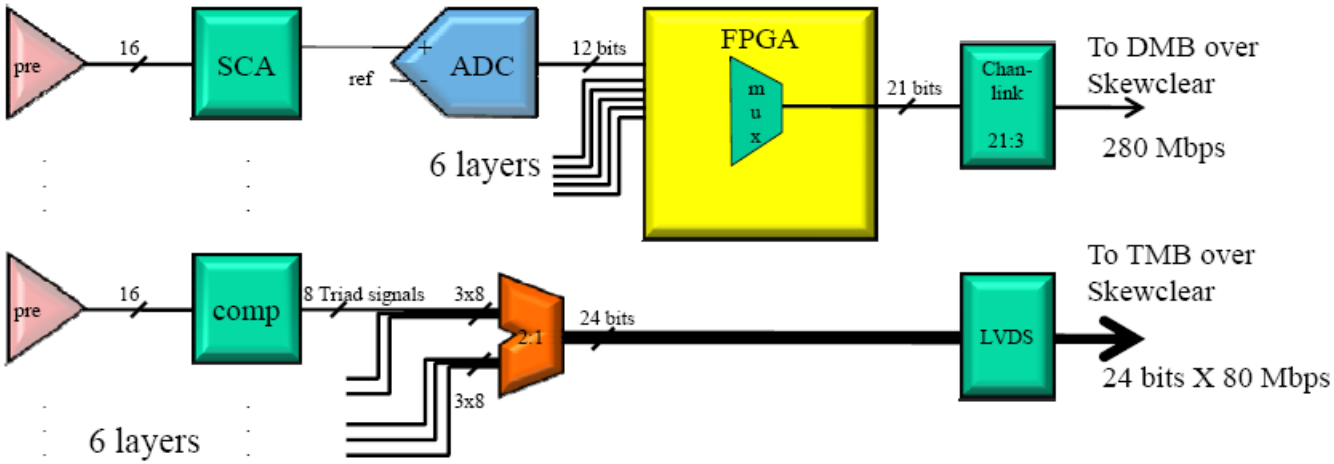
Comparator ASIC - generates trigger hit primitives from shaped pulse

Controller FPGA - controls SCA storage and digitization

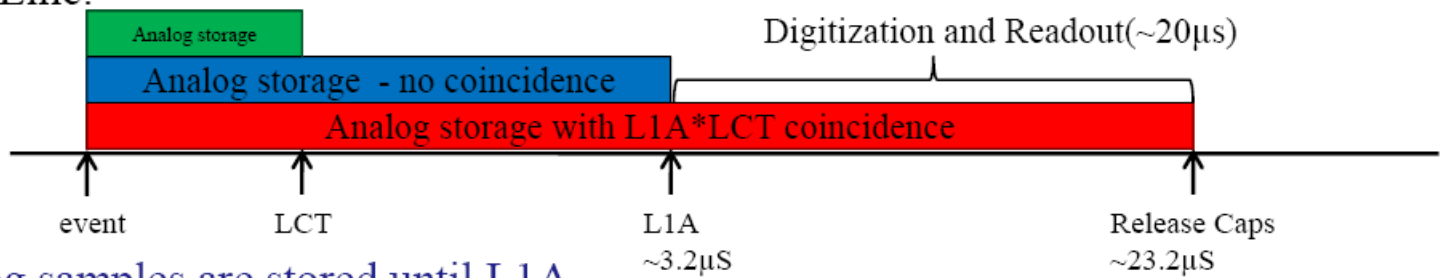
- 4..5 CFEBs per chamber
- 6 planes x 16 strips = 96 strips per CFEB
- 96 switch capacitors per channel, or 96 x 50 ns = 4.8 us

Present CFEB

Basic Block Diagram:



Time Line:



Analog samples are stored until L1A.
Then ADC must digitize 8X16 samples one at a time.
Limited number of capacitors and single channel ADC impose constraints on LCT and L1A latencies.

(B. Bylsma)

CFEB Limitations

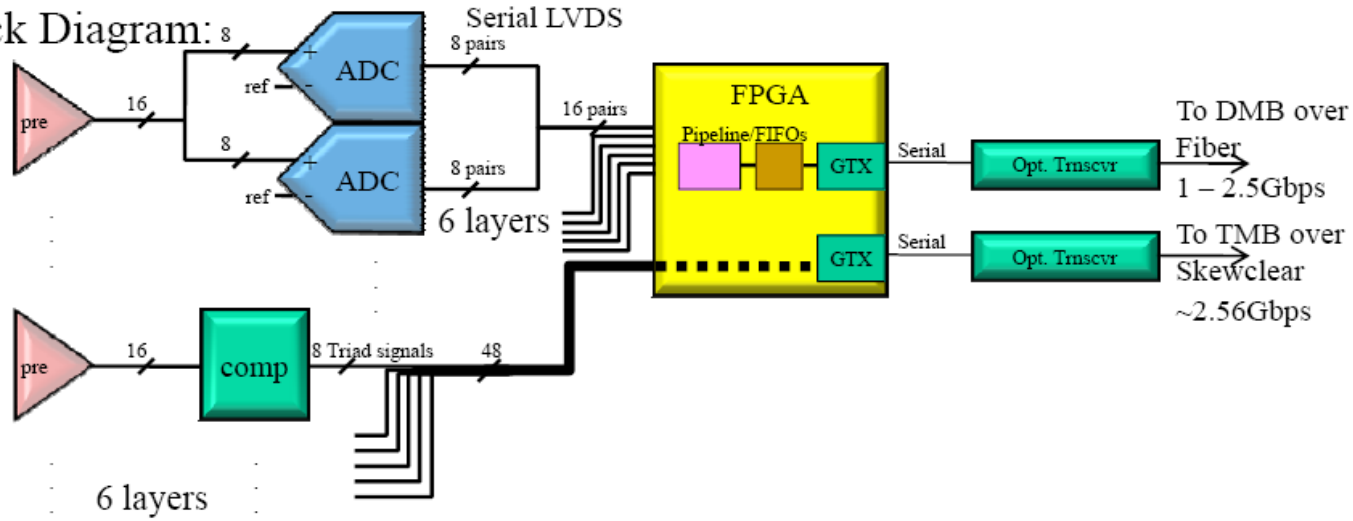
- Estimated LCT rate for ME1/1 chambers at 10^{34} $cm^{-2}s^{-1}$ luminosity is ~70 kHz and, assuming linear rate increase, may reach 700 kHz at SLHC
- Probability of Switch Capacitor Array (SCA) buffer saturation at 700 kHz is estimated to be ~9%

Solution:

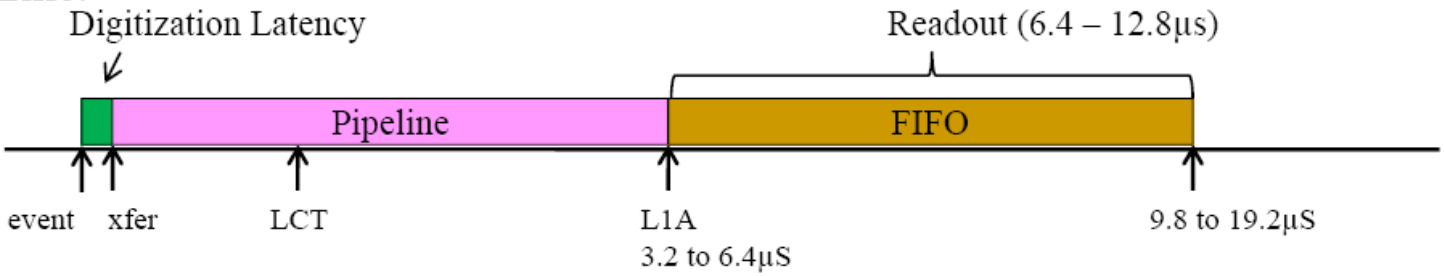
Replace the current "analog" CFEB with SCA and 16:1 multiplexing ADC by "digital" design with flash ADC for each channel and digital pipeline storage

New DCFEB

Basic Block Diagram:



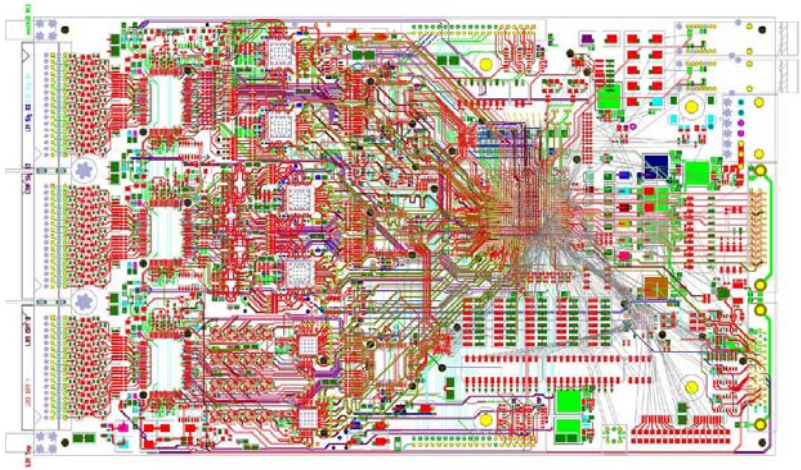
Time Line:

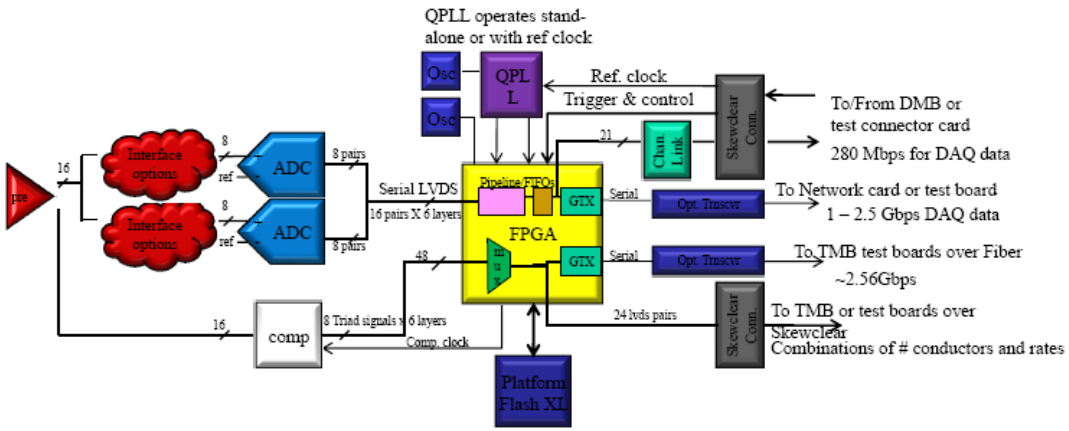


No Dead Time.
All 96 channels continuously digitized (no multiplexing),
Stored and read out on L1A

(B. Bylsma)

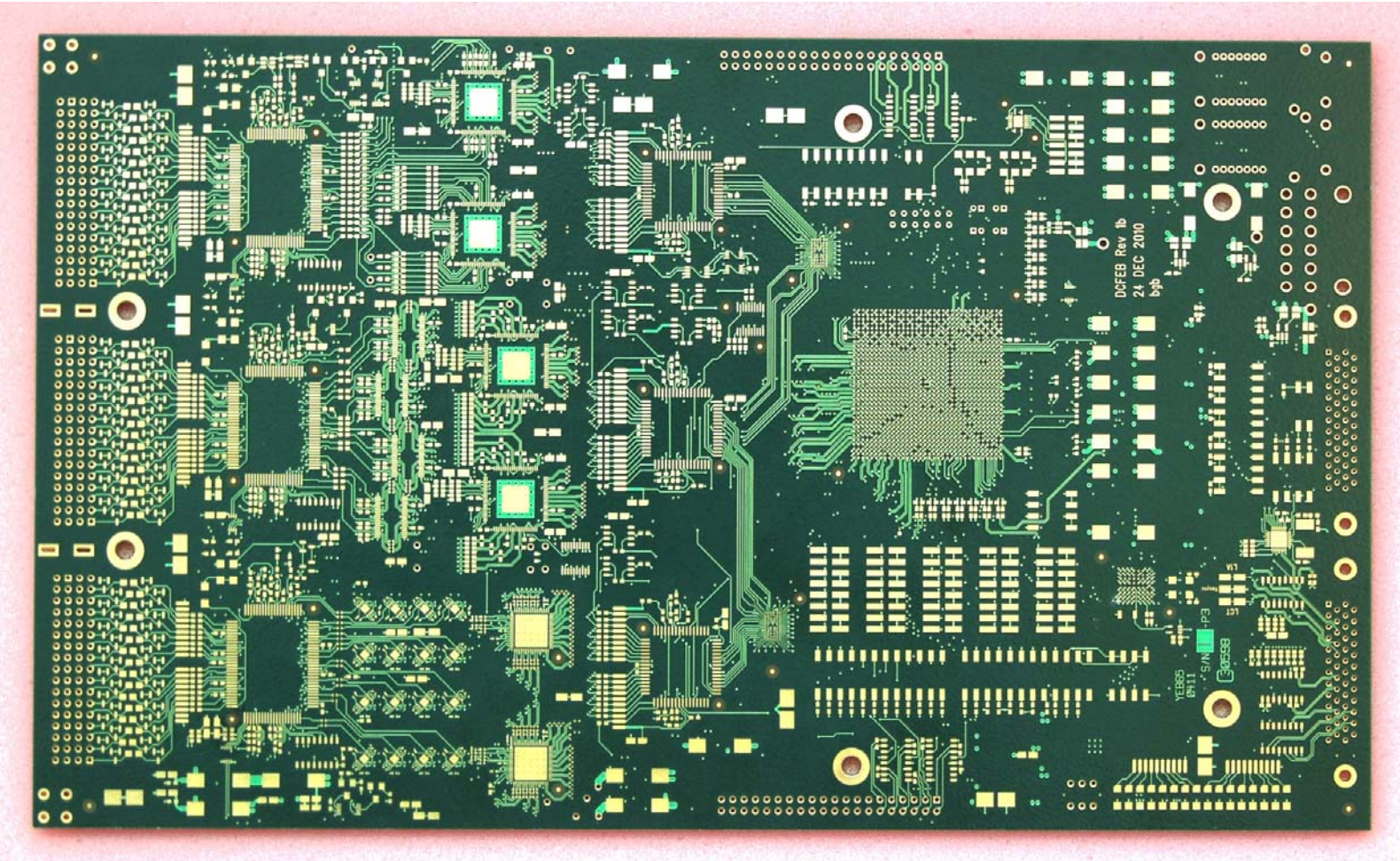
DCFEB Prototype





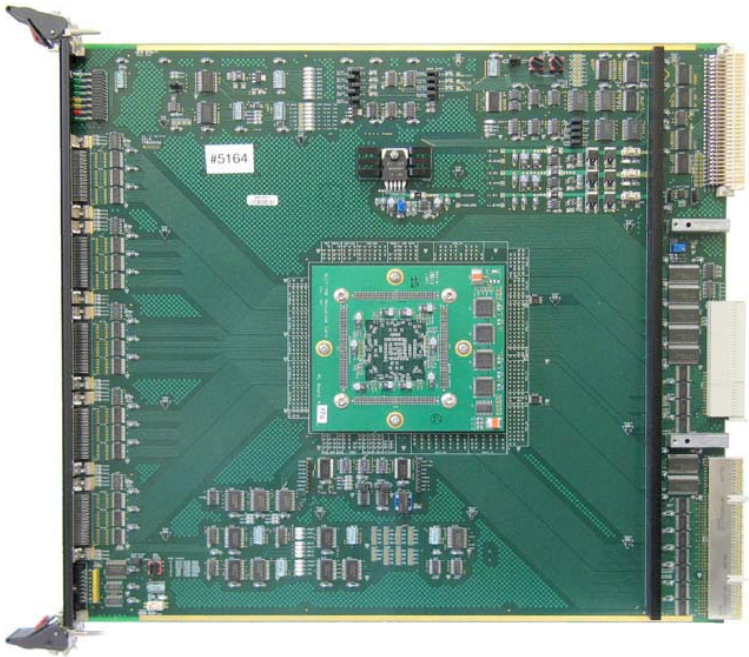
- Same size as old CFEB board
- Same input connections and 6 BUCKEYE amplifier-shaper ASICs
- 12 Texas Instruments ADS5281 ADC (8-channel, 12-bit, 50 MSPS, serial LVDS output)
- 4 options for preamp/ADC interface to evaluate
- 2 legacy skewclear connectors compatible with old TMB and DMB
- 3.2Gbps optical links to new TMB and new DMB
- Xilinx XC6VLX130T-FFG1156 FPGA (~$1,200)
- 20-layer PCB

DCFEB Status



- Two boards are being assembled, expected delivery in mid March

Trigger Motherboard

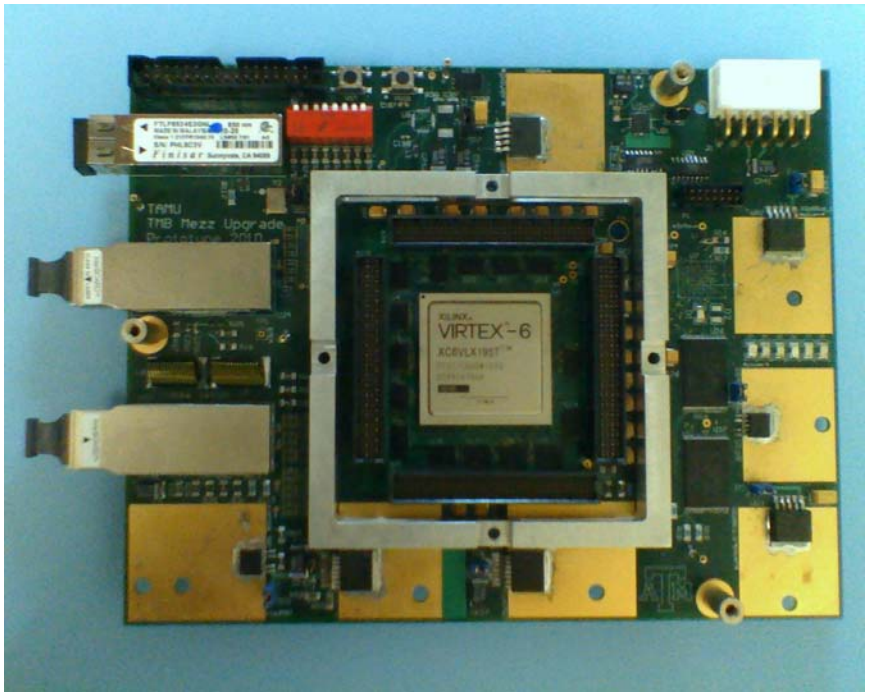


- Reconstructs the cathode trigger stubs (CLCT) and matches them with the anode ones (ALCT)
- Transmits up to two combined LCT to the Muon Port Card via the custom backplane
- Production TMB2005 is based on Xilinx XC2V4000 FPGA which is almost full; no room for further improvement

- Need to implement more complex algorithms to increase trigger stub finding efficiency for high eta $2.1 < |\eta| < 2.4$ with unganged ME1/1a
- Compatibility with seven new DCFEBs which provide comparator outputs for the CLCT processor

Solution: Replace the FPGA mezzanine

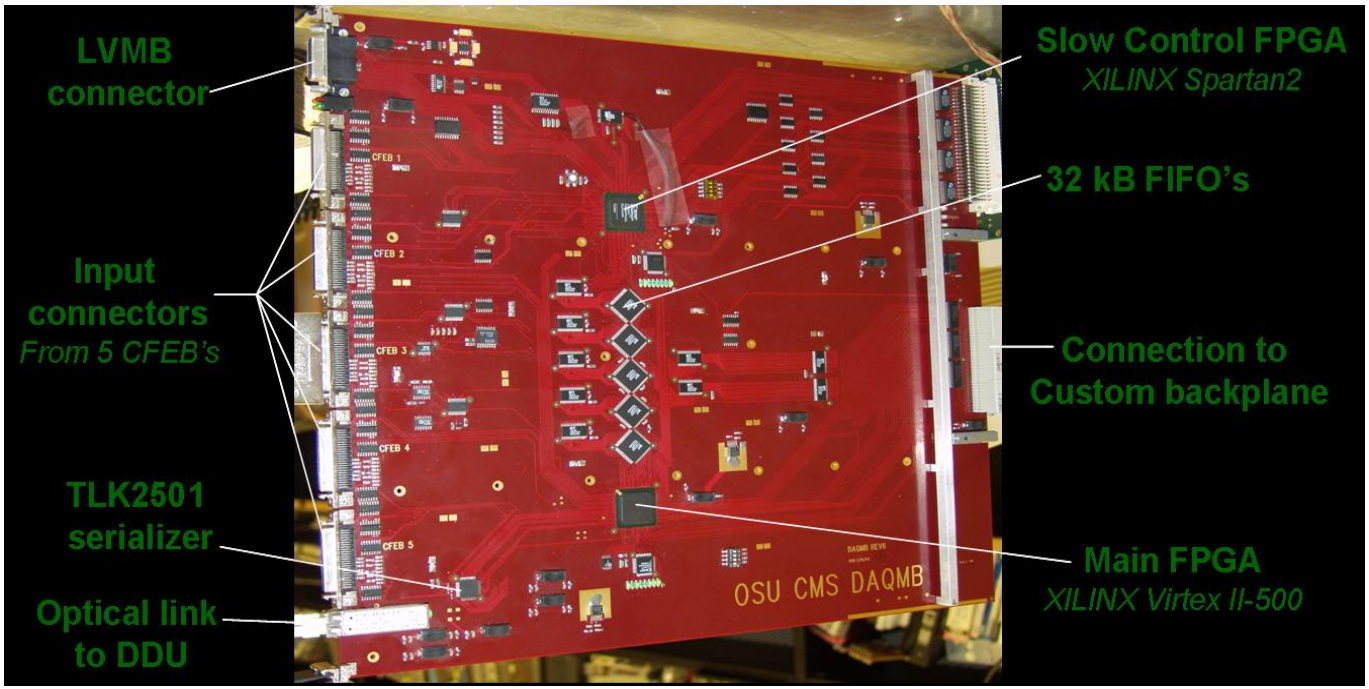
TMB Mezzanine Status



- XC6LVX195T-2FFG1156 (x5 more room than the XC2V4000)
- XCF128X and two XCF32 PROMs
- SNAP12 transmitter and receiver
  - 7 receivers for DCFEB optical links
  - embedded MGT links
- SFP optical transceiver

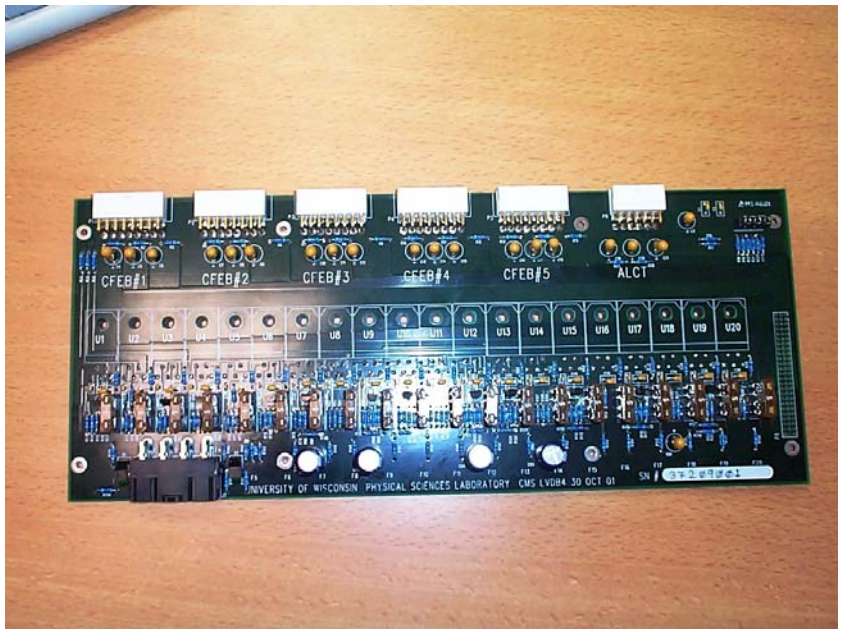
- Two mezzanine boards have been assembled in January
- Successfully passed initial tests (power, FPGA/PROM, optical links)
- UCLA group has been working on the current TMB firmware project targeted to new Virtex-6 FPGA

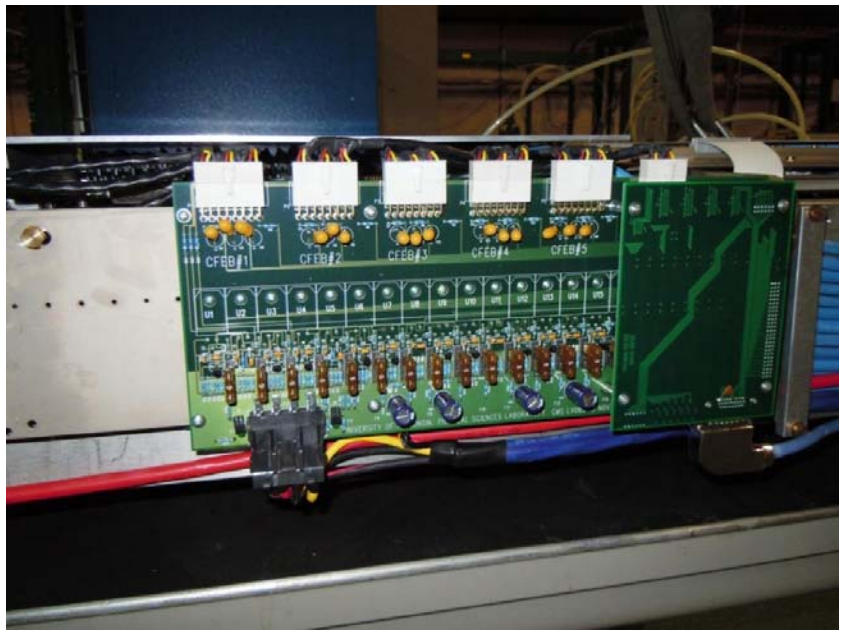
DAQ Motherboard



- Replace 5 copper cables to CFEB with 7 optical links to DCFEB
- Developing radiation tolerant FF-EMU ASIC (IBM CMOS 130 nm) for the integrated distribution of TTC signals and for the data readout
- Implement all FIFO buffers inside the Virtex-6 FPGA
- Custom backplane connections remain unchanged

LVDB and LVMB boards





- LVDB board distributes LV power to on-chamber electronics
- LVMB mezzanine monitors voltages and currents and transmits them to the DMB
- Both boards need to be redesigned for the ME1/1 upgrade (7 DCFEBs, additional temperature sensors)
- Dubna group took responsibility for the LVDB

Scope and Responsibilities

- DCFEB: 72 chambers x 7 boards = 504 boards (OSU)
  504 liberated CFEB boards will be used to populate 72 new ME4/2 chambers (under construction)
- DMB: 72 new boards 9Ux400 mm (UCSB, Northeastern University)
- TMB: 72 new FPGA mezzanines (Texas A&M University)
  UCLA provides the initial firmware for Virtex-6
  Minor mechanical modification to TMB front panel
- LVDB: 72 new boards (JINR Dubna, NCPHEP Minsk)
- LVMB: 72 new mezzanines
- Mechanical integration: JINR
- Engineering coordination: Rice University

Conclusion and Plans

- 1st prototype of the TMB mezzanine has been built; tests in progress
  - production board will be simpler
- 1st prototype of the DCFEB will be assembled in mid March
  - Expect to make a component choice and proceed to preproduction prototype in summer 2011
  - Preproduction prototype will be simpler and cheaper
- DMB schematic is expected to be ready in summer and first prototype in the fall of 2011
- LVDB schematic design in progress, the prototype is expected by summer 2011
- Irradiation tests: TAMU cyclotron, April-May 2011
- Integration tests electronics + chamber : start late 2011 at CERN (b.904)
- Production prototypes: 1st half of 2012
- Mass production and testing: fall 2012 – early 2013
- Ready for installation at CMS: by summer 2013

Backup Slides

ME1/1 Effective SCA Buffer Occupancy at SLHC (Stan Durkin, OSU)

- **At SLHC: use same L1 accept rate assuming rates go up linearly. Maximum LCT rate is 700 kHz (ME1/1),**
- **L1-LCT match rate is 5.25 kHz.**
- **Average number of LCTs during 5.2 ms (=6ms-0.8ms) holding time for 2-blocks: h=5.2x10-6x700x103=3.64**
- **Average number of L1-LCT matches during 26 ms digitization time: r=26x10-6x5.25x103=0.1365**
- **Probability of overuse of SCA:** 0.09 !!!!!! !!!

n	Free	Used	P(η,n)	Q(ρ,n)
0	12	0	0.026	0.86
1	10	2	0.095	0.12
2	8	4	0.174	1.60E-02
3	6	6	0.211	2.10E-03
4	4	8	0.192	3.00E-04
5	2	10	1.40E-01	4.10E-05
6	0	12	8.50E-02	5.60E-06

Backup Slides

FF-LYNX Protocol (Guido Magazzu, INFN/UCSB)

FF-LYNX: protocol and interfaces for the control and readout of future Silicon detectors

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- **Two separate Time Division Multiplexed (TDM) channels for triggers, frame headers and synchronization patterns (THS channel) and frame payload (FRM channel)**
- **Three speed options: 160Mbps, 320Mbps, 640Mbps**