CHIP TO WAFER ASSEMBLY AND THIN CHIP BUMP BONDING – TECHNOLOGIES FOR FUTURE DETECTOR UPGRADES

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Outline

CHIP TO WAFER ASSEMBLY AND THIN CHIP BUMP BONDING – TECHNOLOGIES FOR FUTURE DETECTOR UPGRADES

- Hybridization Technologies
- Chip to Wafer Assembly for Hybrid Pixel Module Fabrication
- Thin Readout Chip Flip Chip Assembly
- Summary and Outlook

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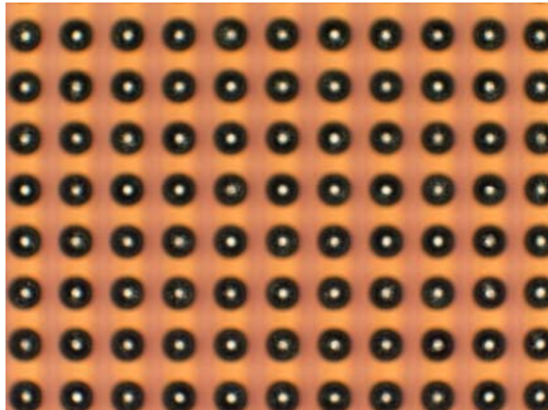
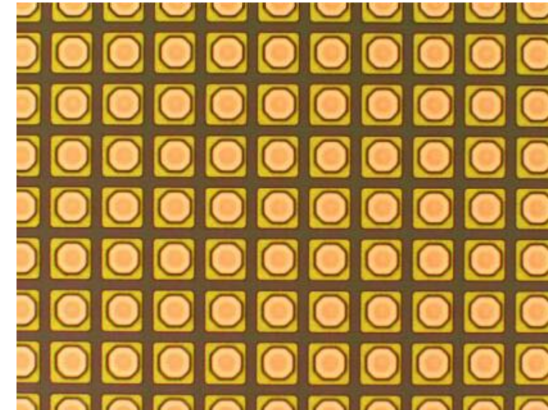
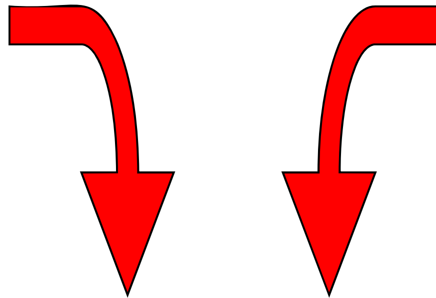
Hybridization Technology

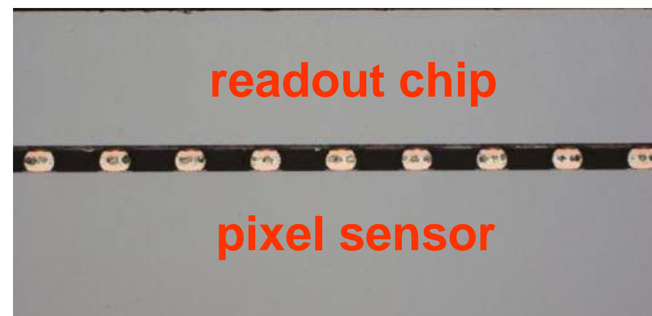
Solder bumping on readout chip



Solderable UBM pads on sensor pixel







Flip chip interconnection

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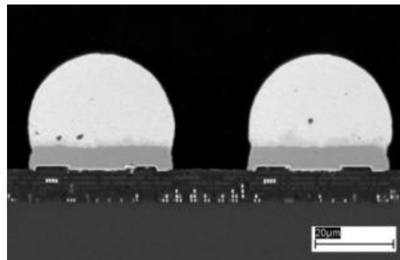
Hybridization Technology

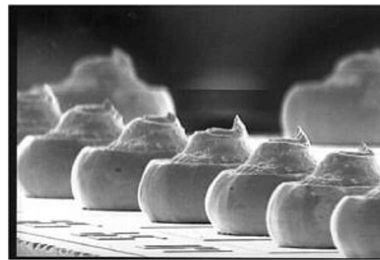
Bump and UBM Deposition Technologies

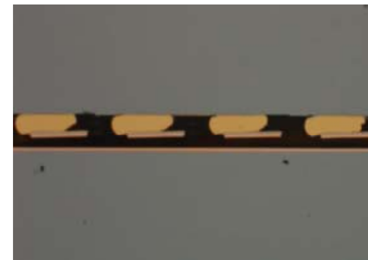
- Electroplating/electroless
- Evaporation
- Solder paste printing
- Solder transfer
- Stud bumping

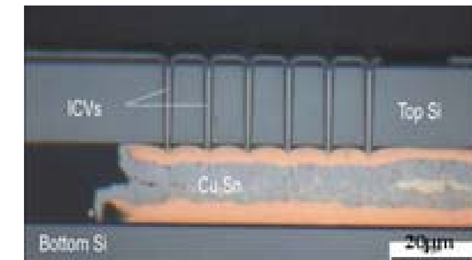
Flip Chip Assembly Technologies

- Solder bump bonding
- Thermo-compression bonding
- IMC bonding
- Conductive adhesive bonding
- Metal-Metal Direct Bonding









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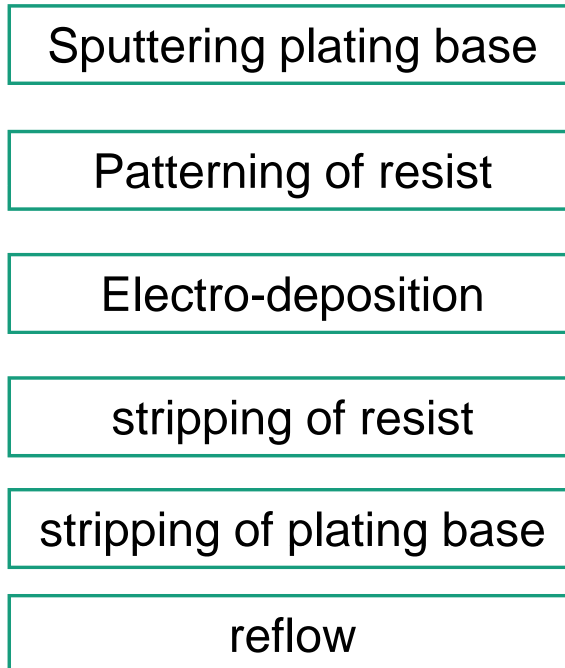
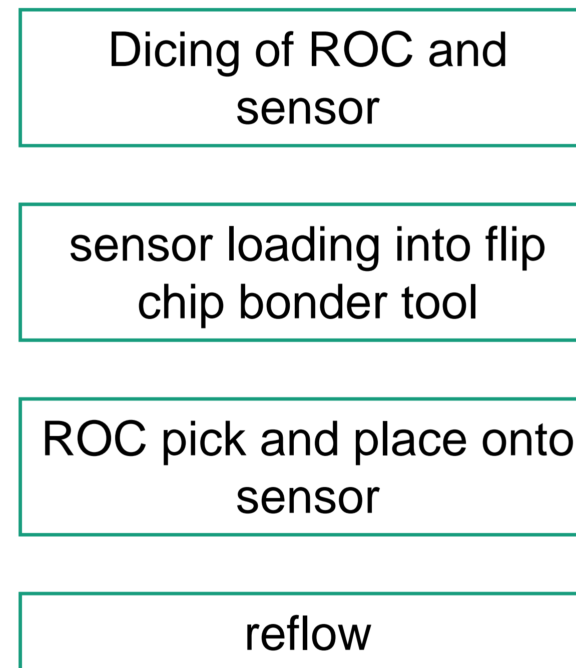
Chip to Chip Assembly





Bump bonding of only one sensor tile per step

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Chip to Wafer Assembly for Hybrid Pixel Modules

Basic Approach:

Placement and assembly of multiple readout chips onto one sensor wafer

Benefit:

- Chip to wafer assembly → less alignment steps
- Less manual handling steps
- Faster bonding tools / less bonding time per module
- Simultanious reflow of all modules per wafer

→ Chip to wafer bump bonding evaluation batch

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Chip To Wafer Flip Chip Assembly

Karl Suss FC150

- accuracy: ± 1 µm at 3 σ
- cycle time: 1-2 min. per die
- maximum die size: 2” x 2”
- maximum substrate size: 6” x 6”
- heating profiles from top and bottom possible
- minimum alignment mark size: 20 µm

Panasonic FCB3

- accuracy: 3 µm at 3 σ
- full automatic FC bonder with feeder unit
- cycle time: 2 s minimum
- maximum substrate size: 300 mm wafer
- TC and TS bonding head

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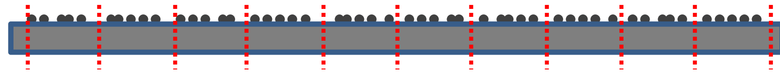
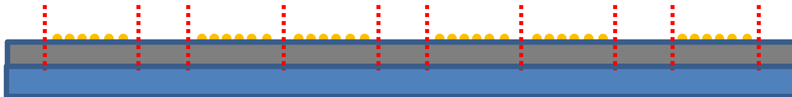
Chip to Wafer Assembly – Process Flow



- SnAg bump deposition on Readout Chipwafer

- UBM pad metal deposition sensor wafer

- mounting of the sensor wafer onto support wafer



- Sensor wafer dicing

- ROC flip chip assembly at wafer level

- Module release from support wafer

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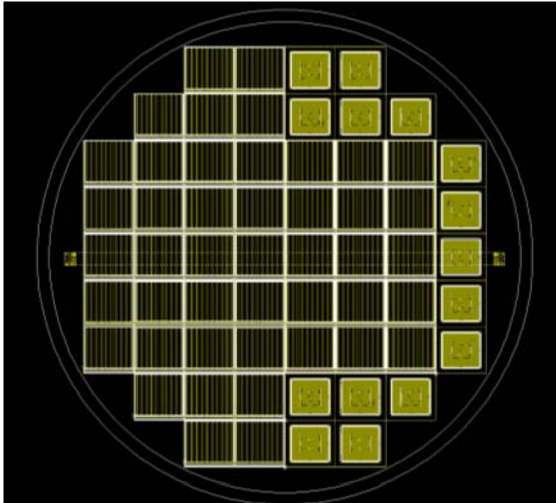
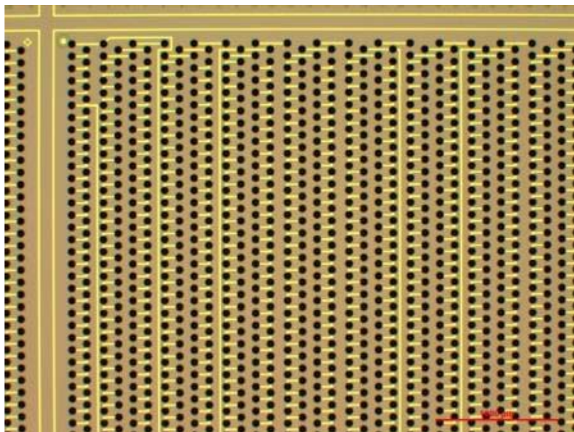
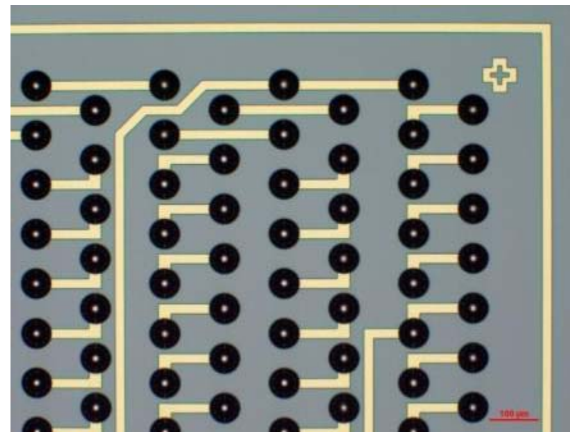
C2W Flip Chip Assembly

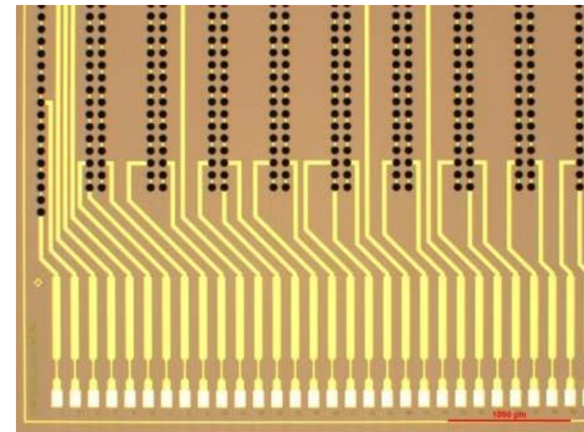
200mm Daisy Chain Wafer – ATLAS FE-I4 size Chips



- FE-I4 size daisy chain test chips, thickness 180µm
- bump size 25µm, 60µm
- bump pitch 50µm, 100µm, stackered







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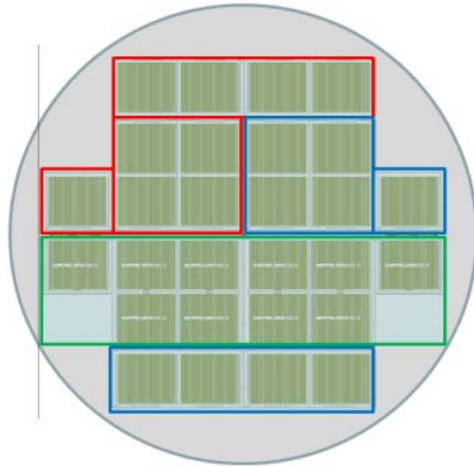
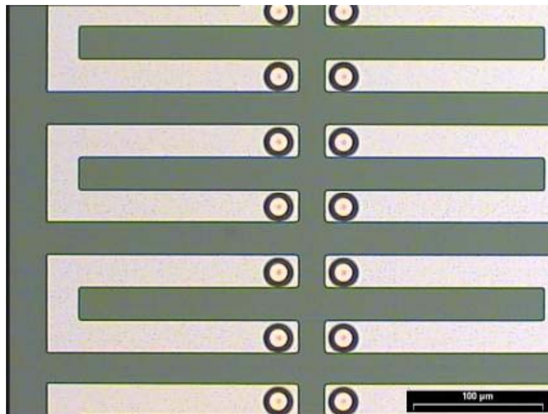
C2W Flip Chip Assembly

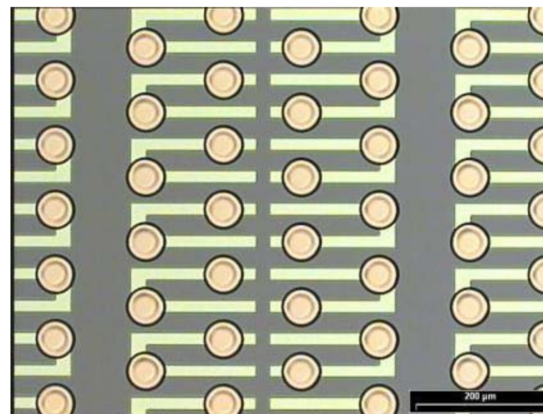
150mm Sensor Daisy Chain Wafer



- Double-Chip Tiles, Single-Chip Tiles
- Quad-Chip Tiles
- Pad size 25µm, 60µm
- Pad pitch 50µm, 100µm, stackered

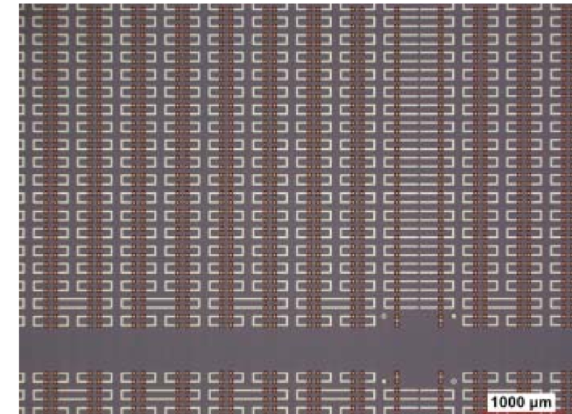


Pad size 20µm, pitch 50µm



Pad size 60µm,

pitch 100µm, stackered



Pad size 60µm, pitch 100µm

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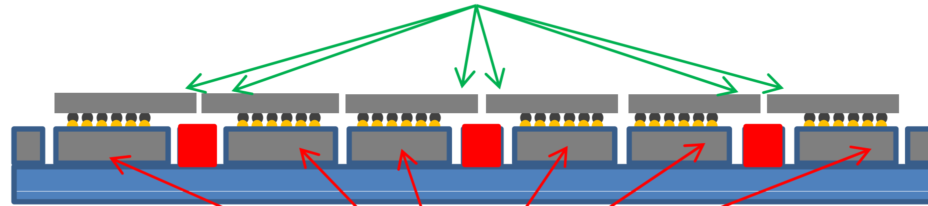
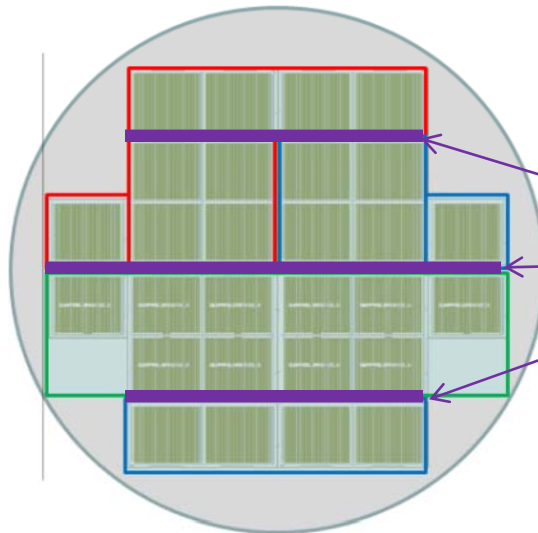
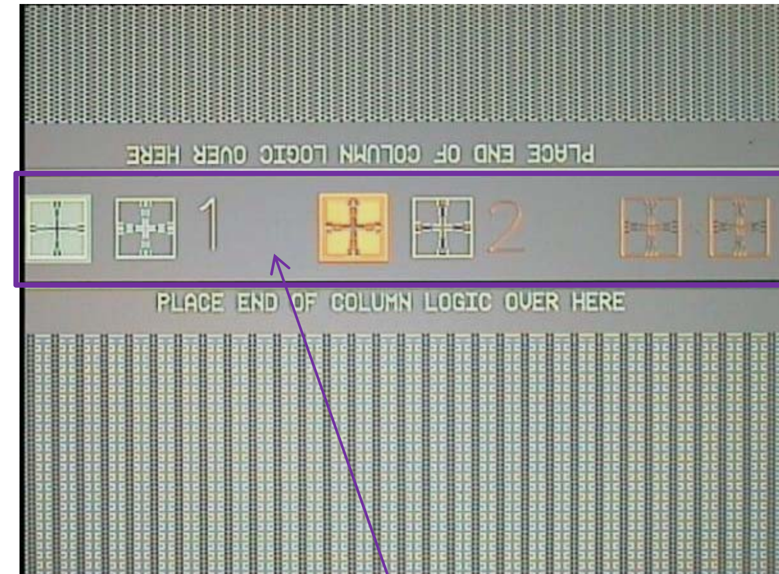
Sensor Wafer Design – Requirements for ROC Assembly

ROC with overhanging
wire bond pad chip edge



sensor





End of column logic overlap area

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C2W Flip Chip Assembly

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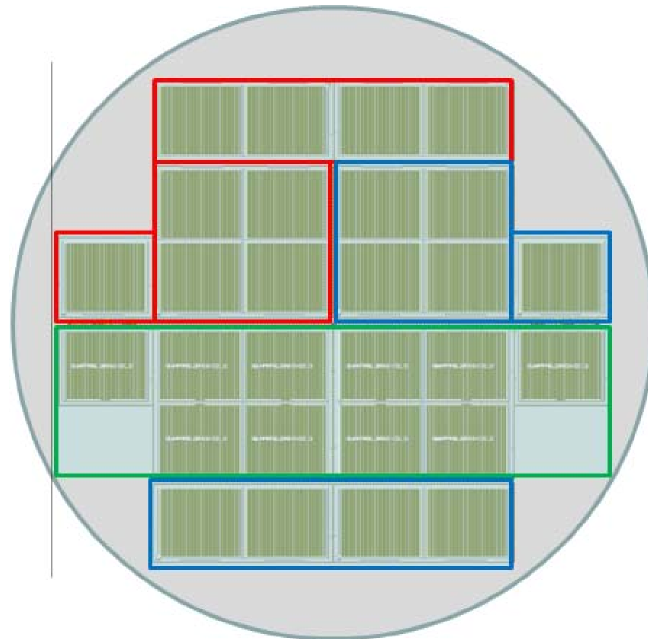
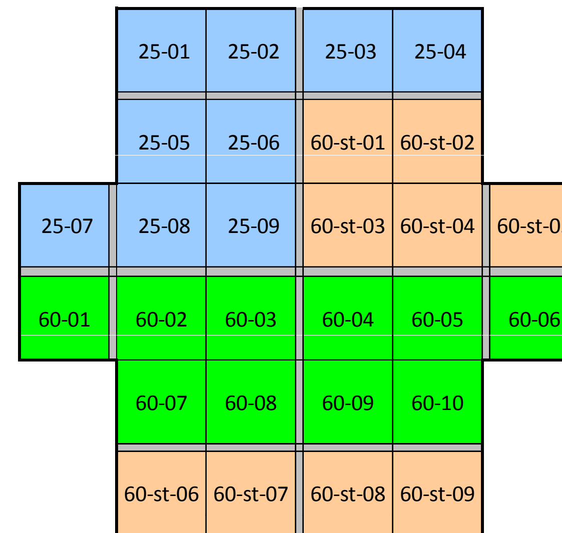
technische universität dortmund

Assembly positions on sensor wafer





25µm bump size, 50µm pitch

60µm bump size, 100µm pitch

60µm bump size, 100µm pitch, staggered

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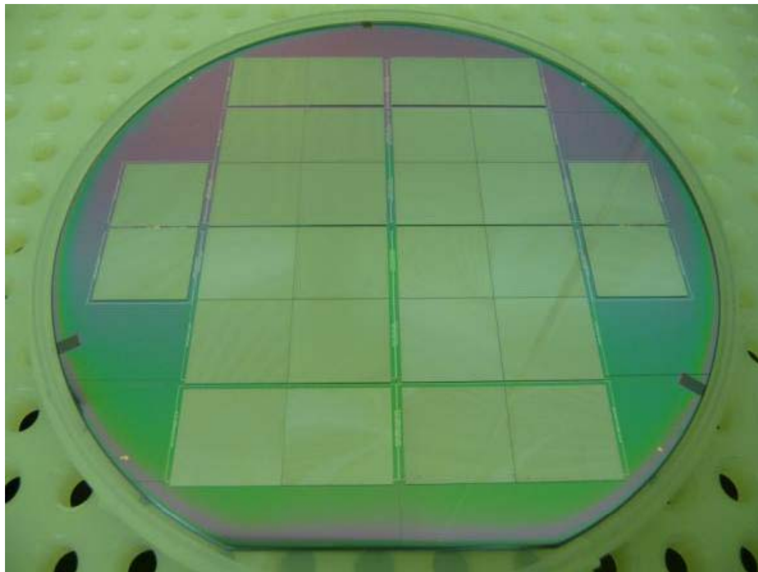
C2W Flip Chip Assembly – Preliminary Results



Sensor wafer processed and diced on support wafer

5 wafers assembled:

20x Quad-Chipmodules
20x Double-Chip modules
20x Single-Chip modules
140 chips assembled

Quality check by IR- and x-ray microscopy:

- 5 chips failed because of tilt failure (3,7%)

Splitted to bump size:

- 4 x 25µm bump size
- 1 x 60µm bump size

Splitted to wafer:

- 4 x wafer 1
- 1 x wafer 2
- 0 x wafer 3, 4, 5

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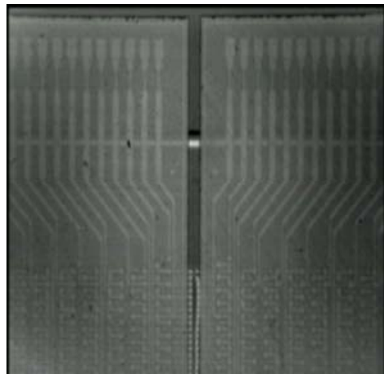
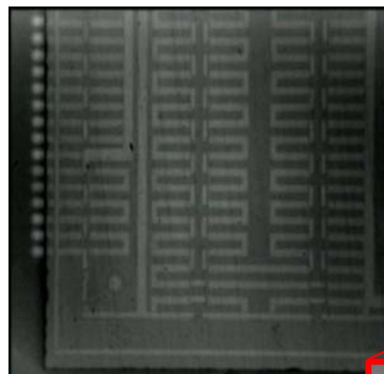
C2W Flip Chip Assembly – Qualification Phase

Transmission microscopy

Infrared microscopy

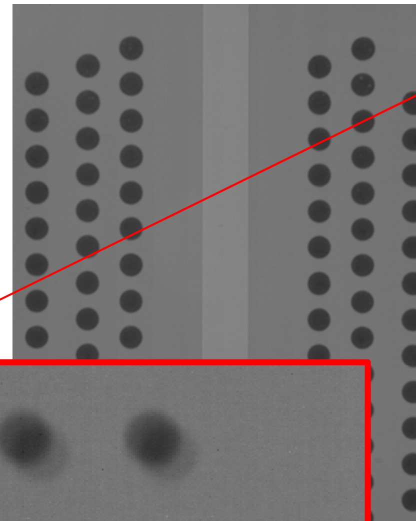


Infrared images 25µm bumped chips



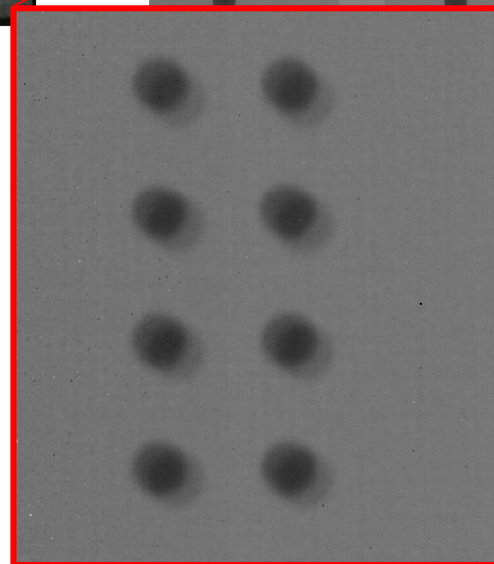
Infrared images 60µm bumped chips

X-ray microscopy



µm

gn)



X-ray images 25µm bumped chips (slightly tilted chip left)

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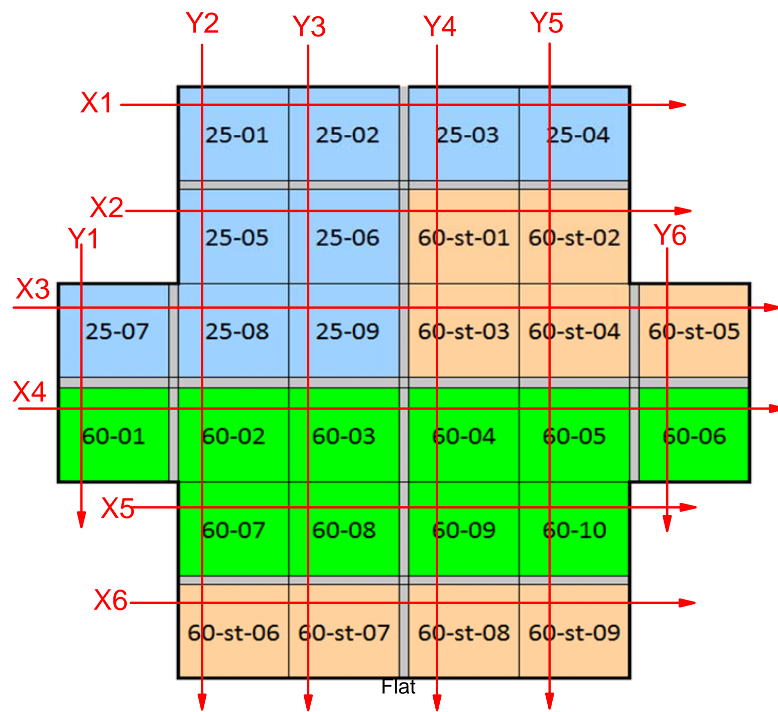
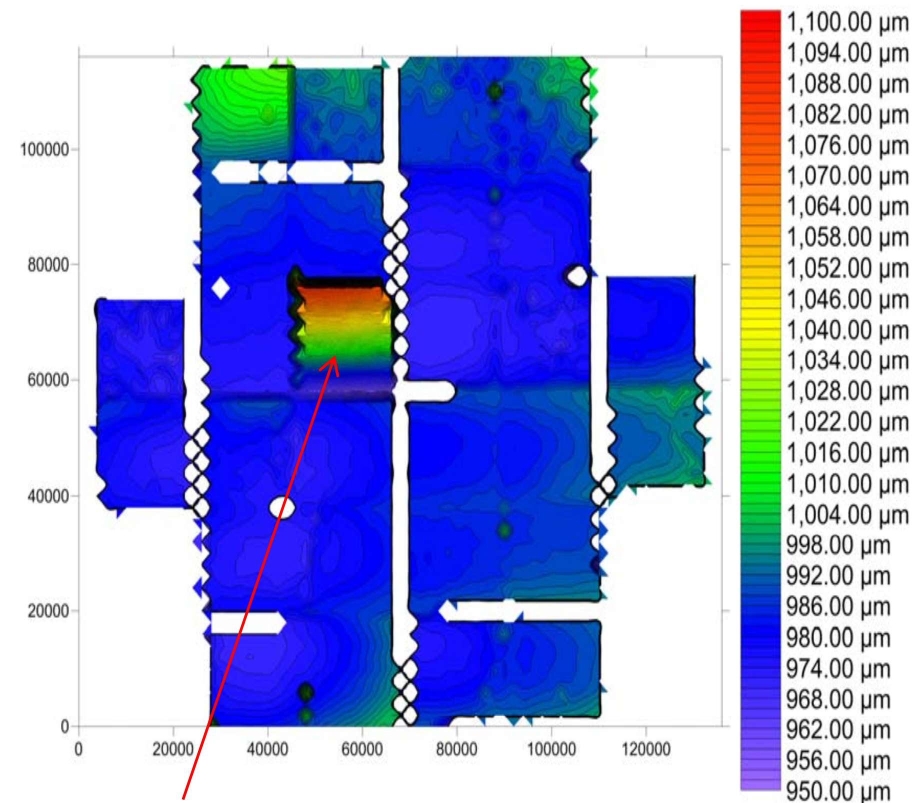
C2W Flip Chip Assembly – Qualification Phase

Laser Profiler Surface Scan

Line Scan Positions:



Area Scan Data:



Misplaced chip

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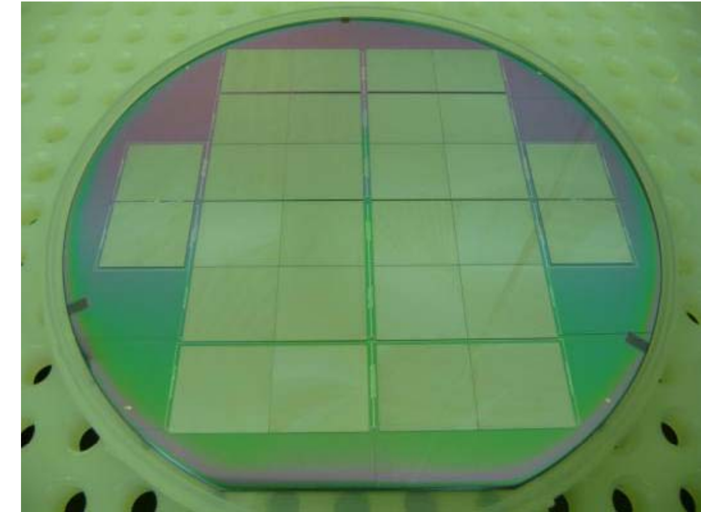
Chip To Wafer Flip Chip Assembly

Preliminary summary chip to wafer bump bonding evaluation:



- Assembly faster than individual chip assembly
  - 14 sec per chip instead of 1-2 min
- Sufficient assembly accuracy
- Daisy chain resistance measurements ongoing

Potential for optimization:

- Future designs using one bonding direction
- Automatization of module release
- Cleaning process after module release (wet chemical, plasma,…)

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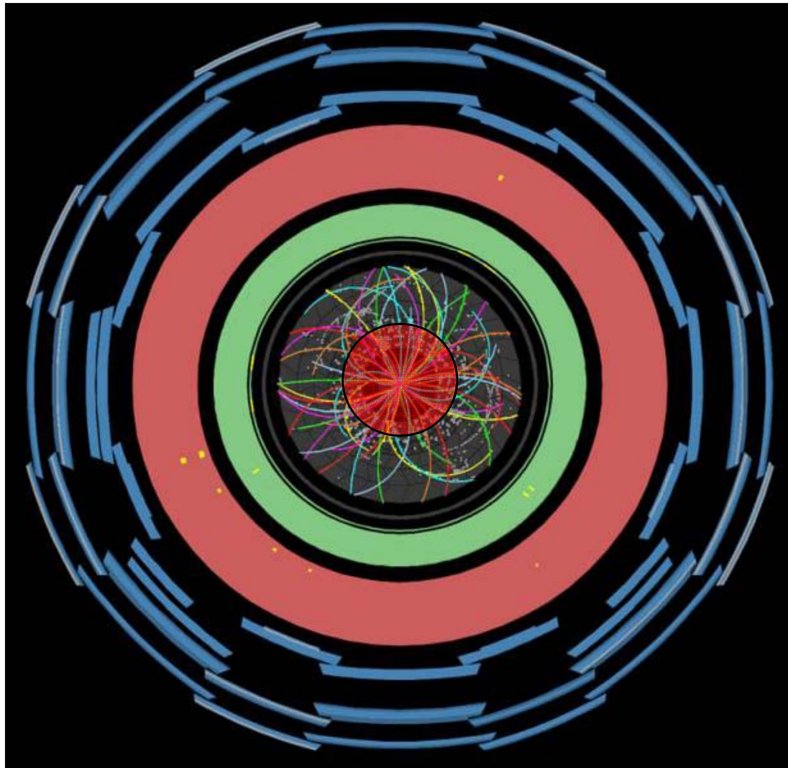
Readout Chip Thinning

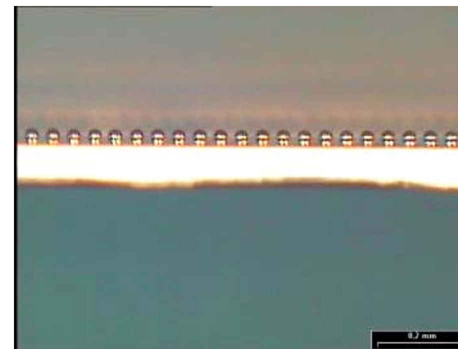
Motivation



Reduction of material budget of the innermost detector layers

	% X_0
Old BL @ R=5 cm	2.7
New BL @ R=3.2 cm	1.5

(F. Huegging, PIXEL 2010)



90µm thin ATLAS FE-I3 ROC

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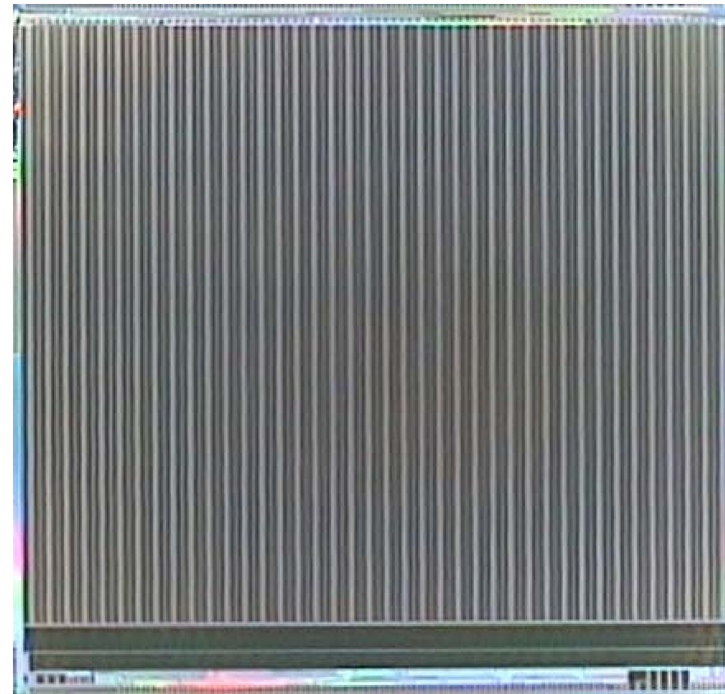
New Readout Chip Generation

Atlas FE-I3

Size: 7300 x 10900 µm²

Atlas FE-I4



Size: 20030 x 18962 µm²

active area FE-I4 = 4,8 * active area FE-I3

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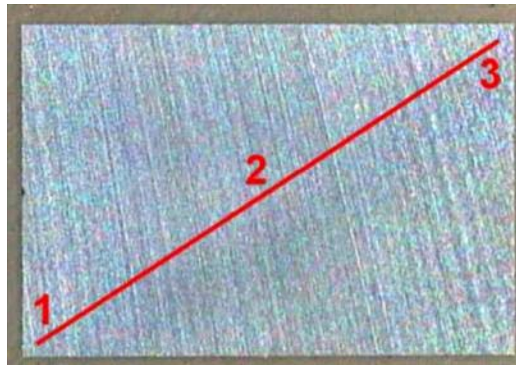
Readout Chip Thinning

Chip Bending at Reflowtemperature – ATLAS FE-I2/FE-I3

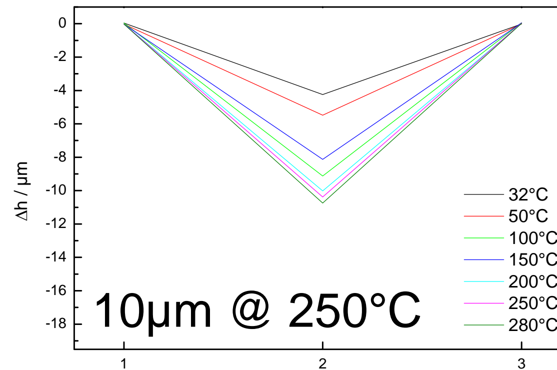


Chip bending measurement

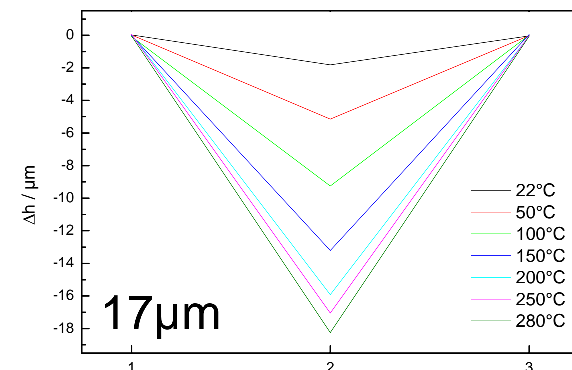
- at three points per chip
- at different temperatures

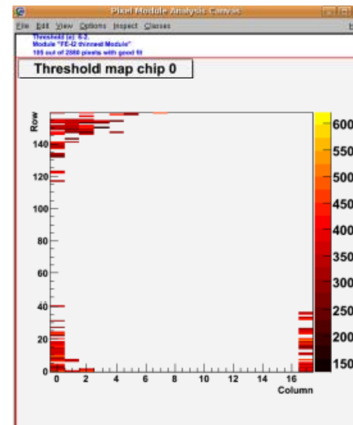
Si-thickness

180µm



130µm





Noisemap of ATLAS FE-I3 module:

Marked dots are pixels with no interconnection to the readout cell

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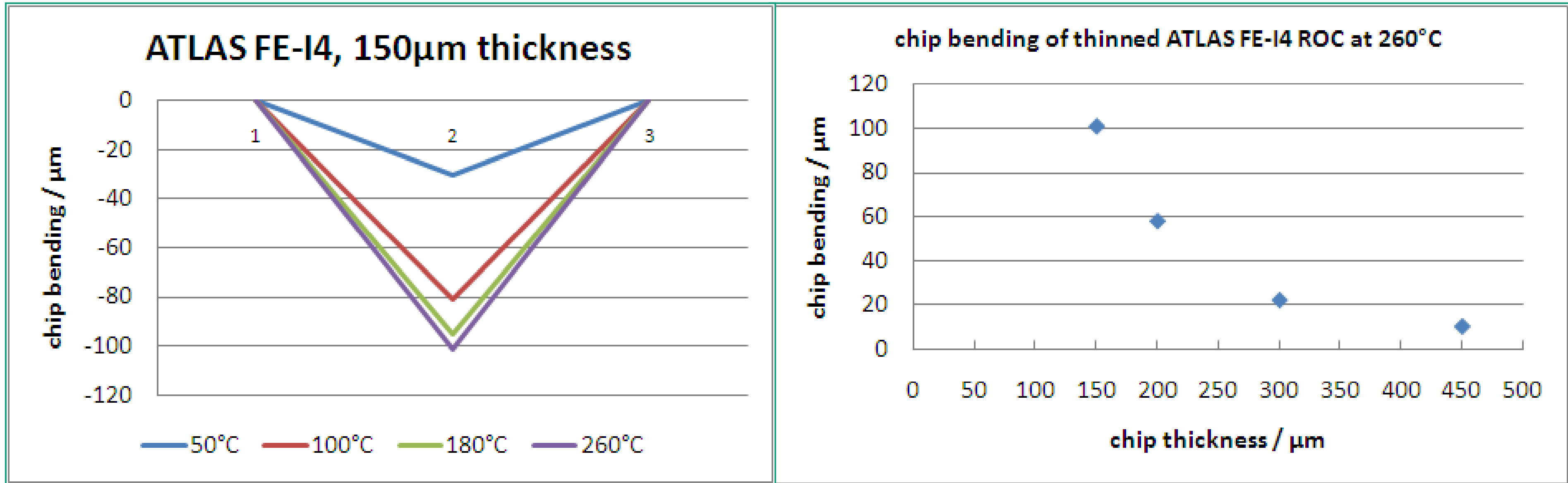
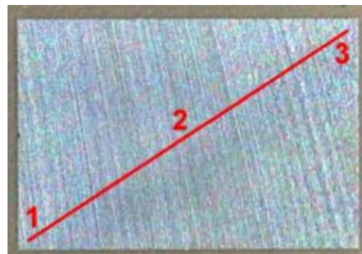
Thinned Readout Chip Flip Chip Assembly

Chip Bending – ATLAS FE-I4



100µm @ 260°C



Chip bending measured on FE-I4 ROCs
Single chips thinned to several thicknesses

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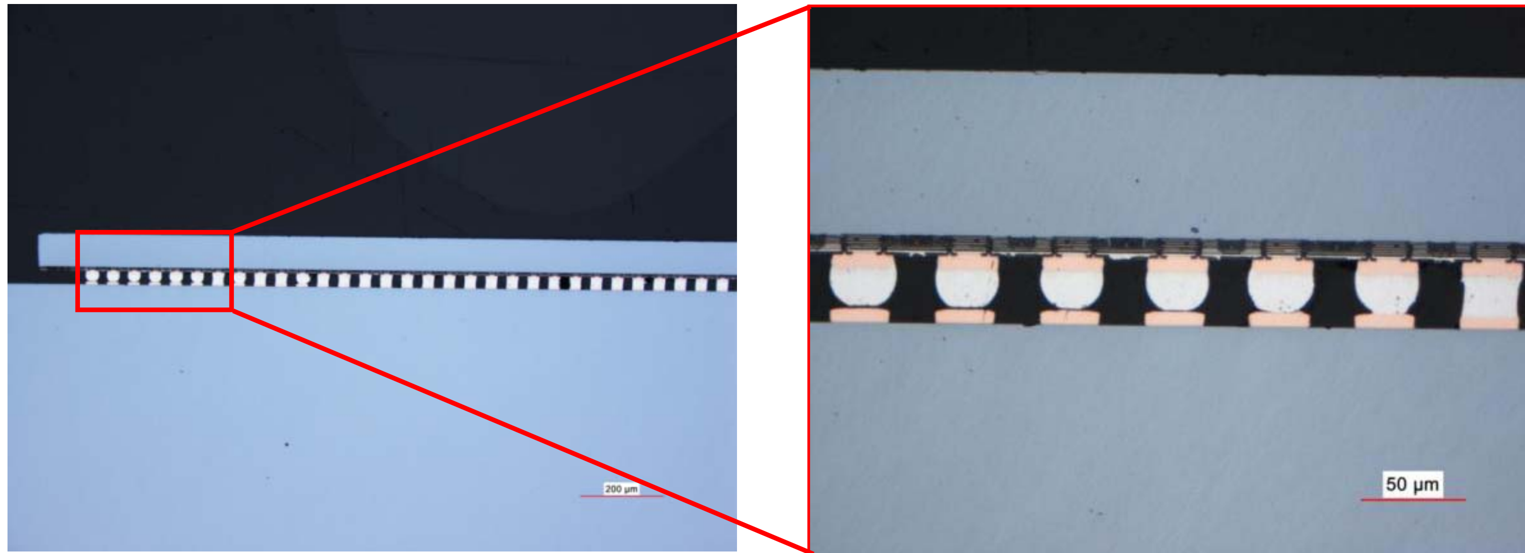
Thinned Readout Chip Flip Chip Assembly

Chip Bending at Reflow Temperature – Cross Section



Avoid chip bending during bonding process:

- Apply pressure during bonding → thermo-compression bonding process
- increase chip stiffness during bonding → temporary support carrier approach

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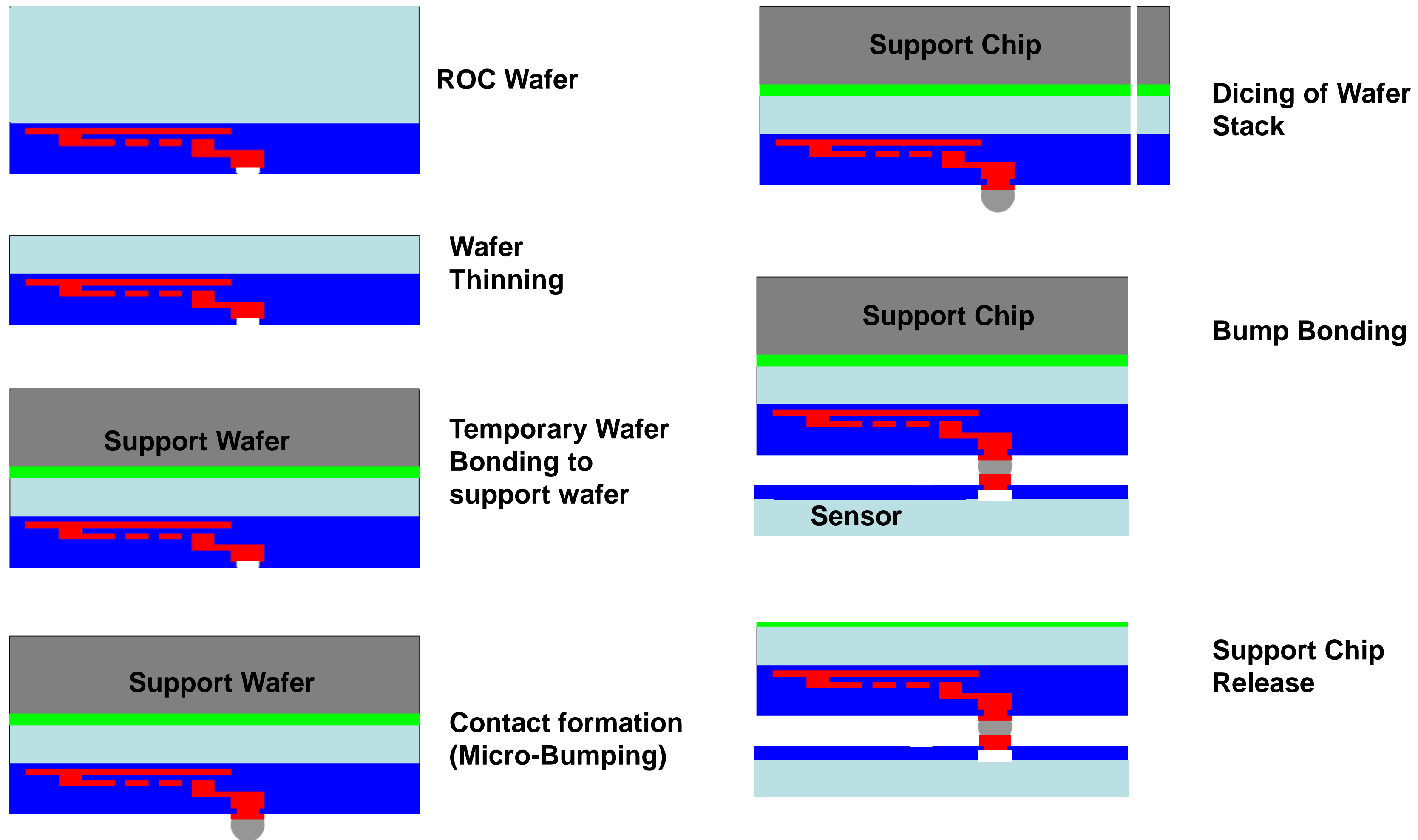
Thin Chip Assembly – Temporary Support Approach

Process Flow



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Thin Chip Assembly – Temporary Support Approach

Requirements for temporary bonding layer

- **Easy to apply on wafer level**

  (voidless bonding interface, good wetability of support wafer)
- **High thermal stability**

  (max temperature: sputtering 150°C, SnAg solder reflow at 260°C)
- **Easy to crack during debonding process**

  (thermal, chemical, optical)
- **Less or no residues on thinned silicon chip**

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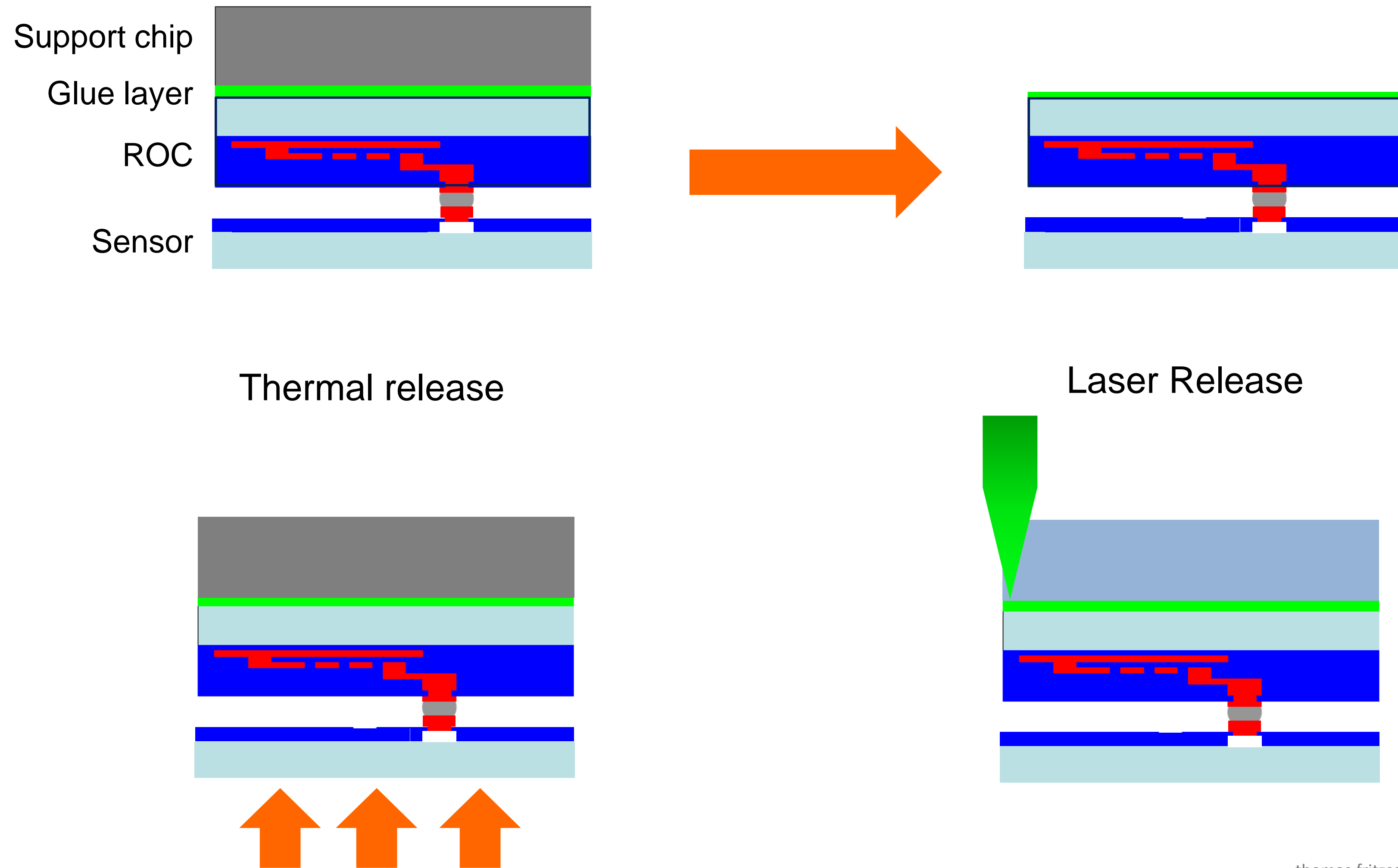
Thin Chip Assembly – Temporary Support Approach

Tested Chip Release Technologies



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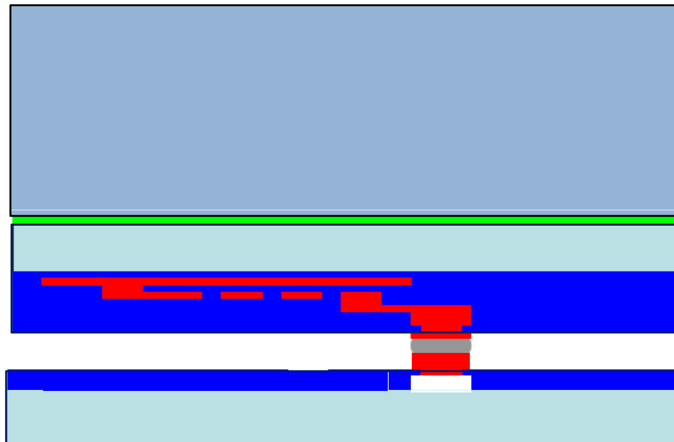
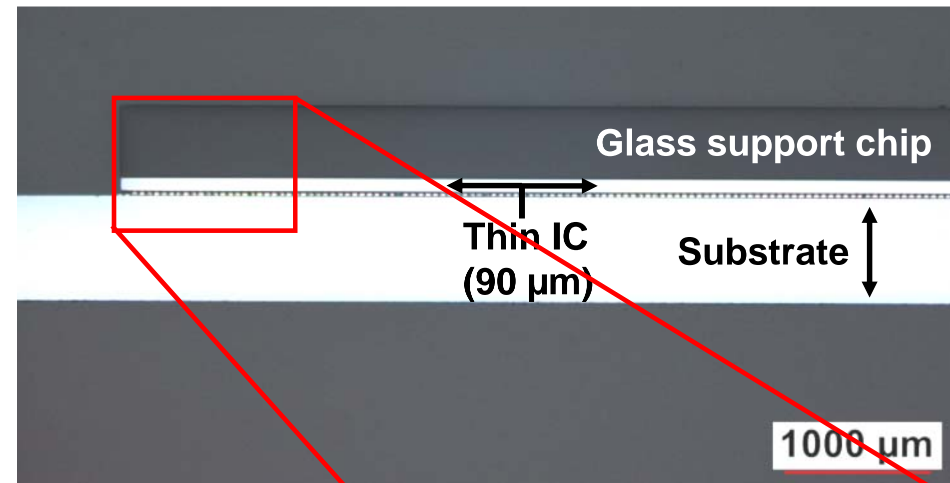
Thin Chip Assembly – Temporary Support Approach

Laser Debonding using UV-Release Glue

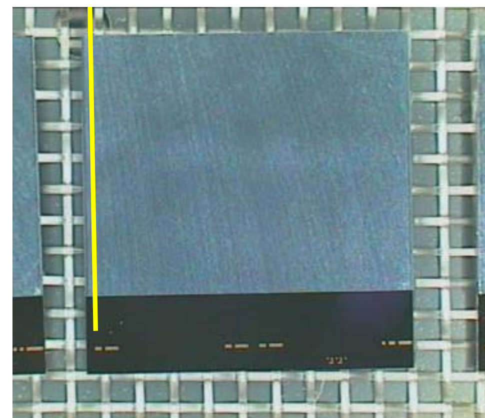
1. Step: Flip Chip Assembly of Chipstack

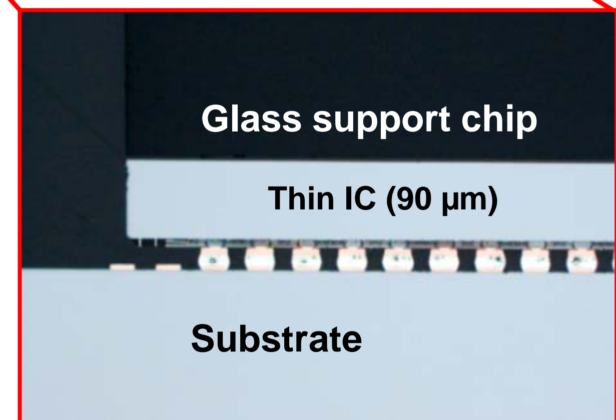




Left:
Chip after bump bonding
size 14x11 mm² (2x1 FE-I3)

Right:
Cross section of the first bump row
(yellow line)





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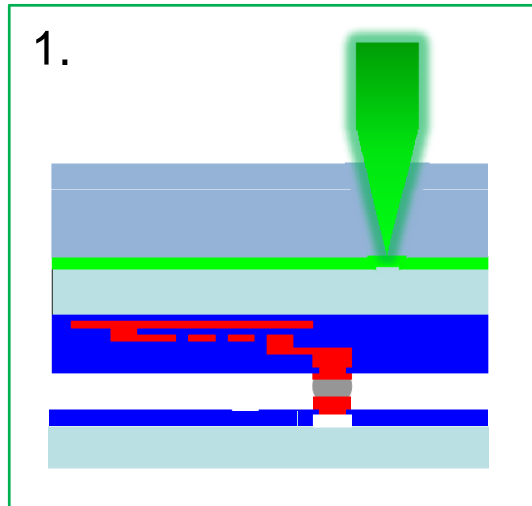
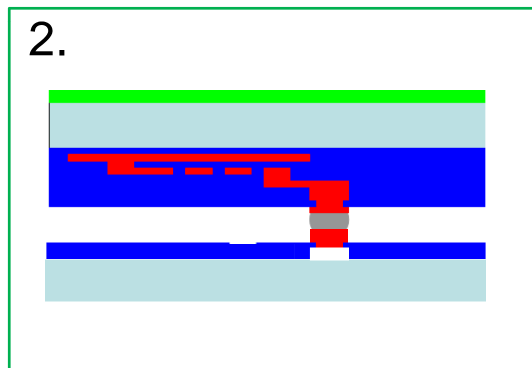
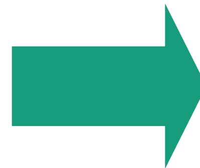
Thin Chip Assembly – Temporary Support Approach

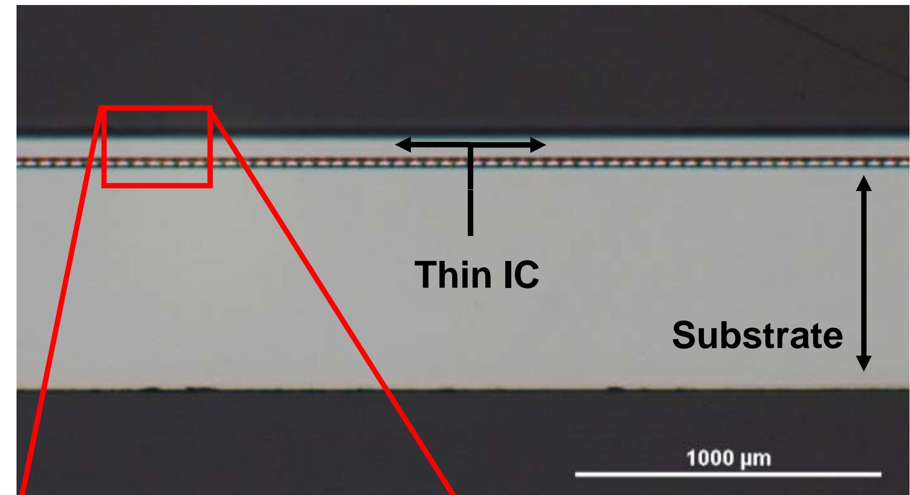
Laser Debonding using UV-Release Glue

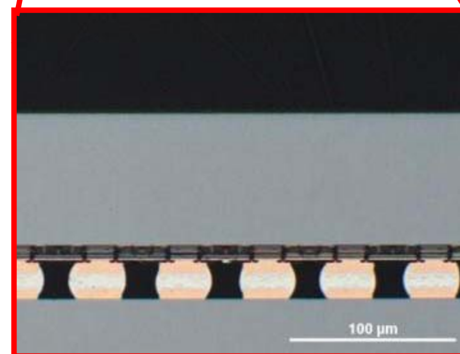
2. Step: Support Chip Release











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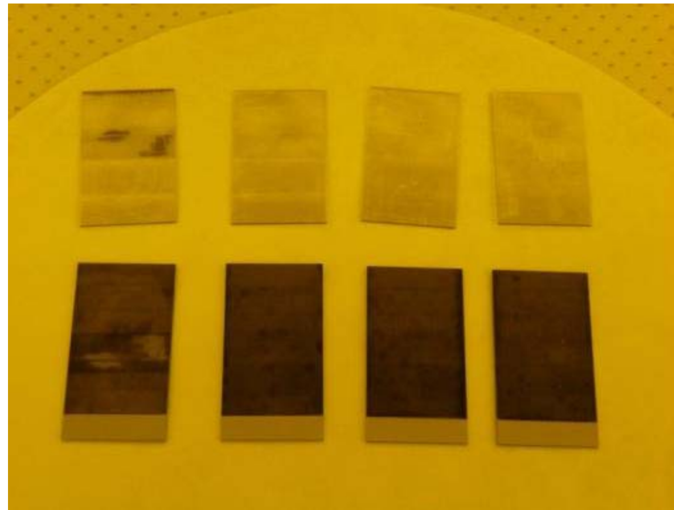
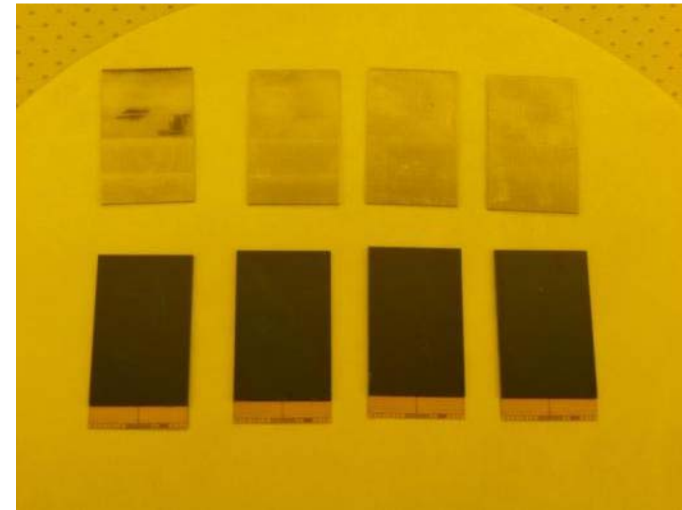
Thin Chip Assembly – Temporary Support Approach

2x2 FE-I3 Reticle After Laser Debonding, ROC thickness 90µm

Glass support chip



Module ROC backside after support chip release



Module dummy sensor backside, end of column logic of ROC visible

- No cracks in 90µm thinned ROC were observed
- Sent to Bonn University for functional tests

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Thin Chip Assembly – Temporary Support Approach

Laser Debonding Process - Next steps:

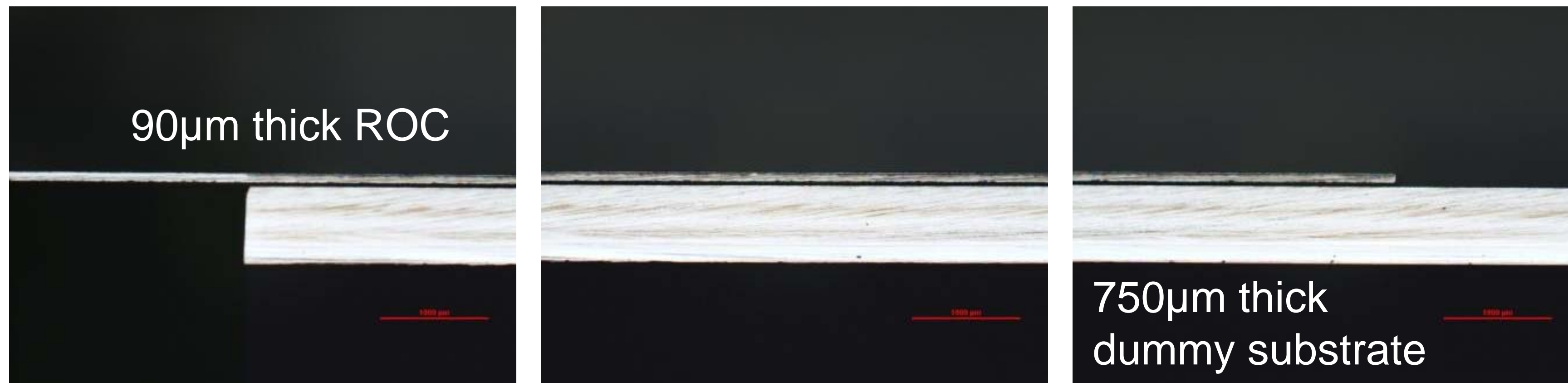
- **Thinning and assembly test with FE-I4 wafer and ROCs**

  - FE-I4 wafer batch with thinned wafers (with/without support wafer)

- **Debonding test with FE-I4 chips and process optimization**

- **Handling and bonding tests of thin chip modules**

  - fragile overhanging wire bond edge on FE-I4 chip



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Summary & Outlook

Chip to wafer bonding evaluation using high throughput flip chip bonder tool:

- Sufficient alignment accuracy
- Pick and place process time reduction

- Next steps:
  - Process optimization of chip to wafer bonding and module release process
  - Measurements of daisy chains and yield analysis

Thin Chip Assembly:

- Flip chip assembly of 90µm thin 2x1 and 2x2 FE-I3 chips without bending
- Laser debonding solution works well

- Next steps:
  - Flip chip assembly of modules using thinned FE-I4 chips
  - Functional test of thinned ROCs after flip chip assembly

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