Ray Yarema
Fermilab
For the HEP 3D Consortium

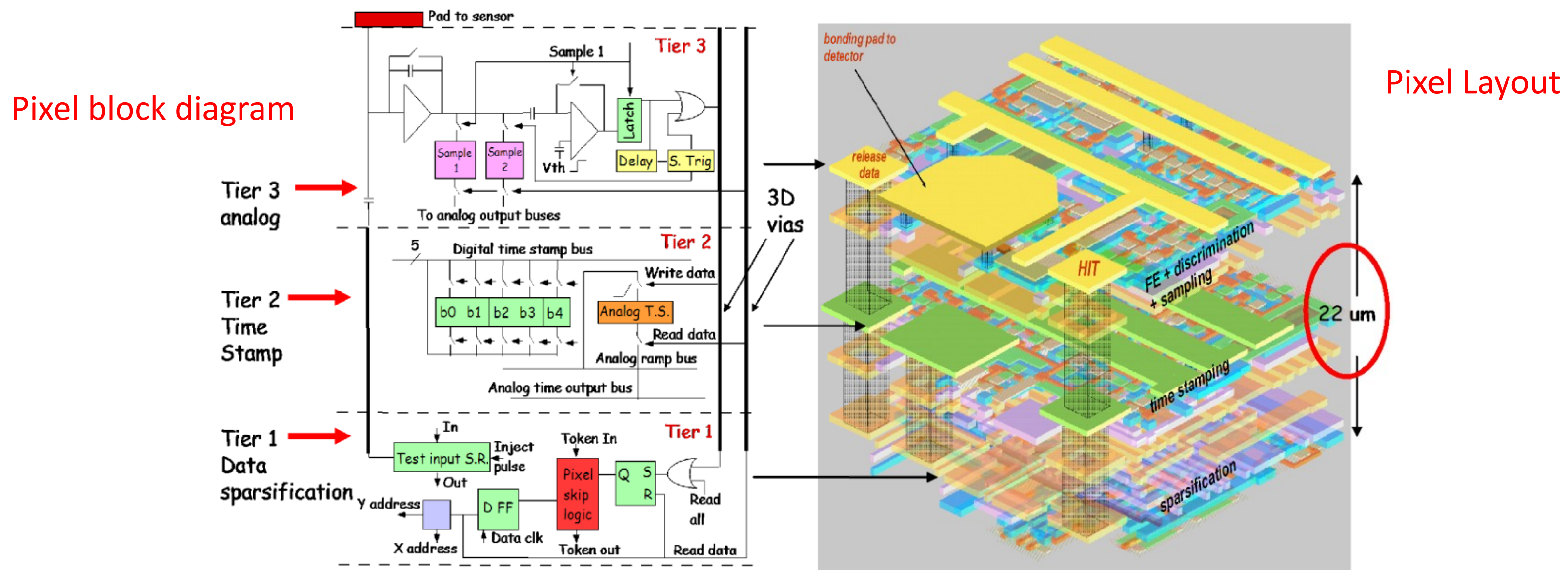
ATLAS-CMS electronics workshop
March 9-11, 2011
Geneva, Switzerland

Introduction

- Much has been learned by HEP groups since our early attempts at 3D circuit integration which began in 2006.
  - Some HEP groups have examined various 3D technologies for different applications.
  - Other groups have been more focused on circuit designs in 3D
- This talk will discuss 3D processes for HEP circuit designs
  - In particular, the talk will focus primarily on the HEP 3D Consortium experience and lessons learned using the Chartered/Tezzaron 3D process
  - A look to what lies ahead will also be presented

Initial 3D Circuit Designs with MIT LL

- MIT LL 3D Process
  - Via last, oxide bonding, 3 tiers
  - 0.18 um SOI (non-commercial)
- First submission 2006 (Fermilab)
  - ILC pixel ROIC
  - Terrible yield
  - No 3D interconnect problems found
  - Significant threshold shifts associated with oxide bonding between tiers raising concern about radiation damage
  - Apparent processing problems
    - Bad current mirrors
    - High leakage currents
  - Took more than 1 year to fab
- Second submission 2008 (Fermilab)
  - Same basic design
  - Relaxed design rules to improve yield (larger feature sizes)
    - Bigger transistors
    - Wider traces
    - Redundant vias (Not TSVs)
  - Yield much better, acceptable performance
  - Almost 2 years to fab
- Fabrications paid for by DARPA



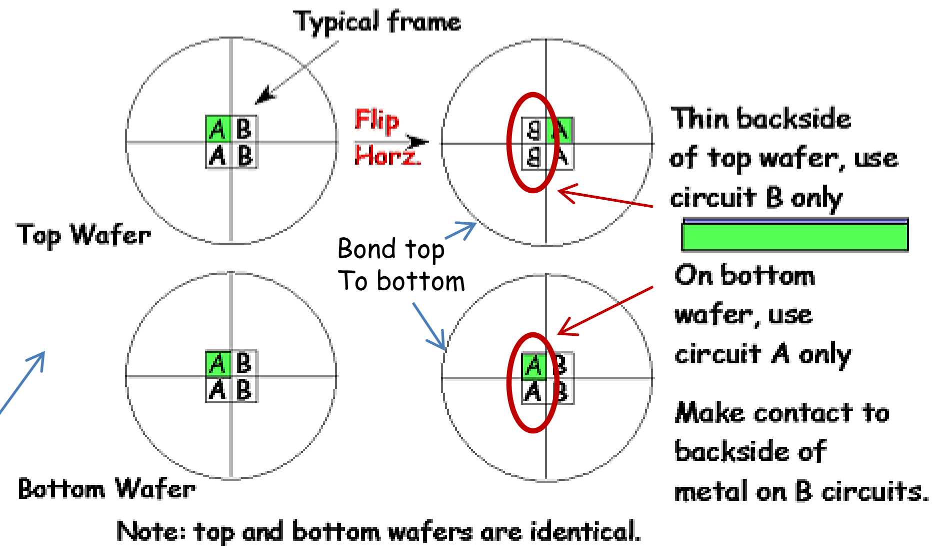
3D Circuit Design Efforts Shift to Commercial Vendors for Better Results

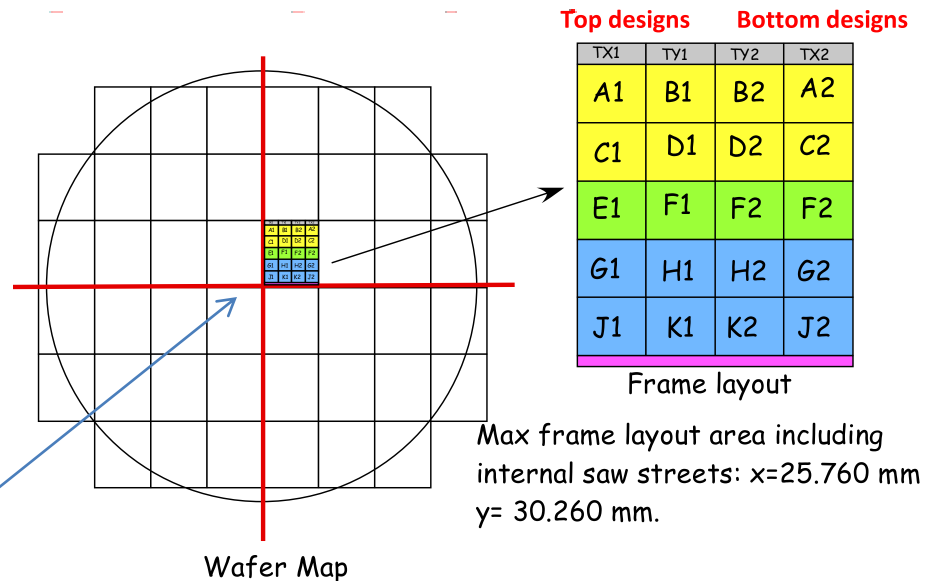
- **Tezzaron Semiconductor**
  - Leader in 3D technology development (received prestigious 2009 Semi North American award for 3D contributions)
  - Has commercial customers using 3D
  - 3D Process
    - Copper to copper bond process
    - Via middle process
    - Very small vias (1.2 um)
    - Process installed at Chartered for several years
    - Relatively low cost process
  - Willing to work with HEP customers (domestic and foreign)

- **Chartered Semiconductor (now GlobalFoundries)**
  - Established foundry (in Singapore)
  - Smaller feature process – 130 nm
  - High yield process
    - Should eliminate any processing problems
  - CMOS instead of SOI
    - Expect better radiation tolerance than standard SOI
    - Hoped to equal to CERN 130 nm CMOS experience (radiation, noise)
  - Cost lower than other 130 nm processes
  - Signed agreement with Tezzaron for 3D development

HEP Interest in 3D Grows

- HEP consortium for 3D circuit design formed in late 2008
  - 17 member groups from 6 countries (Italy, France, Germany, Poland, Canada, USA)
  - First Meeting Dec 2008
    - Began working on 3D MPW run to Chartered/Tezzaron -First MPW run for outside customers
    - Two tiers
    - Identical wafers with Cu/Cu face to face bonding
    - Single set of masks for both tiers
- HEP MPW run - more than 25 two tier designs (circuits and test devices)
  - CMS strips, ATLAS pixels
  - ILC pixels
  - B factory pixels
  - X-ray imaging
  - Test circuits
  - Frame divided into 12 subreticules for top tier and 12 for bottom tier





Issues/Lessons

- Initial design work completed in May 2009
  - In hind sight, much too short a time
  - More design time could have reduced some of the rework problems
- The following sections provide a quick overview of some issues encountered
  - Wafer order issues
  - Design issues
  - Submission issues
  - Processing issues

- Wafer order
  - Extra wafers beyond those needed for 3D assembly must be fabricated
    - Foundry must have wafers with top metalization so that PCMs can be tested
    - Those wafers must be paid for by customer
    - Extra wafers allow designers to add metalization on a few wafers to test individual tiers. This can be of great benefit for some 3D designs but requires some extra thought and design work.

Brief Overview of Some Design Issues

- Everyone did not use the same design kit provided by Tezzaron leading to
  - Stream layer map inconsistencies – big problem
  - Misuse of top metal
  - Incorrect MiM cap rules

Lesson - Use the same design kit

- Some design rules were interpreted incorrectly leading to various TSV design problems.
  - Dishing of wafers where a third layer was to be added
  - Metal 1 over lap on TSV which could cause contamination problems

Lesson-Clarify 3D design rules

- Initially some designs did not use a fill program resulting in fill problems later on

Lesson – use automated fill program

- Custom SRAM cells raised numerous questions.

Lesson – custom SRAM cells should only be used after close discussion with Tezzaron and Chartered since some cells may be rejected by Chartered even if they pass the design rules

- Tezzaron uses MicroMagic to assemble the frame for 3D submissions.
  - In the course of receiving designs, two separate software problems were found due to the nature of our designs
    - A rounding error caused off grid placement of bond interface pads only in some designs leading to unnecessary errors.
    - An ARM cell was used that had off grid vertices that created unnecessary errors
  - The problems have been fixed

Lesson- You can't avoid Murphy's Law

Brief Overview of Some Submission Issues

- Chartered provided initial size of design area in the frame. After all designs were completed and used all the design space, Chartered requested additional street space. It took three submissions before Chartered would finally accept the frame.

  Lesson- get preapproval of frame layout

- Some designs had labels outside the design area causing Chartered to reject submission and much rework.

  Lesson – Nothing can lie outside the design area

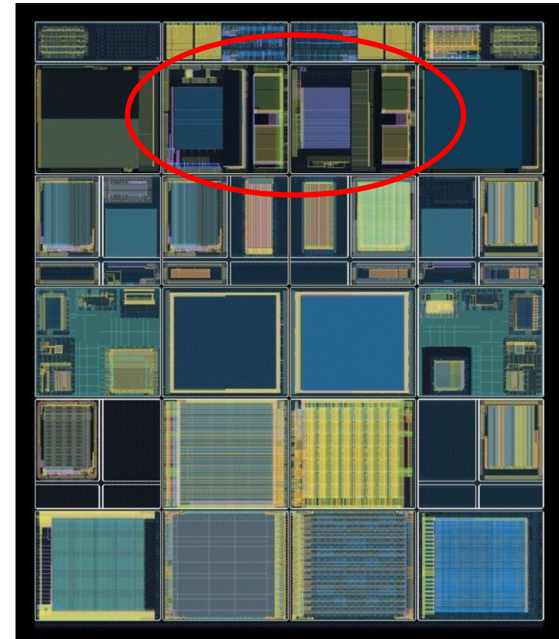
- After designs received by mask house, individual blocks were incorrectly mirrored by the mask house which fortunately was caught by Tezzaron before the masks were made. *Murphy again?*

- Chartered considers every design is for high volume and thus they would not accept some error waivers we thought were acceptable.

  Lesson – fix every error you can

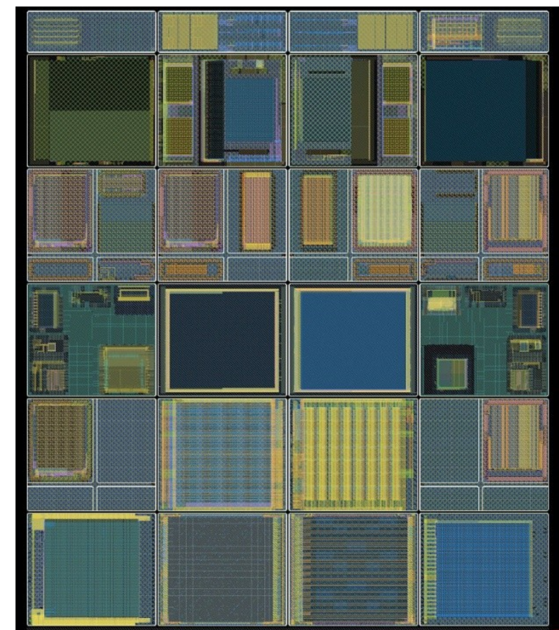
- Some designs were submitted with incorrect mirroring

  Lesson- you can't be too careful in 3D design



MPW run frame

One layout Incorrectly mirrored



All layouts correctly mirrored

Brief Overview of Known Fabrication Issues

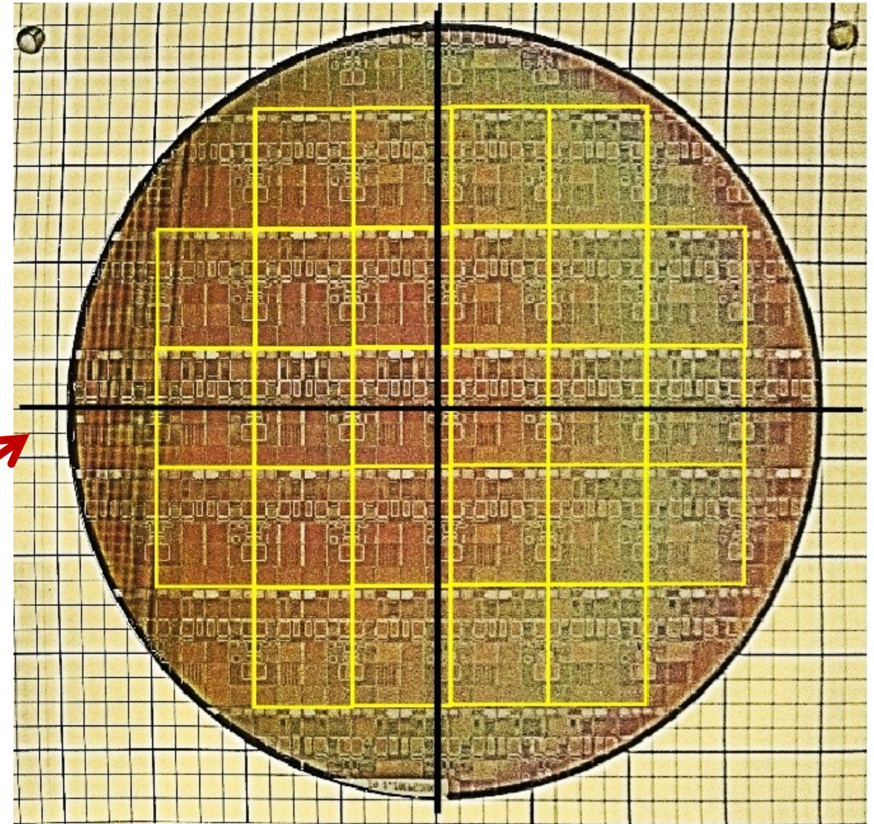
- 3D fabrication done in Chartered prototype line
- Chartered was bought by Global Foundries which slowed our wafer fabrication process
  - Personnel knowledgeable in 3D fab issues were moved
  - Some equipment use for 3D fab moved to higher profit production line
- Global/Chartered did not properly place frames on wafers for 4 different lots of wafers being processed for Tezzaron. The wafers could not be aligned properly for 3D bonding.
  - Never happened before
  - HEP wafers had to be refabricated resulting in several months delay

Murphy's Law at work.

- Due to delays in fabrication, the 3D wafer bonding facilities were not available when the wafers were ready.

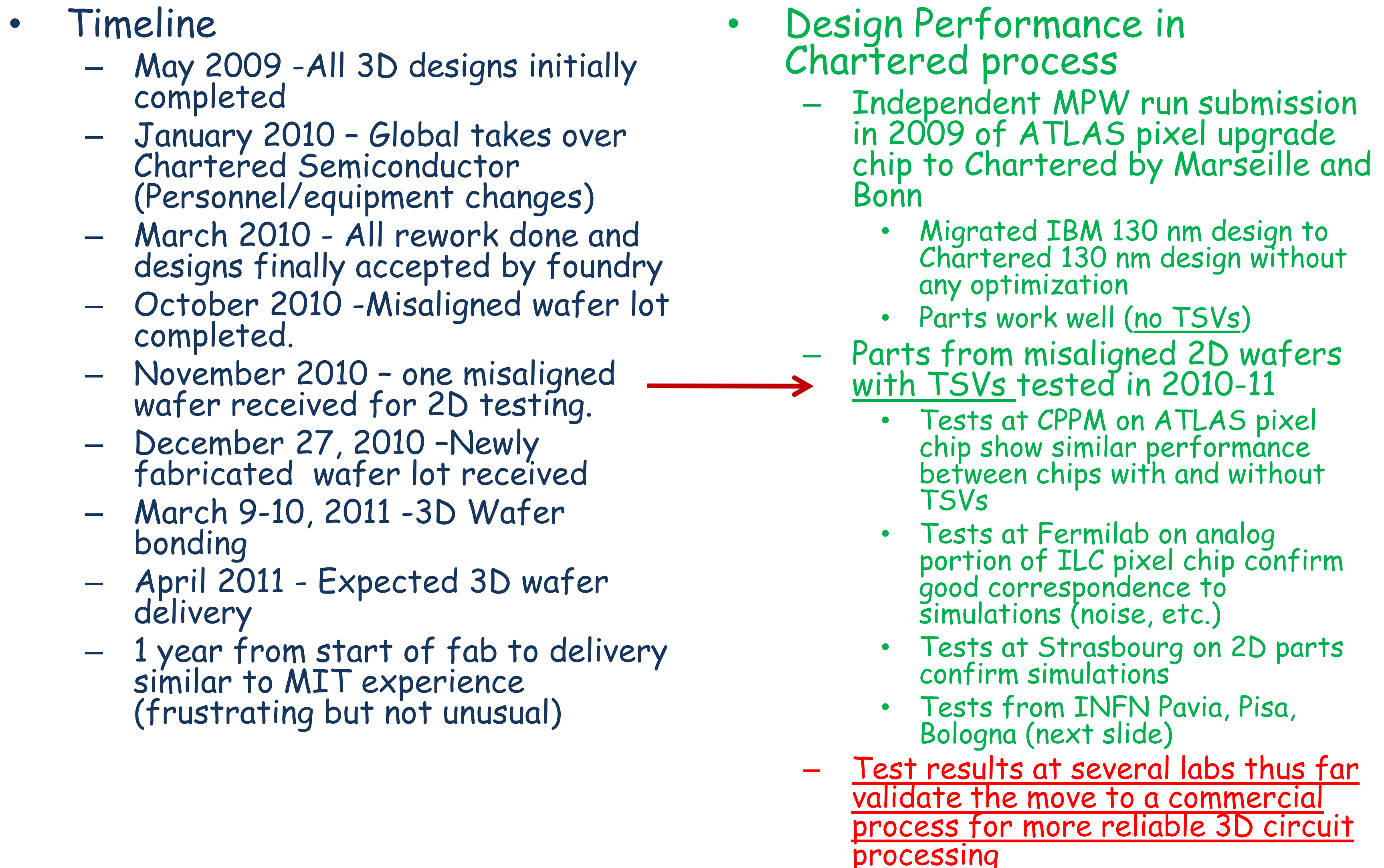
Lesson – Tezzaron working to bring all processing steps to central location to avoid turn time problems

1.2 mm misalignment



Frames are not placed symmetrically about the wafer center lines

Timeline and Test Results



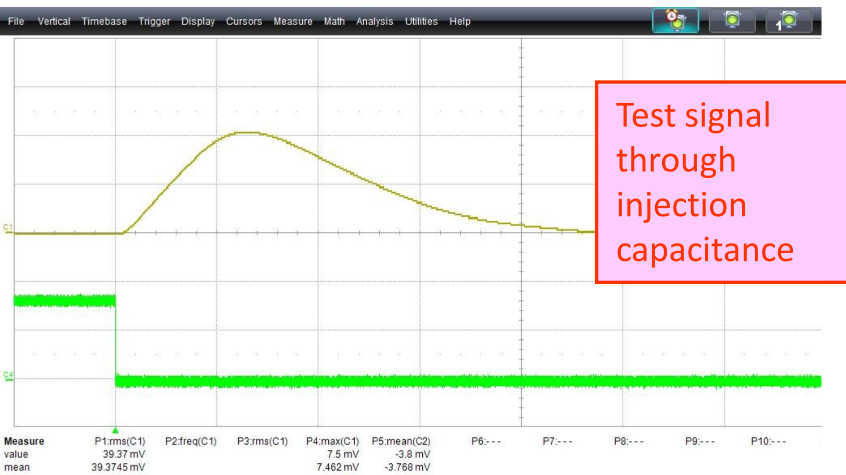
Deep N-Well MAPS, 2D version in the Chartered process

(INFN Pavia, Pisa, Bologna)

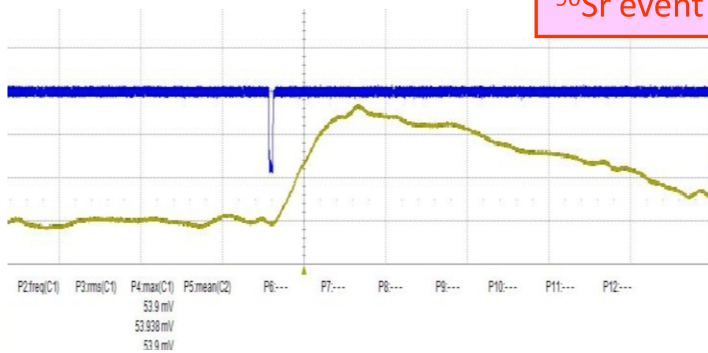
Preliminary

Analog and digital readout sections are functional. Analog signals, electronic noise (ENC ~ 50 e) and spectra from radioactive sources have been measured.

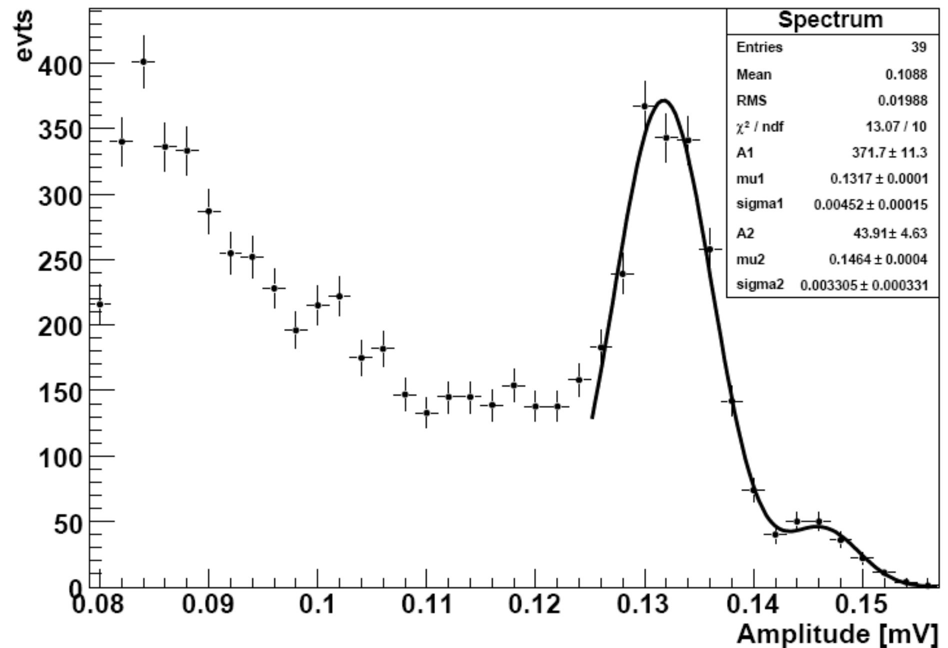
Signal at shaper output



Test signal through injection capacitance

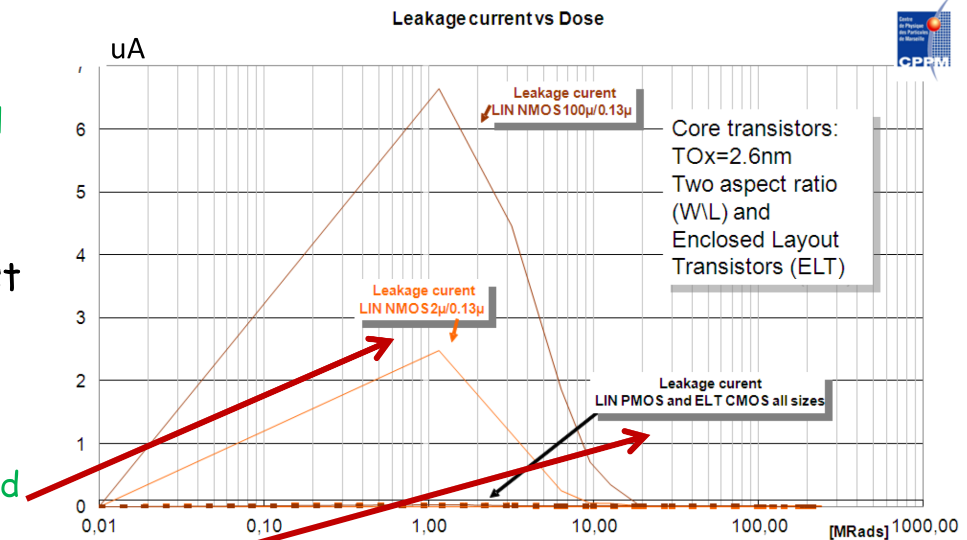


^{90}Sr event

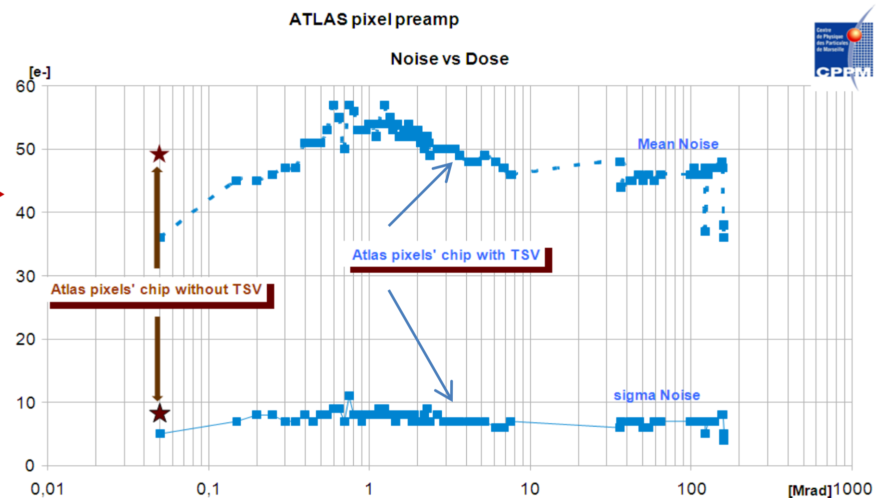


Chartered Radiation Test Results by CPPM

- In 2009, rad tests done on the ATLAS upgrade pixel chip were done in a proton beam
  - No design optimization done for the Chartered process
  - Circuit fully operational up to 160 Mrads
  - Suspect a dose induced problem in digital section ~ 160 Mrads (not confirmed)
- Testing of core linear and ELT transistors and ATLAS pixel circuits on 2D parts <u>with TSVs</u> in CERN's X-ray test lab at 3.2 Mrads/hour (Preliminary results)
- 2D test results (compare transistor results to CERN 130 nm results)
  - NMOS leakage current shows peak around 1 Mrad – similar to other CERN results
    - Linear NMOS leakage may be a concern
  - Linear PMOS and ELT NMOS and PMOS are good
  - NMOS and PMOS Vt shifts are similar to CERN tests on other 130 nm processes, however <u>Chartered NMOS Vt shift is positive instead of negative.</u>
  - Tests on ATLAS pixel preamp show only a small change in noise up to 160 Mrads
- Radiation tests thus far suggest that the Chartered 130 nm process is similar to other 130 nm processes tested at CERN
- <u>Rad tests thus far validate move to commercial CMOS for high radiation tolerance.</u>



Total Ionizing Dose Effects in FETC4 Atlas chip



Commercial Future

- Tezzaron
  - Activities to become a US Trusted Foundry are moving forward
  - Working to bringing all 3D facilities to central location in the US to fix turn time problems.
  - Later this year Tezzaron will be doing TSVs in the Honeywell 150 nm rad hard SOI process at Honeywell using 0.4 um TSVs
  - Next year Tezzaron TSV process is expected to be running on Chartered 12 inch, 65 nm CMOS wafers
  - Tezzaron has demonstrated insertion of TSVs up to M4 at non-Chartered facilities.
  - In about 1 year expects to accept wafers from different foundries and processes for 3D assembly (e.g. IBM 90 nm CMOS)

- MOSIS/CMP/CMC (silicon brokers in US, France, and Canada)
  - June 2010 - Announced plan to offer 3D services using Tezzaron
  - Working with Fermilab to make HEP 3D efforts available to the commercial world
  - Design platform is being developed by Kholdoun Torki at CMP and the first version should be available soon (next slide)
  - MOSIS, CMP, and CMC will all receive designs
  - MOSIS will assemble designs into a reticule
  - Tezzaron will handle the final processing of the 3D frame (e.g. adding bond pad interface fill, etc.) and submit design to Chartered.

Tezzaron/GlobalFoundries Design Platform

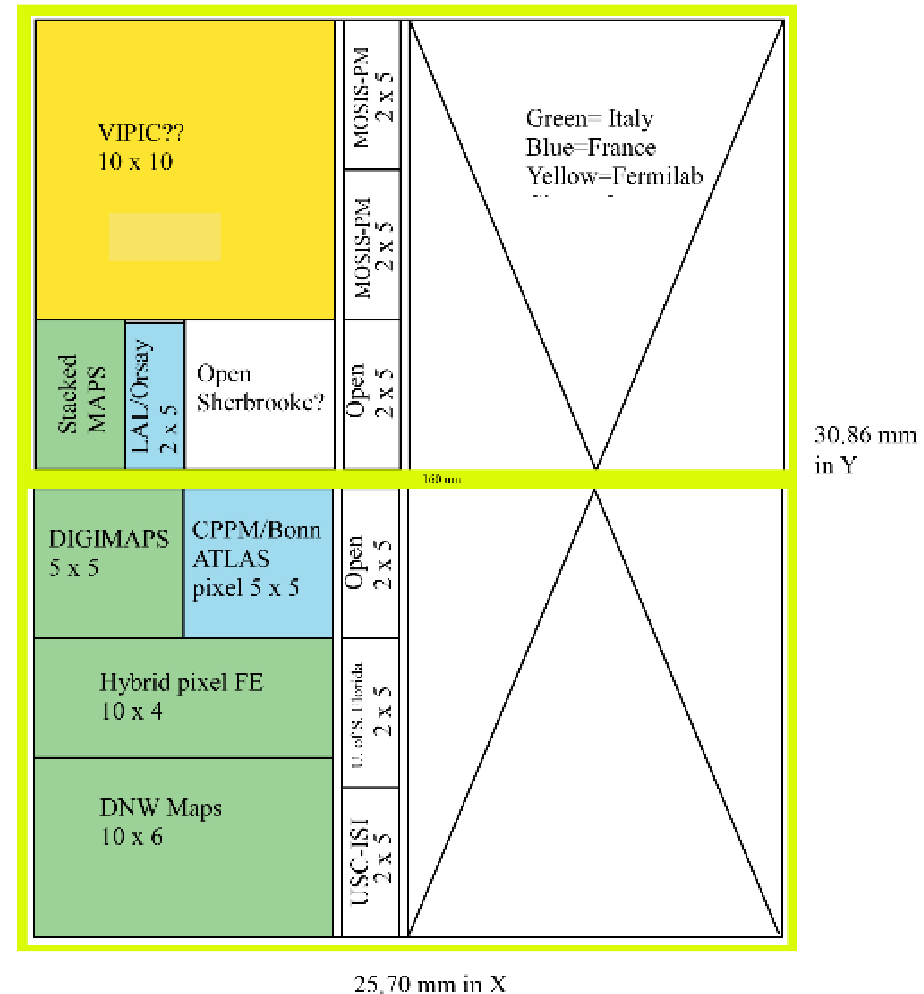
- The Design Platform is modular. It has all features for full-custom design or semi-custom automatic generation design. (From Kholoun Torki, CMP)
  - PDK : *Original PDK from GF + (TSV / DBI) definition*
  - Libraries : *CORE and IO standard libraries from ARM*
  - Memory compilers : *SPRAM, DPRAM and ROM from ARM*
  - 3D-IC Utilities : *Contributions developments embedded in the platform*
  - Tutorials, User's setup.
- All the modules inside the platform refer to a unique variable, making it portable to any site. The installation procedure is straightforward.
- Support of CDB and OpenAccess databases.

Consortium contributions

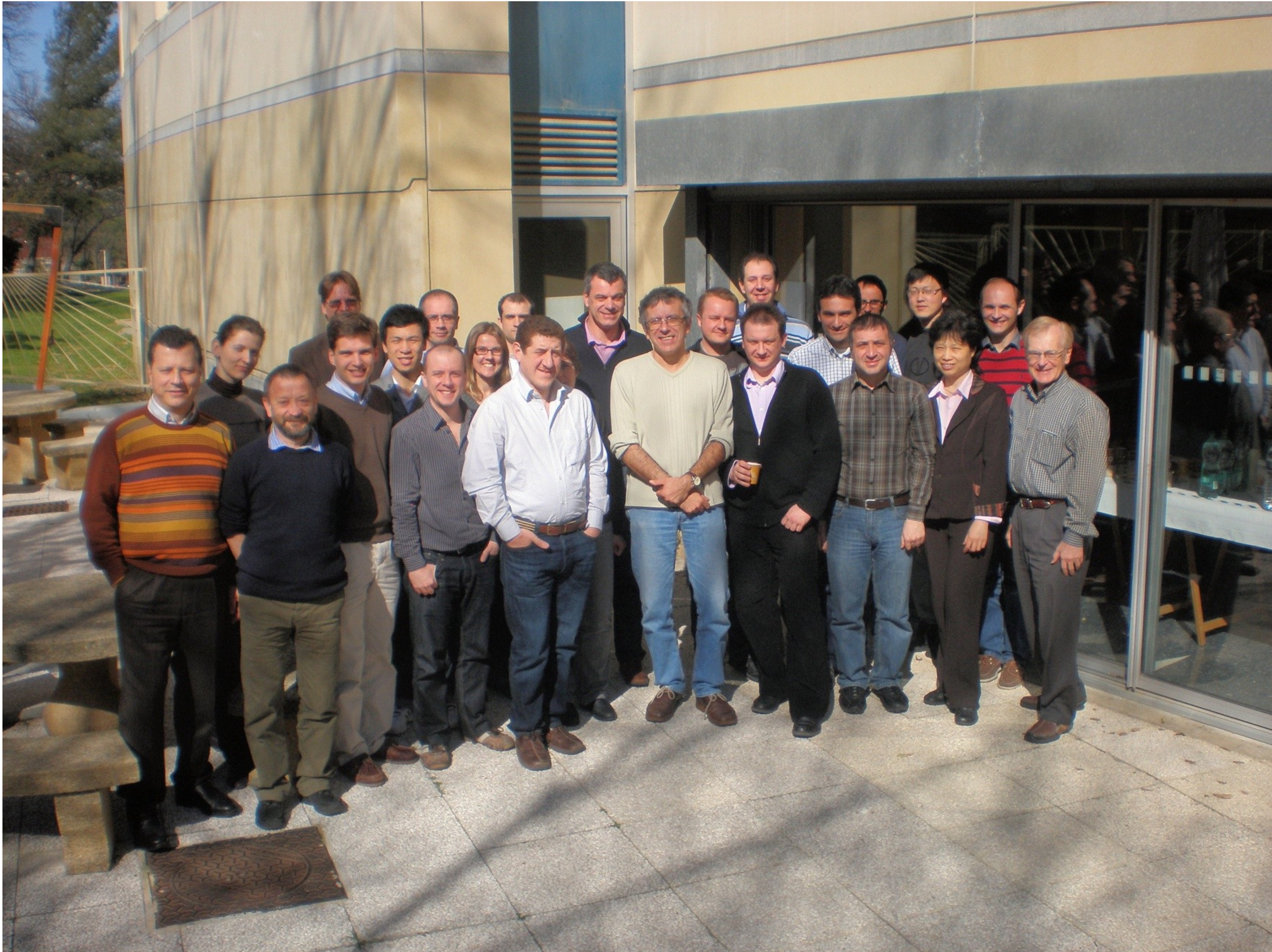
- DBI (direct bonding interface) cells library. (FermiLab)
- 3D Pad template compatible with the ARM IO lib. (IPHC)
- Preprocessor for 3D LVS / Calibre (NCSU)
- Skill program to generate an array of labels (IPHC)
- Calibre 3D DRC (Univ. of Bonn)
- Dummies filling generator under Assura (CMP)
- Basic logic cells and IO pads (FermiLab)
- Floor-planning / automatic Place & Route using DBIs, and TSVs (CMP)
- Skill program generating automatically sealrings and scribes (FermiLab)
- MicroMagic PDK (Tezzaron/NCSU)

Consortium Future Plans

- HEP 3D Consortium
  - Anxiously awaiting first 3D chips
  - Testing of chips to be done at numerous facilities
  - Some chips will be bonded to sensors at Ziptronix and other places
  - Design efforts have been started toward the next 3D submission.
  - Most members want to evaluate the first chips before submitting next chip
  - Preliminary frame has been put together showing HEP designs and some non-HEP users
  - Next submisison - this summer??



Some of the HEP 3D Consortium Members



Summary

- It's been a long road from the first HEP 3D circuits at MIT LL to where we are now with Tezzaron/Chartered. A large consortium of interested partners has been formed for 3D circuit design. The road forward has had many more potholes than we ever expected. Developing a new technology has its challenges. Although expectations should be high, one must be prepared to work through the problems. As a group we have learned a lot. We are working to bring the information gained and lessons learned to commercial vendors who can build upon our work and offer 3D Multi Project Wafers runs to a larger community. The benefit of this effort will be a better and more consistent 3D design platform, less stress for designers, and more efficient use of engineer's circuit design time. HEP should benefit in general by having a new technology to explore for the development of new detector systems.