Laminate Based System in Package (SiP) Utilizing High Density Interconnect (HDI) Substrates in High Reliability Applications

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What is SiP?....An Integrated Solution

- System in Package (SiP) delivers 10-20X reductions from current designs
- Up to 90% weight reductions
- Significantly lower power and improved electrical performance
- Hi-Reliability, Hi-Quality, Hi-Performance
- Remove layers of interconnect
- Addresses growing demand in:
  - Unmanned systems
  - Radar
  - Space satellites
  - Electronic Warfare
  - Medical Applications
  - Research Applications
- The magic dust:
  - Bare die
  - HDI substrates

620mm² PWB reduced to 30mm²
Typically multiple bare die and SMT components on a HDI microelectronics substrate:

- Large and Small Bare Die placement & attach
  - Flip chip die connections
  - Wirebond die connection
  - Dual sided attach
  - Component substitution

- SMT placement & attach
  - Down to 0201’s, 01005’s
  - CSP’s, SOIC’s, PLCC’s, SOJ’s

- Connections to next level assembly
  - SMT pinned connectors
  - Ball Grid Array

- High Density Interconnect Substrates: the secret sauce!
  - Laser drilled through and microvias
  - 25 micron trace width and space
  - Thin, low loss, low dielectric constant materials
System in Package Overview

- **Package Size**
  - Standard JEDEC 13.0mm to 55.0mm
  - Custom size and shape SiPs

- **Assembly to Organic Substrates**
  - FR4 and BT epoxy
  - Particle filled epoxy build-up
  - PTFE dielectric
  - Kapton flex
  - Polyimide
  - LCP

- **Common Product Parametrics**
  - Large MCM/SiP packages
  - Hybrid/double-sided assembly
  - Single chip module and device packages

- **Test**
  - Shorts-opens
  - JTAG/boundary scan
  - Full functional test
System-in-Package Conversion

➢ Where we begin:
  – Technical contact at the customer
  – Si design: Bare die availability
  – Preliminary BOM Analysis
    • Input
      – Bill of Materials & Approved Vendor List
    • Output
      – Smaller package & bare die recommendations
  – Preliminary Area Study
    • Input
      – Board design file & Electrical restraints
    • Output
      – initial conversion of PCB to substrate
        » cross section, dielectric and size estimates
      – Initial assembly layout
  – Substrate design and assembly layout
    • Electrical, thermal and mechanical analysis
Design Tools and Modeling
Overview of Package Behaviors

- **Ceramic**
  - Finite BGA fatigue life
  - Very little warpage
  - No internal packaging issues

- **Direct chip attach to organic**
  - Control of warpage, adhesive strength
  - Smaller chips
  - Coverplate to balance stresses

- **Build-up technology**
  - Use of somewhat compliant outer layer
  - Outer layer electricals less desirable
  - Outer layer strains substantial
# Laminate vs. Ceramic Reliability Comparisons

## 45mm body size

<table>
<thead>
<tr>
<th>Product</th>
<th>Material</th>
<th>Typical Substrate Thickness</th>
<th>Dielectric Constant</th>
<th>Loss Tangent</th>
<th>Component Level Reliability -55 to 125°C</th>
<th>Board Level Reliability 0-100°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>HTCC (solder columns)</td>
<td>Glass Ceramic 11</td>
<td>1.0 mm</td>
<td>8.1</td>
<td>.0034</td>
<td>1000 cycles</td>
<td>2,200 cycles to 1&lt;sup&gt;st&lt;/sup&gt; fail</td>
</tr>
<tr>
<td>HyperBGA&lt;sup&gt;®&lt;/sup&gt;</td>
<td>PTFE</td>
<td>0.47 mm</td>
<td>2.7</td>
<td>.003 (49% silica filled)</td>
<td>1000 cycles</td>
<td>10,000 cycles to no</td>
</tr>
<tr>
<td>CoreEZ&lt;sup&gt;™&lt;/sup&gt;</td>
<td>Epoxy/P-Aramid Fiber Core and particle filled Epoxy build up</td>
<td>0.526 mm (8 layer)</td>
<td>3.5</td>
<td>.022</td>
<td>1000 cycles</td>
<td>5,000 cycles to 1&lt;sup&gt;st&lt;/sup&gt; fail</td>
</tr>
</tbody>
</table>

Plastic solutions offer:
- High electrical performance
- High reliability performance
- Weight reduction
- Smaller x, y, z form factor
PTFE Substrate Chip Joining

Measured flatness of 42.5mm laminate + stiffener subassembly example
Viewed from BGA side: Moiré topographic fringe contours at 8.33 microns / fringe

Room temperature, 20C
Reflow temperature, 183C

14.7 mm size chip bump region (in red) remained flat to within 17 microns
Typical PWB to SiP Prototype Cycle

- Critical Design Inputs
- BOM Analysis
- BOM Substitution Recommendations
- SiP Physical Layout
- Preliminary Design Review
- SiP Physical Layout Optimization
- Critical Design Review
- Substrate Fab
- SiP Assembly & Test

29 weeks from design inputs to ship is common, assuming component availability.
HDI Microelectronics Packaging Menu

Microelectronics Packaging

- **Epoxy Glass Substrate**
  - Cost performance
  - FR4, BT, Polyimide
  - Mechanically drilled holes
  - 75 micron trace
  - 75 micron spaces
  - Flip chip, Wirebond, SMT
  - Radiation Hard Capable

- **CoreEZ®**

- **Thin Core Build Up**
  - Cost performance
  - Particle filled epoxy
  - Thin core (coreless)
  - Laser drilled core
  - Laser drilled build up
  - 25 micron trace
  - 25 micron space
  - Buried resistors
  - Flip chip, Wirebond, SMT
  - Radiation Hard Capable

- **HyperBGA®**

- **PTFE Substrate**
  - High Bandwidth/RF
  - Particle filled material
  - Coreless
  - Laser Drilled Vias
  - Fusion Bonding
  - 25 micron trace
  - 33 micron space
  - Flip chip, Wirebond, SMT
  - Radiation Tolerant
Packaging Attributes applied to SiP conversions

Substrate features and advanced IC Assembly techniques enable bare die implementation

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Standard PCB</th>
<th>HDI Substrate</th>
<th>Shrink opportunity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Through via</td>
<td>Mechanical</td>
<td>Laser</td>
<td></td>
</tr>
<tr>
<td>Through via dia.</td>
<td>200 microns</td>
<td>50 microns</td>
<td>4X</td>
</tr>
<tr>
<td>Through via capture pad diameter</td>
<td>400 microns</td>
<td>100 microns</td>
<td>4X</td>
</tr>
<tr>
<td>Line Width</td>
<td>75 microns</td>
<td>25 microns</td>
<td>3X</td>
</tr>
<tr>
<td>Space Width</td>
<td>75 microns</td>
<td>25 microns</td>
<td>3X</td>
</tr>
<tr>
<td>Semiconductors</td>
<td>Packaged</td>
<td>Bare die or small package</td>
<td>4X to 10X</td>
</tr>
</tbody>
</table>

Flip Chip Bump

3-4-3 CoreEZ®
## 2011 Product Attribute Comparisons

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Standard (Epoxy Glass or Polyimide)</th>
<th>HDI: Dense (Particle Filled Epoxy)</th>
<th>HDI: LCP (liquid crystal polymer)</th>
<th>HDI: PTFE (PTFE)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Line width</td>
<td>75 microns</td>
<td>25 microns</td>
<td>37.5 microns</td>
<td>25 microns</td>
</tr>
<tr>
<td>Line space</td>
<td>75 microns</td>
<td>25 microns</td>
<td>37.5 microns</td>
<td>33 microns</td>
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<tr>
<td>Via type</td>
<td>mechanical</td>
<td>laser</td>
<td>Laser</td>
<td>laser</td>
</tr>
<tr>
<td>Via diameter</td>
<td>200 microns</td>
<td>50 microns</td>
<td>50 microns</td>
<td>50 microns</td>
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<tr>
<td>Stacked vias</td>
<td>Build up only</td>
<td>Build up only</td>
<td>In 2010</td>
<td>In 2010</td>
</tr>
<tr>
<td>Capture pad diameter</td>
<td>400 microns</td>
<td>100 microns</td>
<td>110 microns</td>
<td>110 microns</td>
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<tr>
<td>Surface finish</td>
<td>E-less Ni / I Au, ENEPIG</td>
<td>Same</td>
<td>Same</td>
<td>Same</td>
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<tr>
<td>Solder mask</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
<td>no</td>
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<tr>
<td>Thickness</td>
<td>&lt;1mm</td>
<td>0.4 - .7mm</td>
<td>0.5mm</td>
<td>0.5mm</td>
</tr>
</tbody>
</table>
| Layers                     | 10                                  | 12                               | 4, 6 in 1
|                            | St article                          | 11                               |
## 2011 Product Attribute Comparisons

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Standard</th>
<th>HDI: Dense BU (Particle Filled Epoxy)</th>
<th>HDI: LCP (liquid crystal polymer)</th>
<th>HDI: PTFE (PTFE)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCB Attach</td>
<td>Pin Grid, BGA, LGA, Custom</td>
<td>Pin Grid, BGA, LGA, Custom</td>
<td>Pin Grid, BGA, LGA, Custom</td>
<td>Pin Grid, BGA, LGA, Custom</td>
</tr>
<tr>
<td>Die attach</td>
<td>Wirebondable, Flip Chip &lt;14mm, SMT</td>
<td>Wirebondable, Flip Chip &lt;14mm, SMT</td>
<td>Wirebondable, Flip Chip &lt;14mm, SMT</td>
<td>Wirebondable, Flip Chip 14mm, SMT</td>
</tr>
<tr>
<td>Flexible</td>
<td>Rigid Flex</td>
<td>HDI Rigid Flex</td>
<td>Flex</td>
<td>Flex</td>
</tr>
<tr>
<td>Formable</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>no</td>
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<tr>
<td>Radiation Level</td>
<td>Strategic Rad Hard</td>
<td>Strategic Rad Hard</td>
<td>Strategic Rad Hard</td>
<td>Rad Tolerant</td>
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<tr>
<td>Embedded Passives</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>FC Component level reliability (-55 to 125°C)</td>
<td>1000 cycles</td>
<td>1000 cycles</td>
<td>1000 cycles</td>
<td>1000 cycles</td>
</tr>
<tr>
<td>FC Board level reliability (0 to 100°C)</td>
<td>2,000 cycles</td>
<td>5,000 cycles</td>
<td>In testing</td>
<td>10,000 cycles</td>
</tr>
<tr>
<td>Composite CTE</td>
<td>19ppm</td>
<td>18ppm</td>
<td>17ppm (X&amp;Y)</td>
<td>12ppm</td>
</tr>
<tr>
<td>Er</td>
<td>4.1</td>
<td>3.7</td>
<td>2.9</td>
<td>2.7</td>
</tr>
<tr>
<td>Loss Tan</td>
<td>.011</td>
<td>.016</td>
<td>.0025</td>
<td>.003</td>
</tr>
</tbody>
</table>
Physical Design content

- Physical Design Implementation
  - Component Placement & Routing
  - Physical & formal verification
  - Signal Integrity (SI) & Crosstalk analysis
  - Static Timing Analysis (STA)
  - Multiple Supply Voltage (MSV)
  - Leakage Current Reduction Techniques
  - Clock & Supply Voltage Gating
  - Power Optimization
  - Design for Test to ensure testability
  - Design for Manufacturability to maximize production yields
Signal and Power Integrity
Potential Work Items and Design Flow

➢ Typical Signal Integrity Workflow (varies by application)
  – Customer defines SI specifications in the form of routing constraints by net such as:
    • Z0 (SE, DP), Skew (Group / reference), Crosstalk / Isolation (dB @ Freq), Rdc, Insertion / Return loss (dB @ Freq), etc.
  – EIT ensures that these specifications are met as follows:
    • Pre-layout Design Guidelines:
      – Define stackup, function by layer, recommended component placement
      – Define trace width (and spacing for DP) for Z0 requirements
      – Translate electrical Skew requirements into physical lengths
      – Define spacing and coupled length limitations for crosstalk control
      – Define trace geometries to meet loss specification
    • Post-layout Verification:
      – Extract parameters from design database using Ansoft toolset
      – HFSS, Q3D, SIWave
HDI Substrate Materials Analysis
Evaluation of Materials Subjected to Various Radiation Levels

- Evaluated PTFE BGA (HyperBGA®) and Thin Core (CoreEZ ®) materials radiation response
  
  - Radiation Exposure: Co60 Gamma:
    - Control
    - 32, 50, 100, 300, 500, 700, 1000 and 5000 krad TID
  
  - PTFE Materials evaluated: Rogers 2800, PPE
    - Results: Many applications will be unaffected by radiation
      - PPE has no measurable degradation to 5 Mrad
      - RO2800 shows gradual loss of ductility with exposure

  - Thin Core Build Up Materials Considered: Thermount 55LM, Particle Filled Driclad Epoxy, PSR4000
    - Results: No measurable change of mechanical properties through 5 Mrad
Ductility performance indicates package performance in thermal cycling

- Thin Core Build Up appears to be a good choice for Rad Hard and Strategic apps.
  - Materials show no ductility degradation with radiation level
- PTFE appears to be best suited for Rad Tolerant applications
  - PTFE ductility is higher than all other materials below 300K rad exposure
  - PTFE predictably degrades significantly above 300 Krad exposure levels
HDI Laminate Substrate Technologies
**Typical PTFE® 9 Layer Cross Section**

- **40 micron thick APPE**
  - outer dielectric
  - $\varepsilon_r = 3.2$

- **35 micron thick PTFE**
  - Dielectric, $\varepsilon_r = 2.7$

- **50 micron thick PTFE**
  - Dielectric, $\varepsilon_r = 2.7$

- **15μ thick Cu**
  - redistribution

- **12μ thick Cu**

- **6μ Cu/38μ Invar/6μ Cu**
  - Ground plane

- **15μ thick Cu**
  - redistribution

- **Non soldermask defined pad**

- **12μ thick Cu**

- **12μ thick Cu**
  - 50μ dia. through via

- **APPE filled**

**BGA Pad**

**Chip**

**Bump**

**Underfill**

**Microvia**
# Packaging Electrical Comparisons

<table>
<thead>
<tr>
<th>Property</th>
<th>CBGA Alumina</th>
<th>Build-up 3+3</th>
<th>HyperBGA™</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Line width/pitch (um)</td>
<td>90/22 5</td>
<td>50/15 0</td>
<td>38/9 4</td>
<td></td>
</tr>
<tr>
<td>Zo (Ohms)</td>
<td>35-60</td>
<td>45-75</td>
<td>55-64</td>
<td></td>
</tr>
<tr>
<td>Time Delay (ps/mm)</td>
<td>* 11.8</td>
<td>6.5</td>
<td>5.5</td>
<td></td>
</tr>
<tr>
<td>Dielectric constant</td>
<td>* 9.5</td>
<td>3.8</td>
<td>2.7</td>
<td></td>
</tr>
<tr>
<td>Resistance (mOhms/mm)</td>
<td>* 40</td>
<td>150</td>
<td>300</td>
<td>38</td>
</tr>
<tr>
<td>Inductance (nH/mm)</td>
<td>* 0.52</td>
<td>0.38</td>
<td>0.44</td>
<td>0.29</td>
</tr>
<tr>
<td>Capacitance (pF/mm)</td>
<td>* 0.27</td>
<td>0.28</td>
<td>0.24</td>
<td>0.15</td>
</tr>
<tr>
<td>Coupling Coef.</td>
<td>Kc=0.122</td>
<td>0.135</td>
<td>0.32</td>
<td>0.058</td>
</tr>
<tr>
<td></td>
<td>Ki=0.124</td>
<td>0.140</td>
<td>0.31</td>
<td>0.058</td>
</tr>
<tr>
<td>X-Talk (Vne@1V/ns)</td>
<td>4.8</td>
<td>3.6</td>
<td>7.08</td>
<td>0.78</td>
</tr>
<tr>
<td>X-Talk (Vne-sat-mV/V)</td>
<td>203.4</td>
<td>152.5</td>
<td>300</td>
<td>60.3</td>
</tr>
<tr>
<td>V-G Loop Inductance (pH)</td>
<td>30 agr:22</td>
<td>55</td>
<td>6 - 9</td>
<td></td>
</tr>
<tr>
<td>Loss Factor</td>
<td>0.0005</td>
<td>0.03</td>
<td>0.003</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Alumina, HyperBga F=10GHz Build-up F=1MHz</td>
</tr>
</tbody>
</table>

Notes: * measured values; Loop inductance: Entire package, all C4 pads and BGA’s commoned. The above electrical characteristics are typical of each product. Variations of these parameters can be achieved for a specific design.
PTFE® Electrical Performance

HyperBGA High Speed Data Rate
Time Domain Analysis
Differential Mode Eye Diagram

- Package Deterministic Jitter
  - < 1ps p-p
# PTFE Module Reliability Performance

<table>
<thead>
<tr>
<th>Test</th>
<th>Format</th>
<th>Test Duration</th>
<th>Status</th>
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</thead>
<tbody>
<tr>
<td>Preconditioning - JEDEC Level 3</td>
<td>Component</td>
<td>96 hours</td>
<td>N/A</td>
</tr>
<tr>
<td>Board Level Thermal Cycle (0 / 100°C)</td>
<td>On board w/heat sink*</td>
<td>3600 cycles</td>
<td>Pass</td>
</tr>
<tr>
<td>Board Level Thermal Cycle (0 / 100°C)</td>
<td>On board w/lid</td>
<td>3600 cycles</td>
<td>10K Pass</td>
</tr>
<tr>
<td>Power Cycling (25 / 125°C)</td>
<td>On board</td>
<td>3600 cycles</td>
<td>Pass</td>
</tr>
<tr>
<td>DeepThermal Cycling (-55 / +125°C)</td>
<td>Component</td>
<td>1000 cycles</td>
<td>Pass</td>
</tr>
<tr>
<td>Wet Thermal Shock (-40 / +125°C)</td>
<td>Component</td>
<td>100 cycles</td>
<td>Pass</td>
</tr>
<tr>
<td>TH &amp; B (85°C / 85%RH / 3.7V)</td>
<td>On board</td>
<td>1000 hours</td>
<td>Pass</td>
</tr>
<tr>
<td>HAST (110°C / 85%RH / 3.7V)</td>
<td>On board</td>
<td>264 hours</td>
<td>Pass</td>
</tr>
<tr>
<td>Pressure Pot (121°C / 100%RH / 2atm)</td>
<td>Component</td>
<td>96 hours</td>
<td>Pass</td>
</tr>
<tr>
<td>High Temp. Storage (150°C)</td>
<td>Component</td>
<td>1000 hours</td>
<td>Pass</td>
</tr>
<tr>
<td>Low Temp. Storage (-65°C)</td>
<td>Component</td>
<td>1000 hours</td>
<td>Pass</td>
</tr>
<tr>
<td>Shock/Vibration JEDEC</td>
<td>Component</td>
<td>various</td>
<td>Pass</td>
</tr>
</tbody>
</table>

*Component w/ adhesively attached 200 gm Heat Sink on 9x10 inch card*
HDI - CoreEZ® Overview
Current Product Offering

Current Description

- 4 layer, thin core (200 μm)
- 50 μm UV laser drilled vias
- 199 μm core pitch
- Up to 4 buildup layers
- Typical Cross sections: 1-4-1, 2-4-2, 3-4-3, 4-4-4
  - Stacked buildup vias
  - 35 & 50 μm buildup thickness
  - 150 μm die pad pitch capable
Typical CoreEZ® 10 Layer Cross-Section

- 3-4-3 Stack up (10 copper layers)
- Substrate thickness 0.7 mm
8 Layer X-Section Comparison

CoreEZ® 2-4-2

Standard Build-up 3-2-3

Photographs are at same magnification

- Both packages use 50um blind vias
- CoreEZ® core vias are 4x smaller
- Enhanced high speed electrical performance
HDI With High Core Via Density

- Dense Package Interconnect
  - Dense Core Via Pitch
- Dual Side Component Mounting
- Fine Line Width and Spacing
- Enhanced Z-axis connectivity

Thin Core, SiP  50 um via
Standard Build-Up  500 um via

~9X Core Via Density
CoreEZ™ is available as a 1-4-1, 2-4-2, 3-4-3 or 4-4-4 cross sections

- 1-4-1 = 2 full stripline signal planes, 4 pwr/gnd
- 2-4-2 = 4 dual stripline signal planes, 4 pwr/gnd
- 3-4-3 = 4 full stripline signal planes, 6 power/gnd
- 4-4-4 = 4 full stripline signal planes, 8 pwr/gnd
Embedded Passives in CoreEZ®

- Resistors
  - Thin film resistor material
    - Ticer TCR®
    - 10 - 250 ohms per square
  - Resistor values from 5 ohm to 50 Kohm
  - Resistor tolerances from 2 – 20%
    - Laser trimming 2 – 5%
  - Typical resistor areas
    - 0.2 – 15 mm²
  - Block or Serpentine designs

Eight layer core 285 nF / in²
High Speed SERDES in CoreEZ® Simulation at 12.5 Gbps

- Similar electrical performance as PTFE
  - Within 10% of PTFE jitter performance
Liquid Crystal Polymer (LCP)
Why LCP?

- Is “near” hermetic
  - Low moisture absorption: 0.04%
- Halogen Free (lead free assembly being evaluated)
- Similar in electrical performance to PTFE
  - Low Loss
    - $D_k = 2.9$
    - $D_f = 0.0025$
- Very Lightweight
  - 1.4gm/cm$^3$
- Thermoplastic
- Thin and thick layer combinations in cross sections
  - 25um, 50 um and 100 um thickness
- Capable of Radiation Hardened applications

- Rogers ULTRALAM 3850, 3908
- Nippon Steel Espanex L
4-Layer LCP x-sections:

- 50 micron laser thru vias
- 50 micron buried vias
- 50 micron thick LCP
- 100 micron thick LCP
- 37.5 micron LW & Space
- Staggered Blind Vias
- Rogers Ultralam 3850, 3908
Integrated Circuit Assembly Needs
First level Assembly Overview

Electronic packaging development, fabrication and advanced assembly of complex flip chip and wire bond packages

Key differentiators:
- Flip Chip, Wirebonding and SMT on one package
- BGA balling
- Lead-free assembly
- 01005 component placement and assembly
- Alternative pad finishes
- Teradyne Ultra FLEX
  VLSI platform functional testing
- Leading edge process development
Wire Bond Expertise......

- Die-up and cavity
- Ball bonding 25 micron diameter Au wire to 125 micron pitch
- Pitches down to 57µm on 700+ wire package
- Production qualified for military applications
- Die attach: sizes to 16mm square
- Ribbon bonding packages and cards to 12”
- Al ribbon bonding available
- Coplanarity measurements
- Damming and glob top
Flip Chip Assembly Needs

- Flip Chip Expertise
  - SiGe, Si, GaAs die attach
  - Hi melt, eutectic, Sn cap C4, Pb-free
  - Low alpha Sn/Pb solder
  - High I/O Flip Chip join down to 150µm pitch
  - Die sizes placed to 25mm x 26mm
  - Flux chemistries/dispensing
  - Various low & high modulus underfills
  - BGA attach down to 0.5mm pitch (eutectic, Pb-free)
  - PGA attach
  - Thermal adhesive
  - Heat spreader, heat sink & lid attach
  - 100µm pitch solder dispense
  - Solder volume measurements
  - CSAM acoustic imaging inspection
  - X-ray inspection
  - Part labeling/marking: traceability
Assembly Engineering Support

Support Operations

- Pre/post assembly coplanarity measurement
- Acoustic microscopy for interfacial inspection
- Real time X-ray for process monitors
- Ionic cleanliness measurements
- Wire pull and ball shear
- Solder repair/rework
- Cross section support failure analysis
- Traceability to the component level
- Fixturing and process development

AIR-VAC Hot Air Rework Tool

- Can rework leaded, lead free, and high melt BGA’s, Micro BGA’s, and flip chip die.
System in Package Application Examples
Extreme SiP Miniturization example

Original PCB 620 mm²

- Package Size
  - 30 mm diameter, 391 total components
- 39 different part numbers, 231 components on 2 surfaces
- 5 Bare Die
  - Flip Chip FPGA, 15.95mm x 10.23mm, 2,440 I/O
  - Flip Chip DSP, 4.68mm x 5.134mm, 225 um pitch, 261 I/O
  - Flip Chip Supply monitor, pitch = 114 um, 16 I/O
  - Flip Chip DRAM, pitch = 121 um, 86 i/o
  - Flip Chip Flash memory, pitch = 116 um, 77 I/O
- 178 SMT Capacitors, 14 SMT resistors
- 152 buried resistors imbedded in substrate
- 1 SMT circular connector
- > 100 produced

SiP CoreEZ™ 30 mm²
Intravascular Ultrasound Catheter Sensor Package

- Flip Chip Ultrasound Transducer for Catheter sensor assembly rolled to 1.175mm diameter
- 5 Flip Chip ASIC, .1mm thick, 31 I/O, 2.5mm x .5mm
  - 22 micron flip chip bumps on 70 micron die pad pitch
- 1 PZT crystal
- 12.5mm by 6.5 mm single layer flex circuit
  - 14 micron wide lines and space copper circuitry
  - 12.5 thick polyimide dielectric
- Prototype to production
  - Over 320,000 modules shipped

Single layer HDI Flex
Flip Chip Bumps
Transducer
ASIC Die

7 mm
Low Level Gamma Photon Detector Module

9 layer HyperBGA PTFE Substrate
- Bottom side CZT Crystal
- Passives on mini card
- S. Steel Stiffener
- Top side Wirebonded ASIC
- 50 micron UV laser drilled vias
- 25 micron trace
- 33 micron space

Hyper Substrate X-Section
Enable System Miniaturization using SiP: Bare die, HDI Substrate Materials, Assembly Technology & Manufacturing

- Combining advanced flip chip & wirebond with maximum HDI plastic substrates

- Deliver maximum reliability and electrical performance for RF and High Bandwidth Digital

- System Level Shrink for SWaP
  - PWB redesigns into fully integrated System in Package
  - 24X system size reductions have been realized
  - Lower cost next level assemblies (lower layer count PWB’s)

Deliver the industry’s smallest packages combined with superior package reliability and robust electrical performance!
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