Laminate Based System in Package (SiP) Utilizing High Density Interconnect (HDI) Substrates in High Reliability Applications

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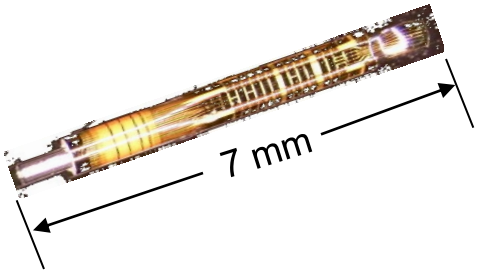
What is SiP?....An Integrated Solution

- System in Package (SiP) delivers 10-20X reductions from current designs
- Up to 90% weight reductions
- Significantly lower power and improved electrical performance
- Hi-Reliability, Hi-Quality, Hi-Performance
- Remove layers of interconnect
- Addresses growing demand in:
  - Unmanned systems
  - Radar
  - Space satellites
  - Electronic Warfare
  - Medical Applications
  - Research Applications
- The magic dust:
  - Bare die
  - HDI substrates



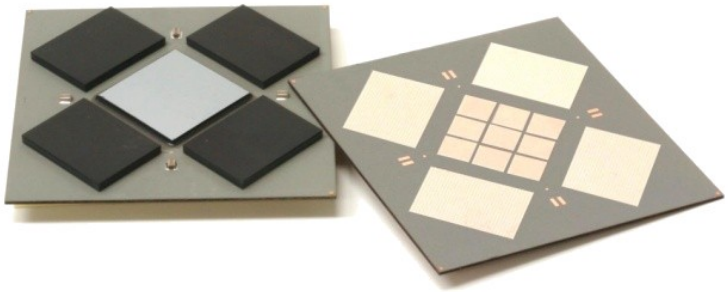
620mm^2 PWB reduced to 30mm^2

System in Package Overview

- Typically multiple bare die and SMT components on a HDI microelectronics substrate:
  - Large and Small Bare Die placement & attach
    - Flip chip die connections
    - Wirebond die connection
    - Dual sided attach
    - Component substitution
  - SMT placement & attach
    - Down to 0201's, 01005's
    - CSP's, SOIC's, PLCC's, SOJ's
  - Connections to next level assembly
    - SMT pinned connectors
    - Ball Grid Array
  - High Density Interconnect Substrates: the secret sauce !
    - Laser drilled through and microvias
    - 25 micron trace width and space
    - Thin, low loss, low dielectric constant materials

System in Package Overview

- Package Size
  - Standard JEDEC 13.0mm to 55.0mm
  - Custom size and shape SiPs
- Assembly to Organic Substrates
  - FR4 and BT epoxy
  - Particle filed epoxy build-up
  - PTFE dielectric
  - Kapton flex
  - Polyimide
  - LCP



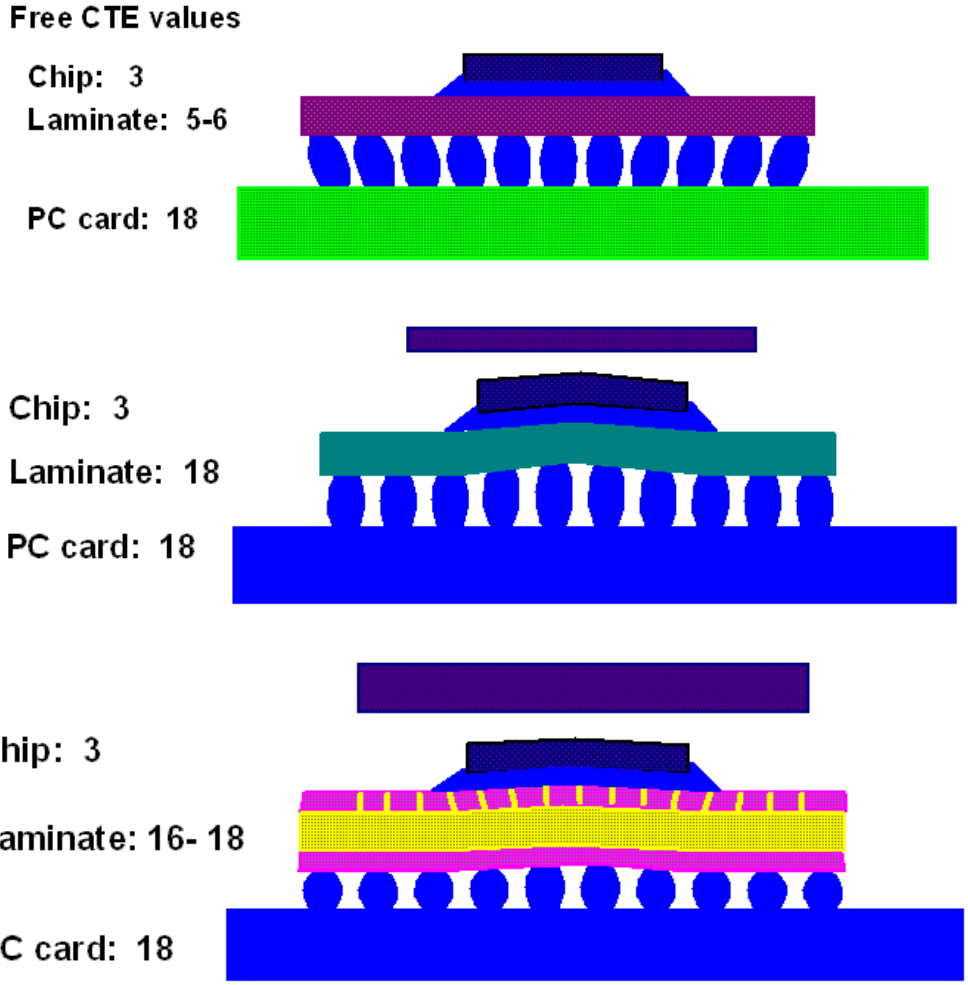
- Common Product Parametrics
  - Large MCM/SiP packages
  - Hybrid/double-sided assembly
  - Single chip module and device packages
- Test
  - Shorts-opens
  - JTAG/boundary scan
  - Full functional test

System-in-Package Conversion

- Where we begin:
  - Technical contact at the customer
  - Si design: Bare die availability
  - Preliminary BOM Analysis
    - Input
      - Bill of Materials & Approved Vendor List
    - Output
      - Smaller package & bare die recommendations
  - Preliminary Area Study
    - Input
      - Board design file & Electrical restraints
    - Output
      - initial conversion of PCB to substrate
        - » cross section, dielectric and size estimates
      - Initial assembly layout
  - Substrate design and assembly layout
    - Electrical, thermal and mechanical analysis

Design Tools and Modeling

Overview of Package Behaviors



- **Ceramic**
  Finite BGA fatigue life
  Very little warpage
  No internal packaging issues

- **Direct chip attach to organic**
  Control of warpage, adhesive strength
  Smaller chips
  Coverplate to balance stresses

- **Build-up technology**
  Use of somewhat compliant outer layer
  Outer layer electricals less desireable
  Outer layer strains substantial

Laminate vs. Ceramic Reliability Comparisons

45mm body size

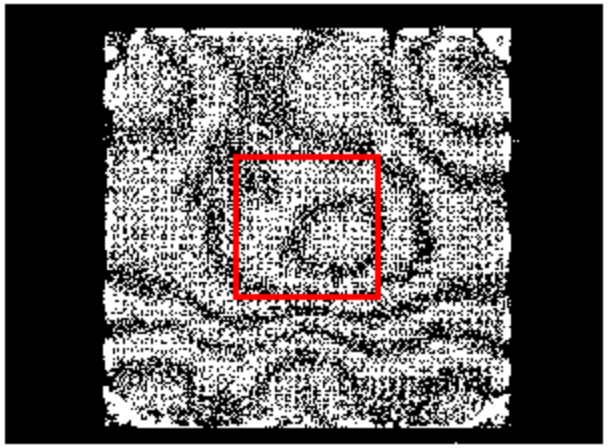
Product	Material	Typical Substrate Thickness	Dielectric Constant	Loss Tangent	Component Level Reliability -55 to 125°C	Board Level Reliability 0-100°C
HTCC (solder columns)	Glass Ceramic 11	1.0 mm	8.1	.0034	1000 cycles	2,200 cycles to 1st fail
HyperBGA®	PTFE	0.47 mm	2.7	.003 (49% silica filled)	1000 cycles	10,000 cycles to no
CoreEZ™	Epoxy/P-Aramid Fiber Core and particle filled Epoxy build up	0.526 mm (8 layer)	3.5	.022	1000 cycles	5,000 cycles to 1st fail

Plastic solutions offer:

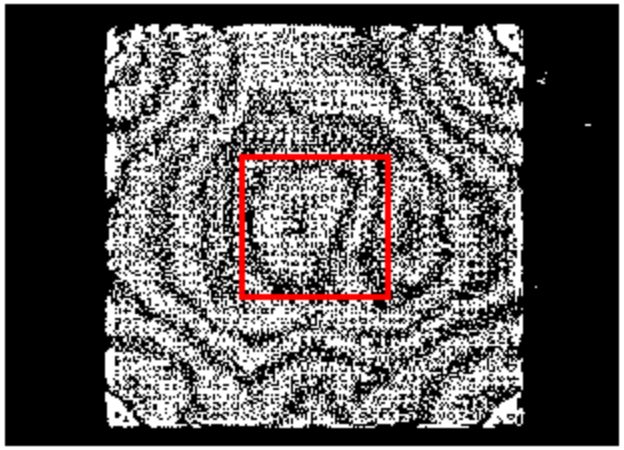
- ✓High electrical performance
- ✓High reliability performance
- ✓Weight reduction
- ✓Smaller x, y, z form factor

PTFE Substrate Chip Joining

Measured flatness of 42.5mm laminate + stiffener subassembly example
Viewed from BGA side: Moiré topographic fringe contours at 8.33 microns / fringe



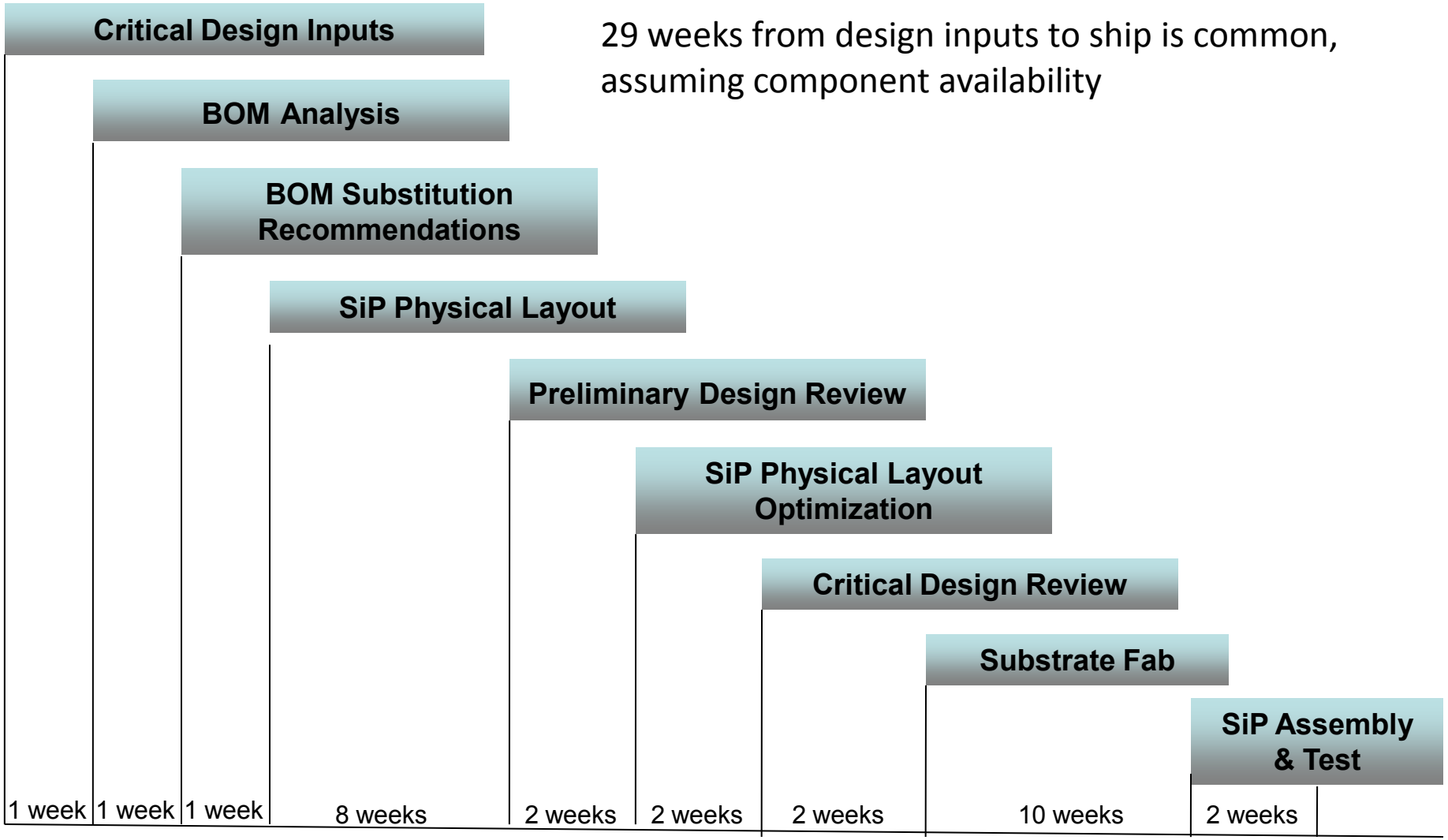
Room temperature, 20C



Reflow temperature, 183C

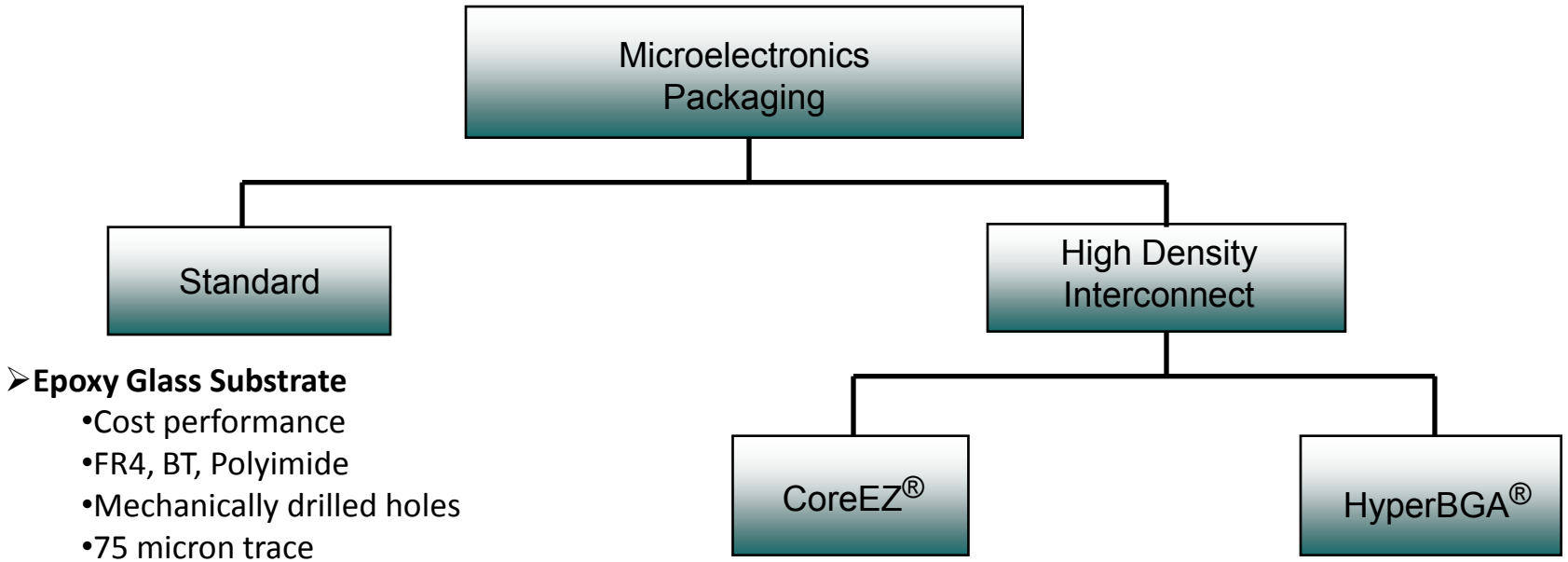
14.7 mm size chip bump region (in red) remained flat to within 17 microns

Typical PWB to SiP Prototype Cycle



29 weeks from design inputs to ship is common, assuming component availability

HDI Microelectronics Packaging Menu



➢ **Epoxy Glass Substrate**
- •Cost performance
- •FR4, BT, Polyimide
- •Mechanically drilled holes
- •75 micron trace
- •75 micron spaces
- •Flip chip, Wirebond, SMT
- •Radiation Hard Capable

➢ **Thin Core Build Up**
- •Cost performance
- •Particle filled epoxy
- •Thin core (coreless)
- •Laser drilled core
- •Laser drilled build up
- •25 micron trace
- •25 micron space
- •Buried resistors
- •Flip chip, Wirebond, SMT
- •Radiation Hard Capable

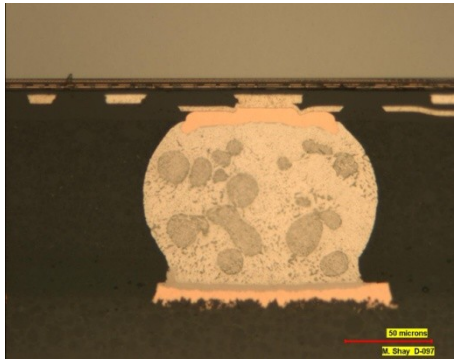
➢ **PTFE Substrate**
- •High Bandwidth/RF
- •Particle filled material
- •Coreless
- •Laser Drilled Vias
- •Fusion Bonding
- •25 micron trace
- •33 micron space
- •Flip chip, Wirebond, SMT
- •Radiation Tolerant

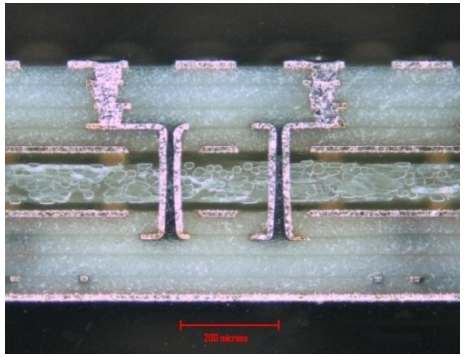
Packaging Attributes applied to SiP conversions

Substrate features and advanced IC Assembly techniques enable bare die implementation

Attribute	Standard PCB	HDI Substrate	Shrink opportunity
Through via	Mechanical	Laser	
Through via dia.	200 microns	50 microns	4X
Through via capture pad diameter	400 microns	100 microns	4X
Line Width	75 microns	25 microns	3X
Space Width	75 microns	25 microns	3X
Semiconductors	Packaged	Bare die or small package	4X to 10X

Flip Chip Bump





3-4-3 CoreEZ®

2011 Product Attribute Comparisons

Attribute	**Standard** (Epoxy Glass or Polyimide)	**HDI: Dense** (Particle Filled Epoxy)	**HDI: LCP** (liquid crystal polymer)	**HDI: PTFE** (PTFE)
Line width	75 microns	**25 microns**	**37.5 microns**	**25 microns**
Line space	75 microns	**25 microns**	**37.5 microns**	**33 microns**
Via type	mechanical	**laser**	**Laser**	**laser**
Via diameter	200 microns	**50 microns**	**50 microns**	**50 microns**
Stacked vias	Build up only	**Build up only**	In 2010	In 2010
Capture pad diameter	400 microns	**100 microns**	110 microns	110 microns
Surface finish	E-less Ni / I Au, ENEPIG	Same	Same	Same
Solder mask	yes	yes	yes	no
Thickness	<1mm	**0.4 - .7mm**	**0.5mm**	**0.5mm**
Layers	10	12	4, 6 in 1st article	11

2011 Product Attribute Comparisons

Attribute	**Standard** **(Epoxy Glass or Polyimide)**	**HDI: Dense BU** **(Particle Filled Epoxy)**	**HDI: LCP** **(liquid crystal polymer)**	**HDI: PTFE** **(PTFE)**
PCB Attach	Pin Grid, BGA, LGA, Custom	Pin Grid, BGA, LGA, Custom	Pin Grid, BGA, LGA, Custom	Pin Grid, BGA, LGA, Custom
Die attach	Wirebondable, Flip Chip <14mm, SMT	Wirebondable, Flip Chip <14mm, SMT	Wirebondable, Flip Chip <14mm, SMT	Wirebondable, Flip Chip 14mm, SMT
Flexible	Rigid Flex	HDI Rigid Flex	**Flex**	**Flex**
Formable	No	No	**Yes**	no
Radiation Level	**Strategic Rad Hard**	**Strategic Rad Hard**	**Strategic Rad Hard**	Rad Tolerant
Embedded Passives	**Yes**	**Yes**	**Yes**	No
FC Component level reliability (-55 to 125°C)	1000 cycles	1000 cycles	1000 cycles	1000 cycles
FC Board level reliability (0 to 100°C)	2,000 cycles	5,000 cycles	In testing	**10,000 cycles**
Composite CTE	19ppm	18ppm	17ppm (X&Y)	12ppm
Er	4.1	3.7	**2.9**	**2.7**
Loss Tan	.011	.016	**.0025**	**.003**

Physical Design content

- Physical Design Implementation
  - Component Placement & Routing
  - Physical & formal verification
  - Signal Integrity (SI) & Crosstalk analysis
  - Static Timing Analysis (STA)
  - Multiple Supply Voltage (MSV)
  - Leakage Current Reduction Techniques
  - Clock & Supply Voltage Gating
  - Power Optimization
  - Design for Test to ensure testability
  - Design for Manufacturability to maximize production yields

Signal and Power Integrity
Potential Work Items and Design Flow

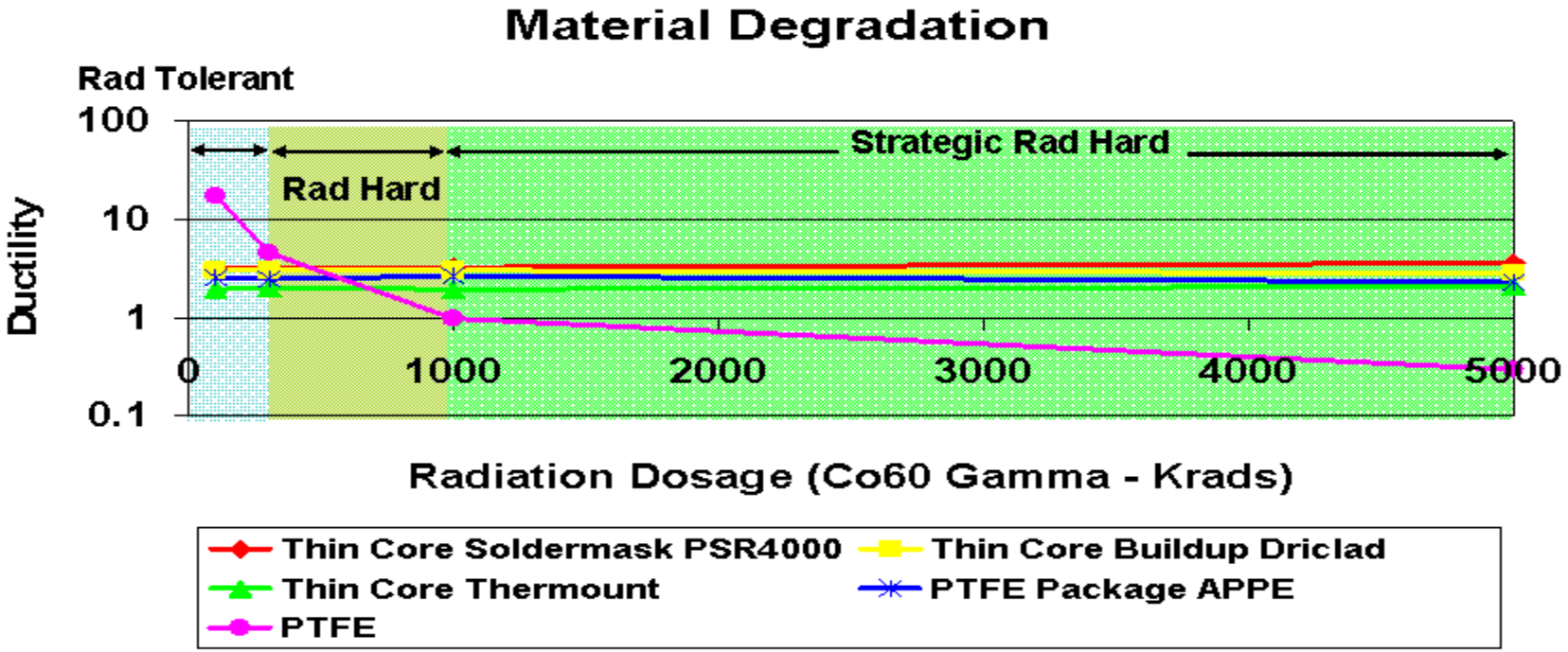
- **Typical Signal Integrity Workflow** (varies by application)
  - Customer defines SI specifications in the form of routing constraints by net such as:
    - Z0 (SE, DP), Skew (Group / reference), Crosstalk / Isolation (dB @ Freq), Rdc, Insertion / Return loss (dB @ Freq), etc.
  - EIT ensures that these specifications are met as follows:
    - Pre-layout Design Guidelines:
      - Define stackup, function by layer, recommended component placement
      - Define trace width (and spacing for DP) for Z0 requirements
      - Translate electrical Skew requirements into physical lengths
      - Define spacing and coupled length limitations for crosstalk control
      - Define trace geometries to meet loss specification
    - Post-layout Verification:
      - Extract parameters from design database using Ansoft toolset
      - HFSS, Q3D, SIWave

HDI Substrate Materials Analysis

Evaluation of Materials Subjected to Various Radiation Levels

- Evaluated PTFE BGA (HyperBGA®) and Thin Core (CoreEZ ®) materials radiation response
  - Radiation Exposure: Co60 Gamma:
    - Control
    - 32, 50, 100, 300, 500, 700, 1000 and 5000 krad TID
  - PTFE Materials evaluated: Rogers 2800, PPE
    - Results: Many applications will be unaffected by radiation
      - PPE has no measurable degradation to 5 Mrad
      - RO2800 shows gradual loss of ductility with exposure
  - Thin Core Build Up Materials Considered: Thermount 55LM, Particle Filled Driclad Epoxy, PSR4000
    - Results: No measurable change of mechanical properties through 5 Mrad

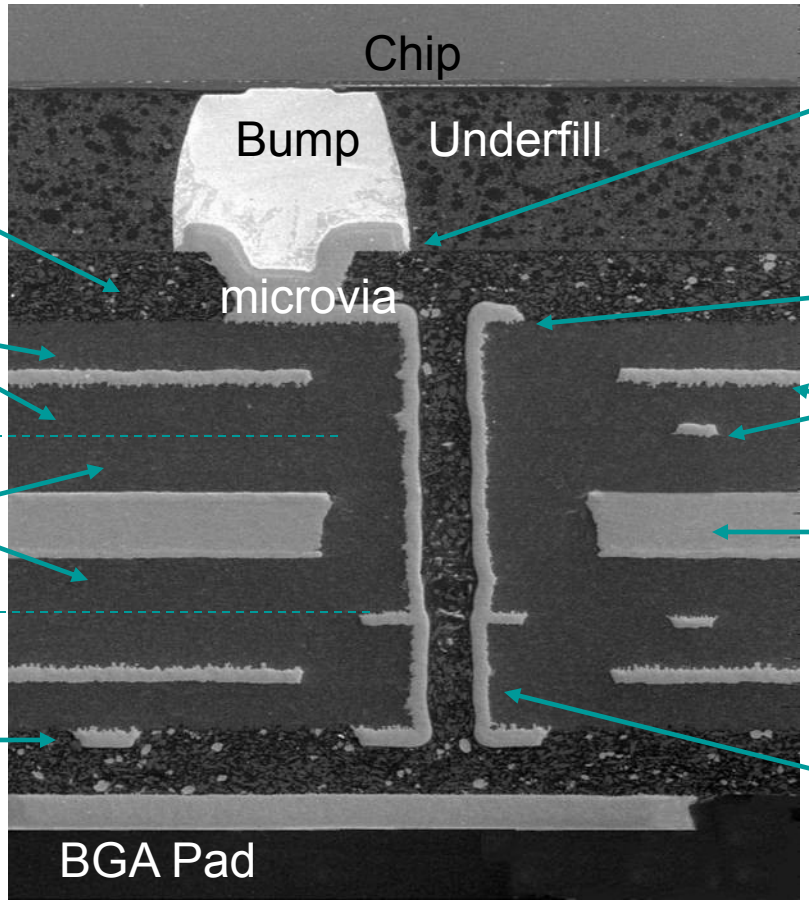
Packaging performance after radiation exposure



- Ductility performance indicates package performance in thermal cycling
  - Thin Core Build Up appears to be a good choice for Rad Hard and Strategic apps.
    - materials show no ductility degradation with radiation level
  - PTFE appears to be best suited for Rad Tolerant applications
    - PTFE ductility is higher then all other materials below 300K rad exposure
    - PTFE predictably degrades significantly above 300Krad exposure levels

HDI Laminate Substrate Technologies

Typical PTFE® 9 Layer Cross Section



40 micron thick APPE outer dielectric Er = 3.2

35 micron thick PTFE Dielectric, Er = 2.7

50 micron thick PTFE Dielectric, Er = 2.7

15μ thick Cu, redistribution

Non soldermask defined pad

15μ thick Cu, redistribution

12μ thick Cu

6μ Cu/38μ Invar/6μ Cu Ground plane

12μ thick Cu, 50m dia. through via APPE filled

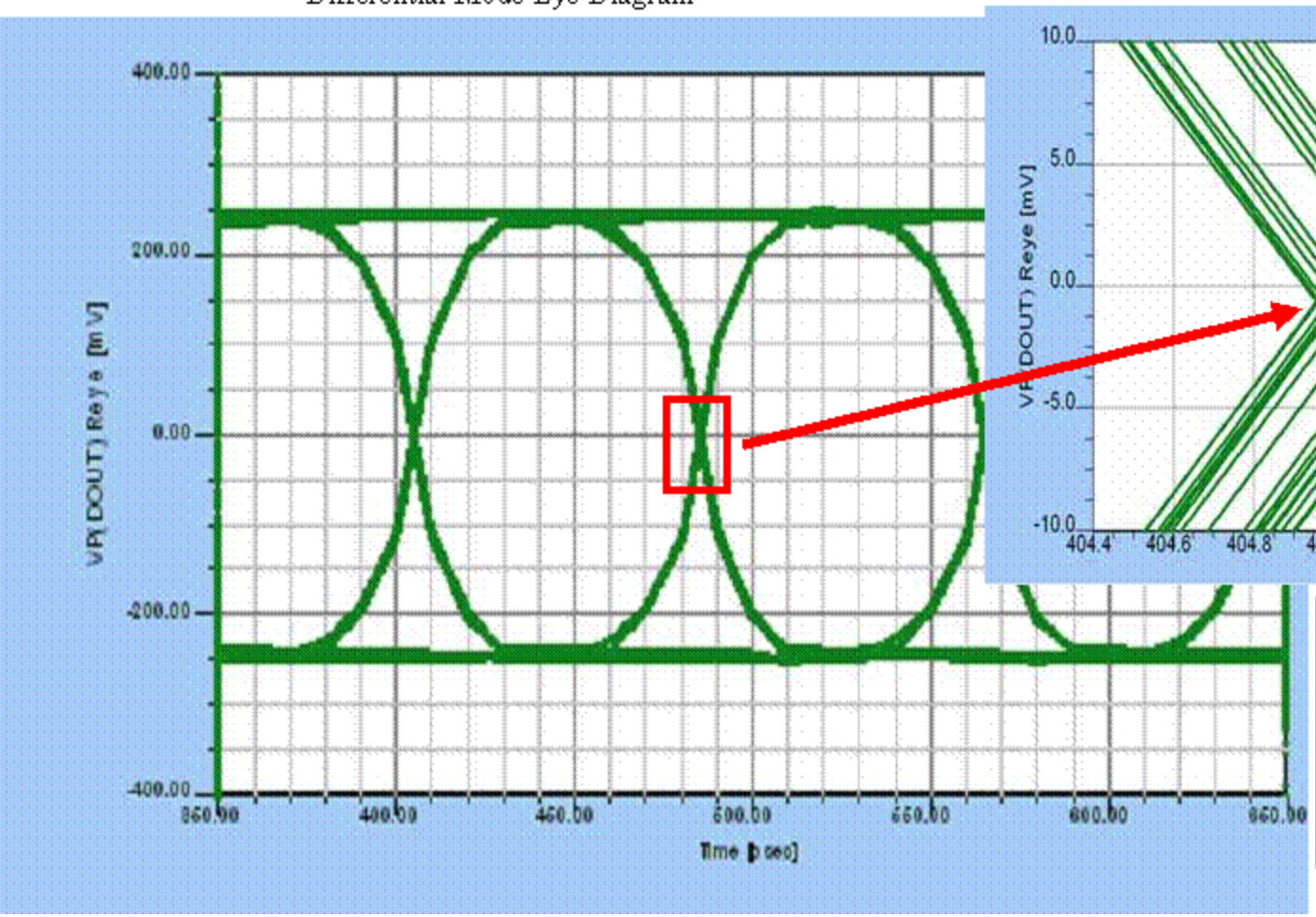
Packaging Electrical Comparisons

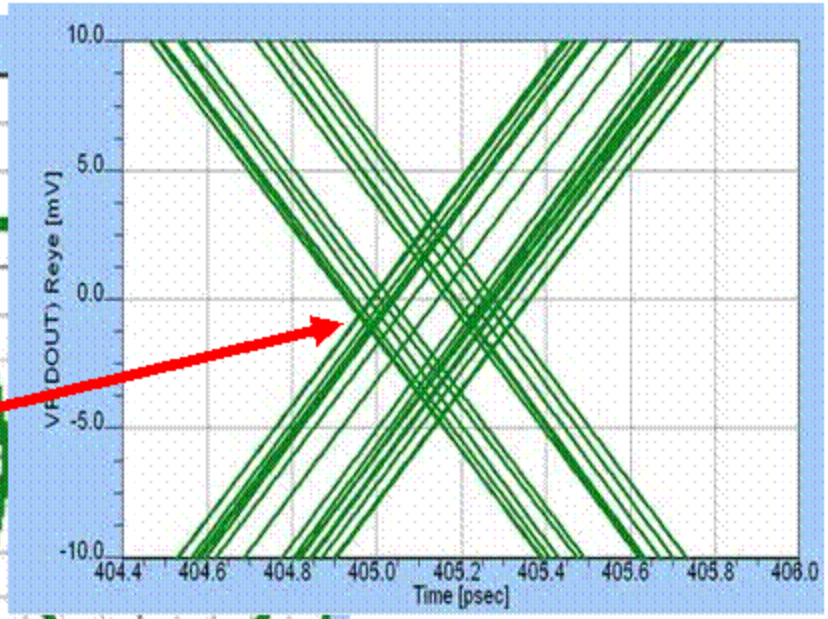
Property	CBGA Alumina			Build-up 3+3	HyperBGA™			Comments
Line width/pitch (um)	90/225	50/150	38/94	40/100	28/61	40/77	40/115	HyperBGA : die,transition,open area Alumina: Regular,AGR
Zo (Ohms)	35-60			45-75	55-64			
Time Delay (ps/mm)	* 11.8			6.5	5.5			
Dielectric constant	* 9.5			3.8	2.7			
Resistance (mOhms/mm)	* 40	150	300	38	76	52	52	
Inductance (nH/mm)	* 0.52	0.38	0.44	0.29	0.35	0.30	0.30	* calculation from meseared values (Time delay and C)
Capacitance (pF/mm)	* 0.27	0.28	0.24	0.15	0.09	0.1	0.1	
Coupling Coef. Kc Kl	 0.122 0.124	 0.135 0.140	 0.32 0.31	 0.058 0.058	 0.16 0.16	 0.12 0.12	 0.04 0.04	based on 2 adjacent lines Kc=C12/C11 Kl=L12/L11
X-Talk (Vne mV/mm@1V/ns)	4.8	3.6	7.08	0.78	1.89	1.42	0.4	based on AAQAA configuration 5 adjacent line, center line quiet
X-Talk (Vne-sat -mV/V)	203.4	152.5	300	60.3	172.5	129.5	35.2	based on AAQAA configuration 5 adjacent line, center line quiet
V-G Loop Inductance (pH)	30 agr:22			55	6 - 9			MLC=42.5mm chip=13.3mm HyperBGA=42.5 chip=14.3mm SLC=33mm,10.09mm chip
Loss Factor	0.0005			0.03	0.003			Alumina,Hyperbga F=10GHz Build-up F=1MHz

Notes: * measured values ; Loop inductance: Entire package , all C4 pads and BGA's commoned. The above electrical characteristics are typical of each product. Variations of these parameters can be achieved for a specific design.

PTFE® Electrical Performance

HyperBGA High Speed Data Rate
Time Domain Analysis
Differential Mode Eye Diagram



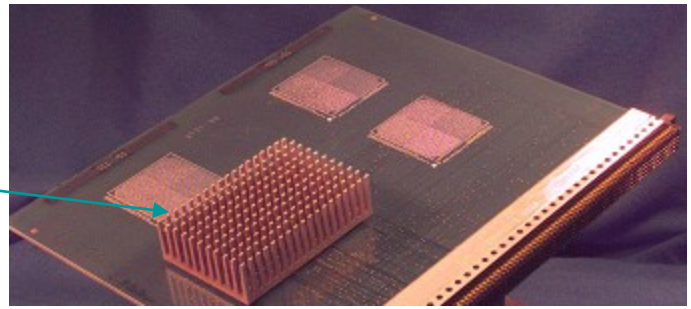


- Package Deterministic Jitter
  - < 1ps p-p

PTFE Module Reliability Performance

Test	Format	Test Duration	Status
Preconditioning - JEDEC Level 3	Component	96 hours	N/A
Board Level Thermal Cycle (0 / 100°C)	On board w/heat sink*	3600 cycles	Pass
Board Level Thermal Cycle (0 / 100°C)	On board w/lid	3600 cycles	10K Pass
Power Cycling (25 / 125°C)	On board	3600 cycles	Pass
DeepThermal Cycling (-55 / +125°C)	Component	1000 cycles	Pass
Wet Thermal Shock (-40 / +125°C)	Component	100 cycles	Pass
TH & B (85°C / 85%RH / 3.7V)	On board	1000 hours	Pass
HAST (110°C / 85%RH / 3.7V)	On board	264 hours	Pass
Pressure Pot (121°C / 100%RH / 2atm)	Component	96 hours	Pass
High Temp. Storage (150°C)	Component	1000 hours	Pass
Low Temp. Storage (-65°C)	Component	1000 hours	Pass
Shock/Vibration JEDEC	Component	various	Pass

*Component w/ adhesively attached
200 gm Heat Sink on 9x10 inch card

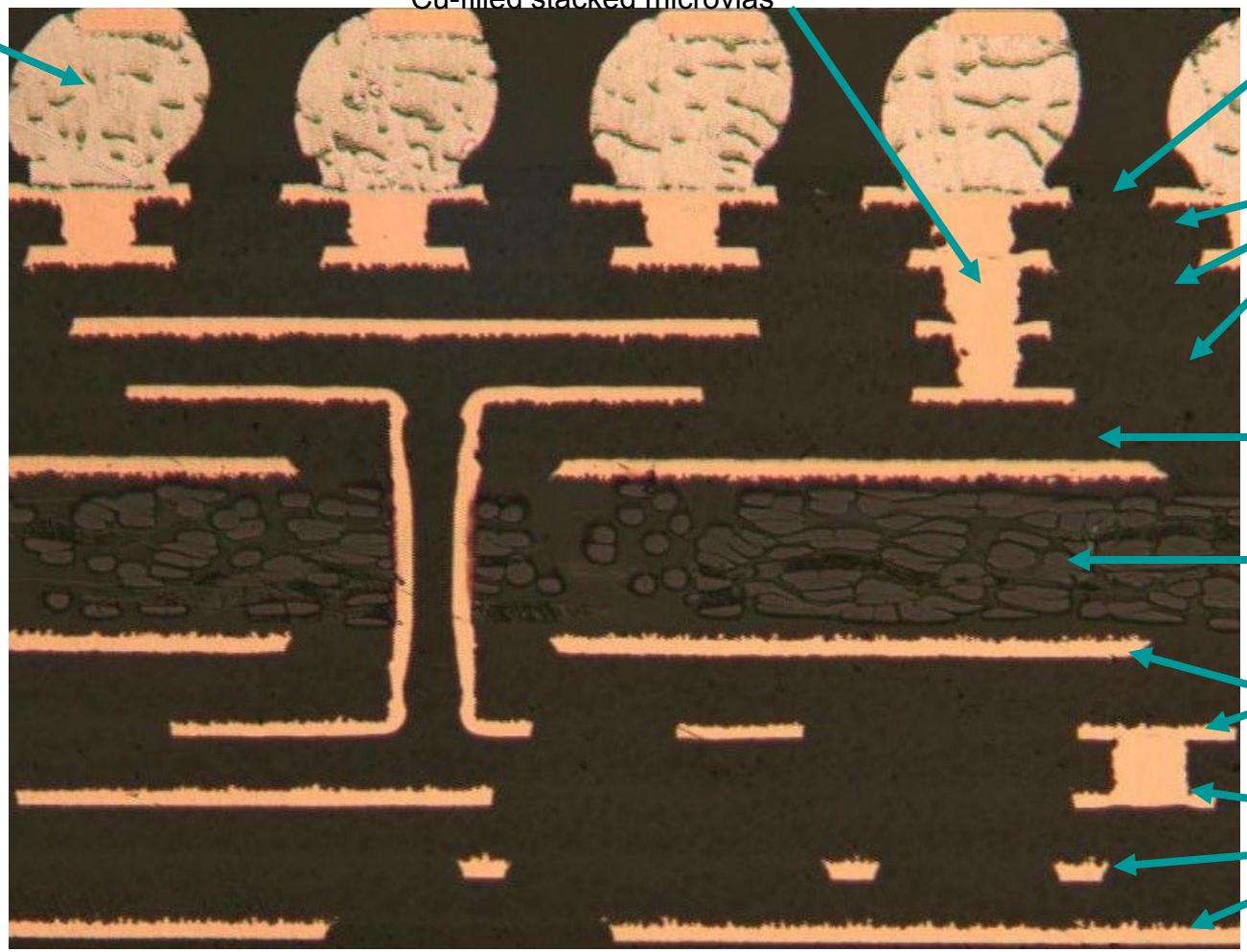


HDI - CoreEZ® Overview

Current Product Offering

- **Current Description**
  - 4 layer, thin core (200 µm)
  - 50 µm UV laser drilled vias
  - 199 µm core pitch
  - Up to 4 buildup layers
  - Typical Cross sections: 1-4-1, 2-4-2, 3-4-3, 4-4-4
    - Stacked buildup vias
    - 35 & 50 µm buildup thickness
    - 150 µm die pad pitch capable

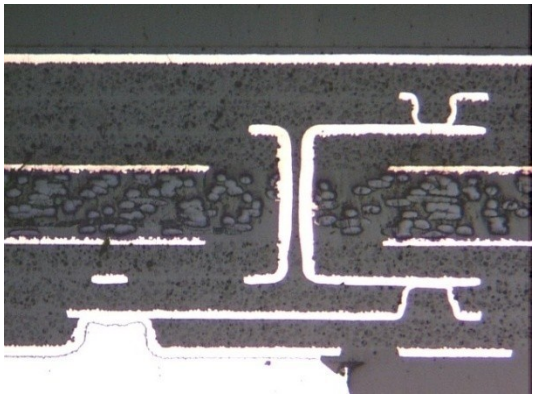
Typical CoreEZ® 10 Layer Cross-Section



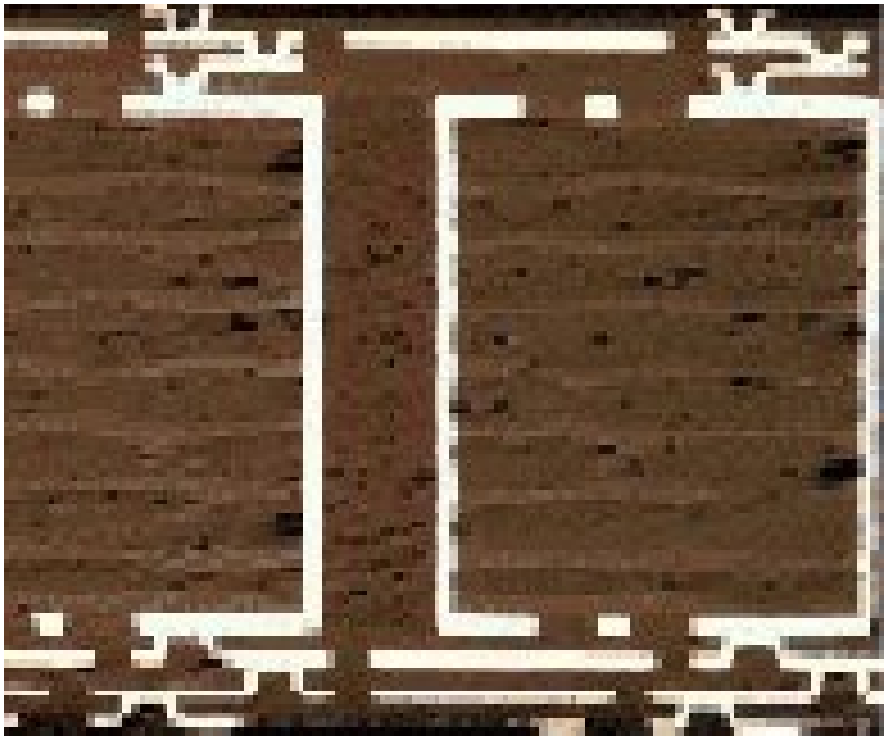
- 3-4-3 Stack up (10 copper layers)
- Substrate thickness 0.7 mm

8 Layer X-Section Comparison

CoreEZ® 2-4-2



Standard Build-up 3-2-3



Photographs are at
same magnification

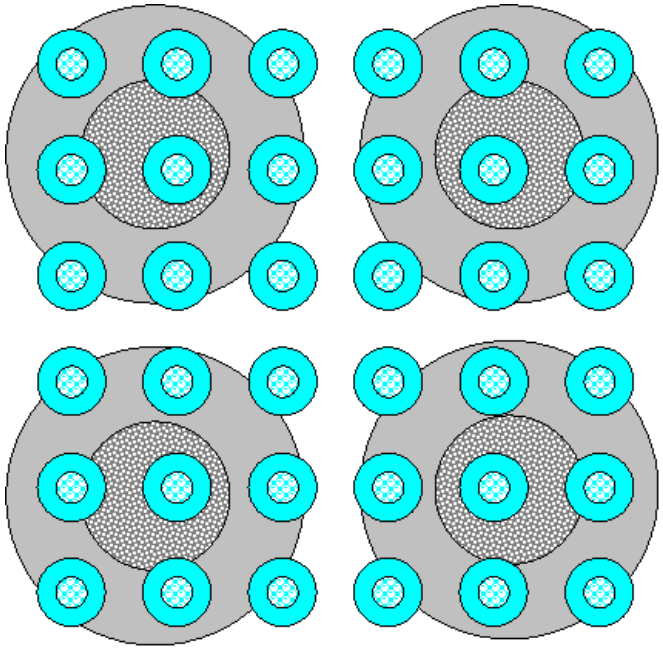
- Both packages use 50um blind vias
- CoreEZ® core vias are 4x smaller
- Enhanced high speed electrical performance

HDI With High Core Via Density

- Dense Package Interconnect
  - Dense Core Via Pitch
- Dual Side Component Mounting
- Fine Line Width and Spacing
- Enhanced Z-axis connectivity

Thin Core, SiP 50 um via

Standard Build-Up 500 um via

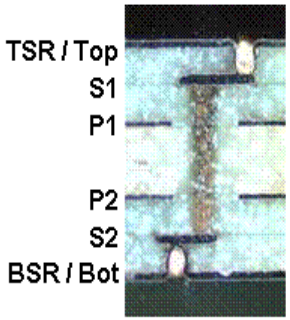


~9X Core Via Density

CoreEZ™ Typical X-Sections

CoreEZ™ is available as a 1-4-1, 2-4-2 , 3-4-3 or 4-4-4 cross sections

- 1-4-1 = 2 full stripline signal planes, 4 pwr/gnd
- 2-4-2 = 4 dual stripline signal planes, 4 pwr/gnd
- 3-4-3 = 4 full stripline signal planes, 8 pwr/gnd



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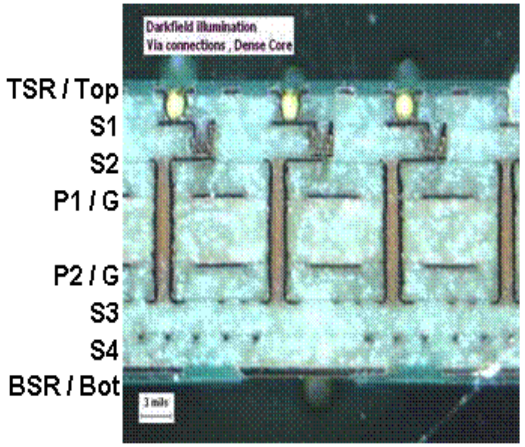
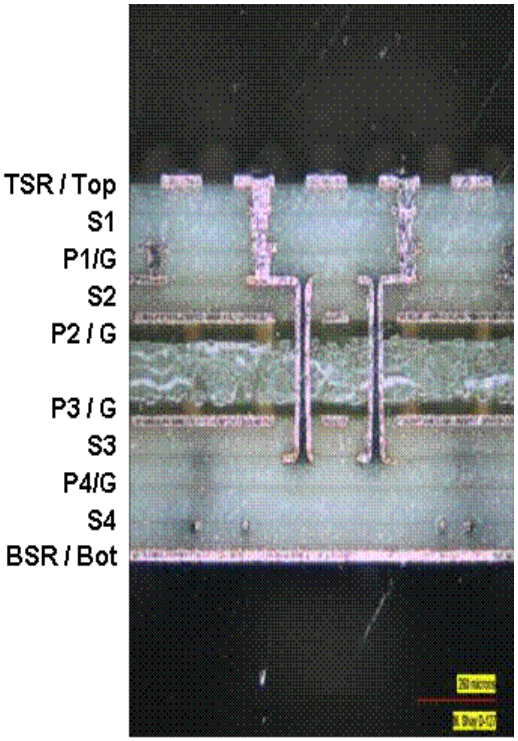
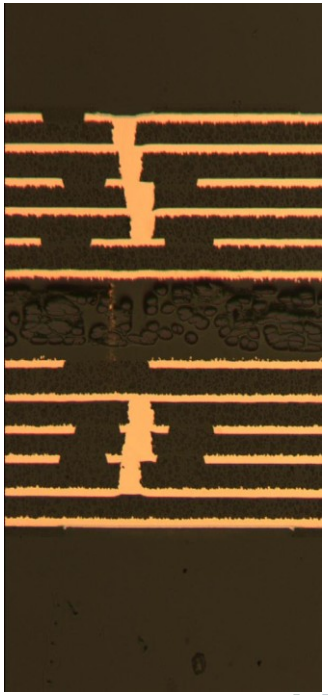


2 – 4 – 2



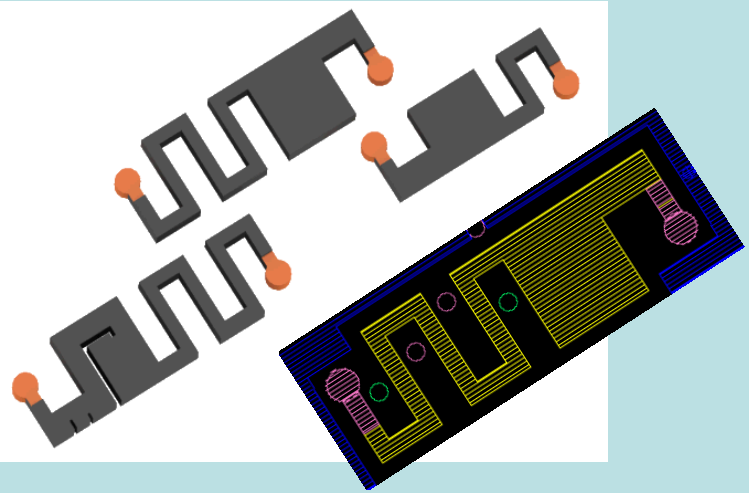
3 – 4 – 3

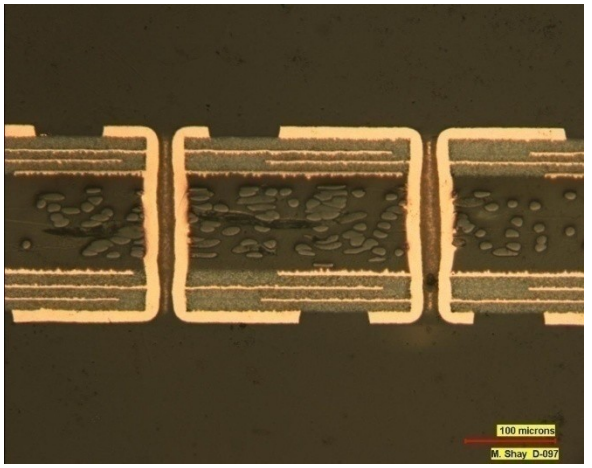


4 – 4 - 4

Embedded Passives in CoreEZ®

- Resistors
  - Thin film resistor material
    - Ticer TCR®
    - 10 - 250 ohms per square
  - Resistor values from 5 ohm to 50 Kohm
  - Resistor tolerances from 2 – 20%
    - Laser trimming 2 – 5%
  - Typical resistor areas
    - 0.2 – 15 mm²
  - Block or Serpentine designs

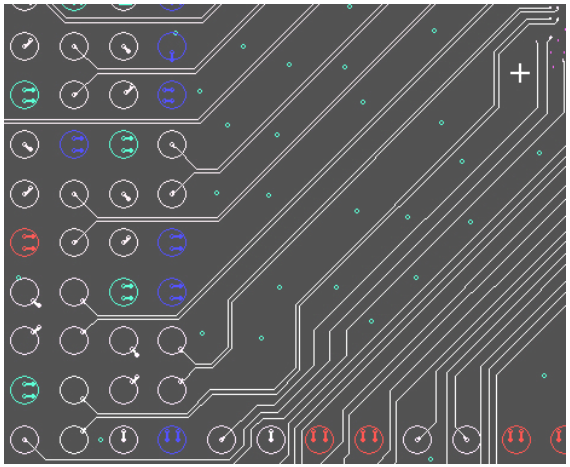


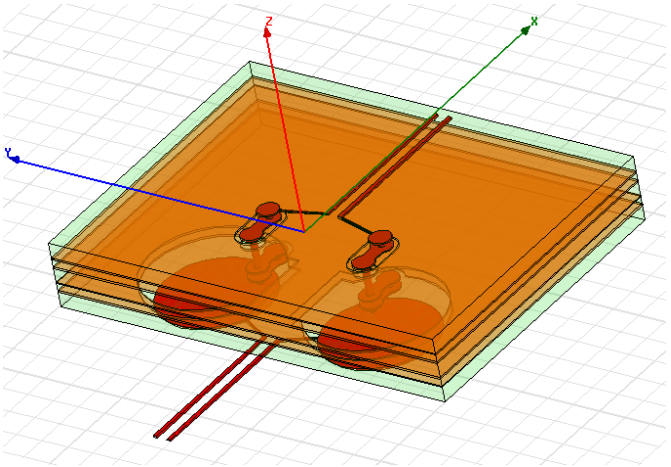


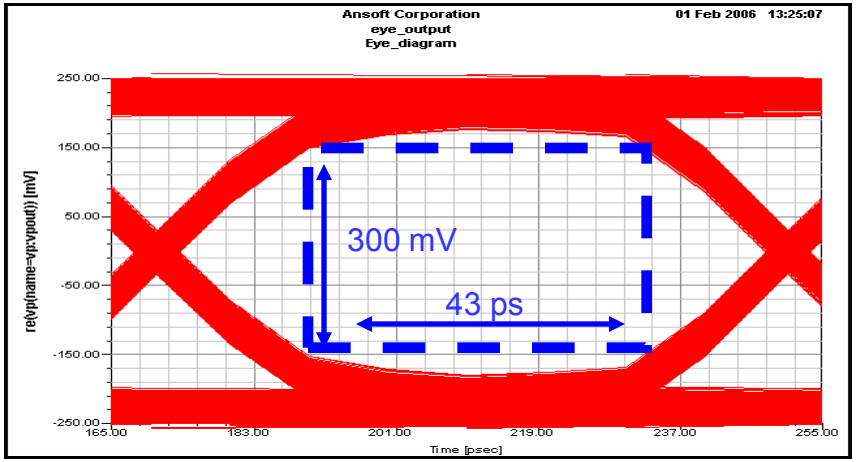
Eight layer core 285 nF / in²

Via Structures	Layer	CoreEZ Thin Build-Up 3-8-3	Estimated Thickness (um)	Potential Function
	Top		12	Mounting / Signal / Power
		Driclad Filled RCC	32	
Stacked (if needed)	2T		12	Signal / Power
		Driclad Filled RCC	32	
	1T		12	Signal / Power
		Driclad Filled RCC	34	
	CL1		18	Power / Signal
		Embedded Capacitance	12	
	CL2		6	Power
		Embedded Capacitance	12	
	CL3		6	Power
		Embedded Capacitance	12	
PTH	CL4	Embedded Resistance	6	Power / Resistance
		Thermount	110	
	CL5	Embedded Resistance	6	Power / Resistance
		Embedded Capacitance	12	
	CL6		6	Power
		Embedded Capacitance	12	
	CL7		6	Power
		Embedded Capacitance	12	
	CL8		18	Power / Signal
		Driclad Filled RCC	34	
	1B		12	Signal / Power
		Driclad Filled RCC	32	
	2B		12	Signal / Power
		Driclad Filled RCC	32	
	Bottom		12	Mounting / Signal / Power
		Total	522	
		Core (Incl cu)	254	

High Speed SERDES in CoreEZ® Simulation at 12.5 Gbps







- Similar electrical performance as PTFE
  - Within 10% of PTFE jitter performance

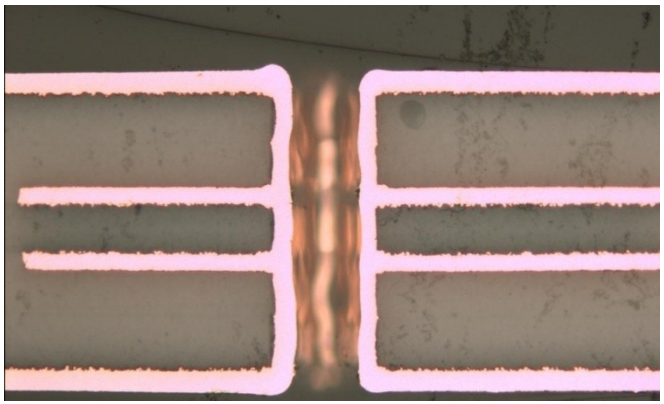
Liquid Crystal Polymer (LCP)

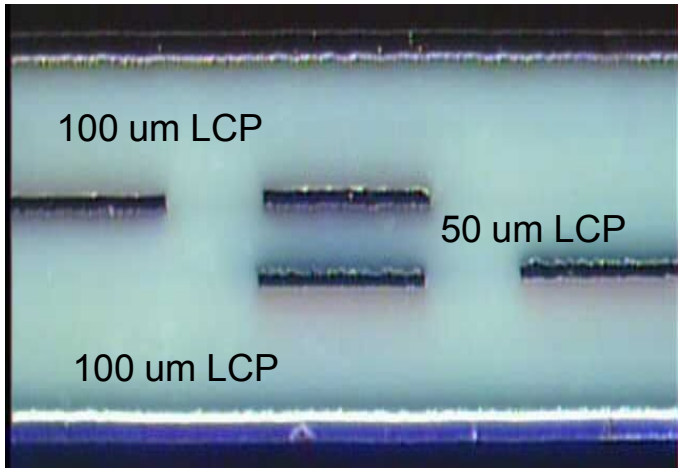
Why LCP?

- Is “near” hermetic
  - Low moisture absorption: 0.04%
- Halogen Free (lead free assembly being evaluated)
- Similar in electrical performance to PTFE
  - Low Loss
    - Dk = 2.9
    - Df = 0.0025
- Very Lightweight
  - 1.4gm/cm^3
- Thermoplastic
- Thin and thick layer combinations in cross sections
  - 25um, 50 um and 100 um thickness
- Capable of Radiation Hardened applications

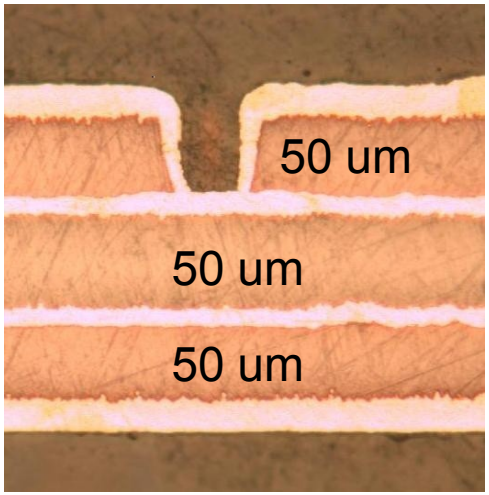
- Rogers ULTRALAM 3850, 3908
- Nippon Steel Espanex L

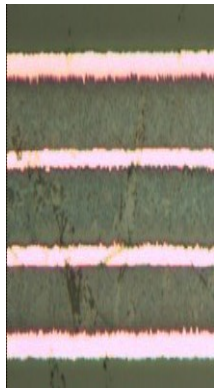
4-Layer LCP x-sections:





- 50 micron laser thru vias
- 50 micron buried vias
- 50 micron thick LCP
- 100 micron thick LCP
- 37.5 micron LW & Space
- Staggered Blind Vias
- Rogers Ultralam 3850, 3908





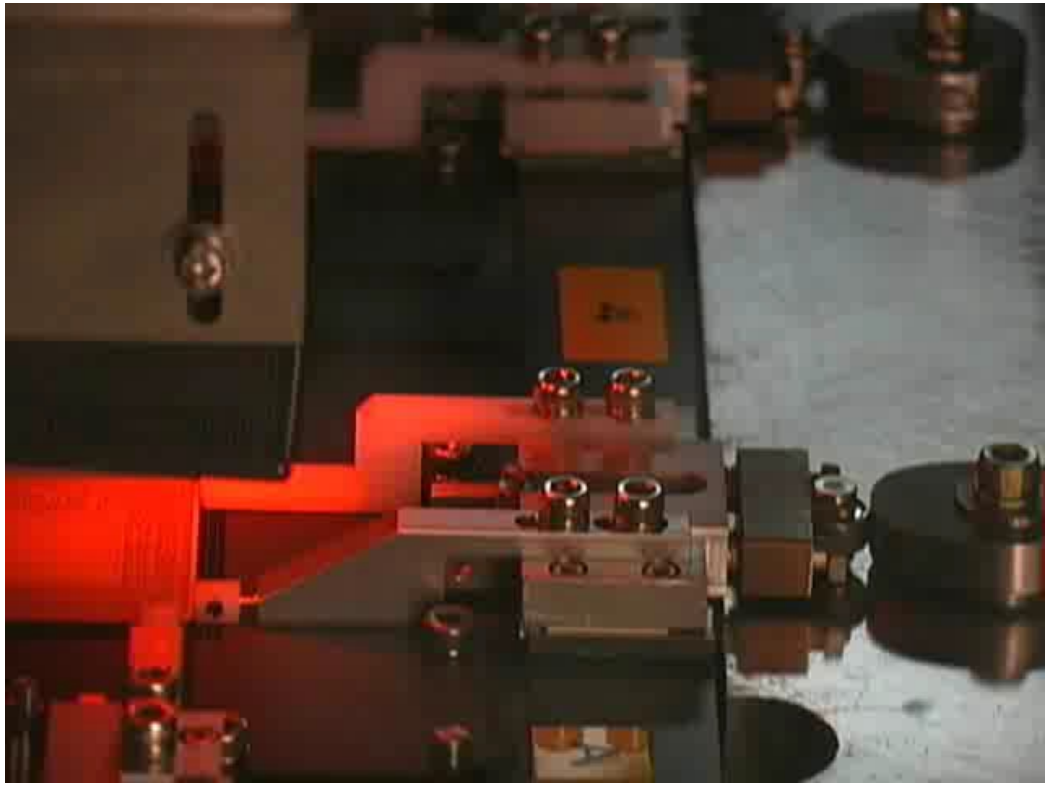
Integrated Circuit Assembly Needs

First level Assembly Overview

Electronic packaging development, fabrication and advanced assembly of complex flip chip and wire bond packages

Key differentiators:

- Flip Chip, Wirebonding and SMT on one package
- BGA balling
- Lead-free assembly
- 01005 component placement and assembly
- Alternative pad finishes
- Teradyne Ultra FLEX
  VLSI platform functional testing
- Leading edge process development



First level Assembly-Wirebond

Wire Bond Expertise……

- Die-up and cavity
- Ball bonding 25 micron diameter Au wire to 125 micron pitch
- Pitches down to 57µm on 700+ wire package
- Production qualified for military applications
- Die attach: sizes to 16mm square
- Ribbon bonding packages and cards to 12”
- Al ribbon bonding available
- Coplanarity measurements
- Damming and glob top

Flip Chip Assembly Needs

- Flip Chip Expertise
  - SiGe, Si, GaAs die attach
  - Hi melt, eutectic, Sn cap C4, Pb-free
  - Low alpha Sn/Pb solder
  - High I/O Flip Chip join down to 150µm pitch
  - Die sizes placed to 25mm x 26mm
  - Flux chemistries/dispensing
  - Various low & high modulus underfills
  - BGA attach down to 0.5mm pitch (eutectic, Pb-free)
  - PGA attach
  - Thermal adhesive
  - Heat spreader, heat sink & lid attach
  - 100µm pitch solder dispense
  - Solder volume measurements
  - CSAM acoustic imaging inspection
  - X-ray inspection
  - Part labeling/marking: traceability

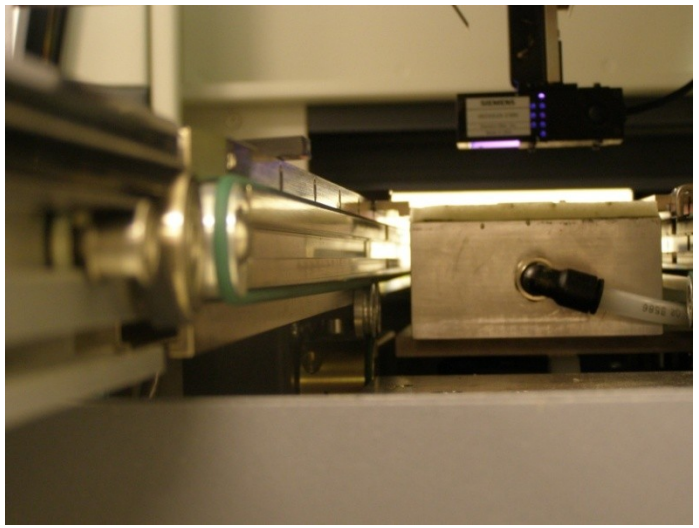
Assembly Engineering Support

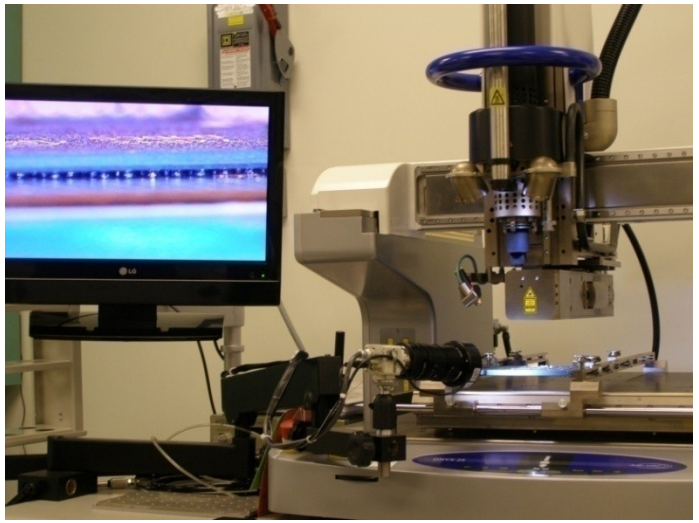
Support Operations

- Pre/post assembly coplanarity measurement
- Acoustic microscopy for interfacial inspection
- Real time X-ray for process monitors
- Ionic cleanliness measurements
- Wire pull and ball shear
- Solder repair/rework
- Cross section support failure analysis
- Traceability to the component level
- Fixturing and process development

AIR-VAC Hot Air Rework Tool

- Can rework leaded, lead free, and high melt BGA's, Micro BGA's, and flip chip die.

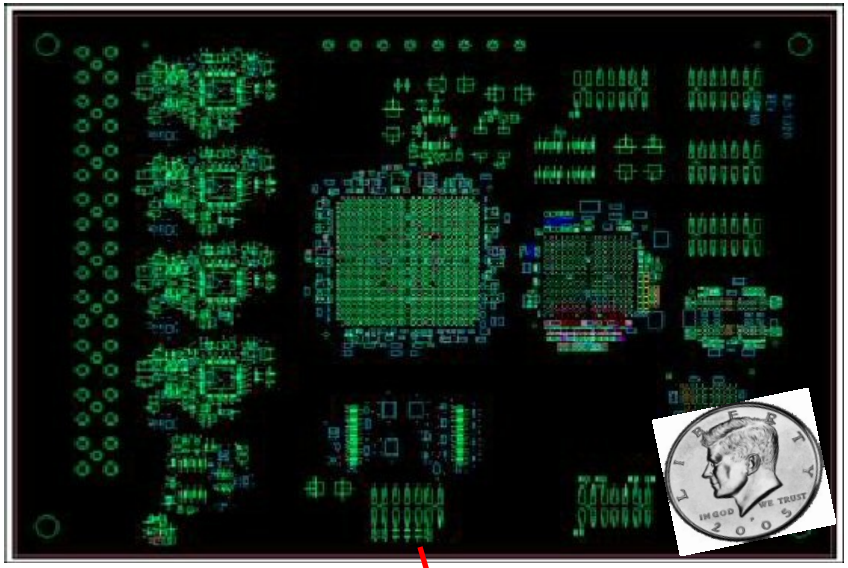


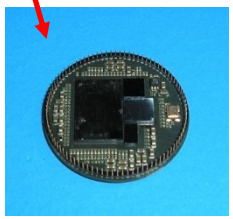


System in Package Application Examples

Extreme SiP Miniturization example

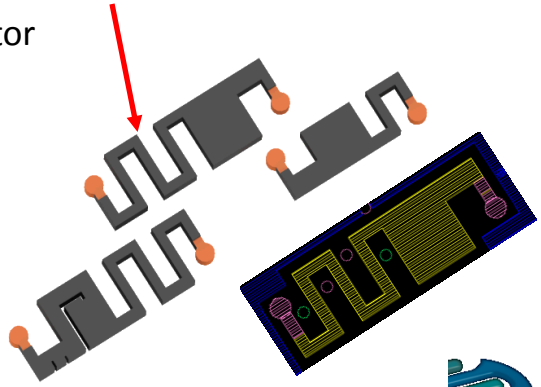
Original PCB 620 mm^2



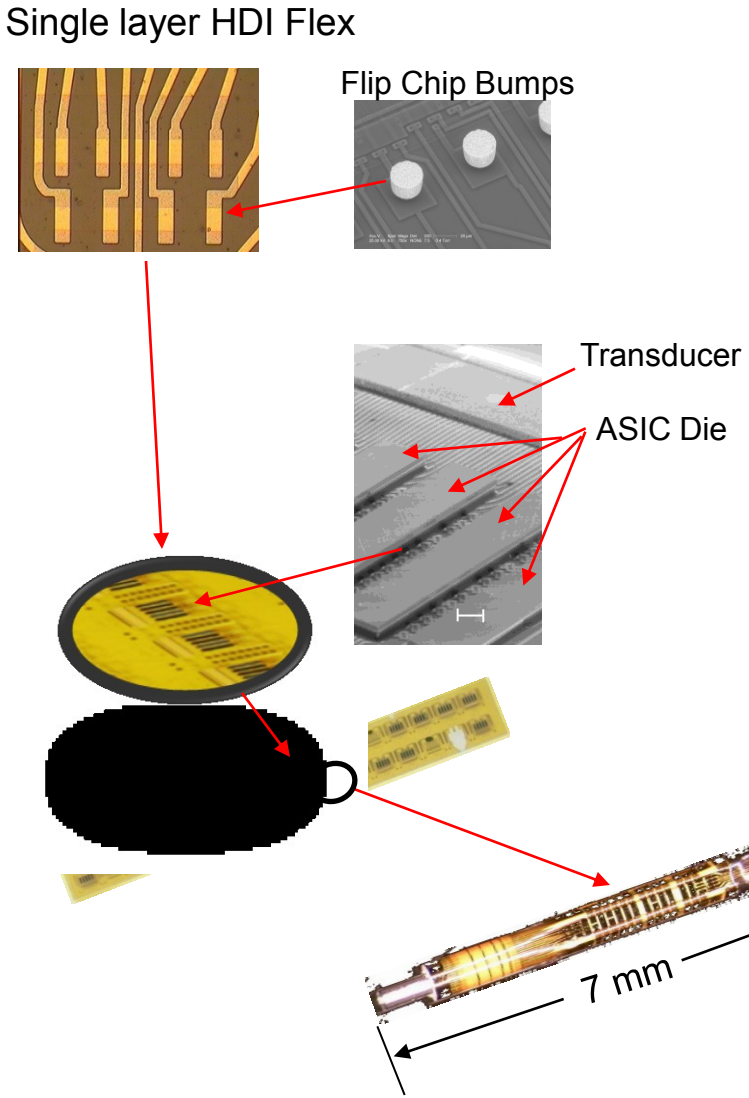


SiP CoreEZ™ 30 mm^2

- Package Size
  - 30 mm diameter, 391 total components
- 39 different part numbers, 231 components on 2 surfaces
- 5 Bare Die
  - Flip Chip FPGA, 15.95mm x 10.23mm, 2,440 I/O
  - Flip Chip DSP, 4.68mm x 5.134mm, 225 um pitch, 261I/O
  - Flip Chip Supply monitor, pitch = 114 um, 16 I/O
  - Flip Chip DRAM, pitch = 121 um, 86 i/o
  - Flip Chip Flash memory, pitch = 116 um, 77 I/O
- 178 SMT Capacitors, 14 SMT resistors
- 152 buried resistors imbedded in substrate
- 1 SMT circular connector
- > 100 produced

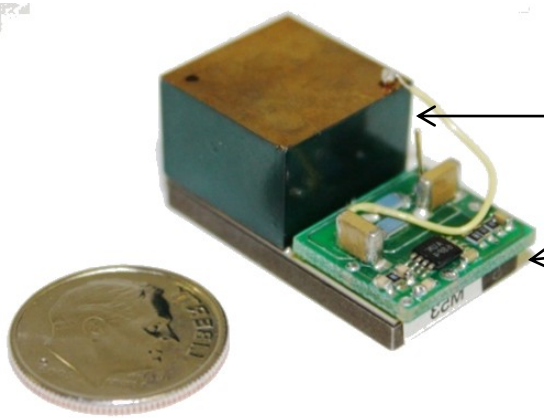


Intravascular Ultrasound Catheter Sensor Package



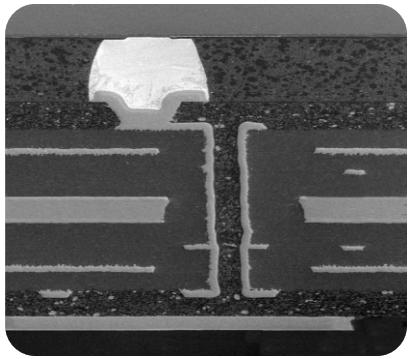
- Flip Chip Ultrasound Transducer for Catheter
- sensor assembly rolled to 1.175mm diameter
- 5 Flip Chip ASIC,.1mm thick, 31 I/O, 2.5mm x .5mm
  - 22 micron flip chip bumps on 70 micron die pad pitch
- 1 PZT crystal
- 12.5mm by 6.5 mm single layer flex circuit
  - 14 micron wide lines and space copper circuitry
  - 12.5 thick polyimide dielec
- Prototype to production
  - Over 320,000 modules shi

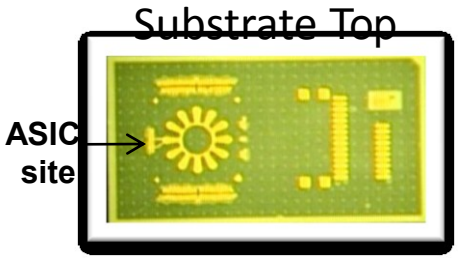
Low Level Gamma Photon Detector Module

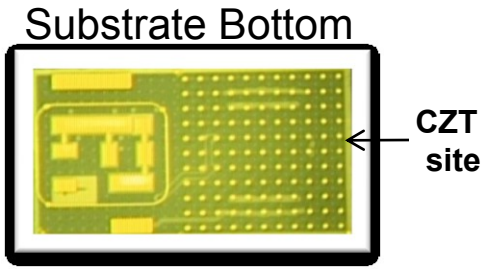


9 layer HyperBGA PTFE Substrate
- Bottom side CZT Crystal
- Passives on mini card
- S. Steel Stiffener
- Top side Wirebonded ASIC
- 50 micron UV laser drilled vias
- 25 micron trace
- 33 micron space

Hyper Substrate X-Section







Microelectronics Packaging Conclusion

Enable System Miniaturization using SiP: Bare die, HDI Substrate Materials, Assembly Technology & Manufacturing

- **Combining advanced flip chip & wirebond with maximum HDI plastic substrates**
- **Deliver maximum reliability and electrical performance for RF and High Bandwidth Digital**
- **System Level Shrink for SWaP**
  - PWB redesigns into fully integrated System in Package
  - 24X system size reductions have been realized
  - Lower cost next level assemblies (lower layer count PWB's)

Deliver the industry's smallest packages combined with superior package reliability and robust electrical performance!

Acknowledgments

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