GBT Project Status

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CERN

Outline

GBT Project Status:

- GBT project overview
  - Radiation hard link
- The GBT chipset
  - The GBTIA
  - The GBLD
  - The GBT – SerDes
  - The GBT - SCA
- The GBT Protocol on FPGAs

The GBTX:

- GBTX-to-Frontend communication
- 8B/10B Transmitter mode
- GBTX packaging
- GBTX power consumption
- GBT Project Schedule

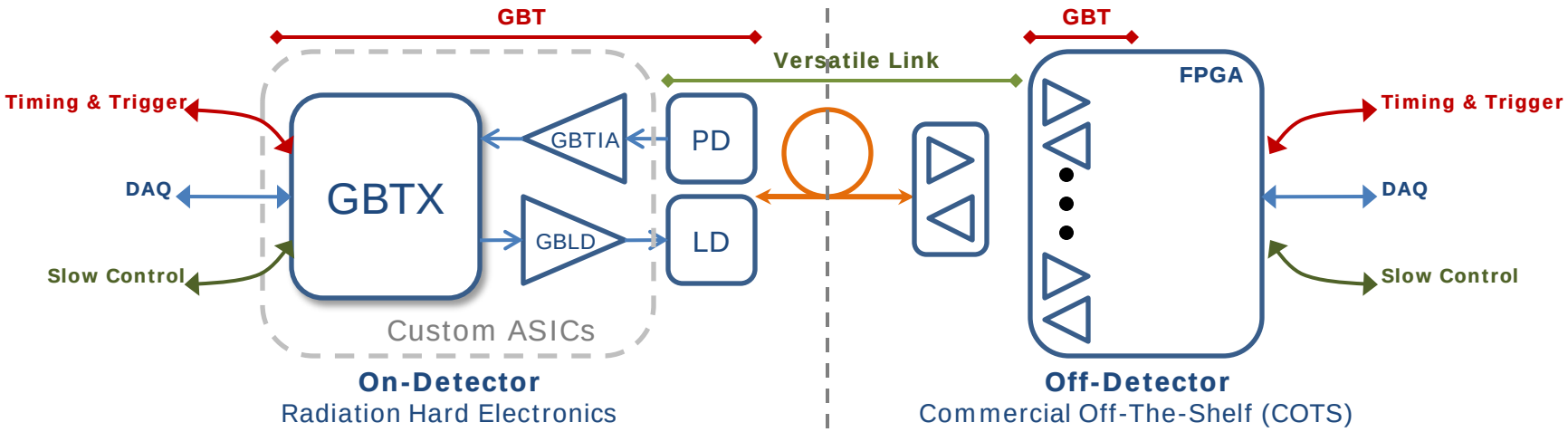
Radiation Hard Optical Link Architecture

Defined in the "DG White Paper"

- "Work Package 3-1"
  - Objective:
    - Development of an high speed bidirectional radiation hard optical link
  - Deliverable:
    - Tested and qualified radiation hard optical link
  - Duration:
    - 4 years (2008 – 2011)

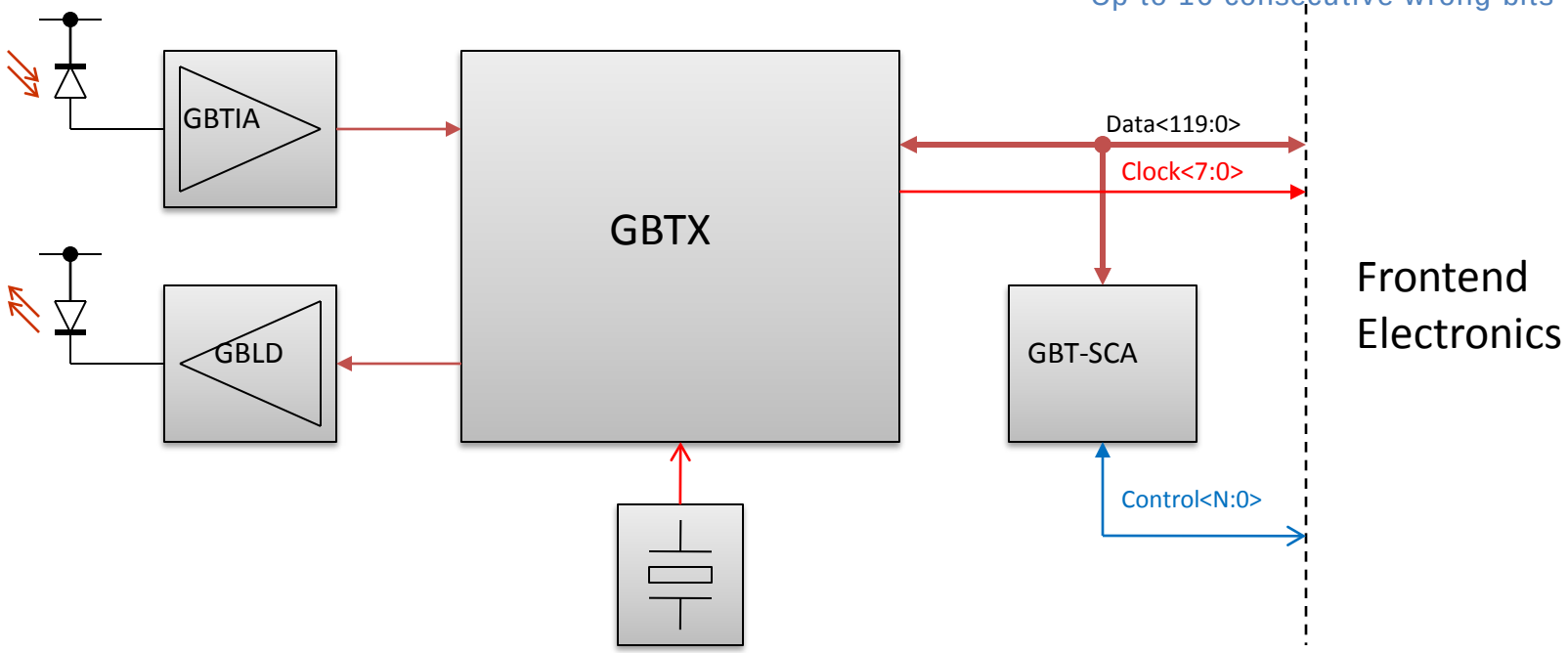
Radiation Hard Optical Link:

- Versatile link project:
  - Opto-electronics components
  - Radiation hardness
  - Functionality testing
- GBT project:
  - ASIC design
  - Verification
  - Radiation hardness
  - Functionality testing



The GBT Chipset

- Radiation tolerant chipset:
  - GBTIA: Transimpedance optical receiver
  - GBLD: Laser driver
  - GBTX: Data and Timing Transceiver
  - GBT-SCA: Slow control ASIC
- Supports:
  - Bidirectional data transmission
  - Bandwidth:
    - Line rate: 4.8 Gb/s
    - Effective: 3.36 Gb/s
- The target applications are:
  - Data readout
  - TTC
  - Slow control and monitoring links.
- Radiation tolerance:
  - Total dose
  - Single Event Upsets
- Custom line code:
  - Offers protection against bursts of errors on optical links
    - Up to 16 consecutive wrong bits



The GBTIA

Main specs:

- Bit rate 5 Gb/s (min)
- Sensitivity: 20 µA P-P (10^{-12} BER)
- Total jitter: < 40 ps P-P
- Input overload: 1.6 mA (max)
- Dark current: 0 to 1 mA
- Supply voltage: 2.5 V
- Power consumption: 250 mW
- Die size: 0.75 mm × 1.25 mm

Engineers :

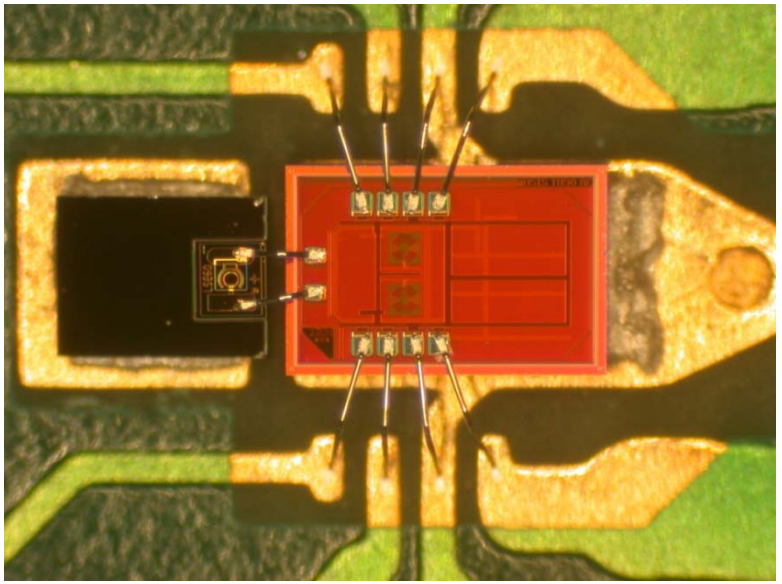
- Ping Gui – SMU, USA
- Mohsine Menouni – CPPM, France

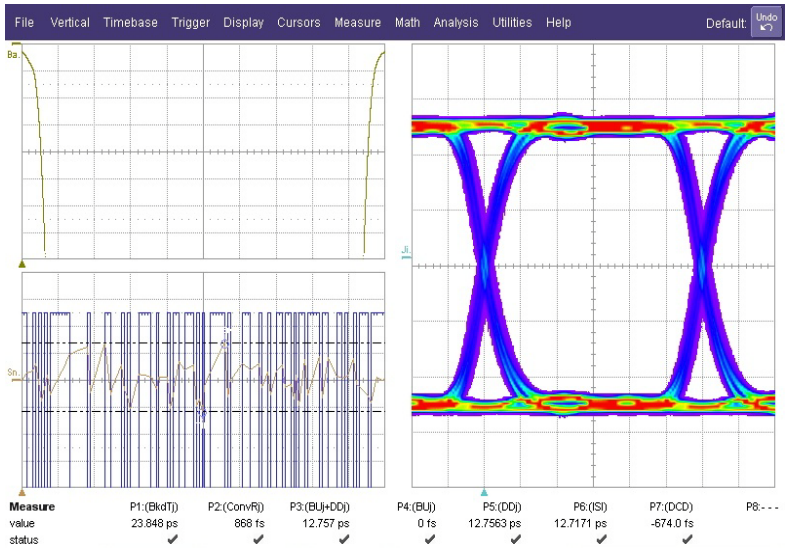
Status:

- Chip fabricated and tested
- Chip fully meets specifications!
- Radiation tolerance proven!
- GBTIA + PIN-diode encapsulated in a TO Package (Versatile link project)

Future:

- Version 2 will address productivity
- Pad positions reworked to facilitate the wire bond operation between the package and ASIC
- Mean optical power monitoring to facilitate pin-diode/fiber alignment
- 2.5 V supply
- Fabrication of the final version in 2011





The GBLD

Main specs:

- Bit rate 5 Gb/s (min)
- Modulation:
  - current sink
  - Single-ended/differential
- Laser modulation current: 2 to 12 mA
- Laser bias: 2 to 43 mA
- "Equalization"
  - Pre-emphasis/de-emphasis
  - Independently programmable for rising/falling edges
- Supply voltage: 2.5 V
- Die size: 2 mm × 2 mm
- I2C programming interface

Engineers :

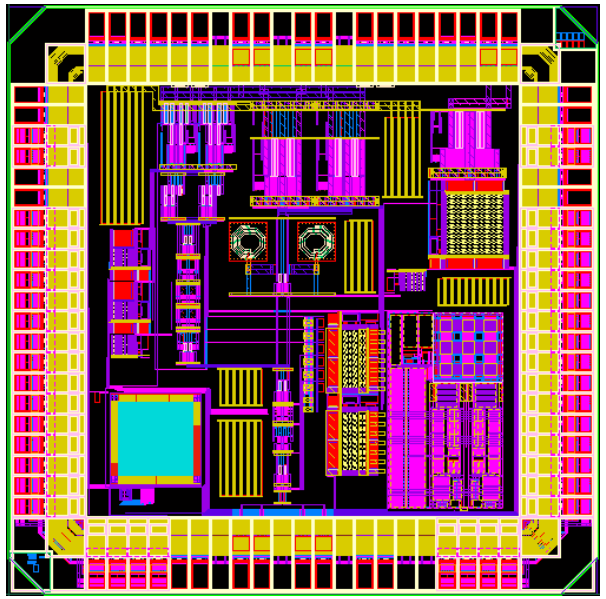
- Gianni Mazza – INFN, Italy
- Angelo Rivetti – INFN, Italy
- Ken Wyllie – CERN
- Ping Gui – SMU, USA

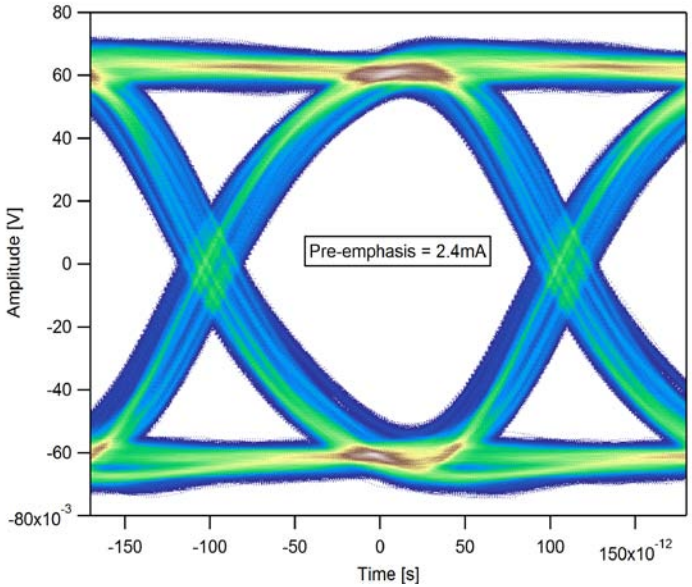
Status:

- Chip fabricated and tested
- Chip fully functional
- Performance close to specs (if corrected for the large input capacitance of the input protection diode)
- One of the protection diodes was removed by a FIB operation:
  - A significant performance improvement was observed confirming the impact of the input capacitive loading on the chip performance

Future:

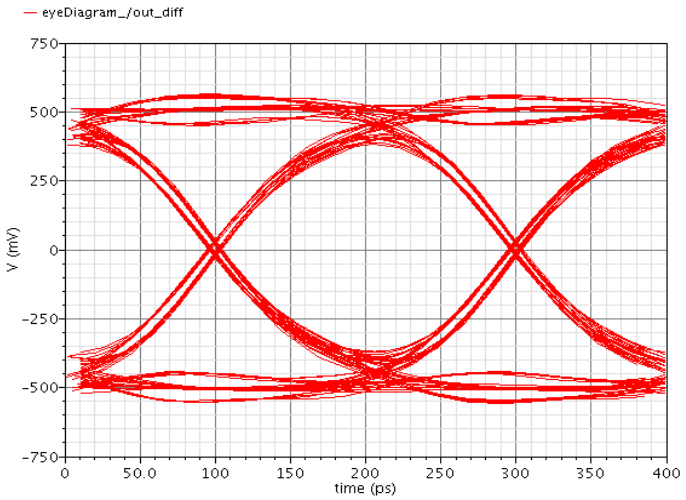
- Reduce the area of the input protection diode
- Improve the bandwidth and gain of the input stage
- Design/choose a package with good thermal conductivity
- Fabrication of the final version in 2011



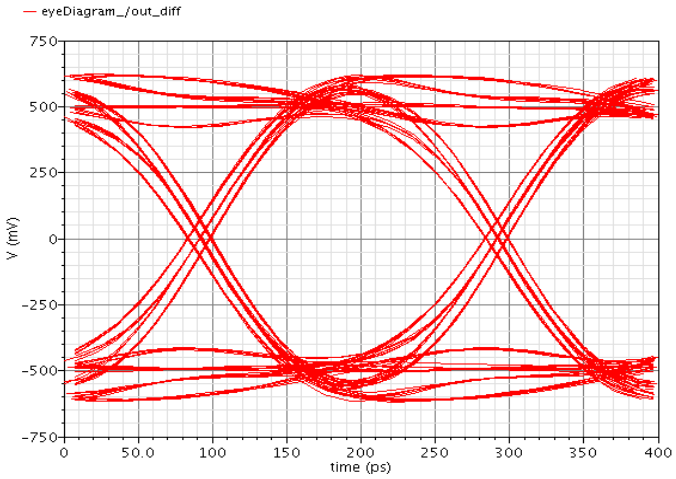


GBLD Measurements/Simulations

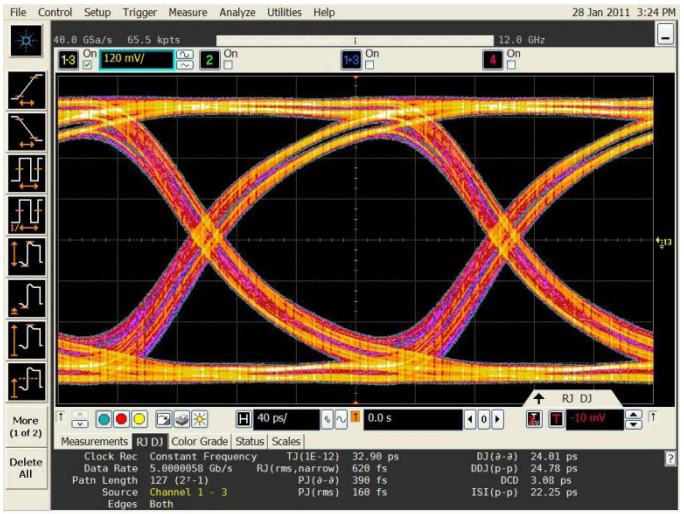
I_{mod} = 12.08 mA and I_{pre} = 0 mA

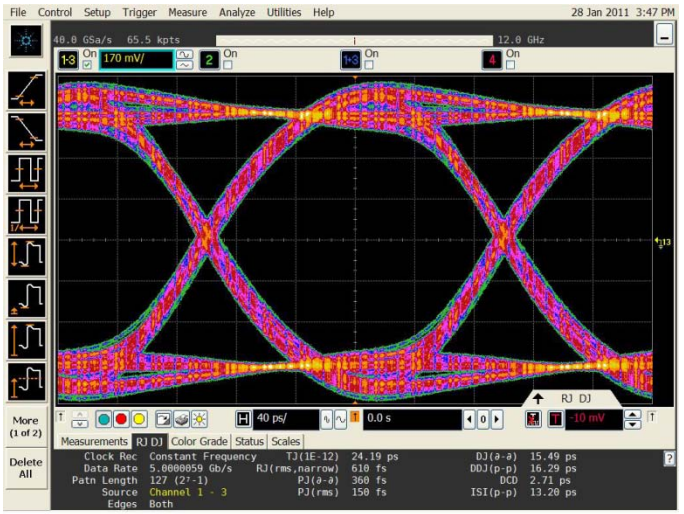


I_{mod} = 12.08 mA and I_{pre} = 3.2 mA



Simulations include a PCB model (SiWave 2 ½ D model)





The GBT – SCA

GBT-SCA Main specs:

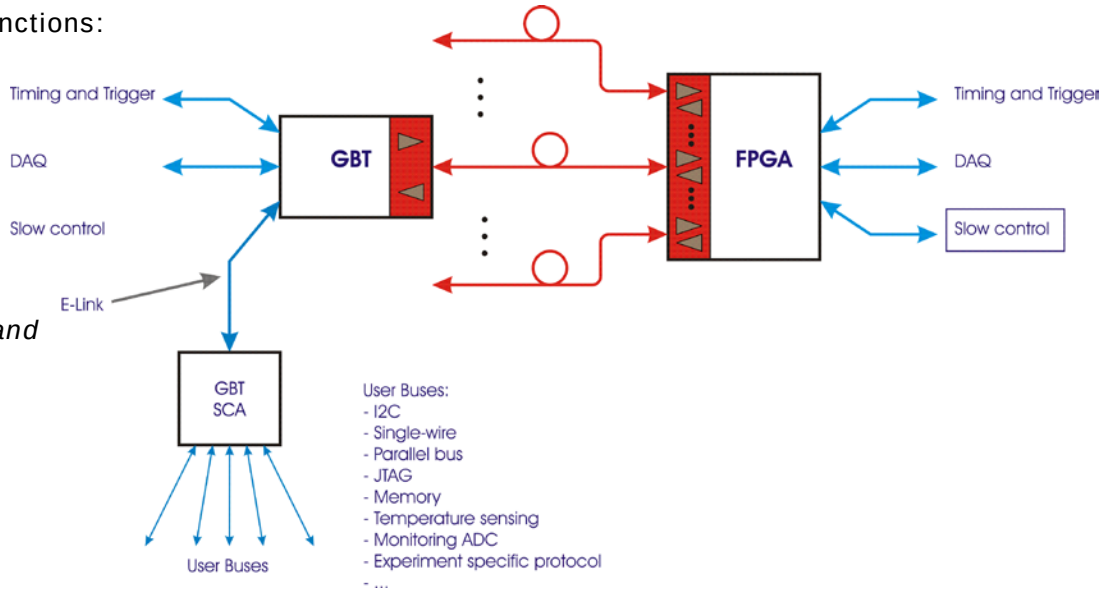
- Dedicated to slow control functions
- Interfaces with the GBTX using a dedicated E-link port
- Communicates with the control room using a protocol carried (transparently) by the GBT
- Implements multiple protocol busses and functions:
  - I2C, JTAG, parallel-port, etc…
- Implements environment monitoring functions:
  - Temperature sensing
  - Multi-channel ADC
  - Multi-channel DAC

Engineers:

- *Alessandro Gabrielli – INFN, Italy*
- *Kostas Kloukinas – CERN, Switzerland*
- Sandro Bonacini – CERN, Switzerland
- *Alessandro Marchioro – CERN, Switzerland*
- *Filipe Sousa – CERN, Switzerland*

Status

- Specification work undergoing:
- 1st Draft already available
- RTL design undergoing
- 10-bit ADC prototype:
  - Submitted for fabrication in April 2010
  - Received from the foundry in February 2011
  - Test results expected soon
- Fabrication of the final version in 2011



The GBT - SerDes

The GBT – SerDes is a demonstrator for:

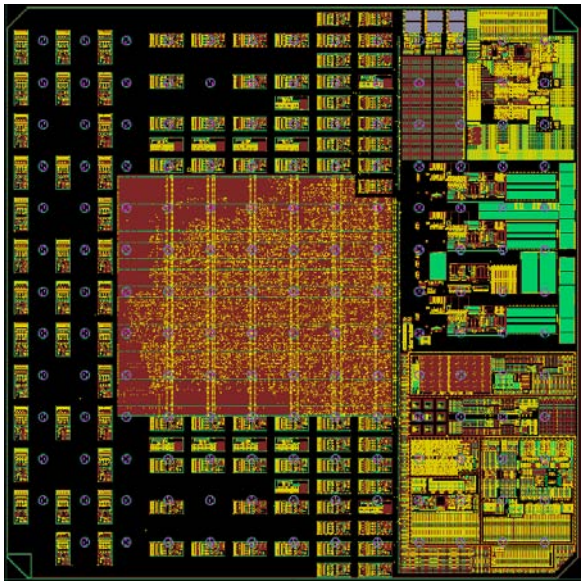
- The Serializer/De-serializer critical circuits:
  - Phase-Locked Loops
  - Frequency dividers
  - Line driver/receiver
  - Constant – latency barrel shifter
  - Phase shifter
- Target data rate: 4.8 Gb/s
- The chip was packaged in a custom flip-chip BGA 13 x 13 pin package

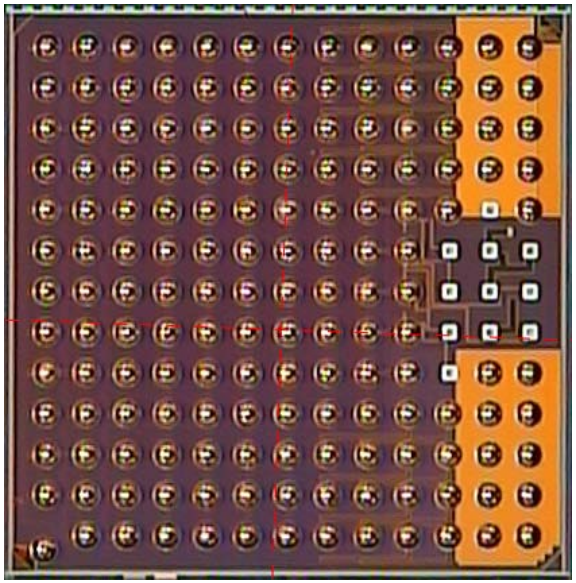
Engineers:

- Ozgur Cobanoglu - CERN, Switzerland
- Federico Faccio - CERN, Switzerland
- Rui Francisco – CERN, Switzerland
- Ping Gui – SMU, USA
- Alessandro Marchioro - CERN, Switzerland
- Paulo Moreira - CERN, Switzerland
- Christian Paillard - CERN, Switzerland
- Ken Wyllie - CERN, Switzerland

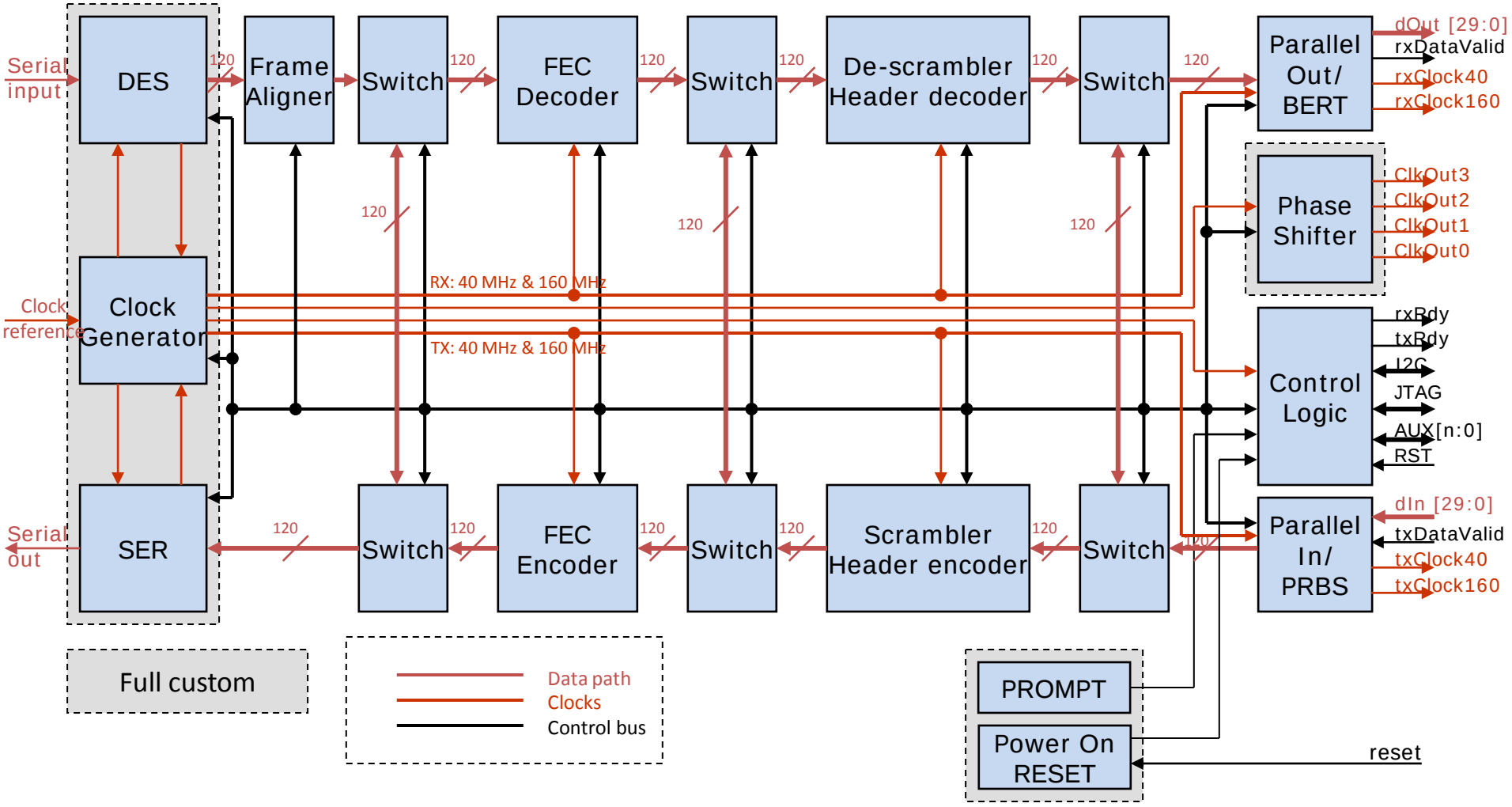
Status:

- Chip is currently under testing





The GBT – SerDes Architecture



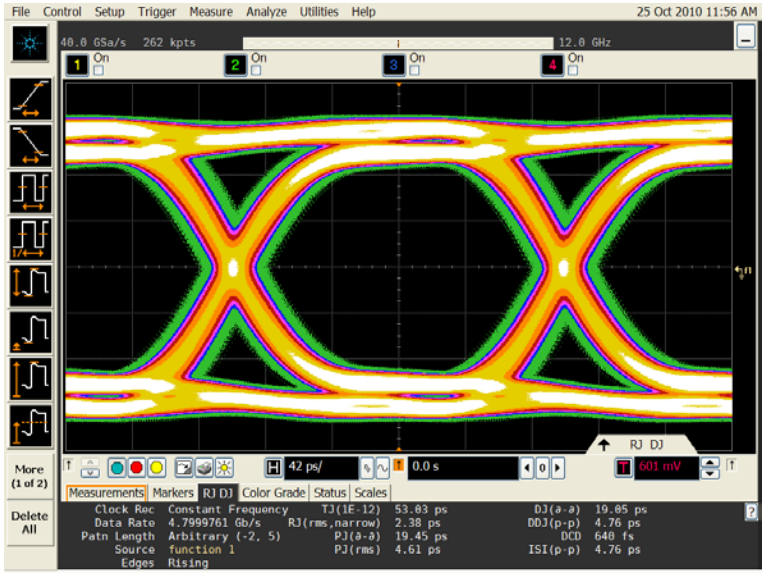
Ser & Des

Serializer

- The serializer if fully functional and fully complies with the specifications:

Performance:

- Data transmission:
  - No error observed
- Jitter:
  - Total jitter ($1e^{-12}$): 53 ps
  - Random jitter: 2.4 ps (rms)
  - Deterministic jitter: 19 ps
    - Data dependent: 4.8 ps
    - Periodic:
      - RMS: 4.6 ps
      - PP: 19.6 ps
    - Duty-cycle-distortion: 0.6 ps
      - Inter-symbol interference: 4.8 ps

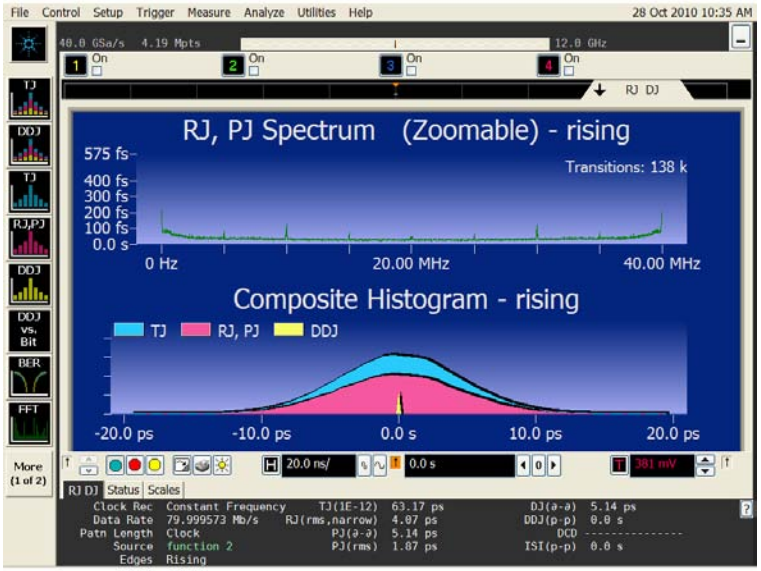


De-Serializer

- The receiver is fully functional but only up to ~3 Gb/s!

Performance:

- Clock recovery operates up to 6 Gb/s
- Jitter:
  - Recovered 40 MHz clock PRBS @ 4.8 Gb/s:
  - Total jitter (1e-12): 63 ps
  - Random jitter: 4.9 ps (rms)
  - Deterministic jitter: 24 ps (pp)
  - Periodic:
    - RMS: 2 ps
    - PP: 5 ps



De-Serializer: Likely causes

De-serializer: timing

- The following functions are operating correctly:
  - The clock recovery
  - The digital receiver functions:
    - Frame aligner
    - FEC decoder
    - De-scrambler
    - I/O parallel interface
- The problem is thus very likely confined to the serial-to-parallel conversion function:
  - The architecture is critically dependent on correct timing
- Very recently it seems that the (main) problem has been located:
  - However, more work is still needed to confirm it behind doubt
- If confirmed it might be possible to do a FIB operation to restore full functionality in a couple of samples!

Package: signal integrity

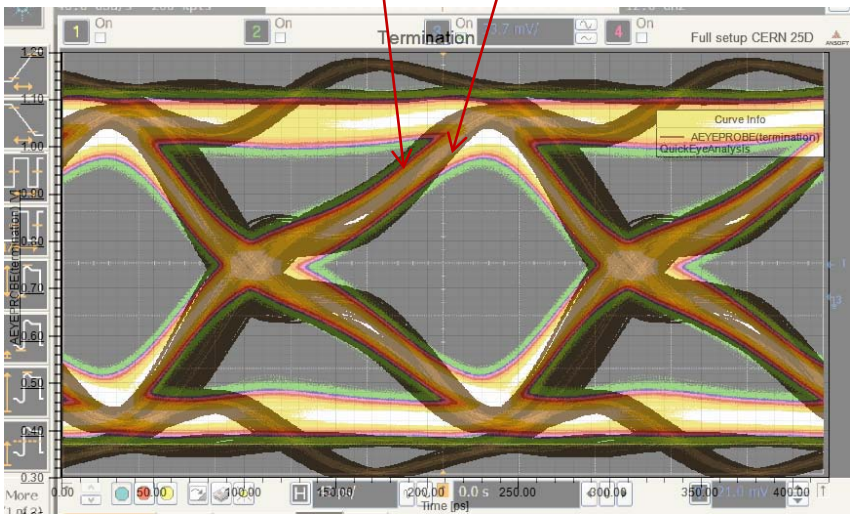
- A bad quality high diagram is observed at the chip input termination!
- Modeling of the package confirmed that the package is partially responsible for the degradation of the signal integrity
- A new package is being designed in collaboration with the packaging company and it will be tried in ~2 months

Eye – Diagram at 4.8 Gb/s

Comparison: Measurement/Simulation

Simulation with a SiWave model

Measured at the termination



Phase – Shifter

Phase-Shifter:

- Main features:
- 8 – channels (3 in the GBT-SERDES prototype)
- 1 PLL + Counter generates the three frequencies: 40 / 80 and 160 MHz
- 1 DLL per channel
- Mixed digital/analogue phase shifting technique:
- Coarse de-skewing – Digital
- Fine de-skewing – Analogue
- Power consumption:
  - PLL: 42 mW (measured)
  - Channel: 16 mW/channel (measured)

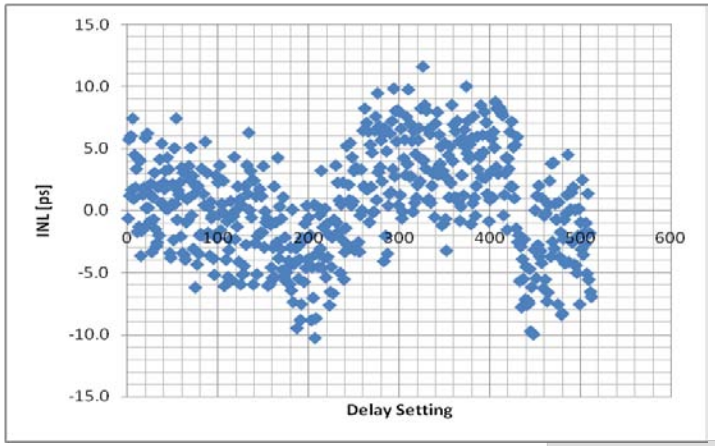
Engineers :

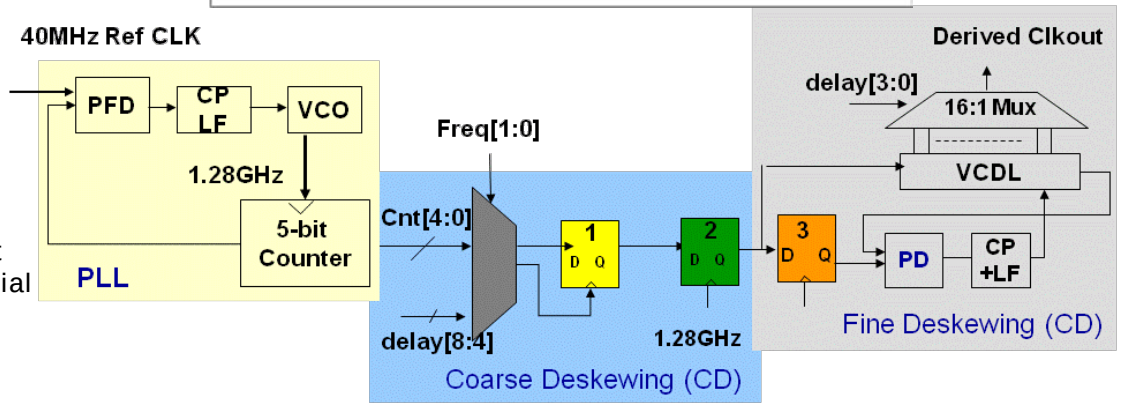
- Ping Gui – SMU, USA
- Tim Fedorov – SMU, USA
- Paul Hartin – SMU, USA
- Nataly Pico – SMU, USA
- Bryan Yu – SMU, USA

Status:

- Fully functional
- Fully meets the specs
  - One channel with timing problems but the cause is clearly identified with trivial solution

- **CK Period Jitter:** σ = 4.8 ps (pp = 29 ps)
- **Resolution:** Δt = 48.83 ps
- **Differential Non-Linearity**:
  - σ = 4.7 ps (9.6% of Δt)
  - pp = 21.5 ps (44% of Δt)
- **Integral Non-Linearity**:
  - σ = 4.3 ps (8.7% of Δt)
  - pp = 21.9 ps (48.7% of Δt)

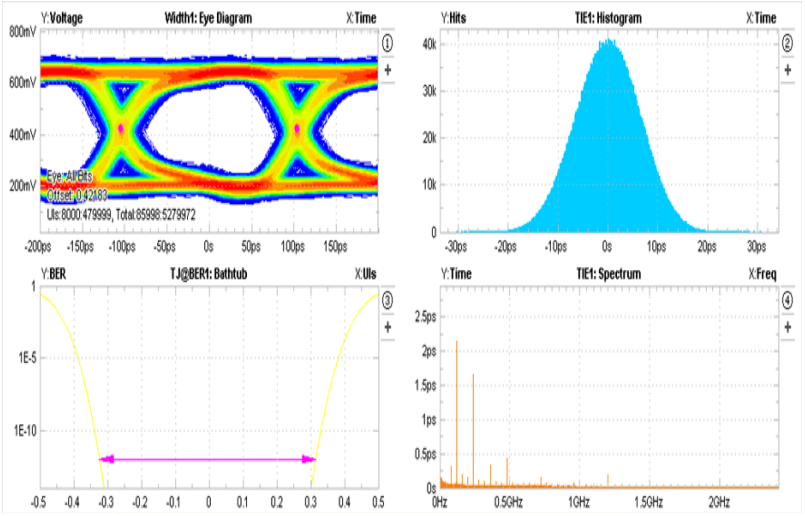




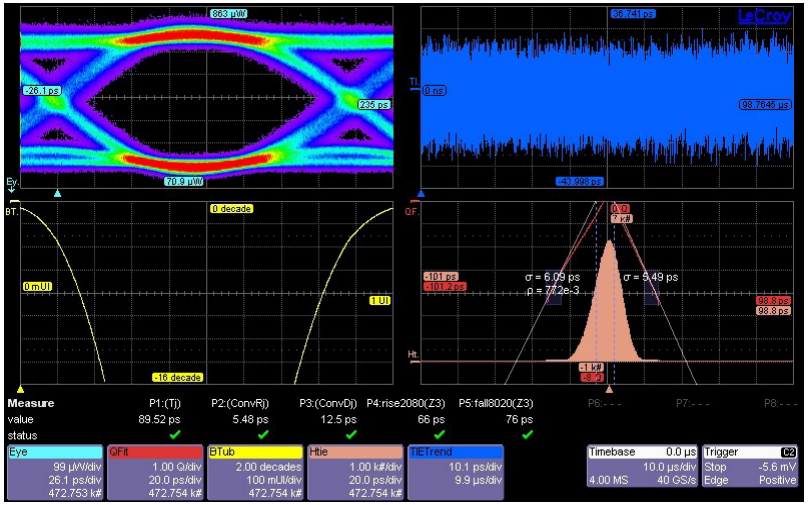
The GBT Protocol on FPGAs

- GBT-SERDES successfully implemented in FPGAs:
  - Scrambler/ Descrambler + Encoder/ Decoder + Serializer/CDR
- FPGA Tested:
  - XILINX Virtex-5FXT and 6LXT
  - ALTERA Stratix II and IV GX
- Optimization studies:
  - Optimization of use of resources
  - Low and “deterministic” latency
- Firmware:
  - “Starter Kit” is available for download with various resources optimization schemes for
    - StratixIIGx and Virtex5FXT
  - Available soon for:
    - StratixIVGx and Virtex6LXT
    - Low latency
- Engineers:
  - Sophie Baron – CERN, Switzerland
  - Jean-Pierre Cachemiche – CPPM, France
  - Csaba Soos – CERN, Switzerland
  - Steffen Muschter - Stockholm University
- Users:
  - 30 registered users from all over the world (most users from collaborating institutes)
  - LHC experiments, but also CLIC, PANDA, GBT
  - Very active users are now part of the development team

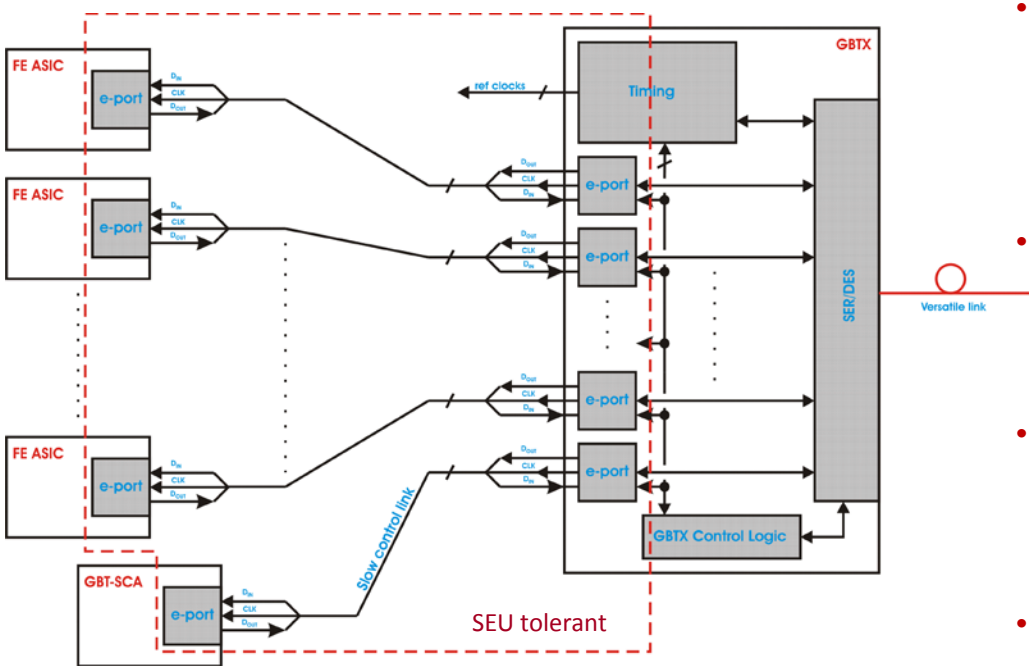
Xilinx - 4.8 Gb/s



Altera + opto TRx - 4.8 Gb/s



GBTX – to – Frontend Communication



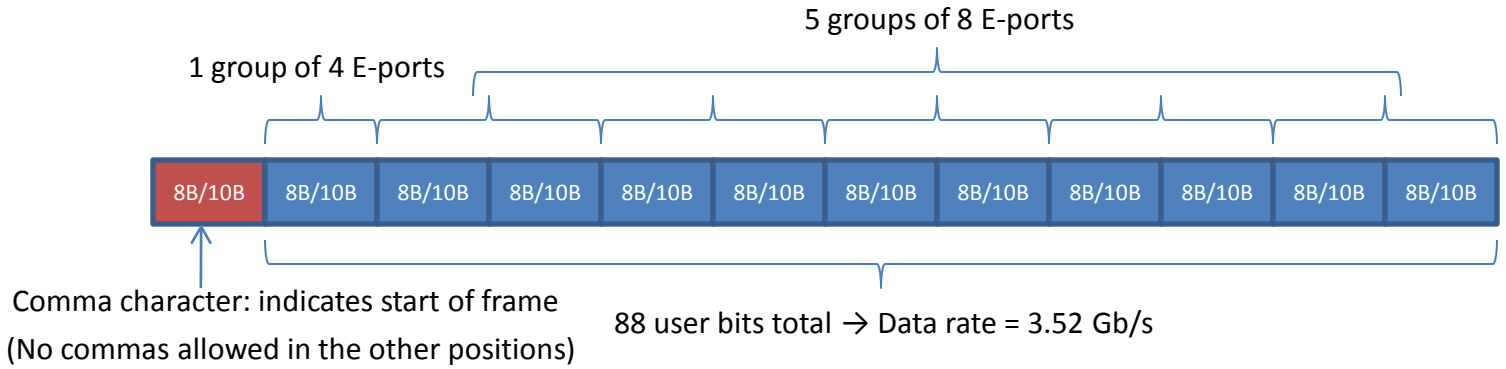
Mode	Type	Data Rate	Notes
OFF	Power off	-	
P-Bus	parallel	80 MW/s	One 40-bit word (DDR)
B-Bus	parallel	80 MB/s	Up to 5 Bytes (DDR)
N-Bus	parallel	160 MN/s	Up to 5 Nibbles (DDR)
2 ×	serial	80 Mb/s	Up to 40 serial links
4 ×	serial	160 Mb/s	Up to 20 serial links
8 ×	serial	320 Mb/s	Up to 10 serial links
8 ×	lanes	> 320 Mb/s	See “Lanes”

JEDEC standard, JESD8-13
Scalable Low-Voltage Signalling for 400 mV (SLVS-400)
http://www.jedec.org/download/search/JESD8-13.pdf

- GBTX – to – Frontend interface:
  - Electrical links (e-link)
  - Bidirectional
  - Operate in:
    - Serial and Parallel Modes
  - Up to 40 active links
- E-Link:
  - Three pairs:
    - D_{OUT}: GBTX –to – Frontend
    - D_{IN}: Frontend – to – GBTX
    - CLK: GBTX –to – Frontend
- Programmable data rate:
  - Independently for up/down links
  - Independently in five groups (of up to 8 links each)
  - 80, 160 and 320 Mb/s
- Lanes:
  - To achieve > 320 Mb/s
  - Two or more e-links can be grouped forming a “lane”
- Slow data rate channel:
  - Fixed data rate: 80 Mb/s
  - General purpose data transmission
  - Compatible with GBT – SCA
- Electrical standard:
  - SLVS electrical levels:
    - 100 Ω termination
    - 400 mV differential
    - 200 mV common mode
    - I_{LOAD} = ±2 mA

GBTX 8B/10B Transmitter Mode

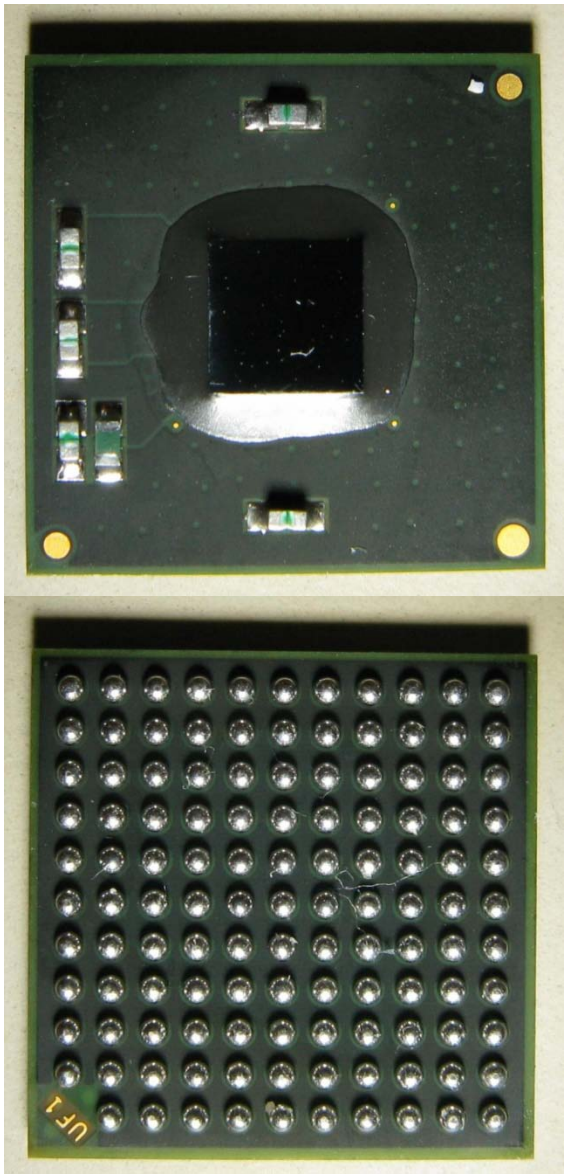
- In this mode:
  - 8B/10B encoding is used
  - No SEU protection
  - **Only available in the simplex transmitter mode**
- Motivation:
  - Simplicity of the FPGA receiver
  - Significant reduction of the resources used by the GBT receiver in the FPGAs
- Implementation:
  - A first special word is required for frame synchronization:
    - Comma character will be used
  - Idle/data frames:
    - Data frame (txDataValid = 1): One comma character followed by 11 8B/10B words
    - Idle frame (txDataValid = 0): To be specified!
  - The 12-word 8B/10B encoder will very likely require additional GBTX latency!
  - To reduce the package cost and the pin count some of the (normally) GBTX output ports will work as inputs
- Bandwidth:
  - User bits: 88 (82 in the GBT protocol)
  - User data rate: 3.52 Gb/s (3.28 Gb/s in the GBT protocol)
    - 3.52 Gb/s vs 3.28 Gb/s → 7.4% increase only!



GBTX Chip and Package Size

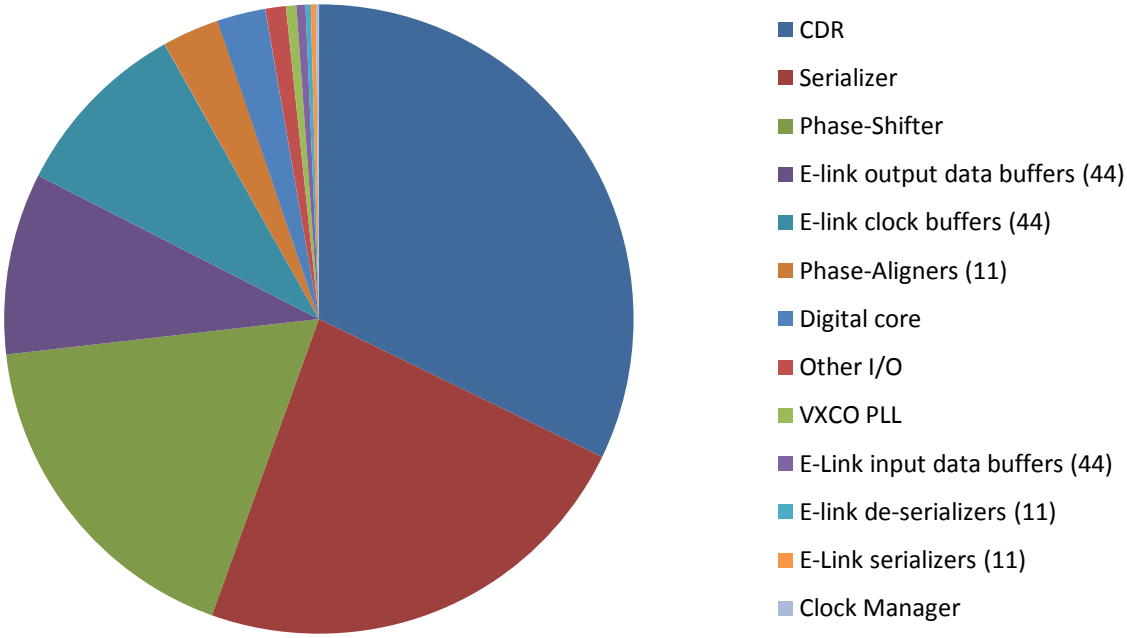
- Total pin count: 434
- Chip size: 5.5 × 5.5 = 30.25 mm^2
- Fits a 21 × 21 pin Package
- Approximate package size:
  - 1 mm pitch: 22 × 22 mm^2
  - 0.8 mm pitch: 18 × 18 mm^2

E-Ports (DIFF: IN/OUT/CLK)	264
E-Port SC (DIFF: IN/OUT/CLK)	6
Transmitter	12
Receiver	12
VCXO PLL	10
Phase-Shifter	16
I2C Slave	2
I2C Master	3
JTAG	5
E-Fuse Programming	4
Chip control	12
I/O Power	34
I/O Ground	34
Core Power	10
Core Ground	10
Total	434



GBTX Power Consumption

GBTX Circuit	Vdd [V]	Idd [mA]	Power [mW]	Comments
CDR	1.5	304	456	Measurement
Serializer	1.5	220	330	Measurement
Phase-Shifter	1.5	167	251	Estimated for 8 channels based on a 3 channel measurement
E-link output data buffers (44)	1.5	88.0	132	Simulation (SLVS driver with maximum current settings)
E-link clock buffers (44)	1.5	88.0	132	Simulation (SLVS driver with maximum current settings)
Phase-Aligners (11)	1.5	27.7	42	Estimated
Digital core	1.5	23	35	Estimated based on current measurement and new functionality
Other I/O	1.5	10.0	15	Estimated
VXCO PLL	1.5	5	8	Estimated
E-Link input data buffers (44)	1.5	4.4	7	Simulation
E-link de-serializers (11)	1.5	2.5	4	Estimated
E-Link serializers (11)	1.5	2.5	4	Estimated
Clock Manager	1.5	1	2	Estimated
Total	1.5	943	1414	



Project Schedule

Tasks remaining:

- GBT – SerDes:
  - Understanding the receiver behaviour:
    - 3 Gb/s error free operation instead of 4.8 Gb/s
  - SEU tests
- GBTX:
  - Receiver rework
  - Power down functions (SER/CDR)
  - TX 8B/10B mode
  - Clock Manager
  - VXCO based PLL
  - 8 channel Phase-Shifter (only 3 on GBT - SerDes)
  - Implement the 8B/10B transmitter mode
  - E – Links
    - Bi-directional C4 pad
    - Serializers
    - Phase-Aligners
  - E-Ports:
    - Implement a bidirectional C4 pad with switchable termination resistor
  - Control Logic:
    - Watchdog and start-up state machines
    - IC channel logic
    - I2C master
  - Configuration logic:
    - Fuse bank
  - Chip assembly and verification
  - From industry:
    - BGA package (flip-chip)
    - 80 MHz crystal
  - Testing:
    - Test setup
    - Early behavioral model needed for test development
    - Software
    - Firmware
- GBLD:
  - Reduce the area of the input protection diode
  - Improve the bandwidth and gain of the input stage
  - Design/choose a package with good thermal conductivity
  - Change I/O to 1.5V
- GBTIA
  - Change pad ring
  - Average power detector circuit
  - 2.5V Supply

Project Schedule 2011

- SEU tests on GBT – SerDes
  - May
- ASIC submissions:
  - GBLD: August
  - GBT – SCA: November
  - GBTIA: November
  - GBTX: November