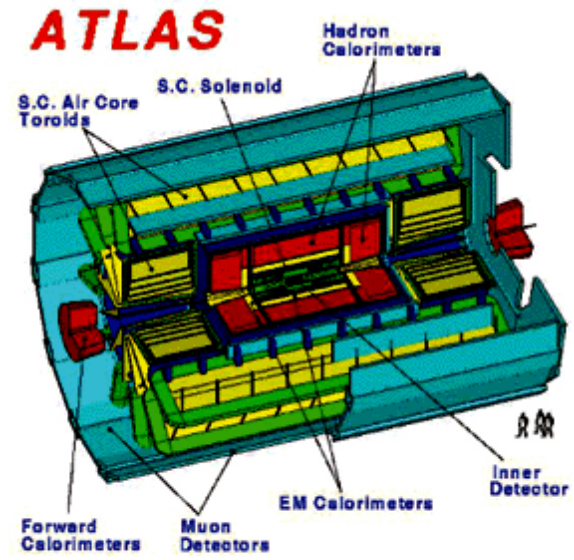
ATLAS tile calorimeter electronics upgrade

Christian Bohm for the TileCal upgrade groups

- Background
- Overview of upgrade
- Upgrade R&D projects

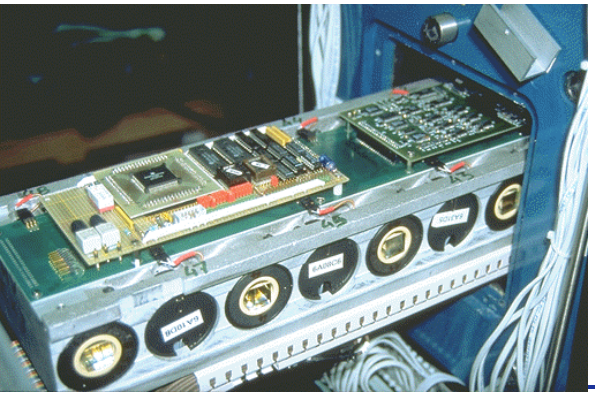
Upgrade R&D projects

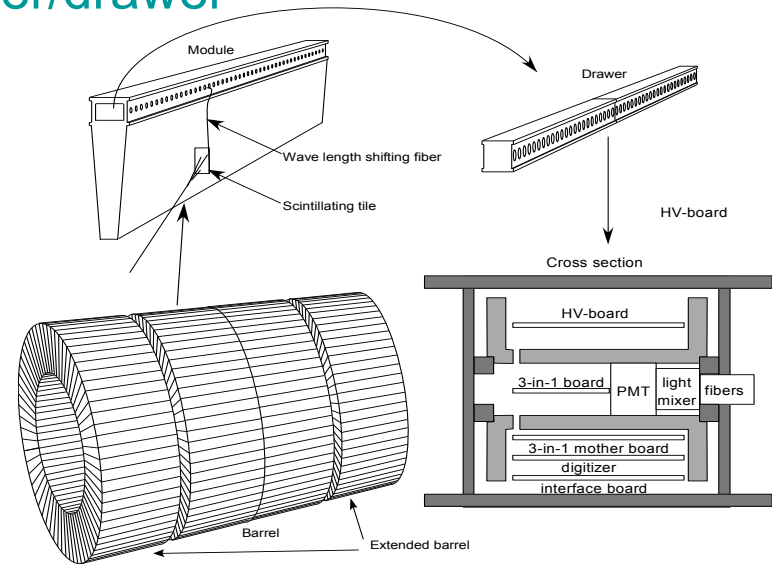
The present TileCal system



A TileCal drawer contains up to 48 PMT

- Their signals are digitized and stored in a pipeline
- The signals are also combined into tower sums for . transfer off the detector via analog trigger cables
- L1a selects sampled pulses for readout to off-detector RODs -1 fiber/drawer





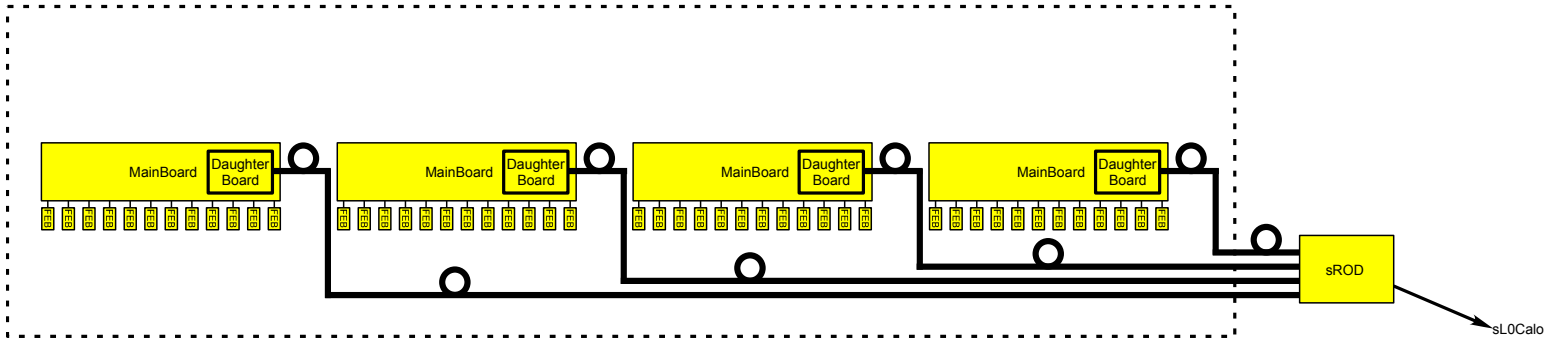
Upgrade R&D projects

TileCal readout system upgrade is driven by need for additional information to L1Calo to keep sATLAS L1 rate below 100 kHz

FULL READOUT OF ALL DATA

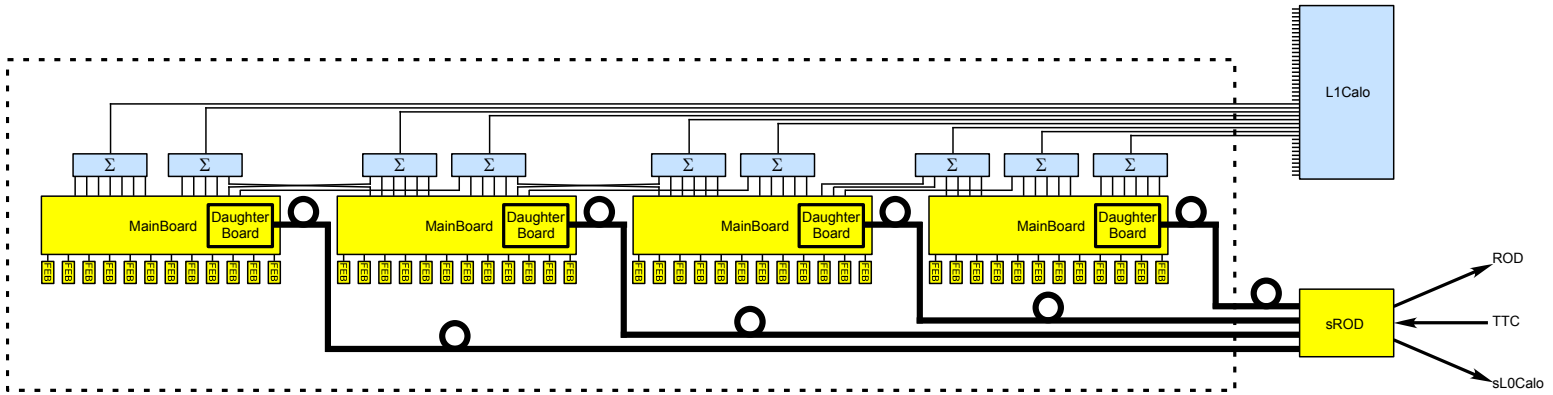
- New drawer mechanics
- New PMT dividers & HV supply
- New on-detector LV electronics
- New Low Voltage Power Supplies
- New off-detector electronics

Upgrade readout and control



- The main components of an upgraded drawer are:
  - Front-End boards – three alternative designs
  - MainBoards – digitizing the FE signals
  - Processing Daughter Board
  - Off detector - sROD modules

Hybrid design



- Provides both analog and digital trigger signals
  - Allows a backwards compatible upgrade path
  - Allows parasitic digital test in running analog system
  - The FE-boards must also provide analog trigger signals

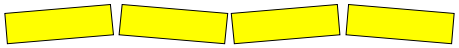
New drawer mechanics

Clermont - Ferrand

- Mini-Drawers quarter of super drawer length
- Potential advantages – easier to service and require smaller opening

First goal is to answer: is it possible to use mini-Drawers?

- Study at several levels:
  - Improving sliding: a factor 2 expected.
  - Study mechanical links to prevent "zigzagging" when pushed.



- Make 4 mini-Drawers models with correct weight to test several solutions for mechanical links and sliding.

- Tests of sliding at CERN in two Tilecal module positions:
  - Vertical: in building 175, - Horizontal: at test beam
  compare with standard Drawers.

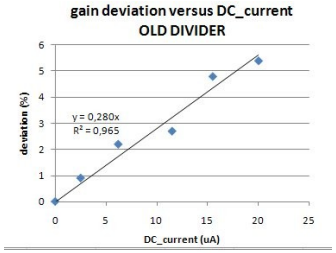
- Later necessary to test solutions for water, electrical and optical connections

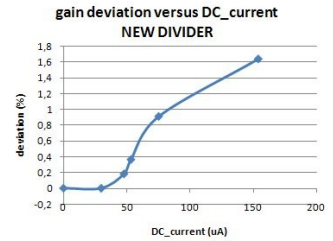
PMT dividers & HV supply

Clermont - Ferrand

Active dividers

- Active components in the last stages
- → linearity recovery at higher Luminosities.
  - Old Dividers: ~1% non linearity at ~ 3 μA
    ~2% ~ 7.5 μA
  - New Divider: ~1% non linearity at ~75 μA
    only 1.6% at ~150 μA
- Radiation sensitivity of active parts must be verified





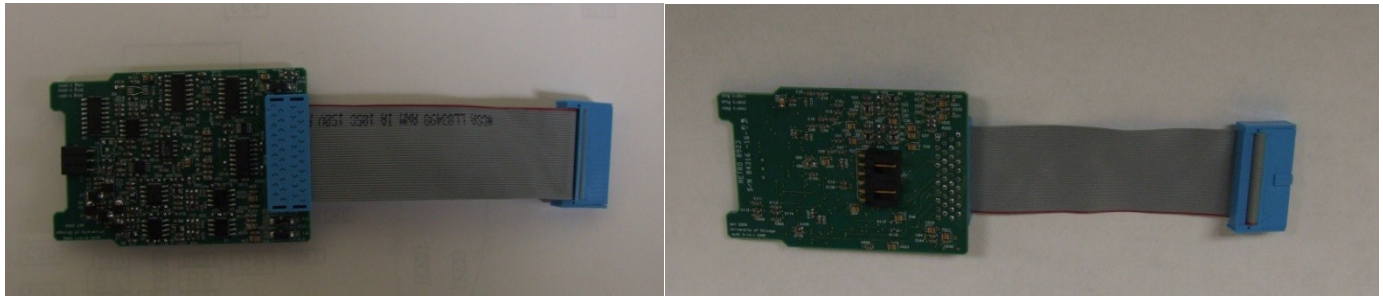
HV-regulation

6 alternatives

On Drawers	USA15
Option 0: Full re-use - Aging: at least 15 years old in 2019. - Radiations? True radiation level waited. - Compatibility with new Drawers. - No R&D manpower, except maintenance.	Option 3: Re-use of present cards - Aging: at least 15 years old in 2019. - Integration in USA Racks: space? - Long cables for services + Drawer Bus. - R&D manpower : 2.0 FTE (0.5Ie, 0.5Te, 0.5Tm + 0.5 on-line)
Option 1*: New design with COTs - New radiation tests. - New design. - R&D manpower: 4.0 FTE (2Ie, 1Te + 0.5 Test Benches + 0.5 on-line)	Option 4*: New design - Conception and integration in USA15, including HV source (commercial?). - Long cables for services + Drawer Bus. - R&D manpower : 3.5 FTE (1.5Ie, 0.5Te, 0.5Tm, + 0.5 Test Benches + 0.5 on-line)
Option 2*: New design with radhard components … COST! - Radiation tests to validate. - New design - R&D manpower : 4.0 FTE (2Ie, 1Te + 0.5 Test Benches + 0.5 on-line)	Option 5: Commercial solution (CAEN?) … COST! - Integration and long cables for services + Drawer Bus. - R&D manpower : 1.5 FTE (0.5Ie and Te, 0.5Tm + 0.5 on-line)

FEB1 – Modified 3-in-1 boards

Chicago



- Compatible with (i.e derived from) existing system with the 3 functions:
  - Analog signals to be sampled by 2x12 bit high and low gain
  - Charge injection calibration
  - Integrator to read out Cesium calibration data
- Prototypes built and tested
- Improved functionality - Better linearity
- Radiation test successful

FEB2 – ASIC solution

Clermont - Ferrand

- Well advanced project IBM 130 µm technology,
  1st run back from foundry

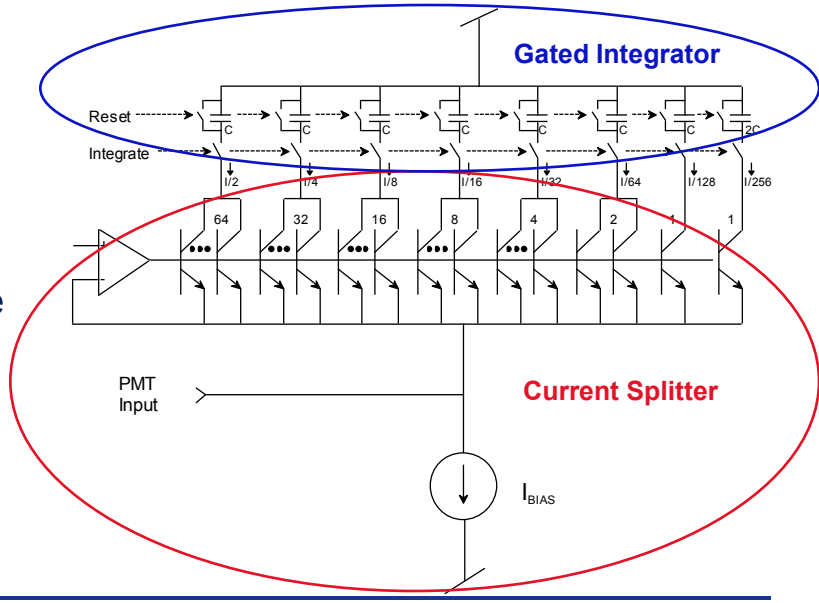
- Key points
  - Operating in current mode → better adapted to PMT
    ⇒ low noise, low sensitivity to voltage power supply.
  - Operating at 80 MHz ⇒ improved noise reduction.
  - Only 1 voltage supply requested for ASIC,
    1 or 2 voltages likely for the DACs.
  - Low power consumption.
  - Low radiation sensitivity ← choice of IBM technology by CERN.
  - Possibility to adjust peaking time externally .
  - to apply optimal filtering inside ASIC (many samples at 80 Mhz).

- Environment
  - DACs outside ASIC but on 3in1 card.
  - LV regulators on 3in1 card.
  - Design compatible with Chicago studies concerning commands, data flow, interface (GBT) in the Drawer (Chicago, Stockholm, Valencia…).

FEB3 – QIE ASIC solution

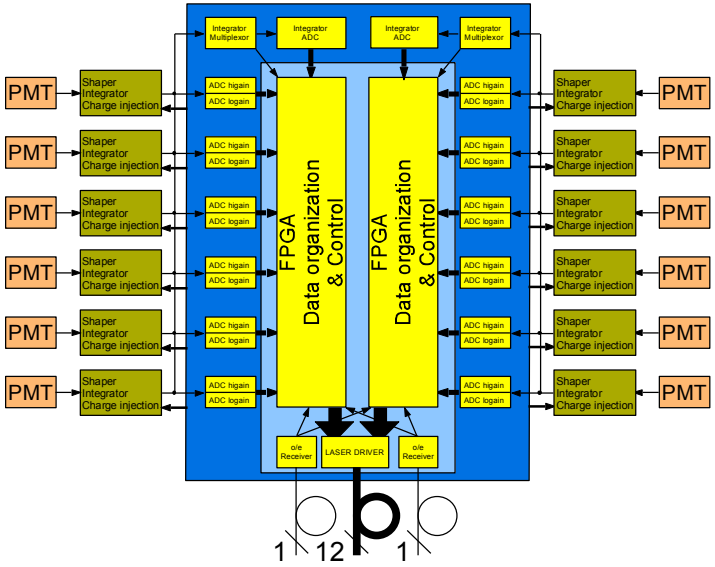
Argonne National Laboratory

- Custom IC family developed at Fermilab over 20 years
  - Currently being used by CMS HCAL
- Present features:
  - "Current Splitter" with 8 (or 4) binary ranges
  - 53 MHz (or 40) operation
  - Pipelined operation
  - On-board flash ADC
  - Dead-timeless digitization
  - 16 bits of dynamic range
  - ~10 fC least count resolution
- New design → In progress
  - Add internal TDC – 1 nSec resolution
  - Improved radiation tolerance → 0.35 micron SiGe
  - Development in collaboration with CMS HCAL
- Status
  - 2 prototypes designed and tested
  - 1st fully-functional version ~Fall, 2011



MainBoard + DaughterBoard

Chicago - Stockholm

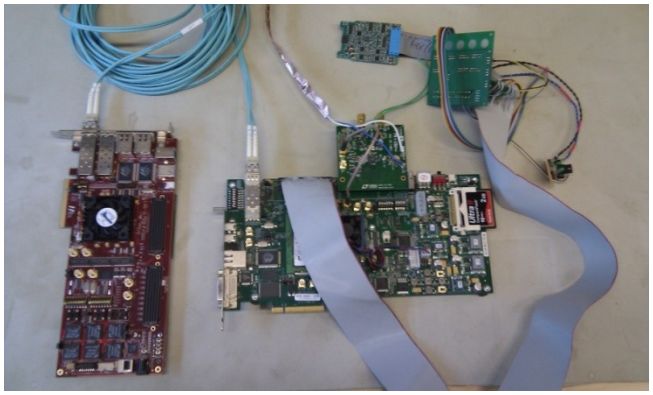


- Two independent parts – MainBoard and Daughter board
- 4-fold redundancy – all fibers duplicated and 2 channels (on different fibers) per cell
- The Clock, Trigger and Control is obtained via the GBT protocol
- Early prototypes are being developed
- Should be FE-board agnostic

MainBoard + DaughterBoard

Stockholm - Chicago

See poster:
A Full Slice
Test Version of
a Tentative ….



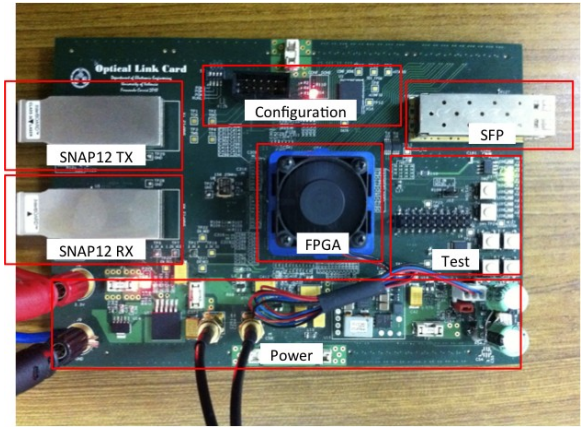
To study
functionality
and help develop
firmware and
software

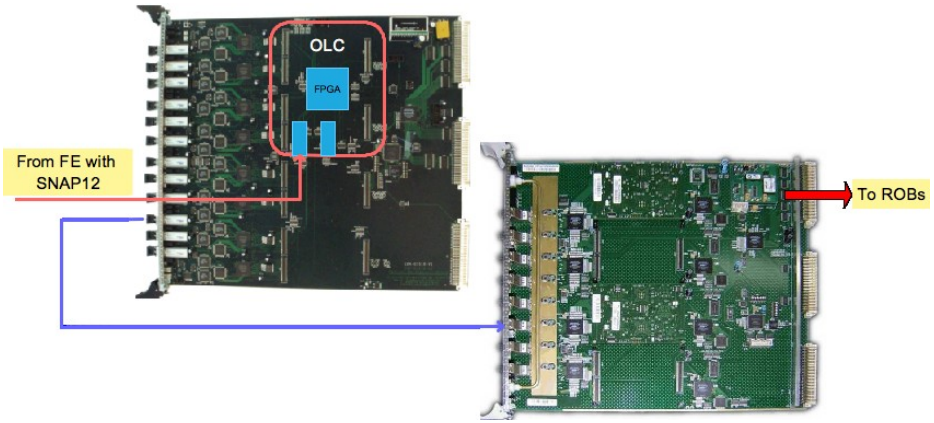
- A full readout chain test set-up consisting of:
  - A 3-in-1 FE board (1 channel with 2 gains)
  - A LTC2264-12 ADC evalution board emulating the MainBoard
  - A XILINX ML605 evaluation board emulating the DaughterBoard
  - 100 m fiber
  - A HiTech Global FPGA board emulating the off-detector electronics
  - A PC emulating an ATCA crate controller (with PCIe)

  The communication and clock distribution protocol is GBT.

Off Detector Electronics

Valencia - Lisbon





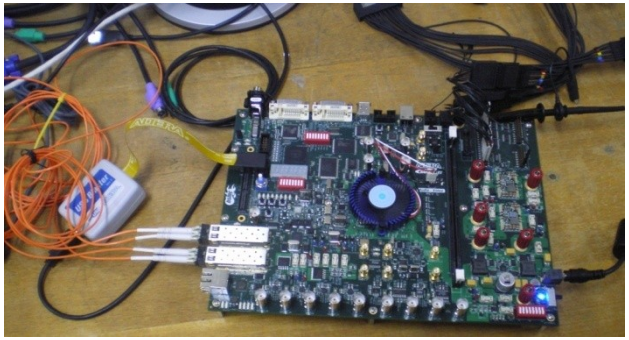
- The Optical Link Card is a demonstrator for studying and gaining experience with multifiber high speed links especially for application in the off detector electronics
- The card is now fully tested and allows transmission and reception of 12 optical fibers with GBT protocol at 4.8 Gbps (also tested with raw protocol at 6.25 Gbps)
- Pin to pin compatible with ROD PU's and OMB PU's (allows testing of new front-end designs for the upgrade with existing backend system)

See poster: Evaluation of an Optical Link Card ….

Off Detector Electronics

Valencia - Lisbon

Xilinx Virtex-5 Eval Board



Altera Stratix II GX Eval Board

- Implementation studies for device occupancy and timing constrains when multiple GBT links working at the same time
  - Identify limitations in the instantiation
- Xilinx
  - Virtex-5: limit of 10 GBT links on available device
  - Virtex-6: ongoing
- Altera
  - Stratix II GX: no limitation (up to 12 transceivers)
  - Stratix IV GX: only simulation (no device available to test yet)

Summary

- There is a general consensus about how to build the upgraded on and off-detector electronics
- but different R&D projects to explore detailed solutions
- The results from these are necessary to determine the final solution