CMS Binary Chip (CBC) status

130nm CMOS chip for short strip readout at sLHC

contents
    introduction to CBC architecture
    first test results

ACES Workshop, March 2011
Mark Raymond, Imperial College.

CBC architecture

targeted at phase II short strips
>   ~2.5 – 5 cm
>   not contributing to L1 trigger

**binary unsparsified architecture**
>   chip & system simplicity, low power

main functional blocks
- fast front end amplifier – 20 nsec peaking
- comparator with programmable threshold trim
- 256 deep pipeline (6.4 us)
- 32 deep buffer for triggered events
- output mux and SLVS driver
- fast (SLVS) and slow (I2C) control interfaces

some target specs
- DC coupled to sensor – up to 1 uA leakage
- can be used for both sensor polarities
- noise: < 1000e for C_{SENSOR} ~5 pF
- power consumption
    > < 0.5 mW/channel for C_{SENSOR} ~ 5 pF
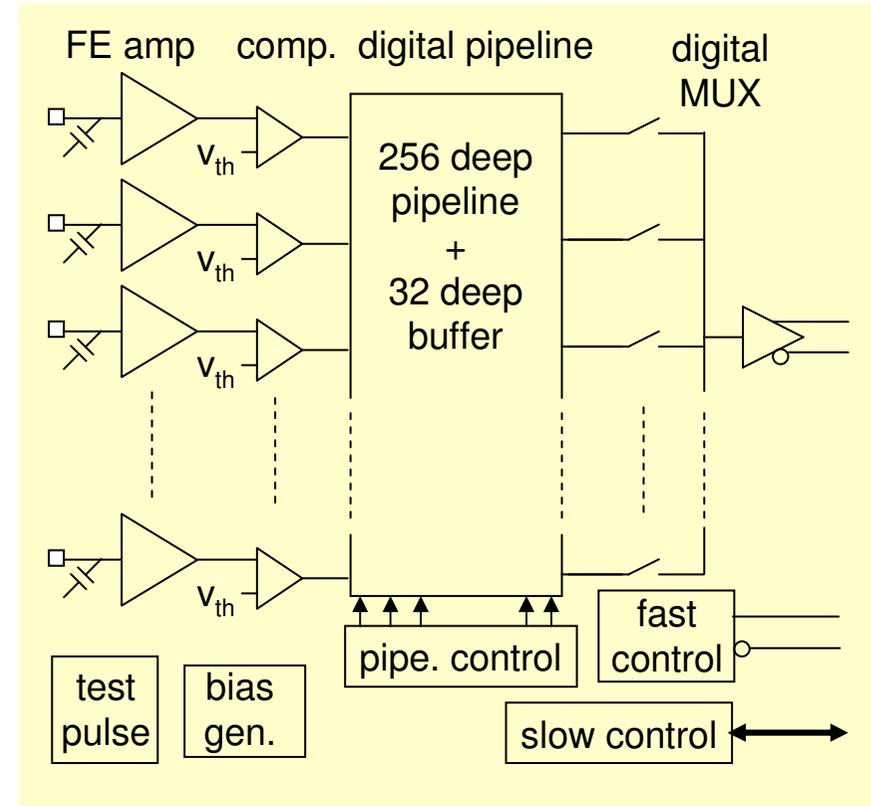
CBC front end
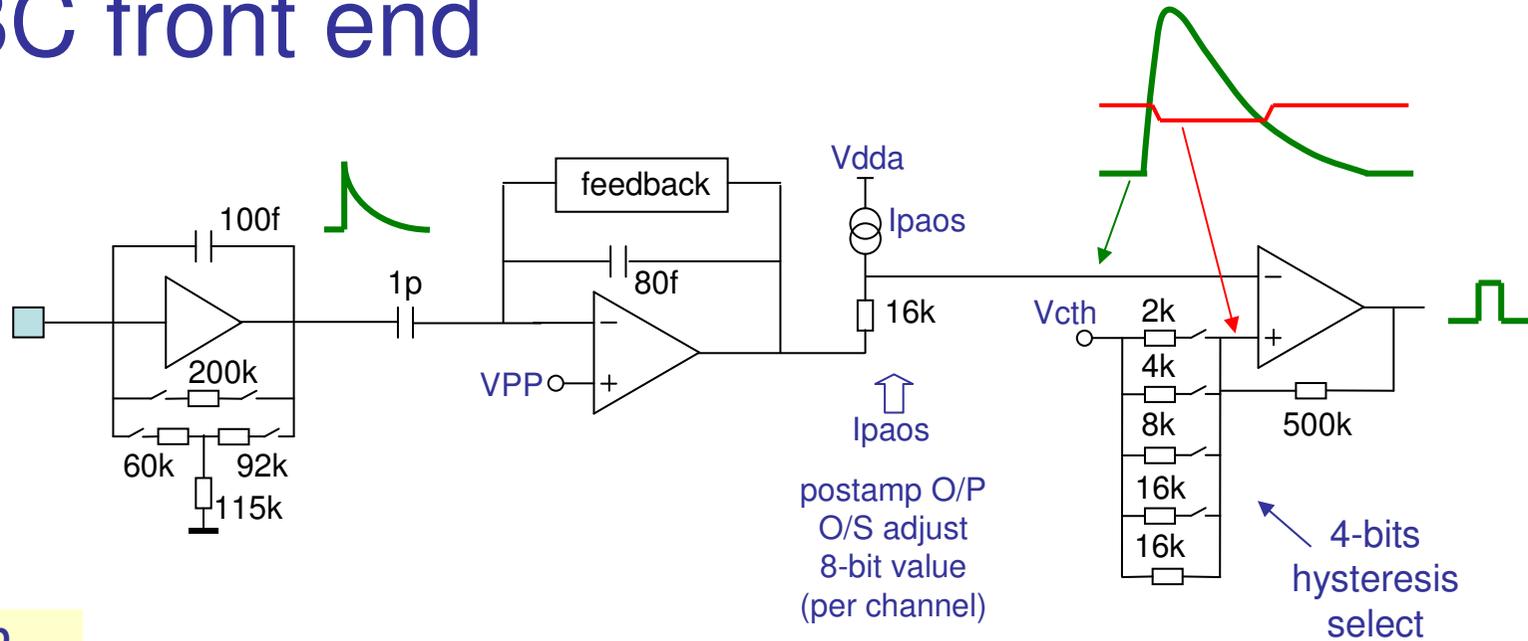
preamp
resistive feedback absorbs I_{leak}
T network for holes
Rf.Cf implements short
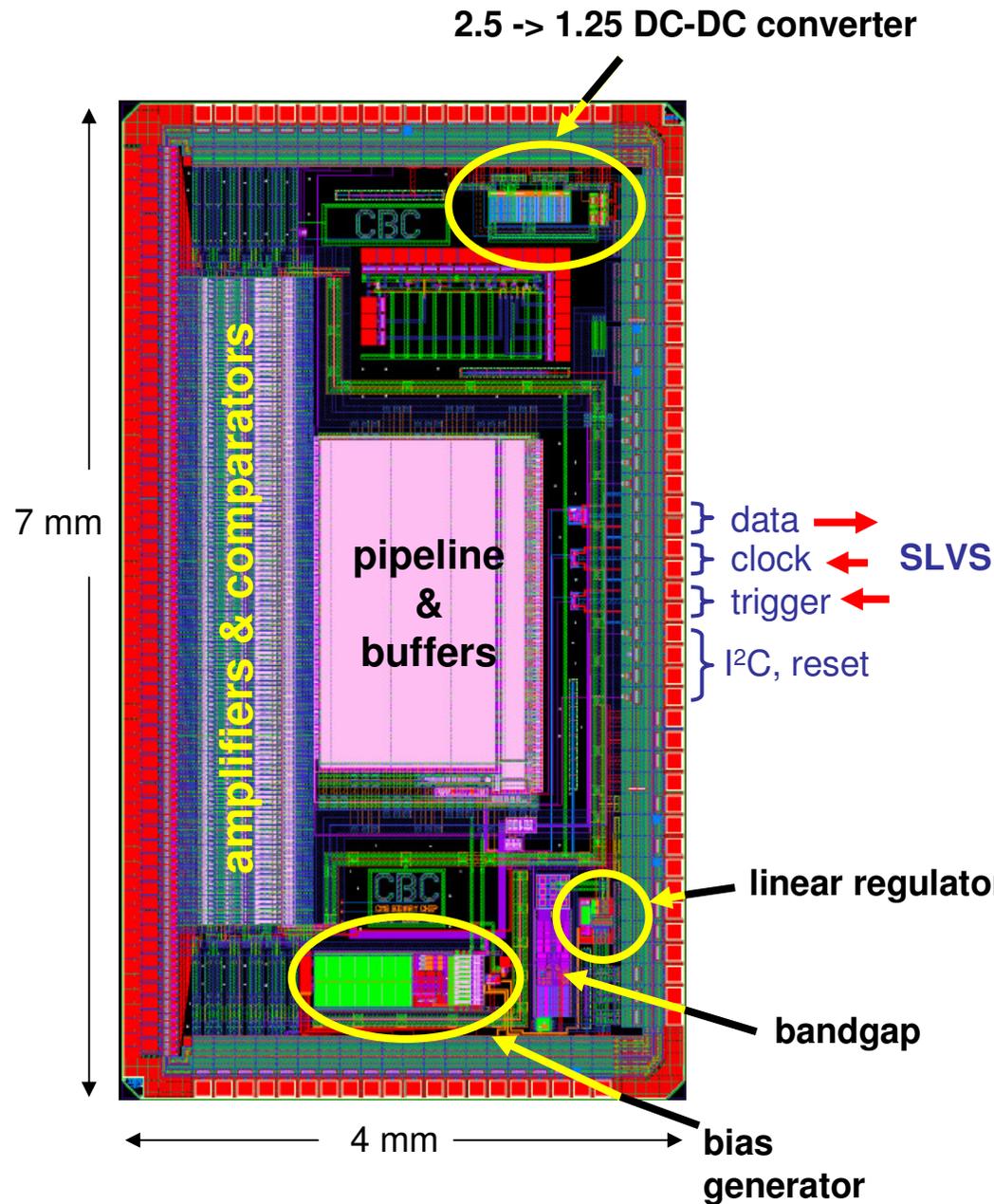20ns diff. time constant
(good for no pile-up)

postamp
provides gain and int. time constant
~ 50 mV / fC
AC coupling removes I_{leak} DC shift
individually programmable O/P DC level
implements channel threshold tuning
8-bits, 0.8 mV / bit, 200 mV range

comparator
global threshold
(indiv. tuning at postamp O/P)
programmable hysteresis)

Circuit labels: 100f, 200k, 60k, 92k, 115k, 1p, feedback, 80f, VPP, Vdda, Ipaos, 16k, Vcth, 2k, 4k, 8k, 16k, 16k, 500k, postamp O/P O/S adjust 8-bit value (per channel), 4-bits hysteresis select

CBC layout

2.5 -> 1.25 DC-DC converter

7 mm

4 mm

amplifiers & comparators

pipeline & buffers

CBC

CBC

} data →
} clock ← **SLVS**
} trigger ←
} I2C, reset

linear regulator for front end (LDO)

bandgap

bias generator

128 inputs, 50 μm pitch
back edge pads mostly power
but also data out, clock and trigger in
I2C slow control

power features included to study
     DC-DC switched capacitor
          CERN (M.Bochenek et al)
     low dropout linear regulator
          uses CERN bandgap (P.Moreira)

test features
     top edge: dummy channel with access
     to signals along analog chain

     bottom edge: access to all bias generator
     outputs

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status

chip design begun ~March 2009 in 130nm IBM CMOS
      Lawrence Jones (RAL engineer)
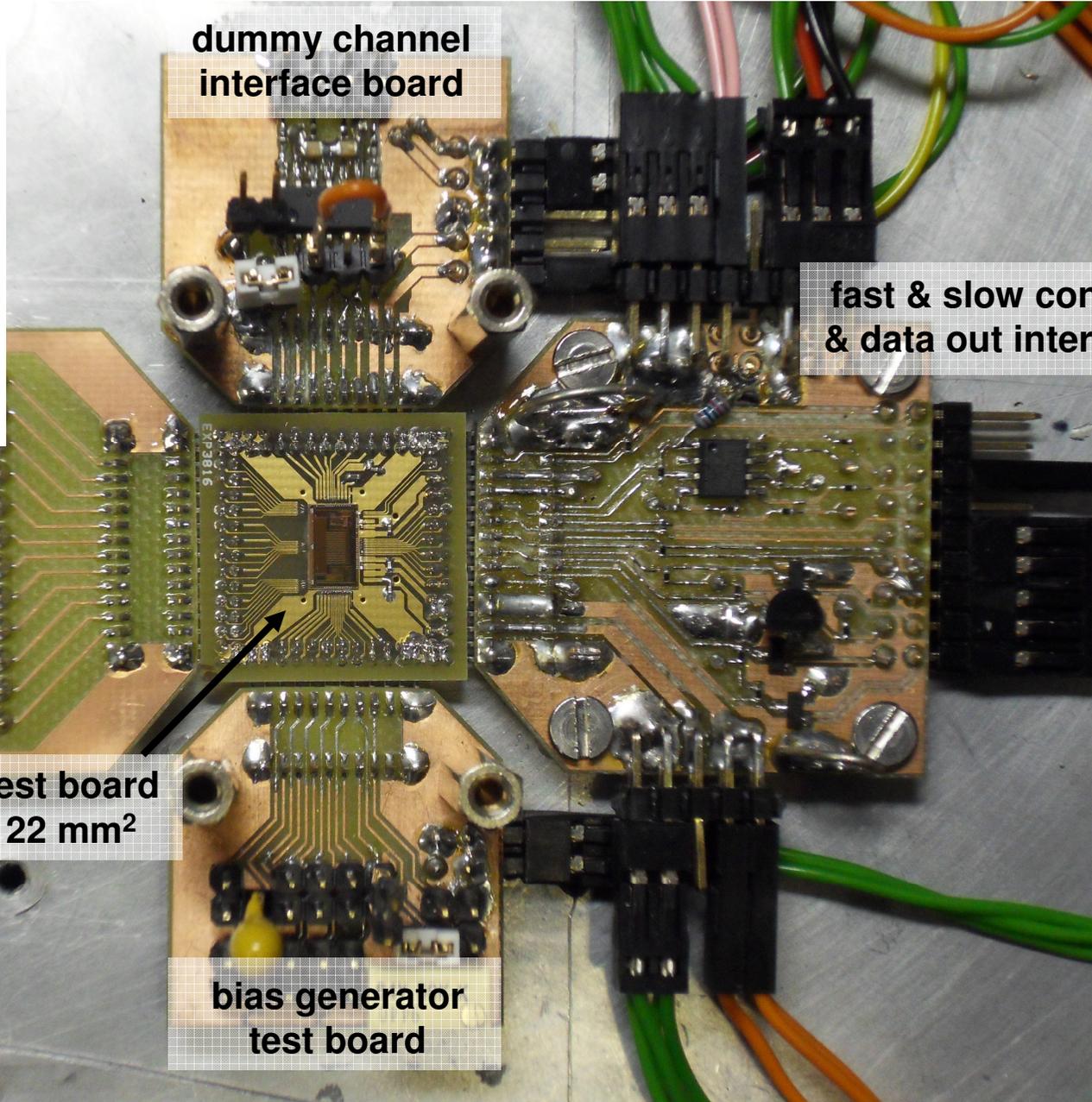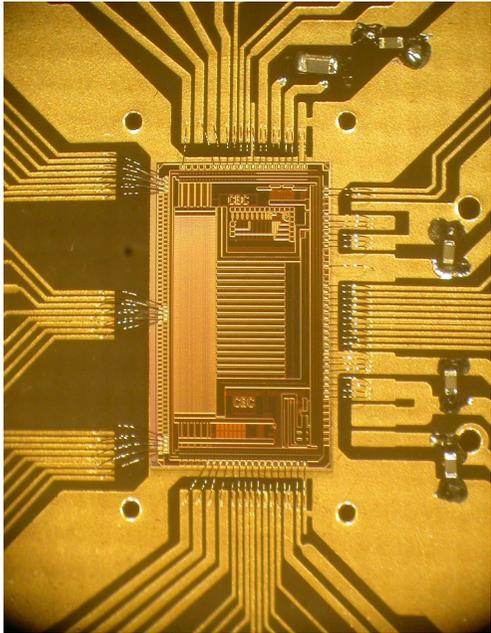
submission: July 2010, expected turnaround
      ~ 3 months (~ end October)

unexpected delays
      foundry busy with volume production
      wafers available just before Xmas – not diced till after

      => chips under test since 14th February

results here from a handful of die
      not all features yet investigated
        … and nothing at a thorough level

test setup
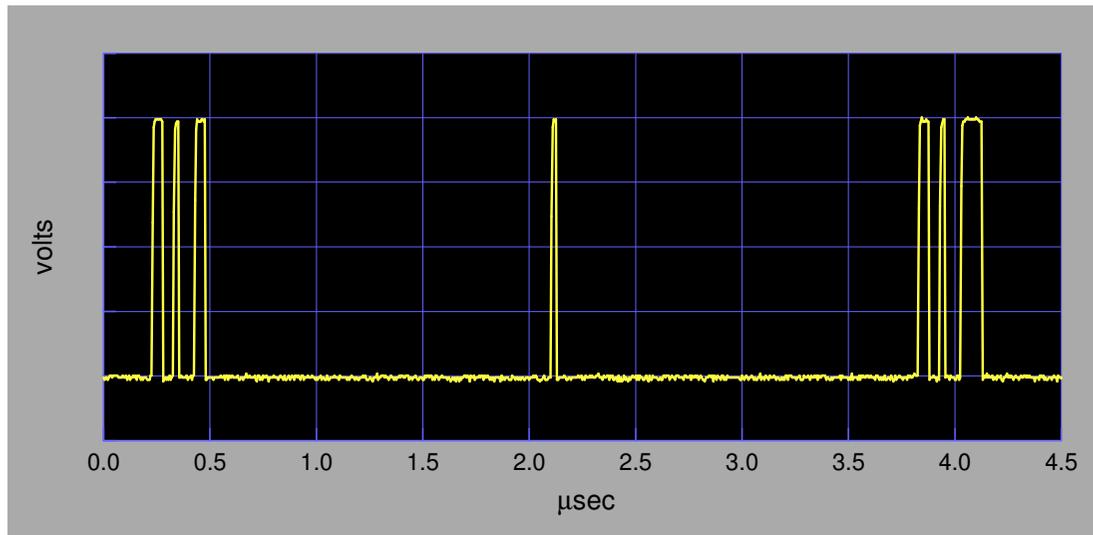
dummy channel interface board

fast & slow control & data out interface

test charge injection

CBC test board ~ 22 x 22 mm²

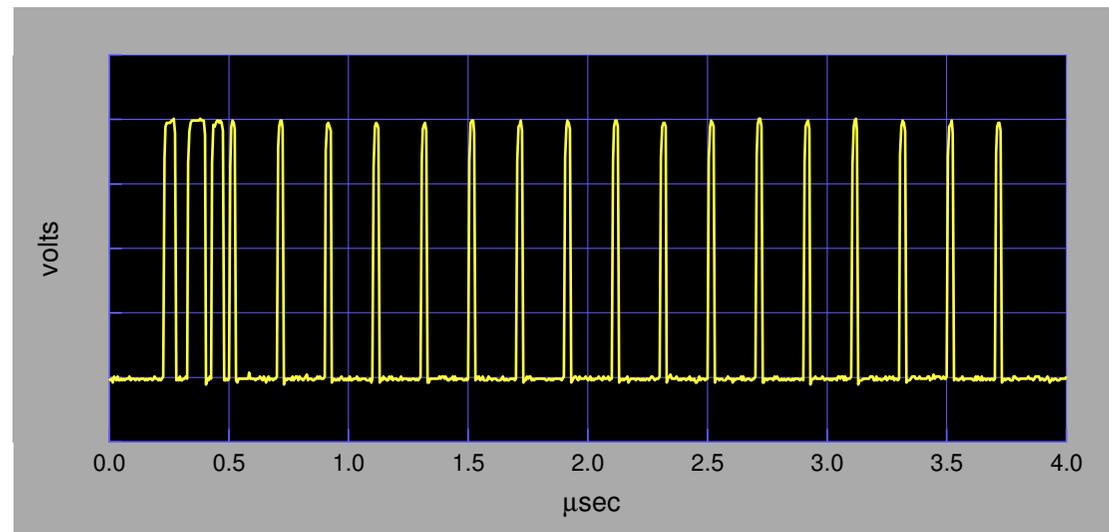bias generator test board

output data frame pictures

2 consecutive data frames (2 headers)
1 fC signal injected on one channel

data frame comprises:
  2 start bits
  2 error bits (latency, fifo overflow)
  8 bit pipeline address
  128 channel bits

16 "hits" produced by on-chip test pulse feeding every 8th channel
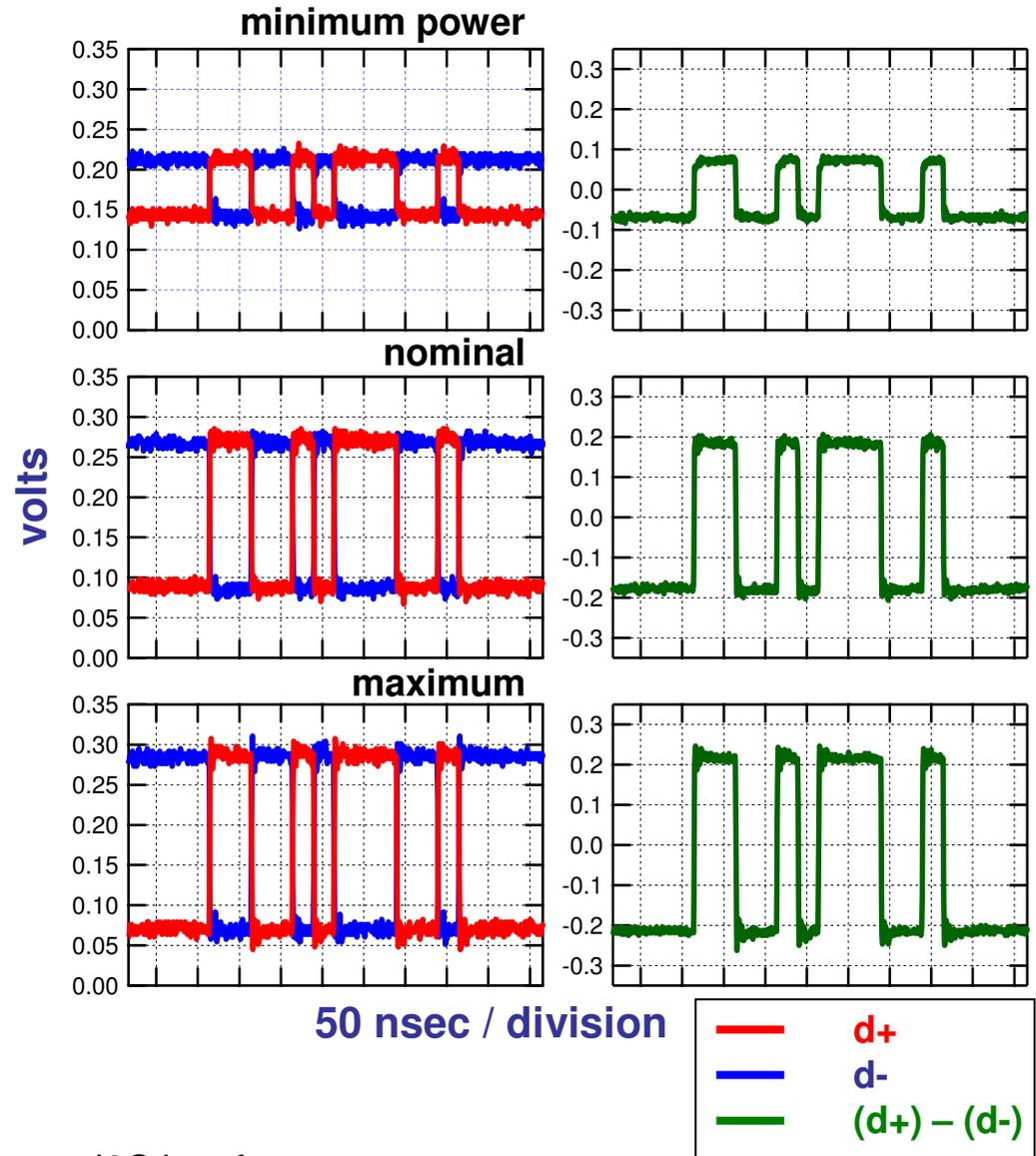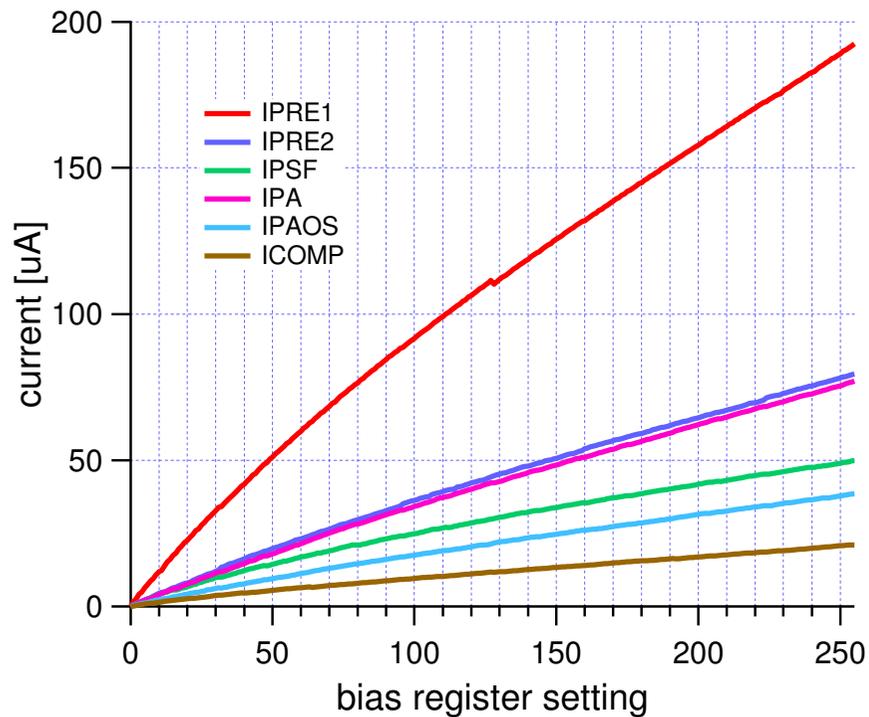
signal size ~ 1.5 fC

fast and slow control interfaces

SLVS interface circuits provided by CERN
S. Bonacini, K.Kloukinas

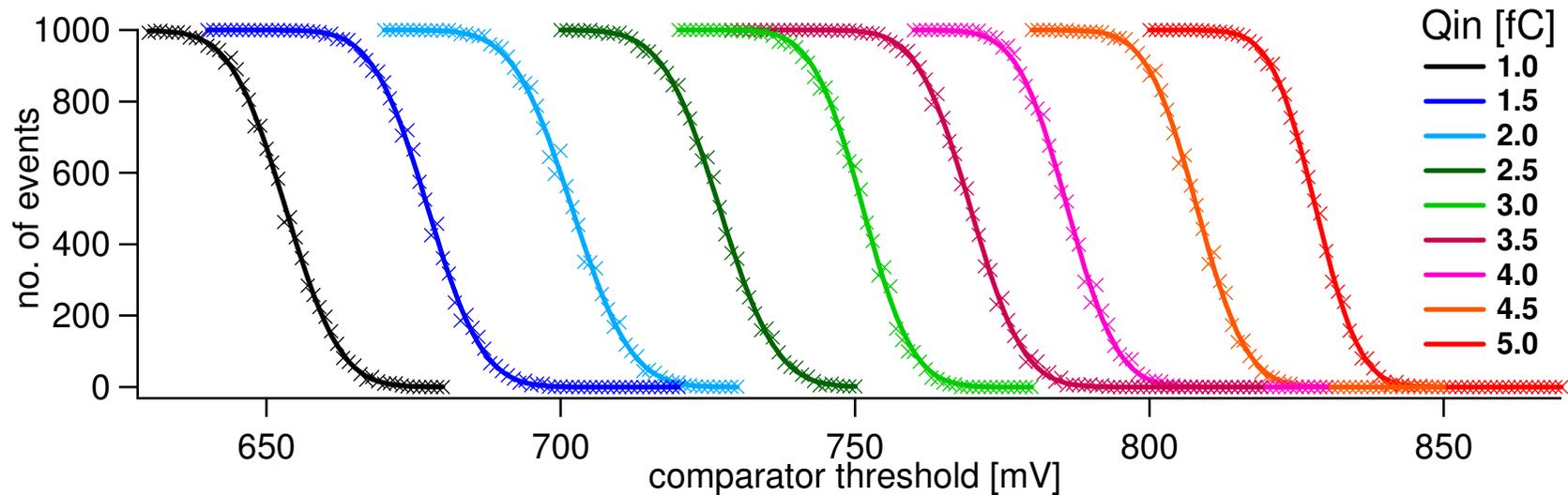programmable current (amplitude)
0.5 – 2.0 mA

pictures show digital header

minimum power

nominal

maximum

50 nsec / division

— d+
— d-
— (d+) – (d-)

I2C interface to programme
currents
voltages
operational modes
128 individual channel offsets

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S-curves & gain

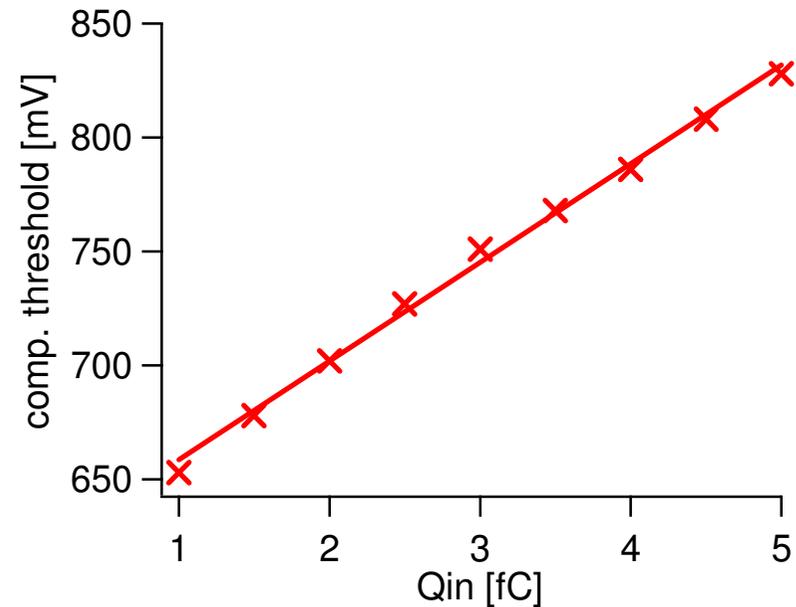can extract gain and noise by plotting S-curves

  sweep comparator threshold over range from where it fires all time to not at all

count no. of events exceeding threshold

repeat for different values of injected charge

plot S-curve mid-point vs. Qin to give gain $\longrightarrow$

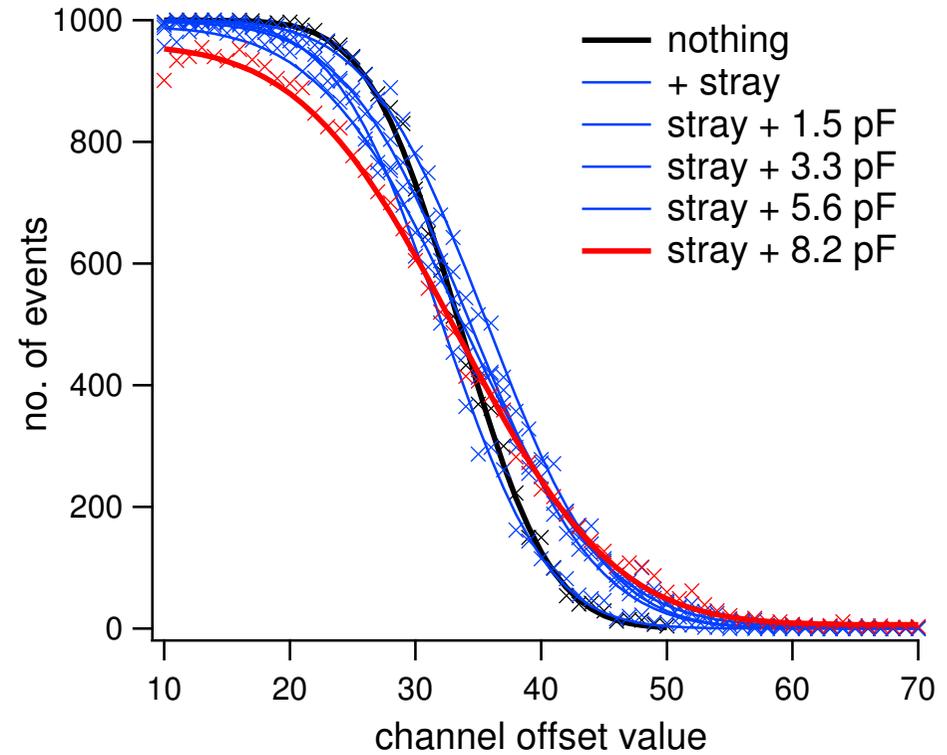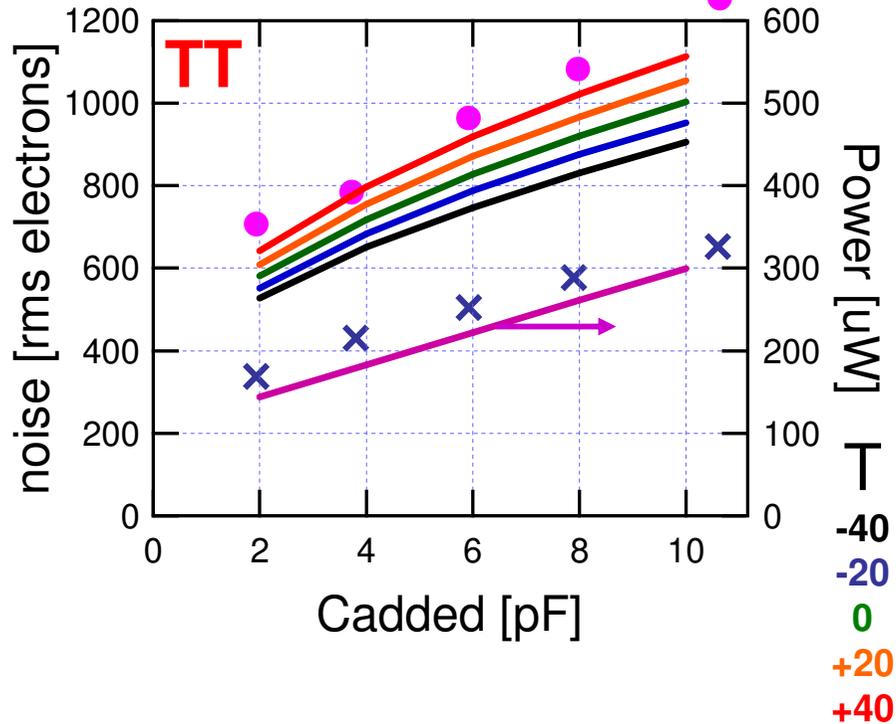 -> gain ~ 50 mV / fC (close to expectation)

noise

measure from fit to S-curves

technique needs refining
(accurate determination of stray cap.)

but results look believable
close to (bit worse than) expectation

← lines show simulation
(for different temperatures)

dots ● show noise measurements
at ✕ power/channel

(power tuned to maintain same pulse
shape for different sensor capacitance)

timewalk

measure by triggering same pipeline timeslice and sweeping charge injection time

smaller signals have to be injected earlier to exceed comp. threshold
within the sensitive (triggered) period
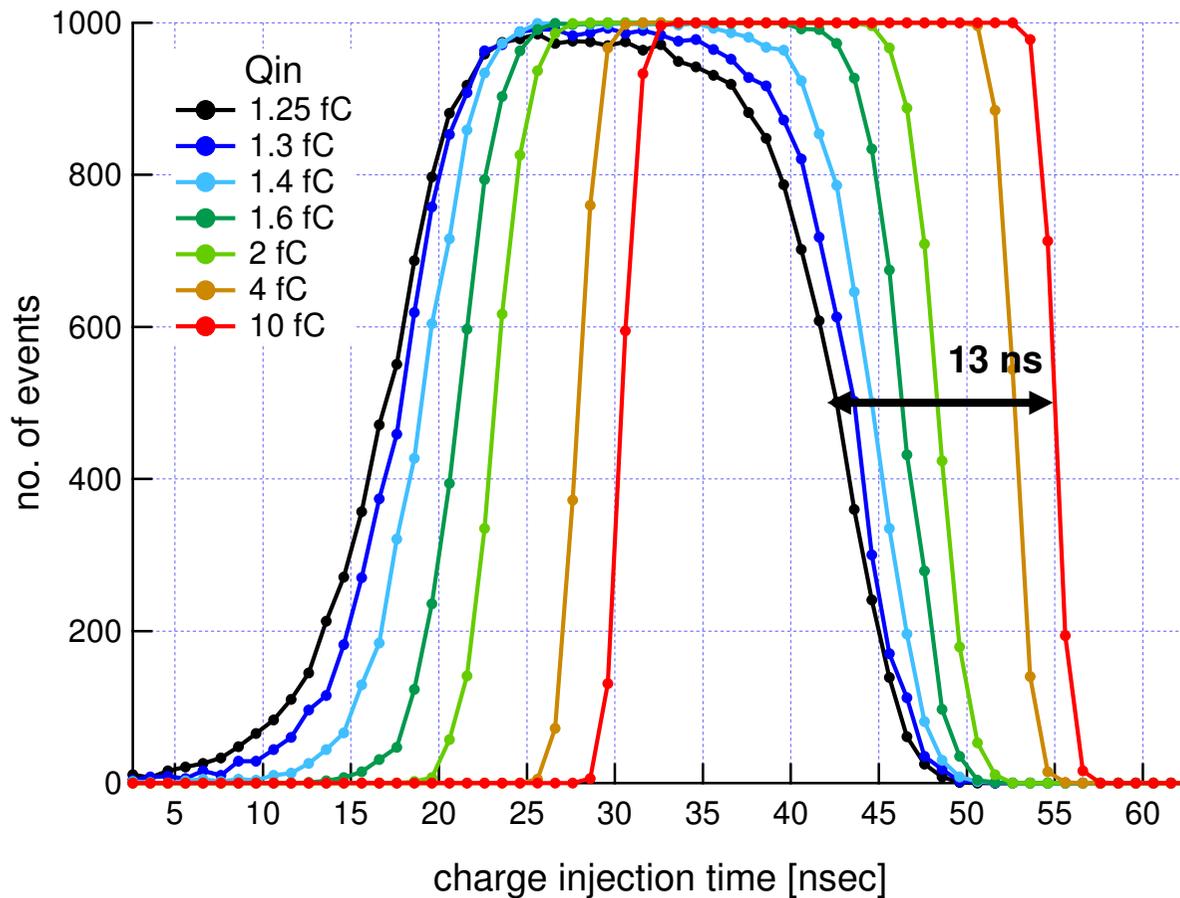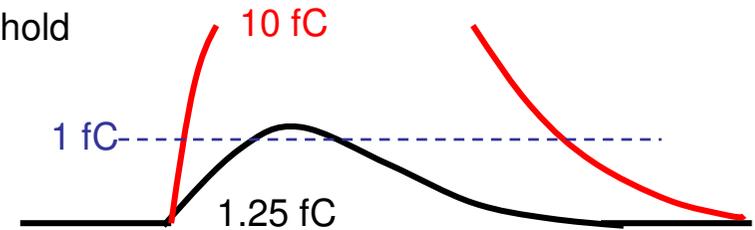
comparator threshold at 1 fC

timewalk specification:
   <16 ns between 1.25 and 10 fC
   signals with threshold at 1 fC

power consumption

target

> **0.5 mW / channel** based on

> **analogue**
>
>> **150 - 300 uW** depending on sensor capacitance

> **digital**
>
>> ~ **300 uW** based on rough estimates
>> (including 150 uW contingency)

measured

> **analogue**
>
>> have been biasing up to now in line with simulation
>>
>>> **150 - 300 μW / channel**
>
> **digital**
>
>> I_{VDD} = 2.8 – 4.5 mA for whole chip depending on SLVS bias setting
>>
>>> **< 50 μW / channel**
>>
>> no measurable dependence on L1 trigger rate (0 – 100 kHz)
>> digital circuitry functions correctly down to VDDD = 0.9V

> **total**
>
>> **200 – 350 uW / channel**
>
>> significantly less than original design target

summary

CBC seems to be working well

> still early days, but already seems clear that enough is working to allow us to learn as much as we need to from this prototype
>
> > works for both polarities
> > noise, gain, timewalk close to expectation
> > power consumption lower than estimated
> > powering features verified functional (see backup)

a long testing programme ahead, including

> powering options studies - supply sensitivity with/without various on-chip options
> temperature effects
> tests with sensors
> radiation: ionizing & SEU sensitivity
> test beam

future directions – currently looking at:

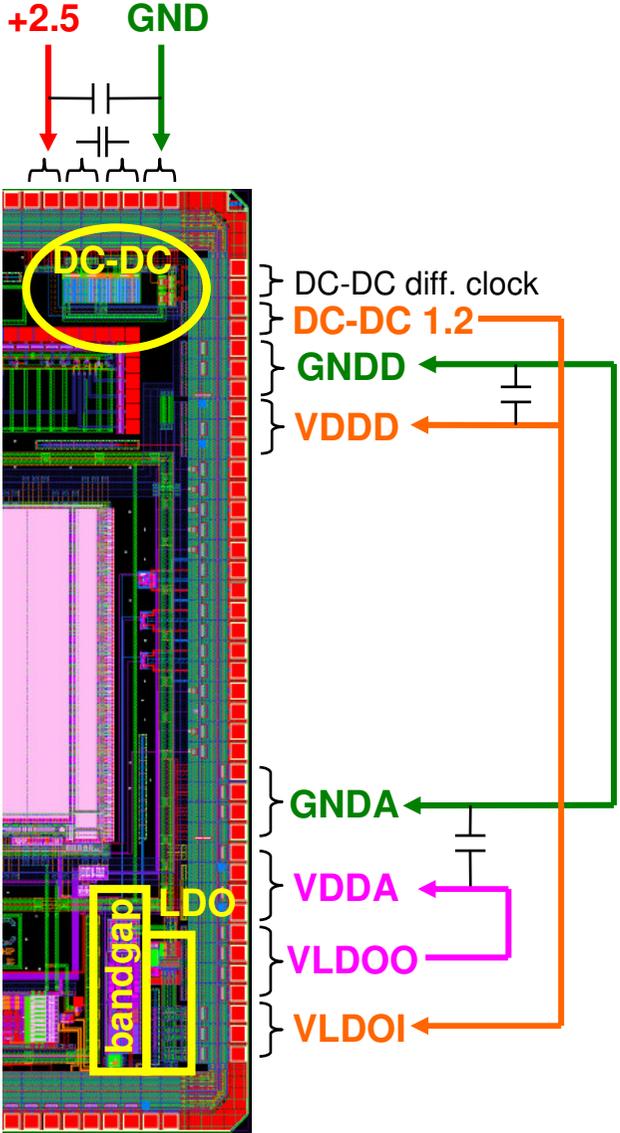> bump-bonded version – allows to integrate pitch adaption to sensor on hybrid
> 256 channel version with "2-in-1" triggering features (talk tomorrow)

CBC documentation:

> http://icva.hep.ph.ic.ac.uk/~dmray/CBC_documentation/

EXTRA

powering features

DC-DC switched cap. – CERN (M.Bochenek et al)
> converts 2.5 -> 1.2
> can use 1.2 to provide CBC digital rail (**VDDD**)
> and to feed LDO input (**VLDOI**)

have powered up and observed functionality - no detailed study

LDO linear regulator
> regulates 1.2V input to 1.1V output (**VLDOO**)
> can use to power analog circuitry (**VDDA**)
>> (analog front end designed for 1.1V operation)
> should provide good power supply rejection
> uses **CERN bandgap circuit** (P.Moreira) for ref. voltage

also appears to be functioning ok – again no detailed study

LDO output vs. input
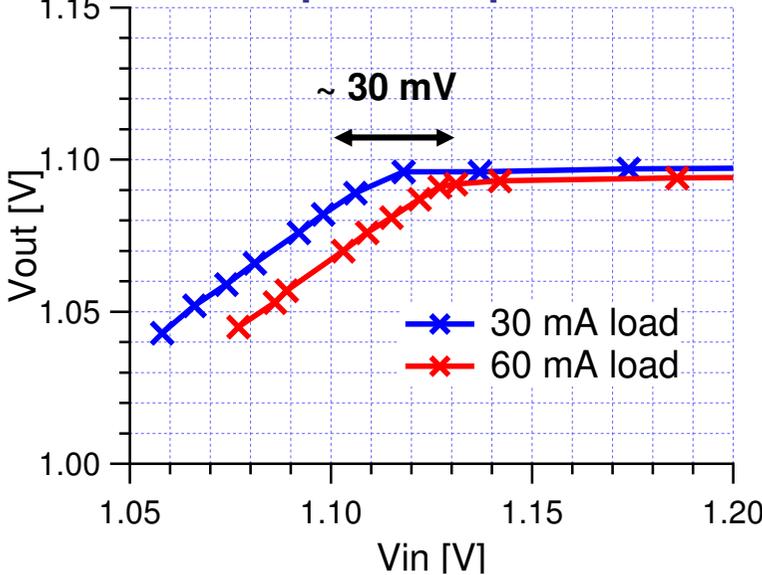
dropout ~ 30 mV
at 60 mA load

(normal analogue
current < 30 mA)

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channel uniformity
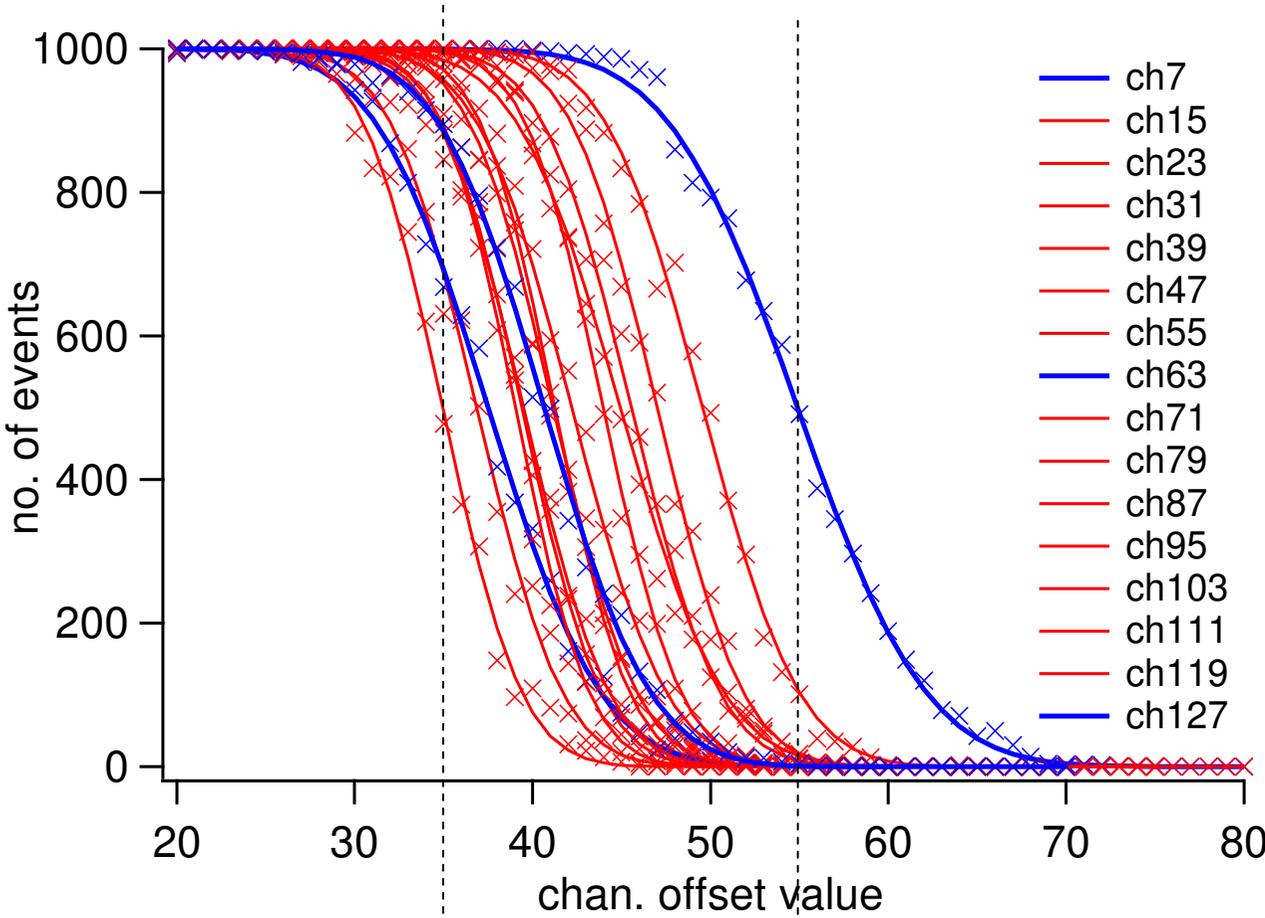
can investigate using on-chip
test charge injection

  (though don't know how
    uniform test capacitors are)

sweep channel offsets for all
16 channels simultaneously

spread ~ 20 offset units
= 17 mV (0.34 fC)

note: blue channels are those bonded
out to board
    => higher capacitance (noise)

testing programme

baseline performance (conventional (clean) powering scheme)

        digital functionality
            fast (Ck/T1 - SLVS) & slow control (I2C) interfaces setup and operation
        analogue functionality
            amplifier
                pulse shape, noise, linearity,..
                    C_{IN} dependence, signal polarity dependence, across chip & chip-to-chip uniformity
            leakage current tolerance
        comparator
            timewalk, threshold tuning and uniformity, hysteresis

        all above will depend on bias generator settings
            => large parameter space to cover   lots to study
        power consumption   have only scratched the surface so far

powering options studies
        supply sensitivity with/without various on-chip options

longer term
        temperature effects (~ all of above vs. T)
   tests with sensors
        radiation: ionizing & SEU sensitivity
        test beam

problems so far

not everything perfect – a couple of things have shown up so far

1) global comparator threshold voltage output (VCTH)
      get interaction between multiple channels and VCTH
          comparator has 500k feedback resistor (for hysteresis)
          but 128 x 500k resistors in parallel -> 4k (not so big)
          so VCTH gets pulled around if many channels switch at once
      would not have shown up on test chip with just a few channels
      can be fixed by providing external voltage
      probably not difficult to fix by design

2) another of the bias generator outputs needs external decoupling
      ~ similar effect associated with postamplifier

2) dummy analogue channel doesn't provide clean signals
      can be used to study DC behaviour, but transient response shows ringing
          may be due to test board layout – coupling between outputs and inputs
             will investigate further
      (not really an issue – but would have been if chip had not worked so well)

VCTH   2k

4k

8k   500k

16k

16k   4-bits
hysteresis
select

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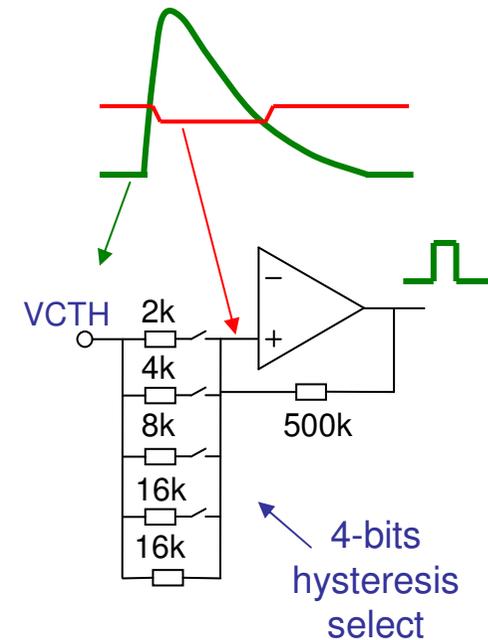
CBC-to-GBT interface

put e-port in separate GBT interface chip

incorporates circuitry to combine CBC data streams

extra chip on FE hybrid but could offer some future flexibility

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