MiniCactus CMOS timing DMAPS *
Sub 100 ps timing detector for future experiments

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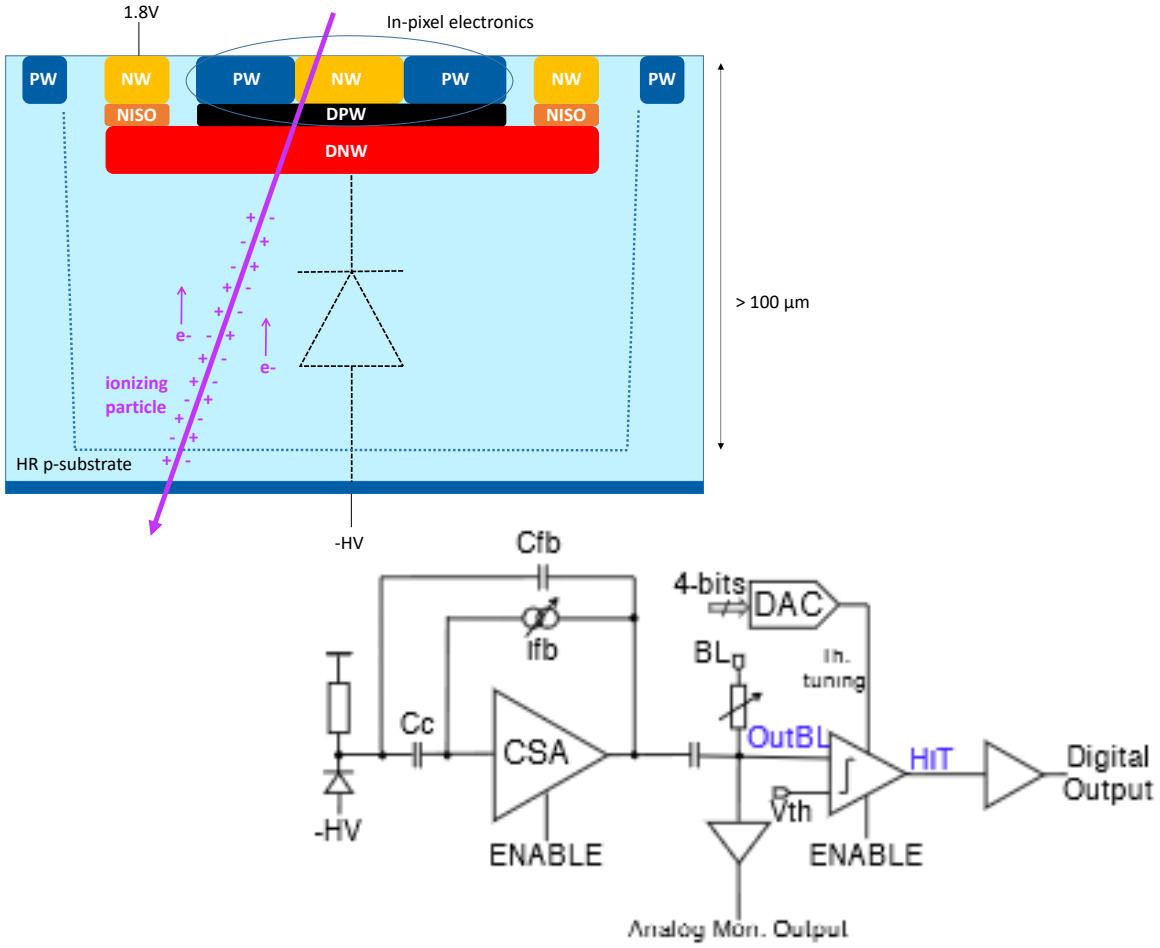
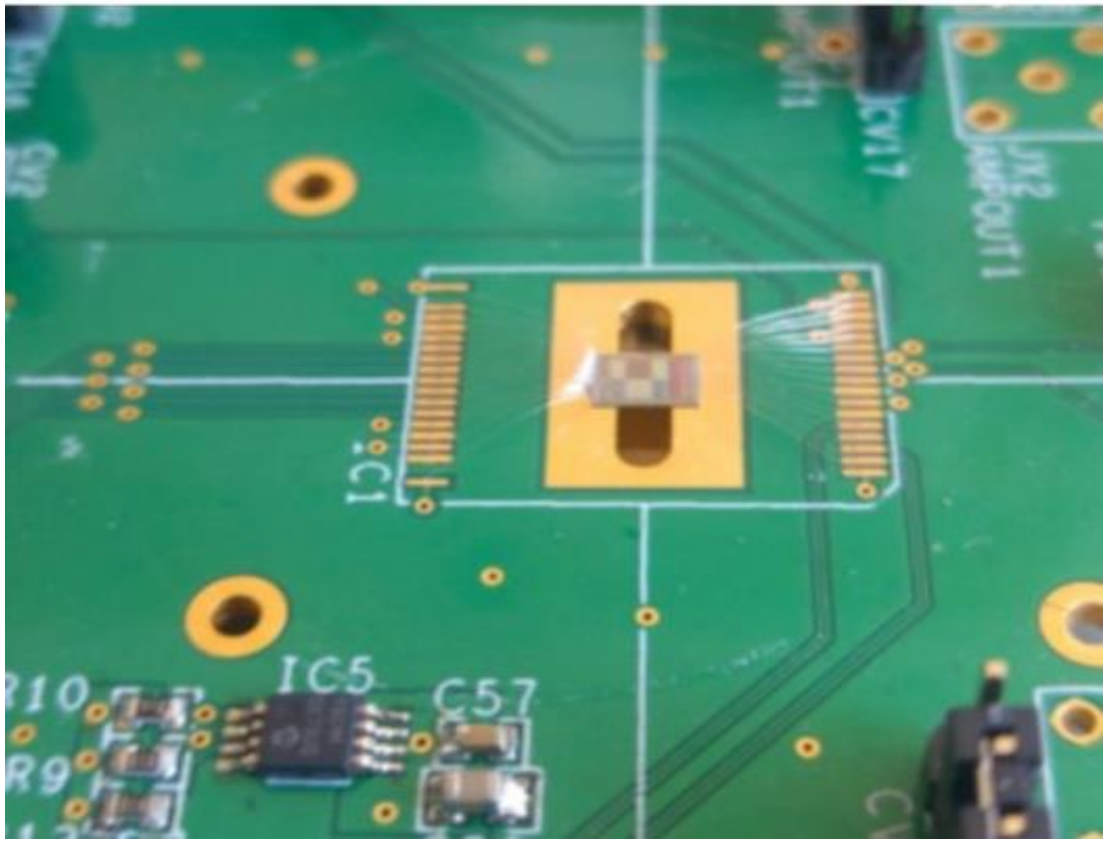
T. Hemperek (Bonn)

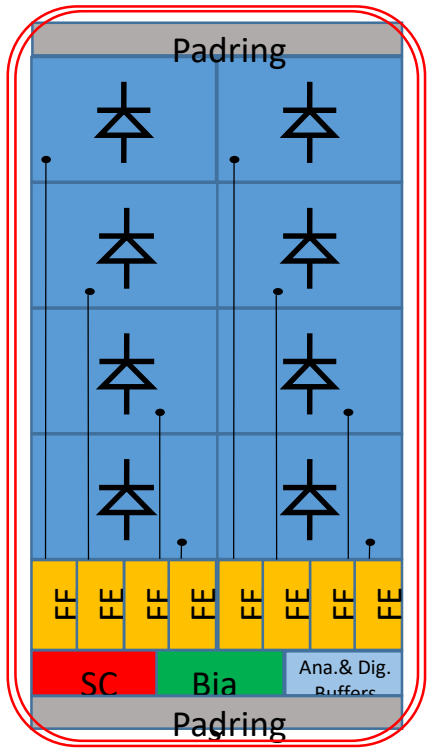




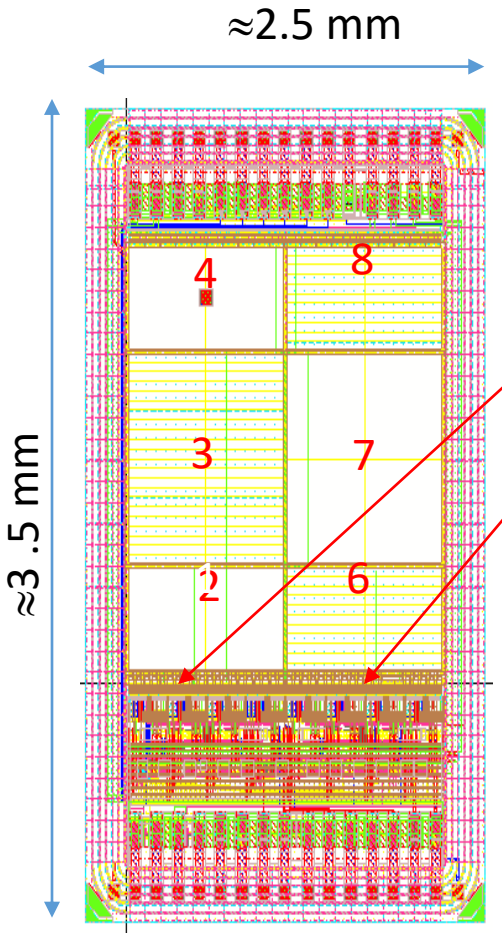
* Depleted Monolithic Active Pixel Sensors

MiniCACTUS Version2 of CACTUS (https://arxiv.org/abs/2003.04102)

Block diagram of the MiniCACTUS chip (not on scale).



Guard-rings



Pixel Flavors :

Pixels 3 & 7 : 1 mm x 1 mm baseline pixels
Pixels 2, 4, 6 & 8 : 0.5 mm x 1 mm pixels
Pixel 8 : 0.5 mm x 1 mm pixel with
in-pixel AC coupling capacitor (20pF)
Pixel 1 : 50 µm x 50 µm test pixel
Pixel 5 : 50 µm x 150 µm test pixel

For Version 2 called MINICactus:

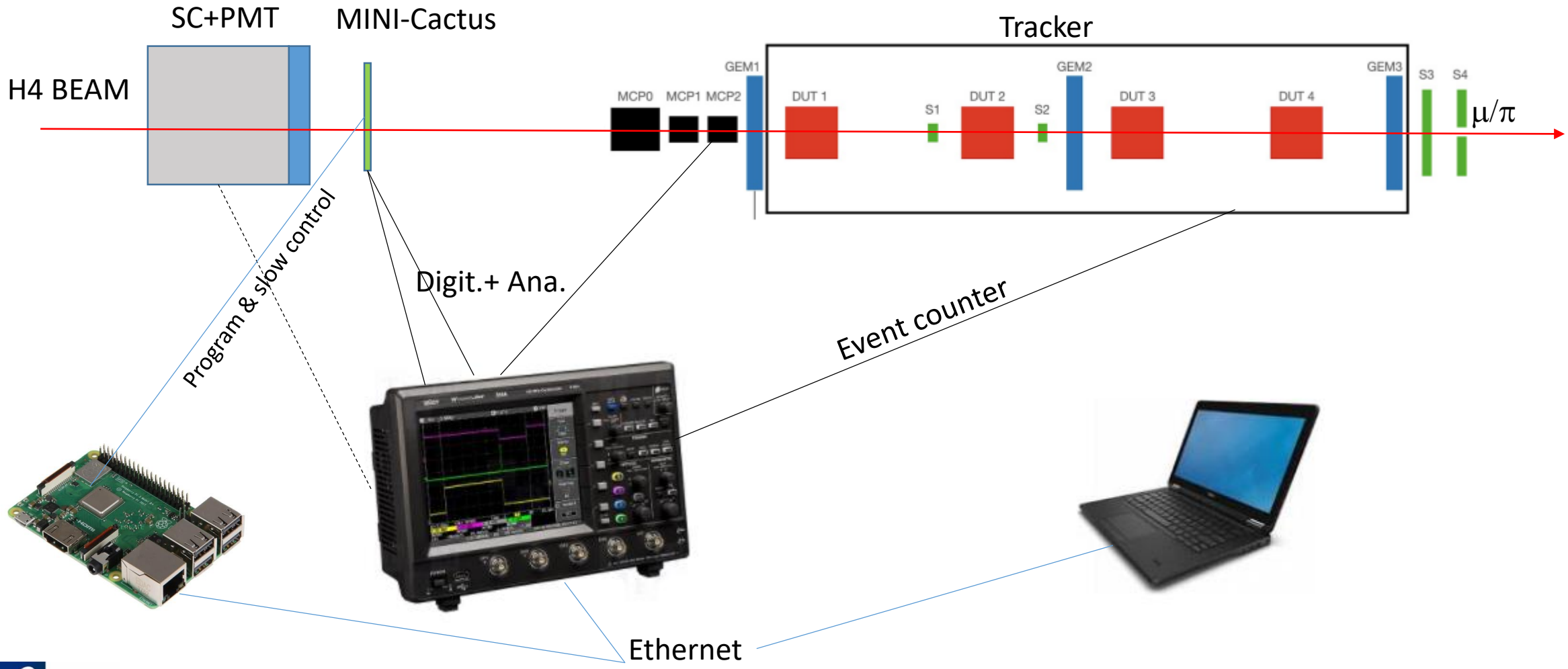
- Try several pixel sizes
- Different internal structure
- electronics outside pixel
- Front end optimized for 1x1mm2 pixel peaking time of 1-2 ns @ 1-2pF

Exist in 4 thicknesses:
-**700 µm** → no processing
3 different post processing
(sliming and back side metallization):
-**100** µm ; **200** µm and **300** µm

Test Beam Setup (parasitic mode RD51):

- Period 1: October 21 for ~2 weeks
- Period 2: mid-may 22 for ~3 weeks

Muon beam some times Pions at higher intensity which are difficult to use for timing because of pileup



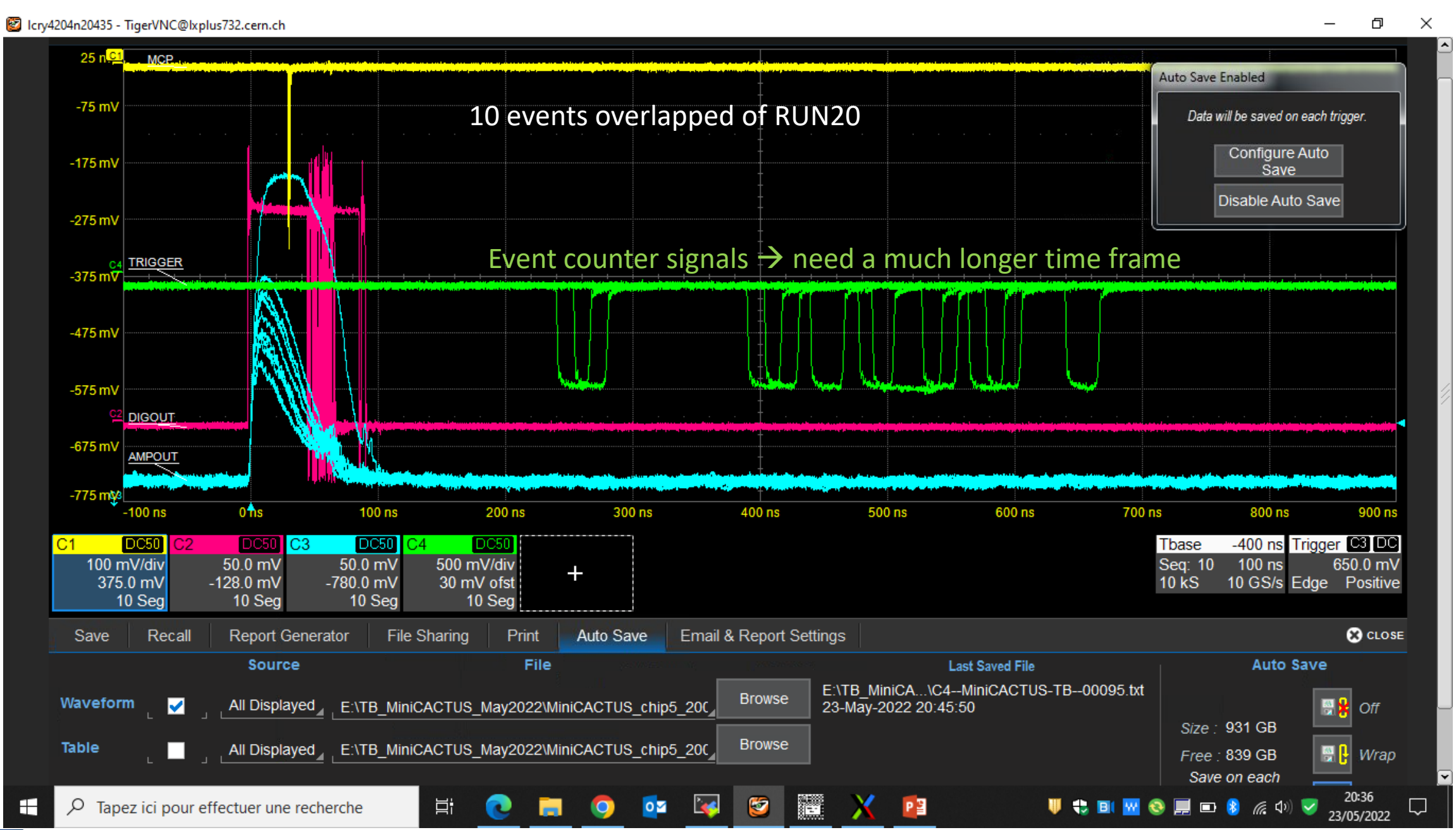
Data Taking

- During the 3 weeks of data taking we took about 560k events

- 3 thickness of chip have been tested:
  - ❑ 200μm Chip →DUT 5 and 6
  - ❑ 300μm Chip → DUT 3
  - ❑ 100μm Chip → DUT 8

- Main goal of the studies:
  - Front end parameter studies
  - HV Scan

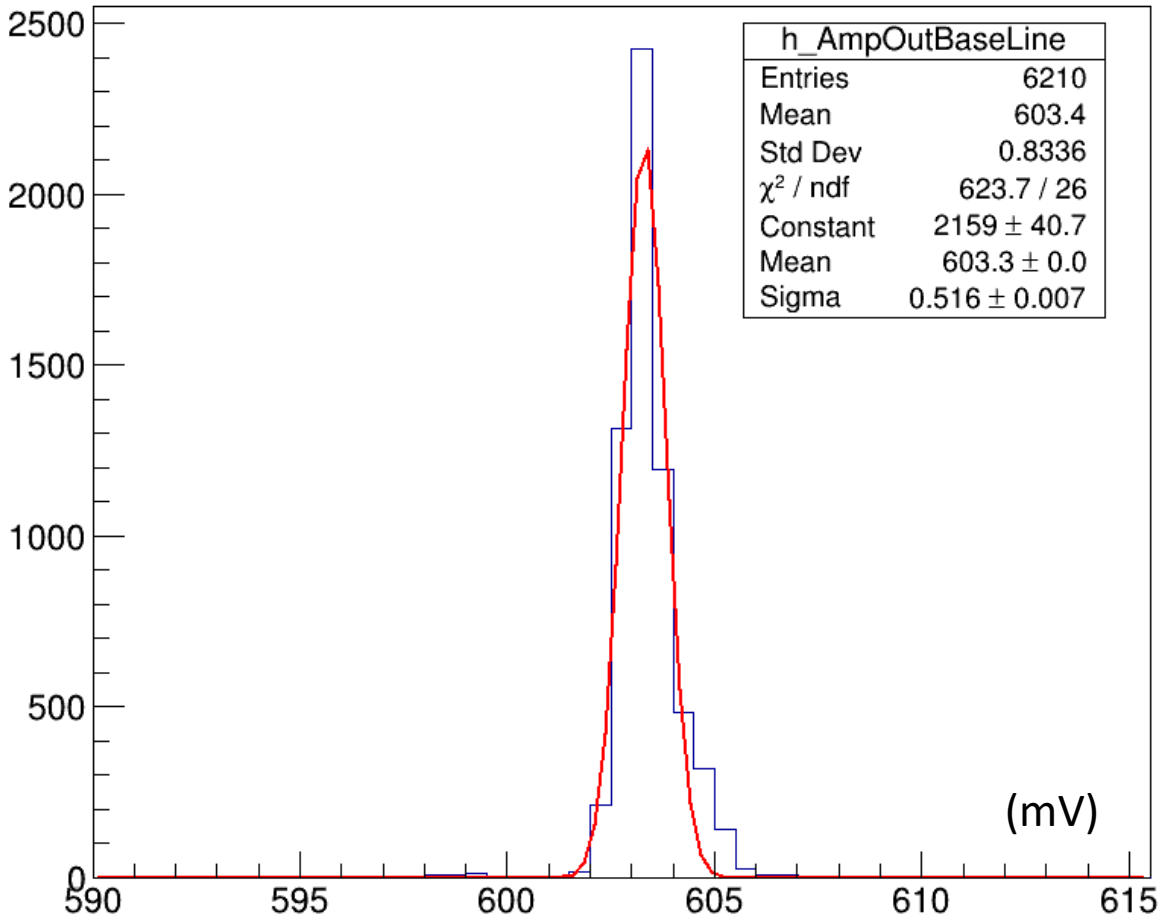
- Data were also taken with the RD51 tracking information (encoded event counter) for uniformity studies


Icry4204n20435 - TigerVNC@lxplus732.cern.ch
10 events overlapped of RUN20
Event counter signals → need a much longer time frame
MCP
TRIGGER
DIGOUT
AMPOUT
25 mV
-75 mV
-175 mV
-275 mV
-375 mV
-475 mV
-575 mV
-675 mV
-775 mV
-100 ns
0 ns
100 ns
200 ns
300 ns
400 ns
500 ns
600 ns
700 ns
800 ns
900 ns
Auto Save Enabled
Data will be saved on each trigger.
Configure Auto Save
Disable Auto Save
C1 DC50 100 mV/div 375.0 mV 10 Seg
C2 DC50 50.0 mV -128.0 mV 10 Seg
C3 DC50 50.0 mV -780.0 mV 10 Seg
C4 DC50 500 mV/div 30 mV ofst 10 Seg
Tbase -400 ns Seq: 10 100 ns 10 kS 10 GS/s
Trigger C3 DC 650.0 mV Edge Positive
Save
Recall
Report Generator
File Sharing
Print
Auto Save
Email & Report Settings
CLOSE
Source
File
Last Saved File
Auto Save
Waveform
All Displayed
E:\TB_MiniCACTUS_May2022\MiniCACTUS_chip5_20(
Browse
E:\TB_MiniCA...\C4--MiniCACTUS-TB--00095.txt
23-May-2022 20:45:50
Table
All Displayed
E:\TB_MiniCACTUS_May2022\MiniCACTUS_chip5_20(
Browse
Size : 931 GB
Free : 839 GB
Save on each
Off
Wrap
Tapez ici pour effectuer une recherche
20:36
23/05/2022

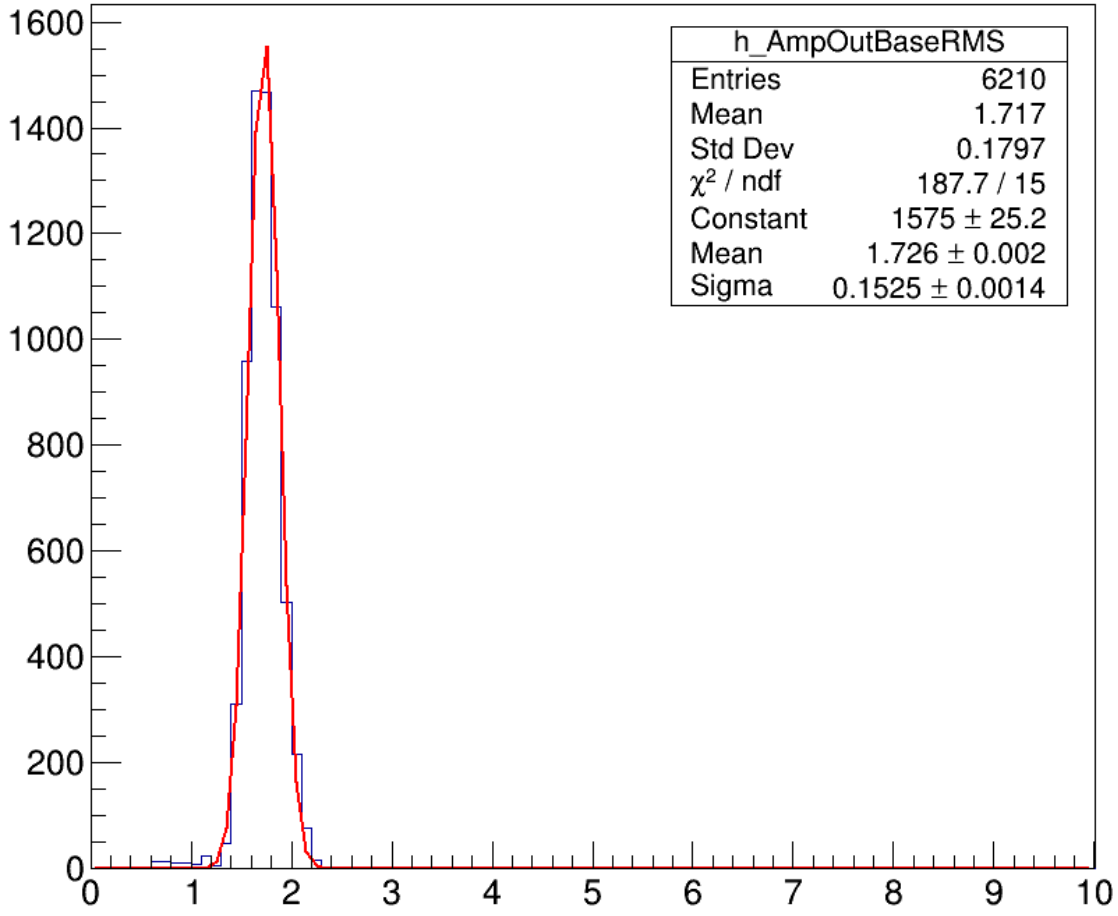
First good RUN on pixel 8 with optimized front end parameters and 500V on the chip

RUN15

Ampout Base Line Position (mV)

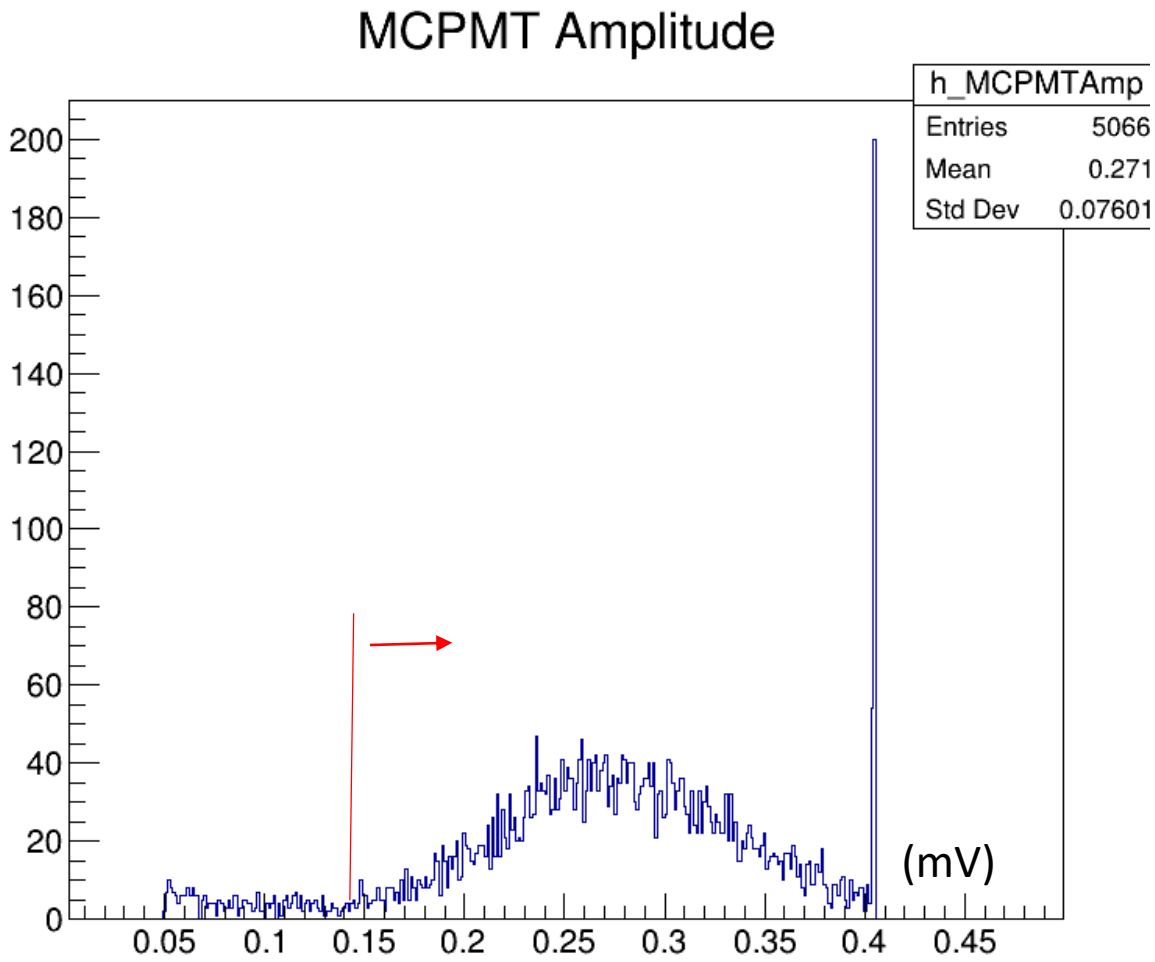


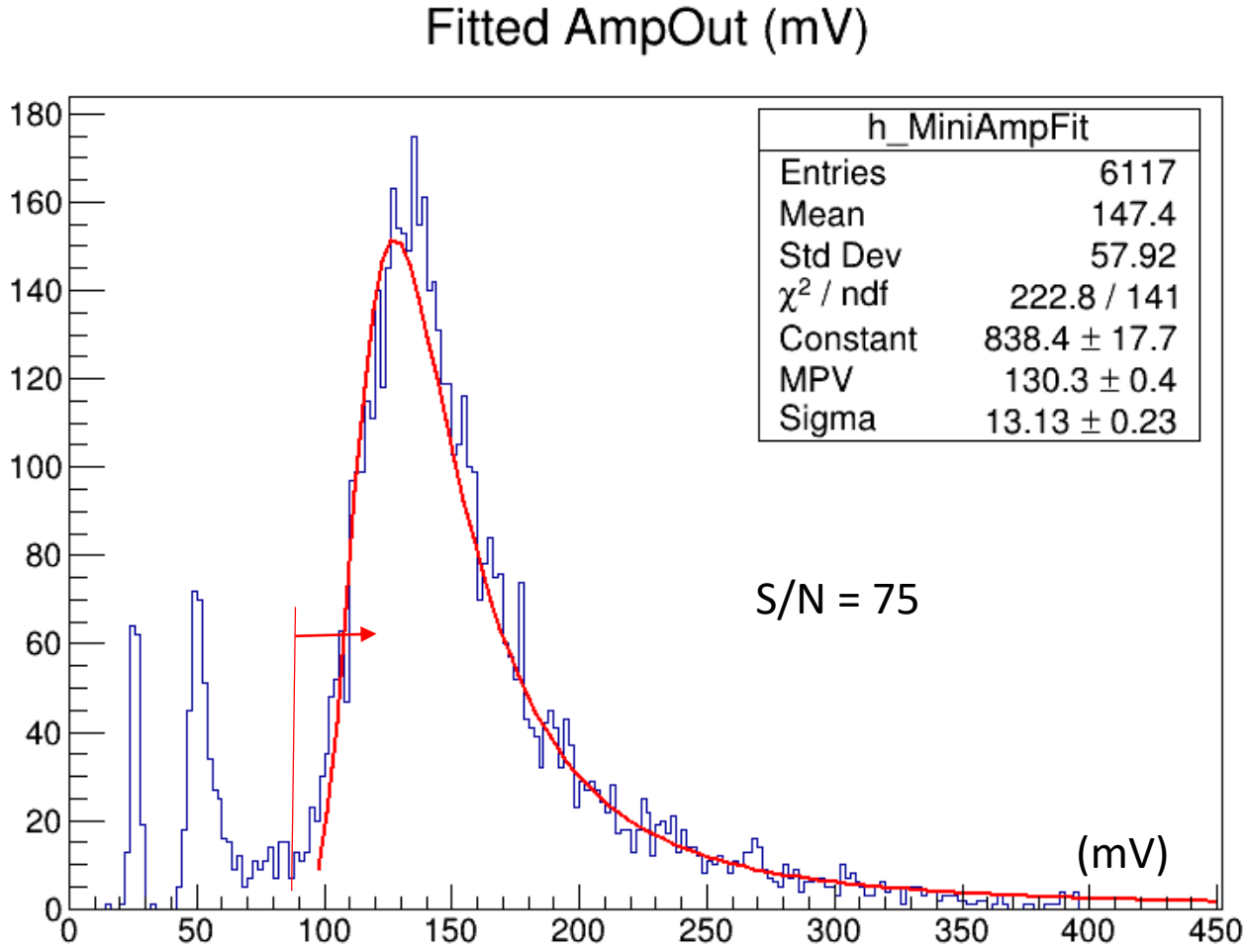
Ampout Base LINE RMS



Event Selection

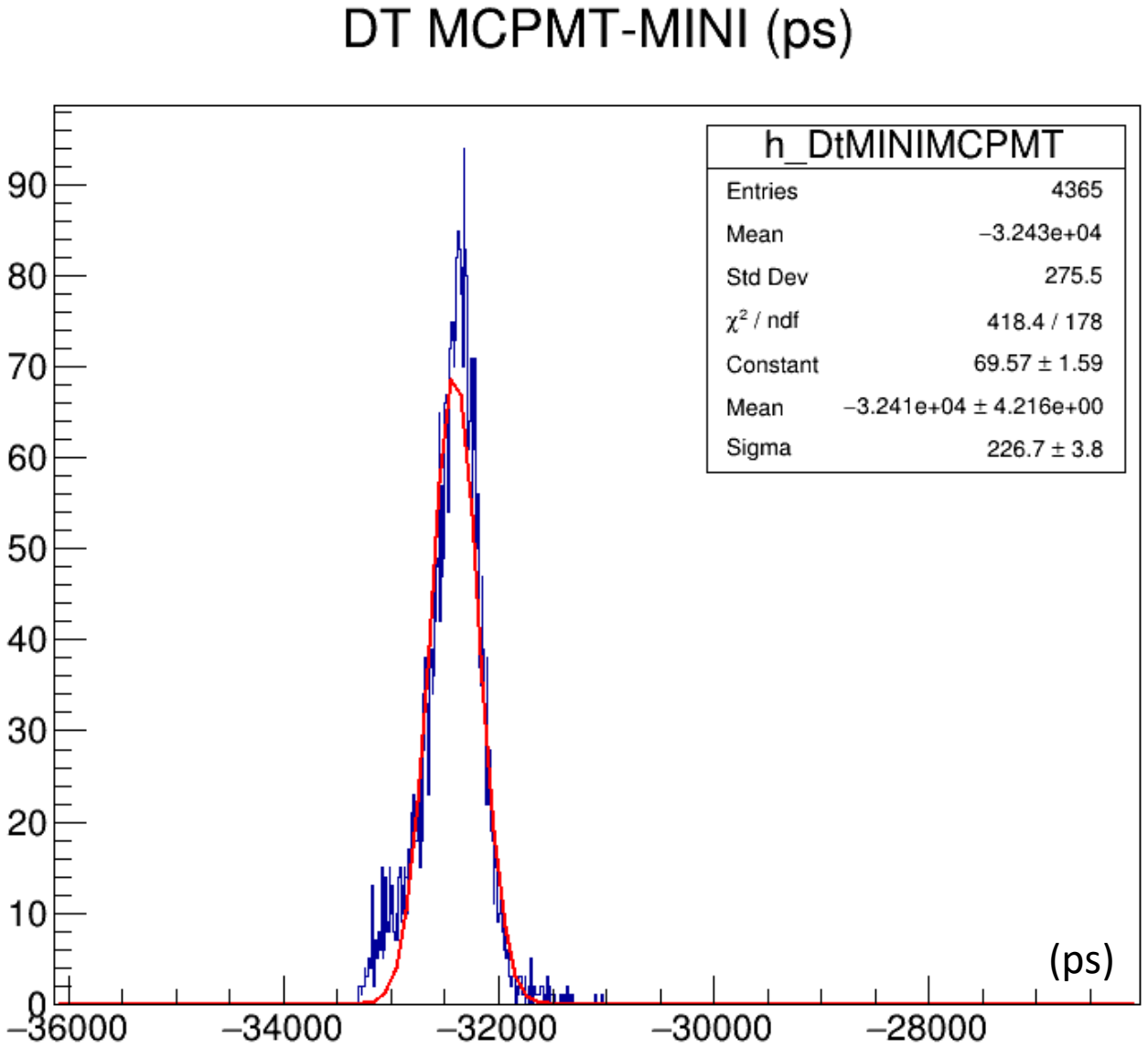
RUN15 Trigger on AmpOut at 650mV





Before Time Walk correction

RUN15

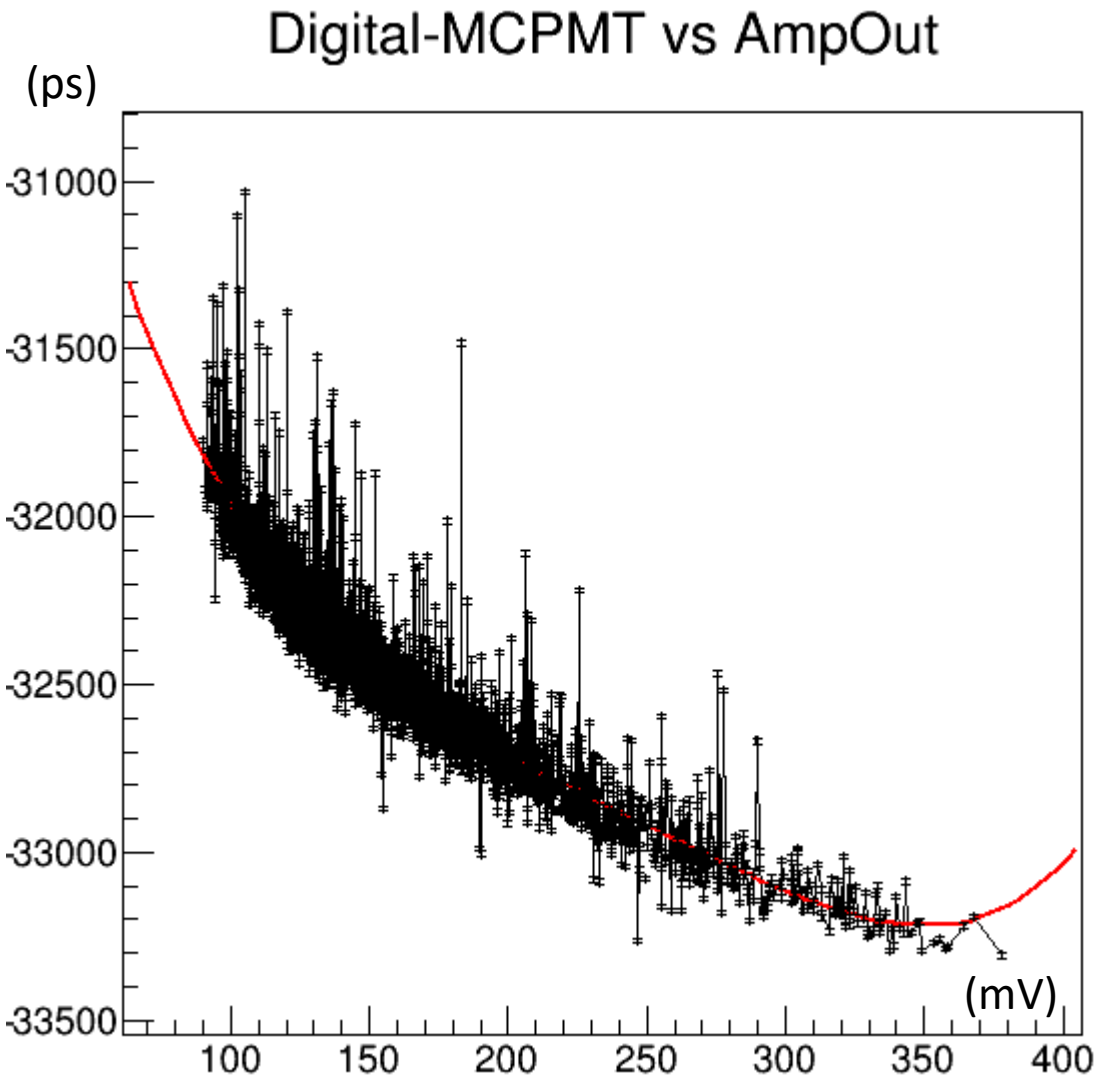


2 possible Time Walk (TW) corrections :

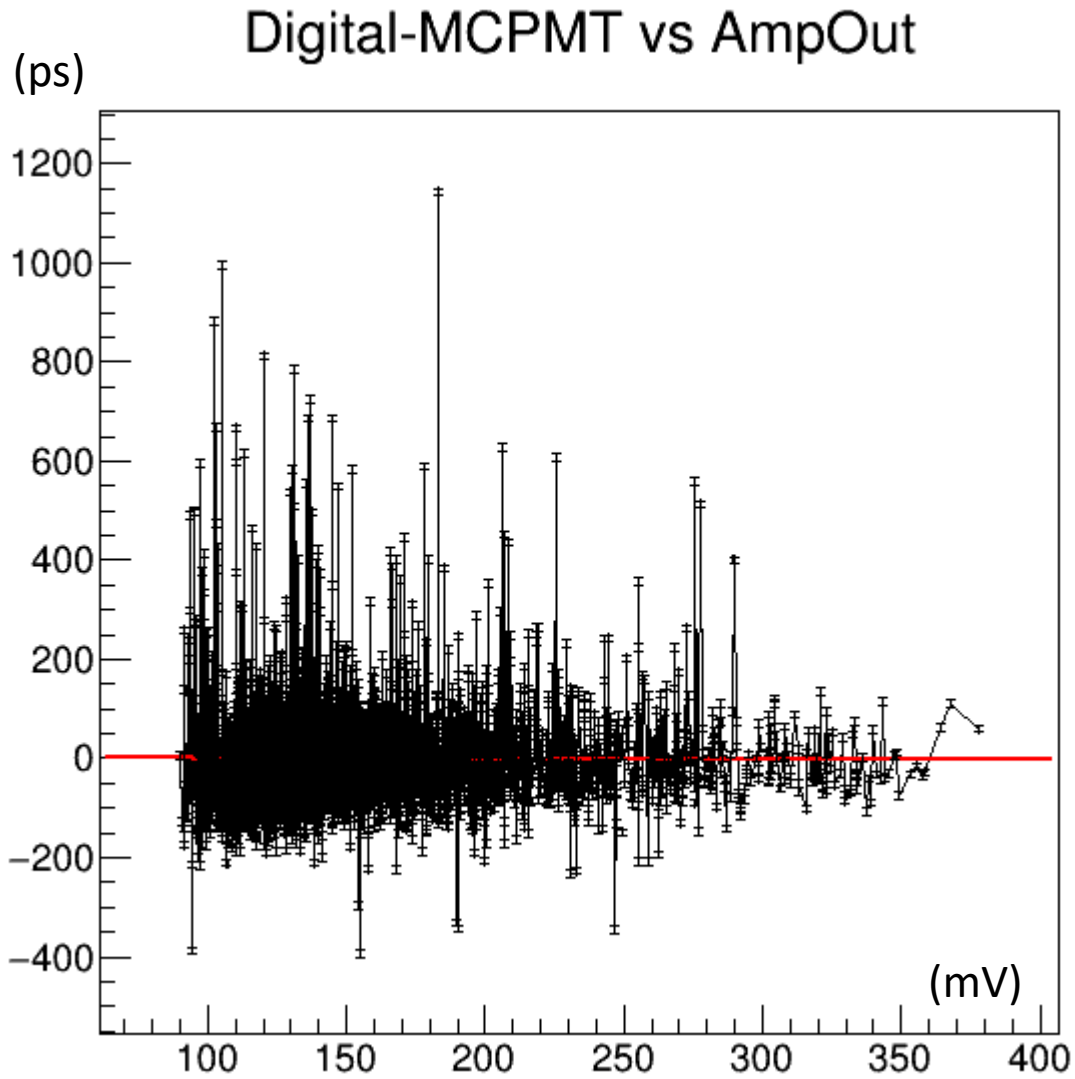
- Use the amplitude of the analogue output
- Use the digital signal ToT

RUN15

Use the amplitude of the analogue output



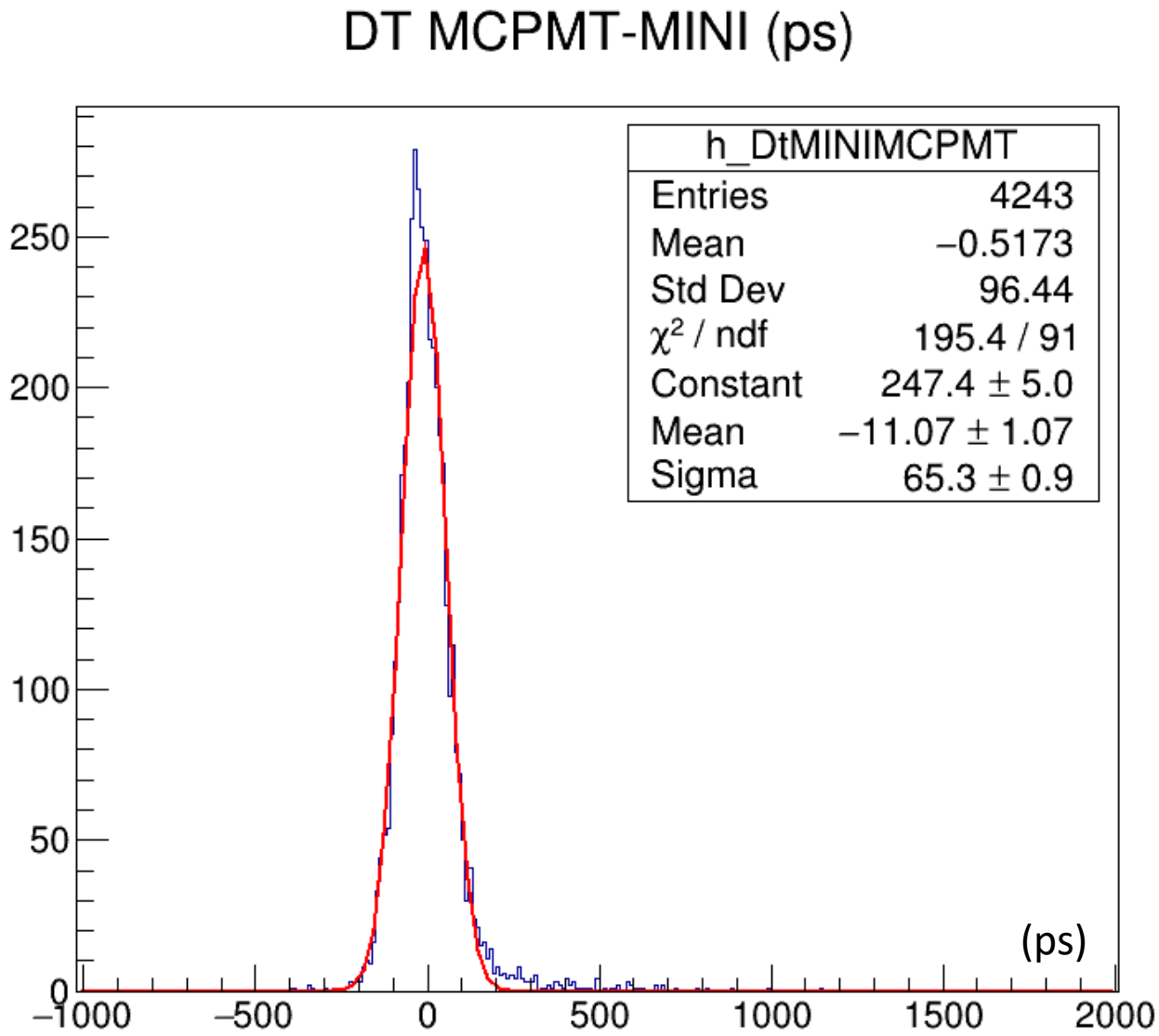
TW corr.



RUN15

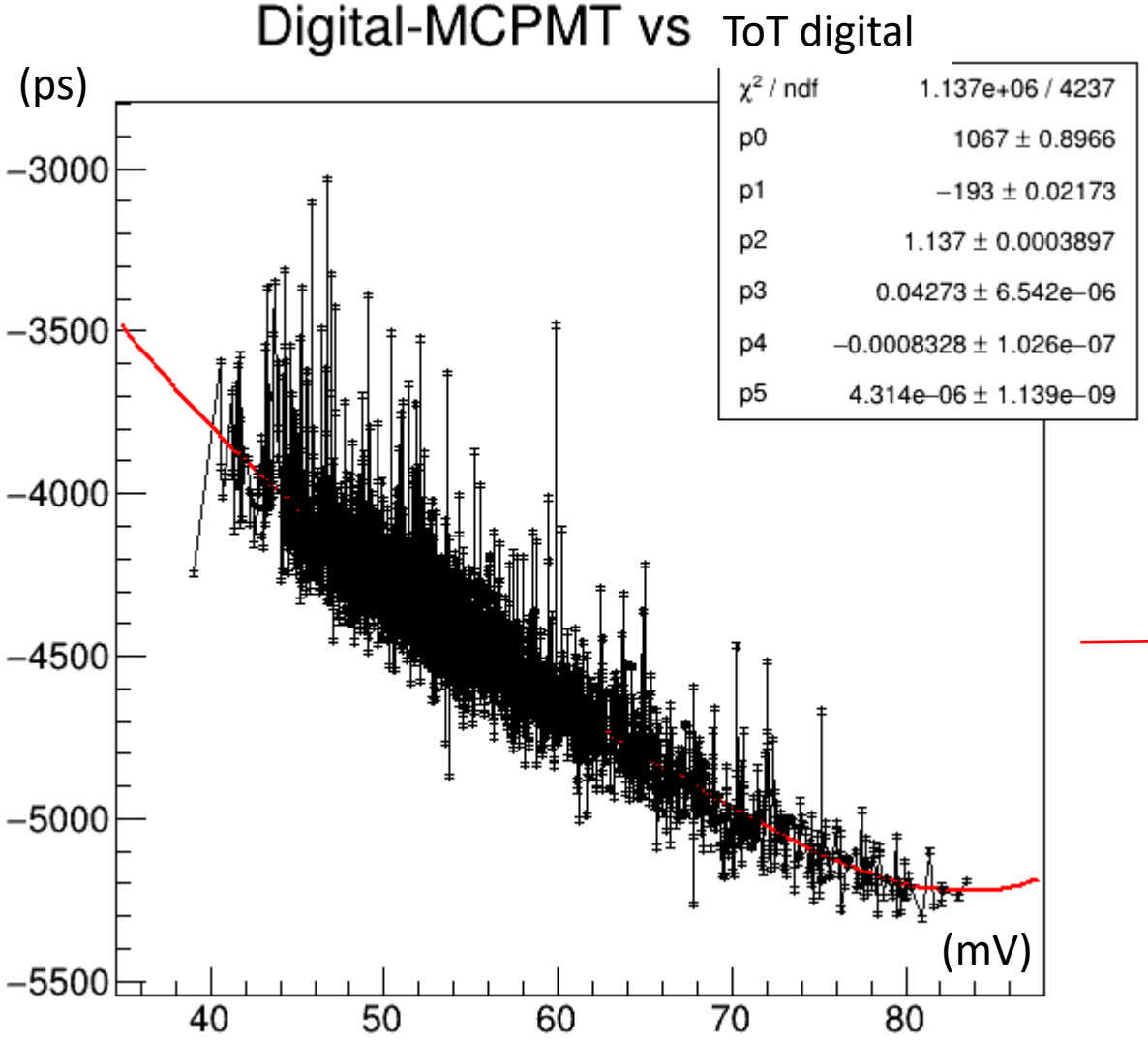
Use the amplitude of the analogue output

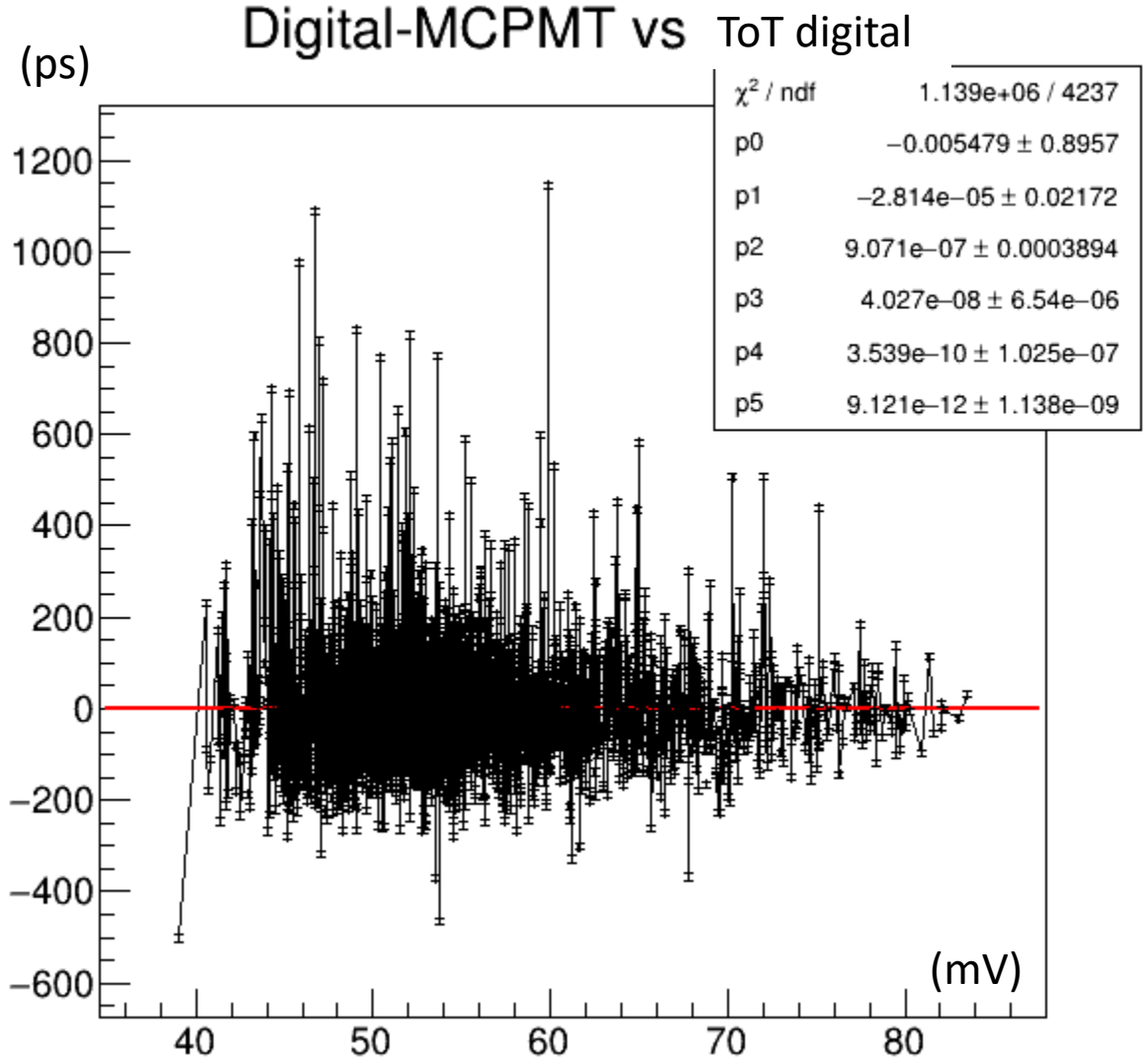
After TW correction



RUN15

Use the digital ToT

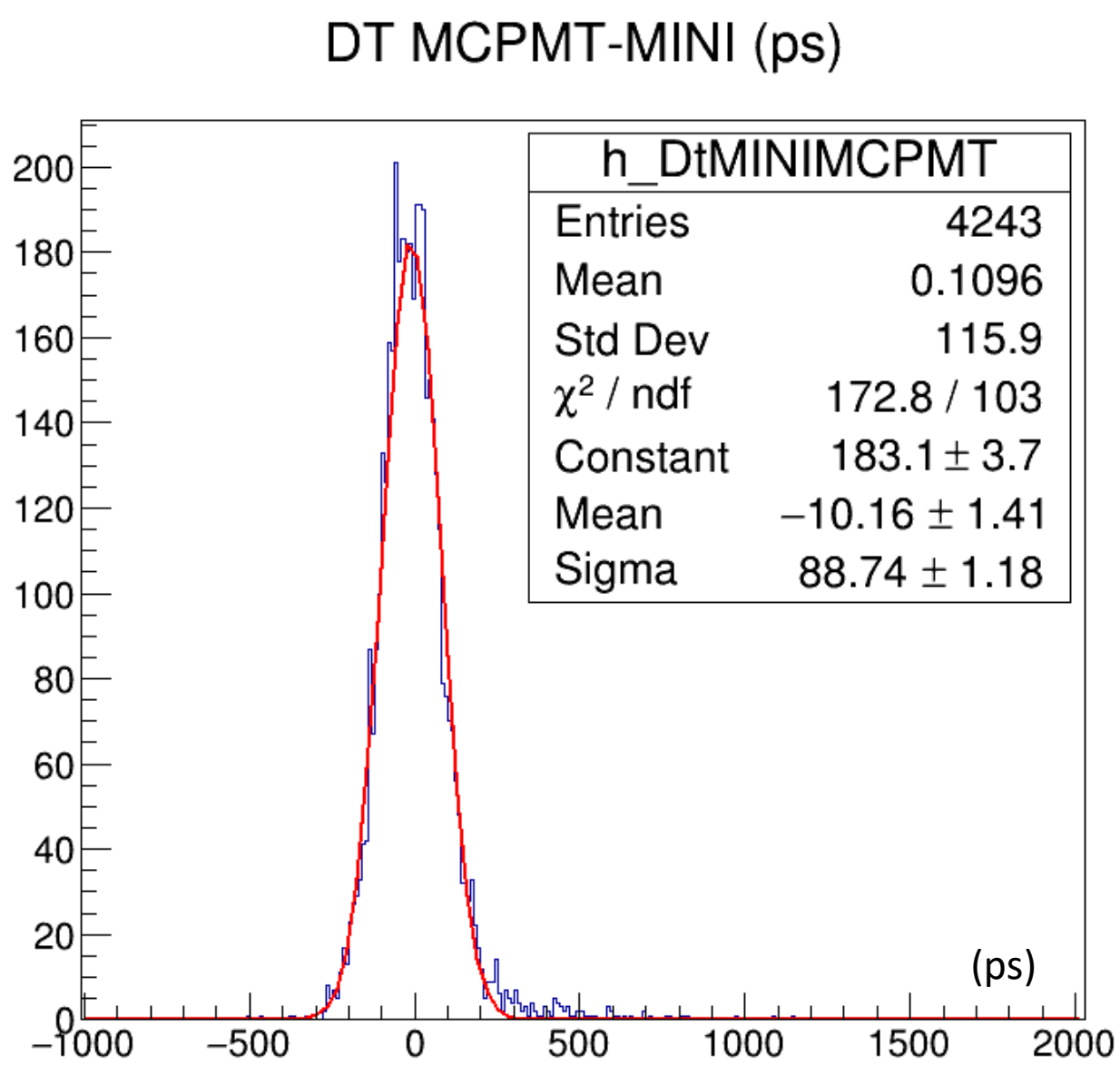




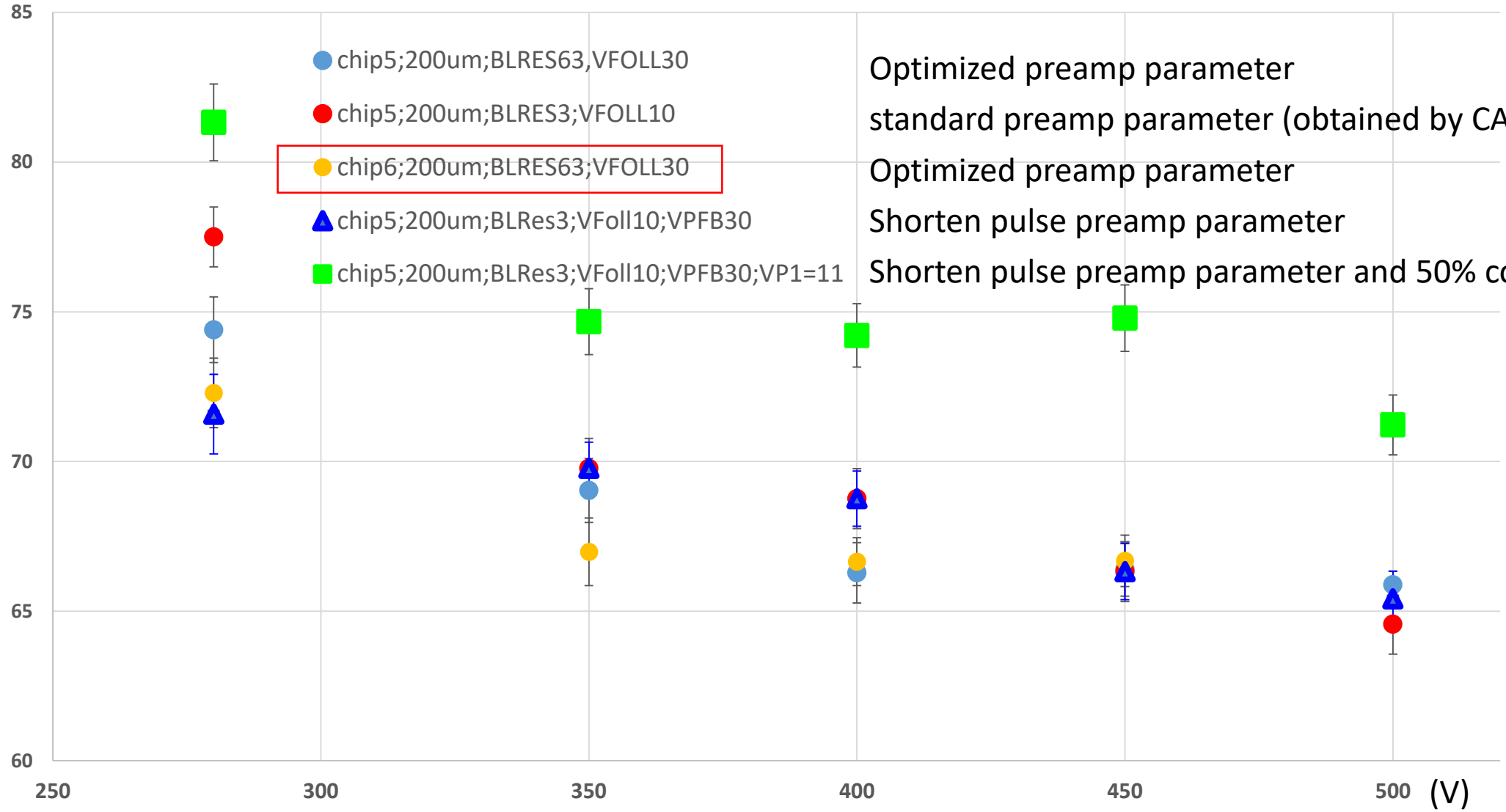
RUN15

Use the digital ToT

After TW correction



Pixel 8;200µm; Resolution versus HV



Optimized preamp parameter

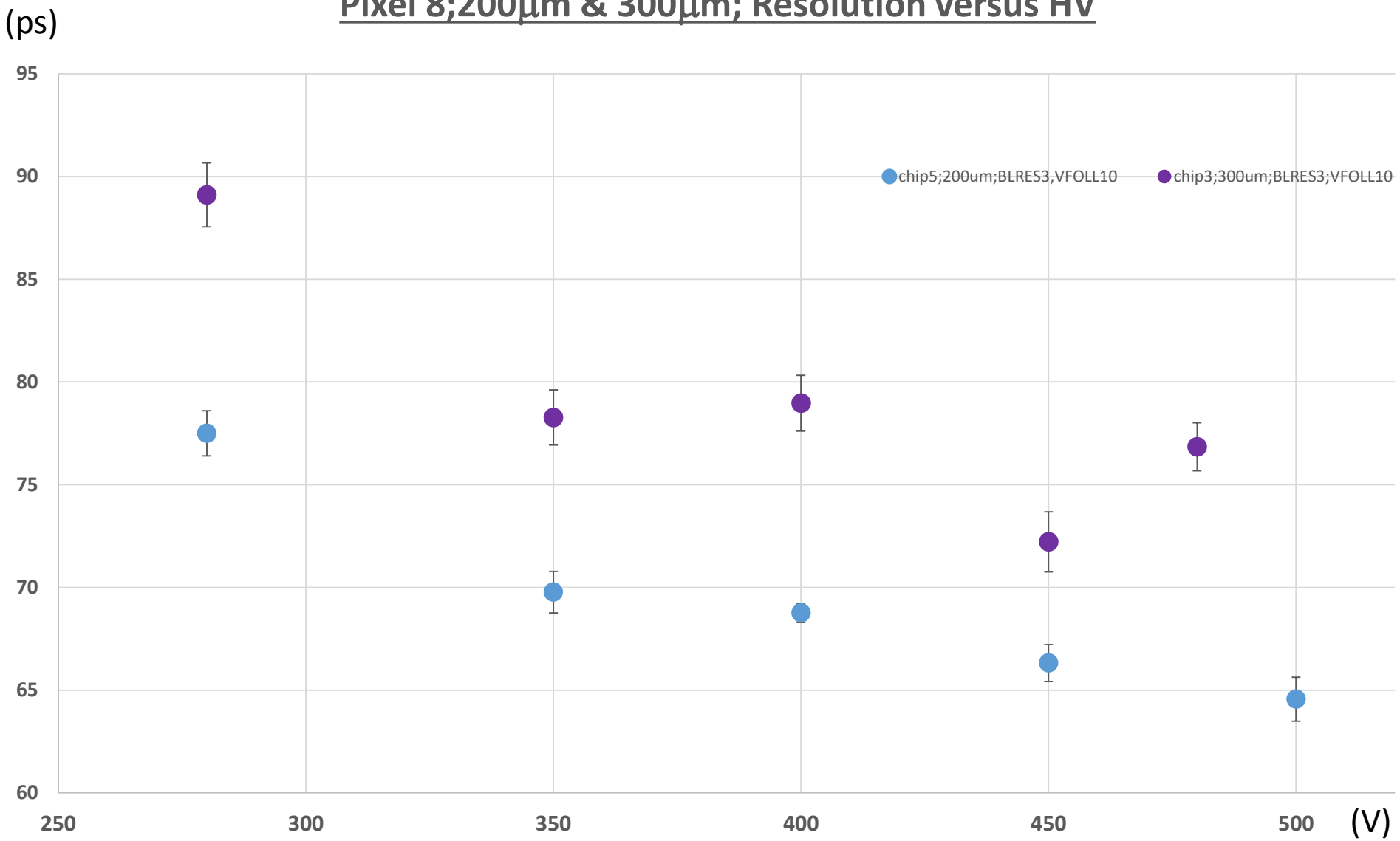
standard preamp parameter (obtained by CADENCE)

Optimized preamp parameter

Shorten pulse preamp parameter

Shorten pulse preamp parameter and 50% consumption

Pixel 8;200µm & 300µm; Resolution versus HV



CONCLUSIONS AND NEXT STEP

- Many thanks to RD51 collaboration

- It was a real good beam period for use which allows to test 4 chips under different conditions

- There is still some black magic for us with the MCPMT (split changes and probably HV too)
  - ❑ For the first 13 runs the MiniCactus time resolution was much worse.
  - ❑ We observed big improvement on the 23 of may without any changes from our side

- We reached 65ps time resolution with two different chips and we where able to check this result on many runs.

- The 200μm thickness chips give the best result in the HV range 400 to 500V

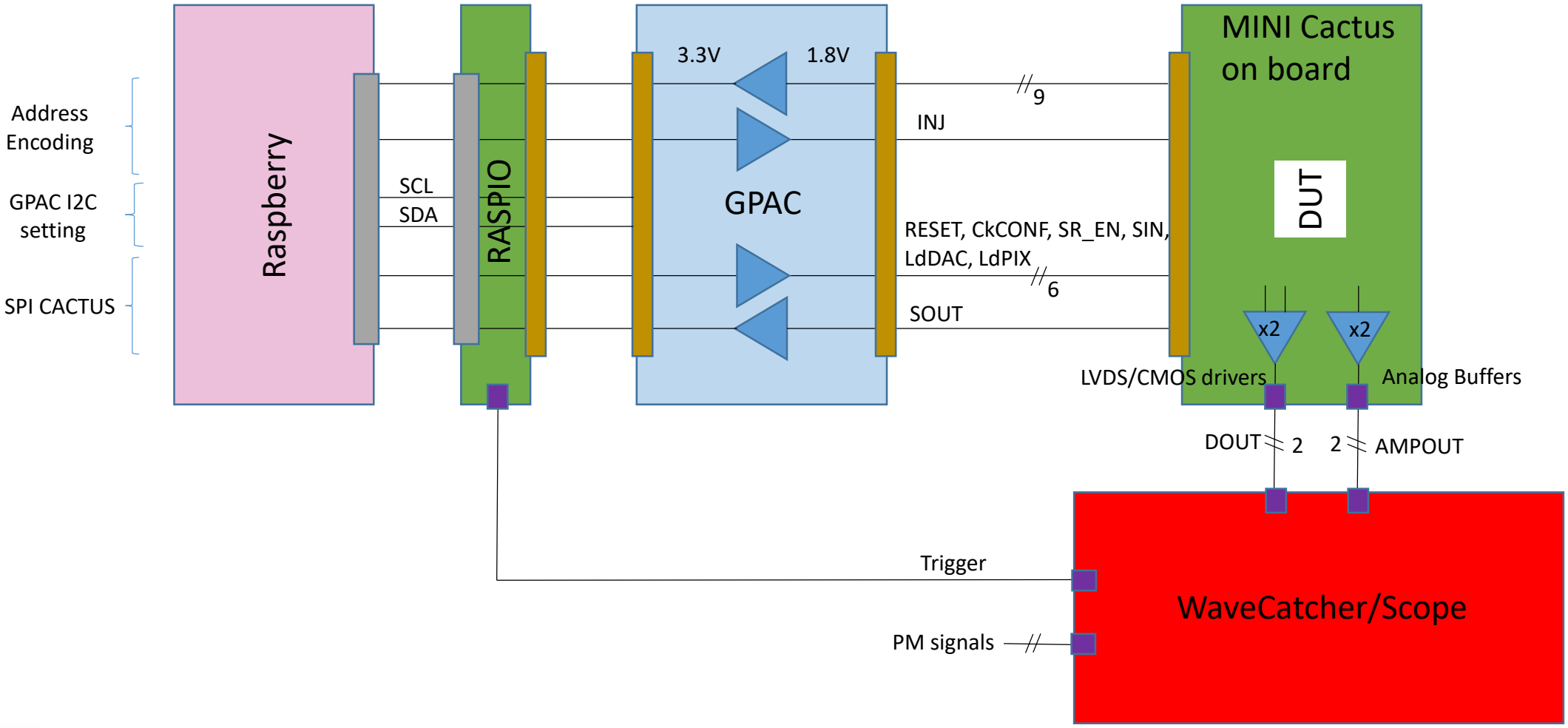
- Irradiation campaign underway at Ljubljana (Slovenia) and new test are forseen (source or Tbeam)

- Stabilise the temperature and study temperature effects on the chip

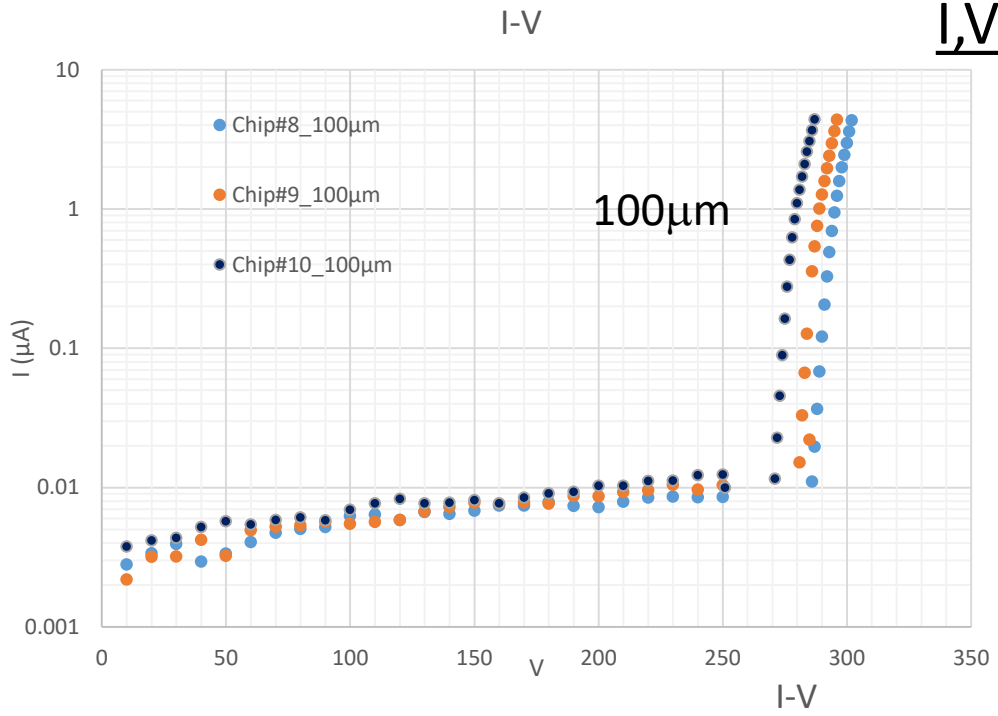
- Build a new version of MiniCactus to fix the ringing problems and add functionalities

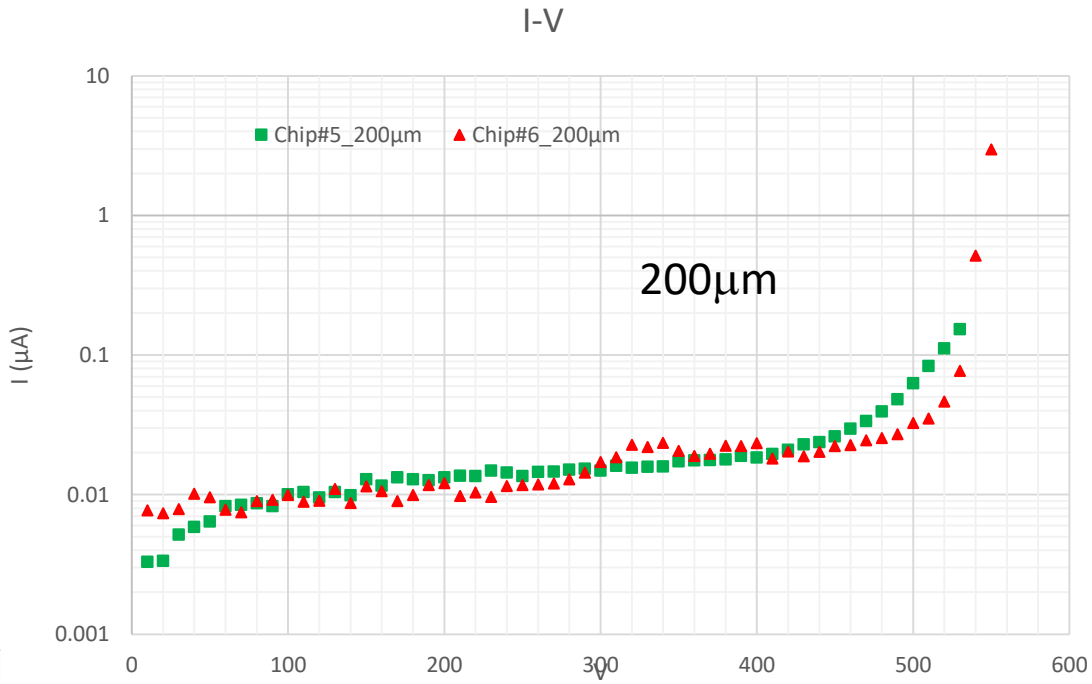
Backup

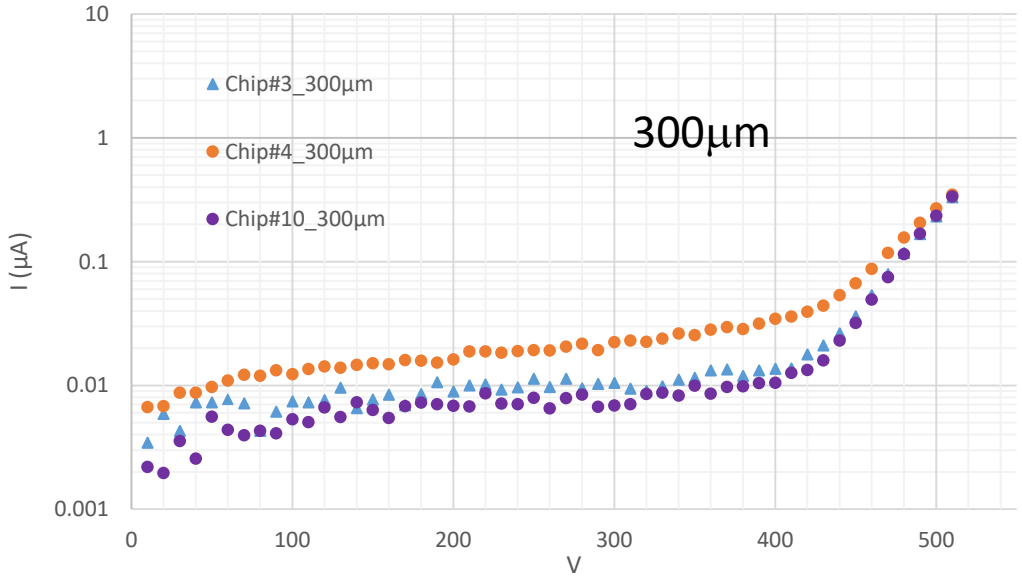
CACTUS/MINICactus testbed



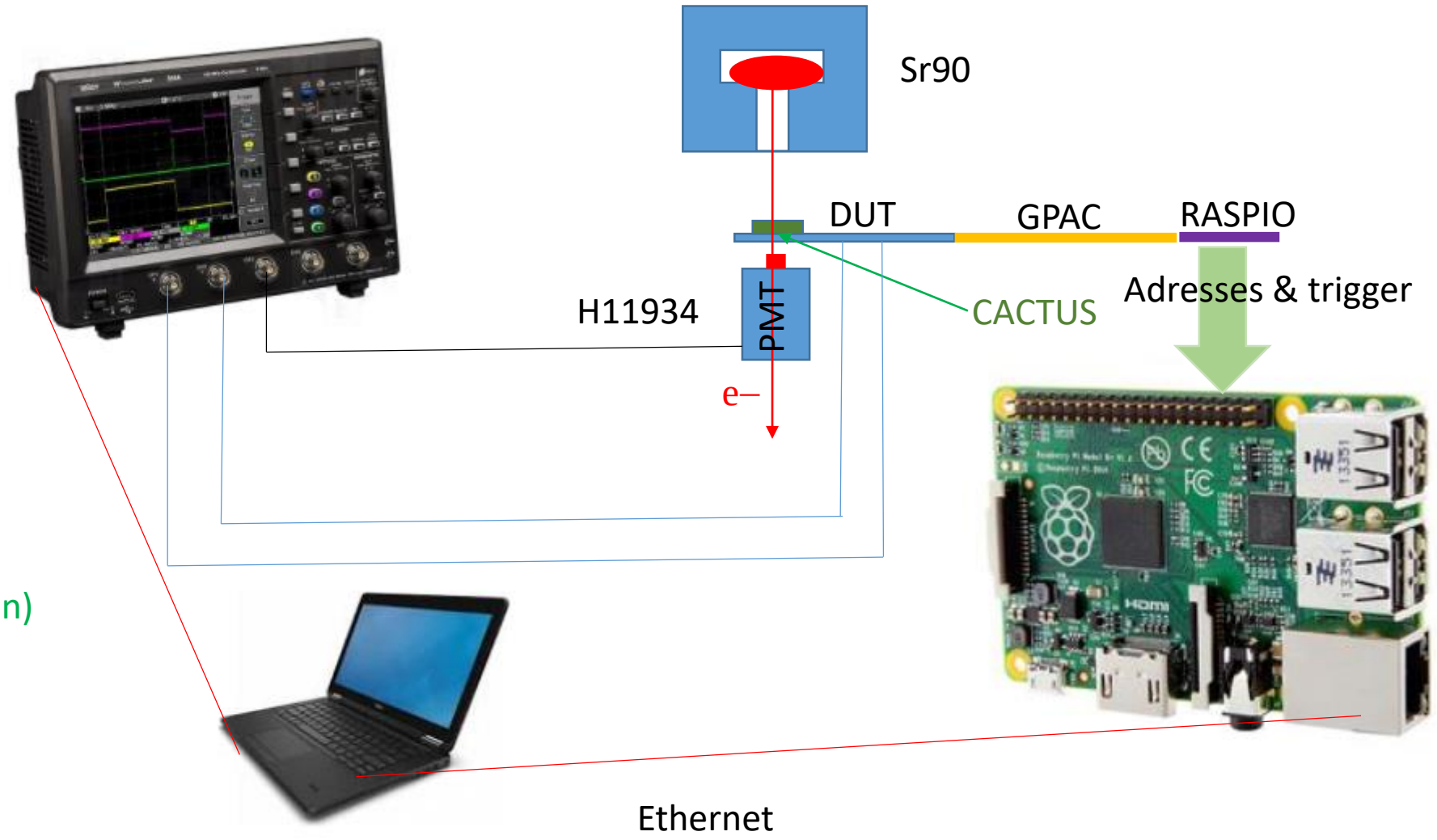
I,V Curve of MiniCactus







Sr90 Mini-CACTUS Test setup



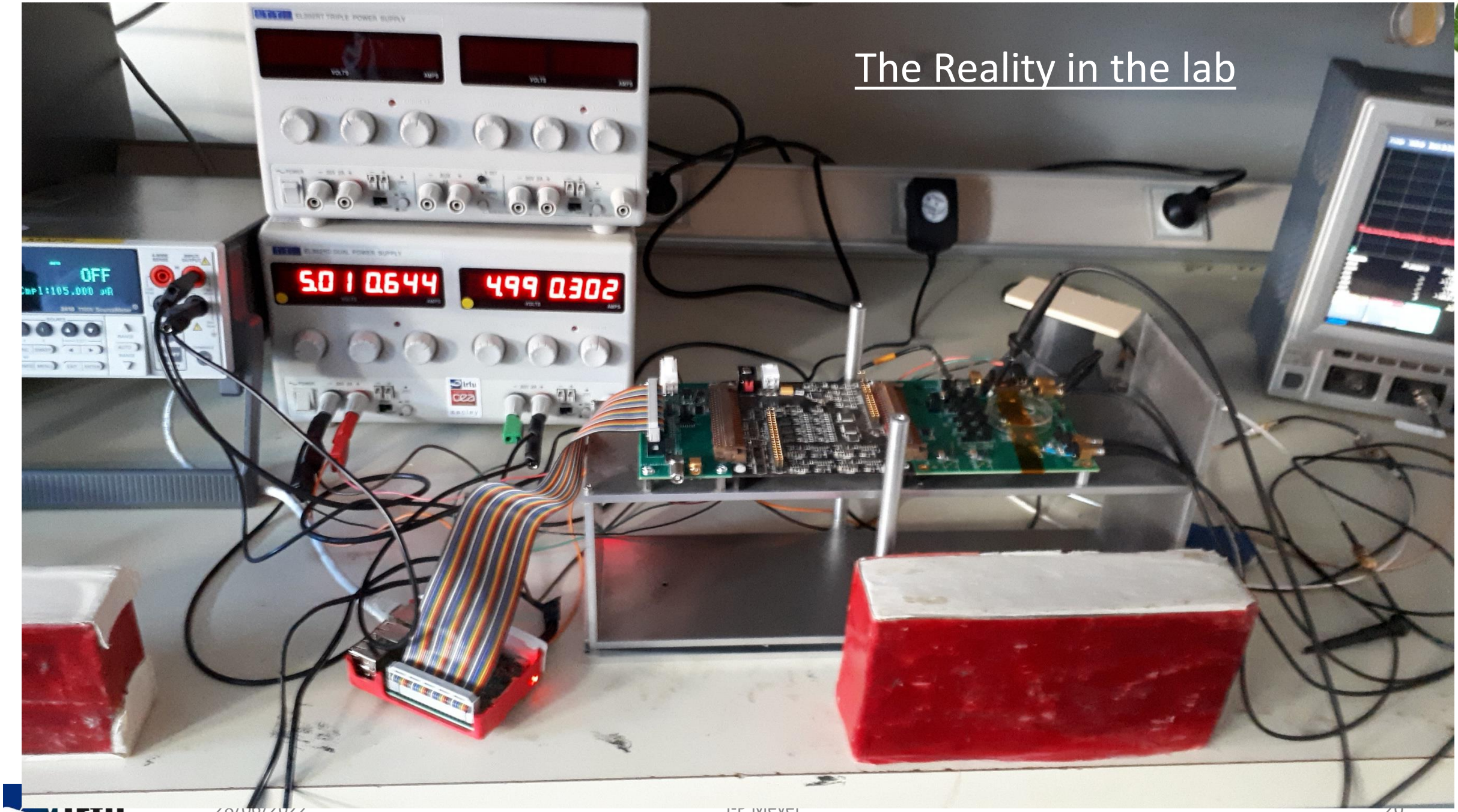
Used for :

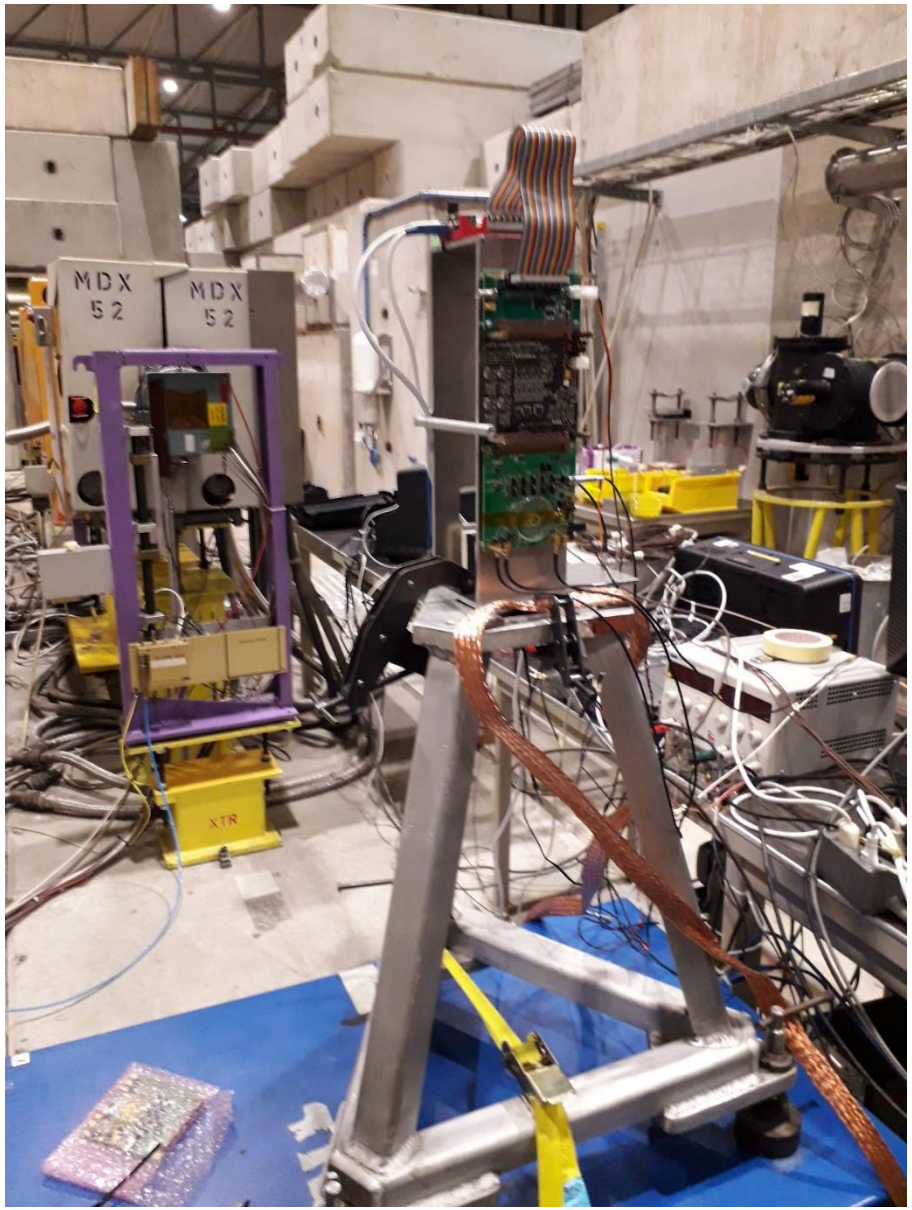
- First test and debug

- Calibration (see last presentation)

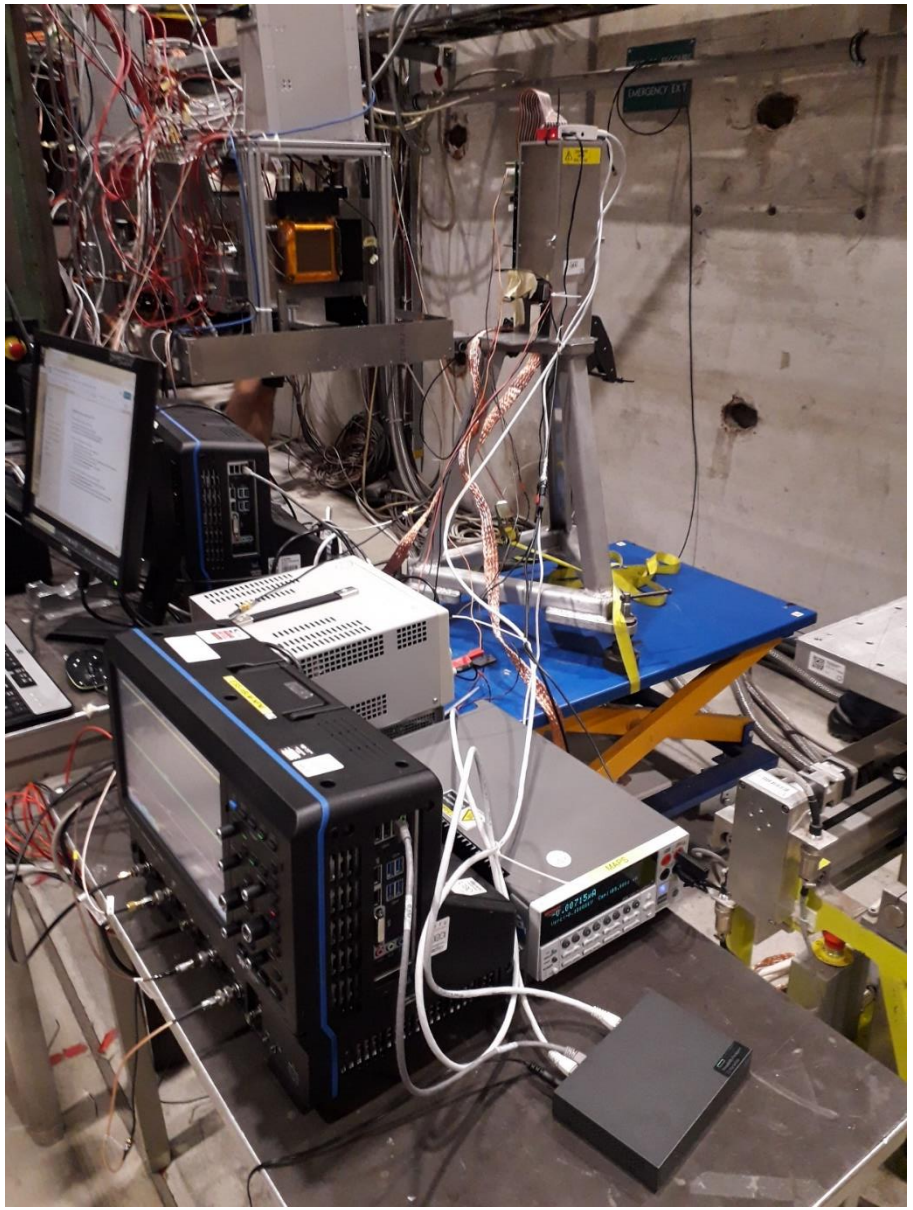
- parameter optimisation studies looking for relative performance improvements

The Reality in the lab

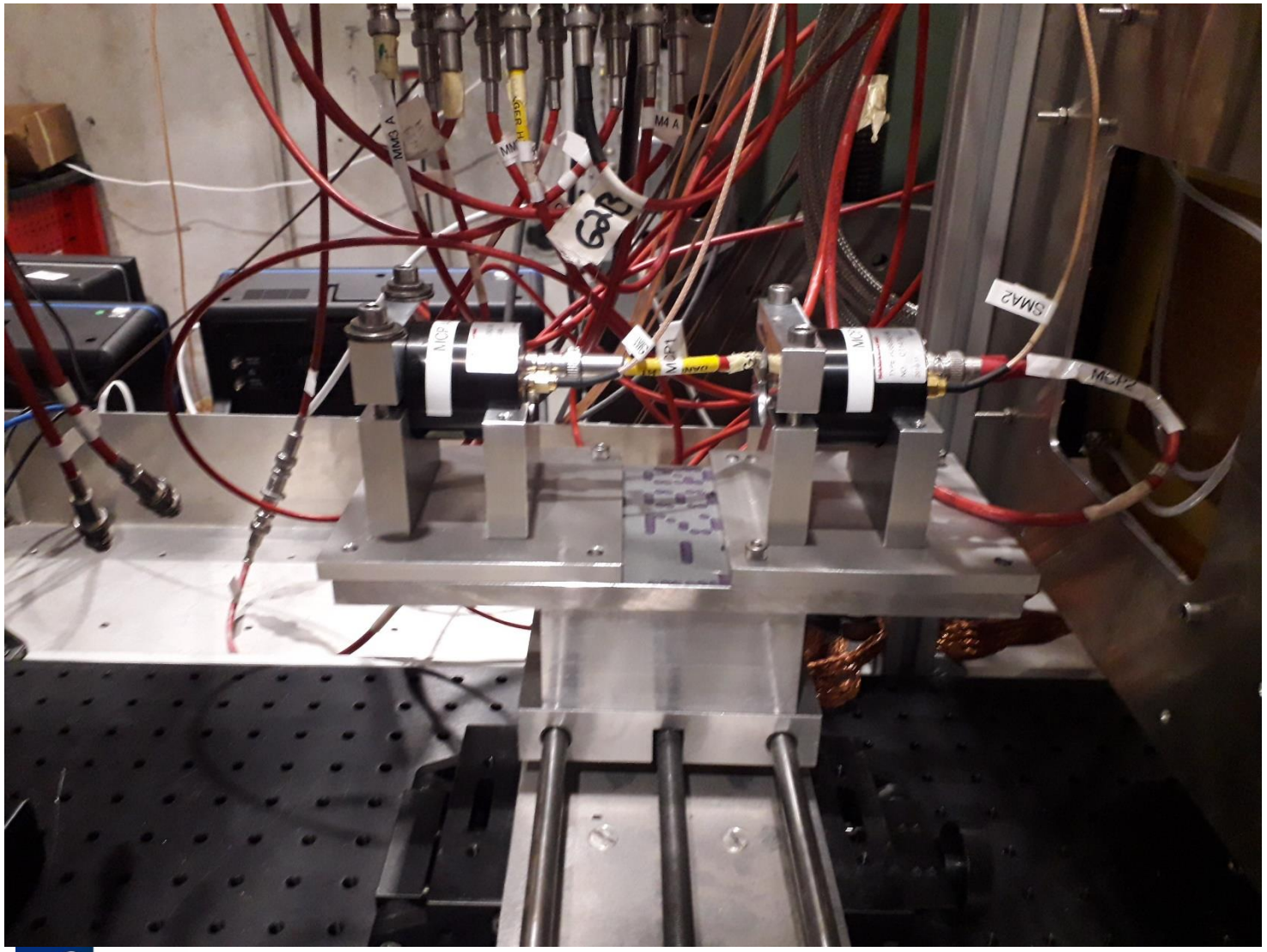




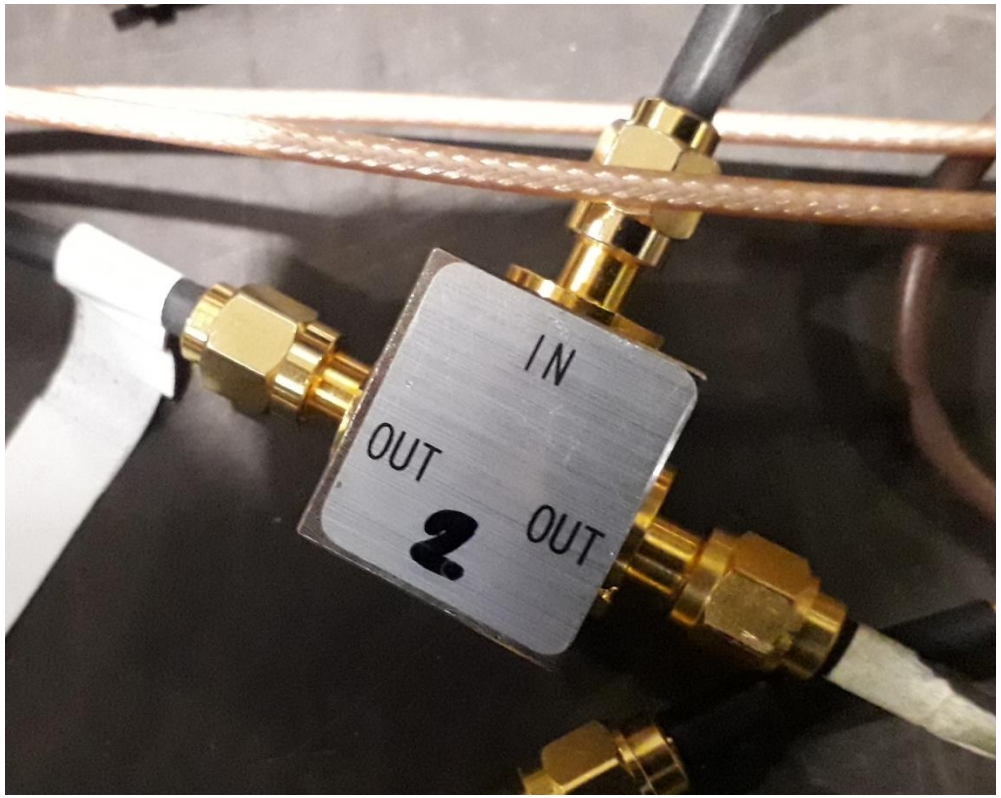
On H4 North Area
At CERN in
parasitic mode



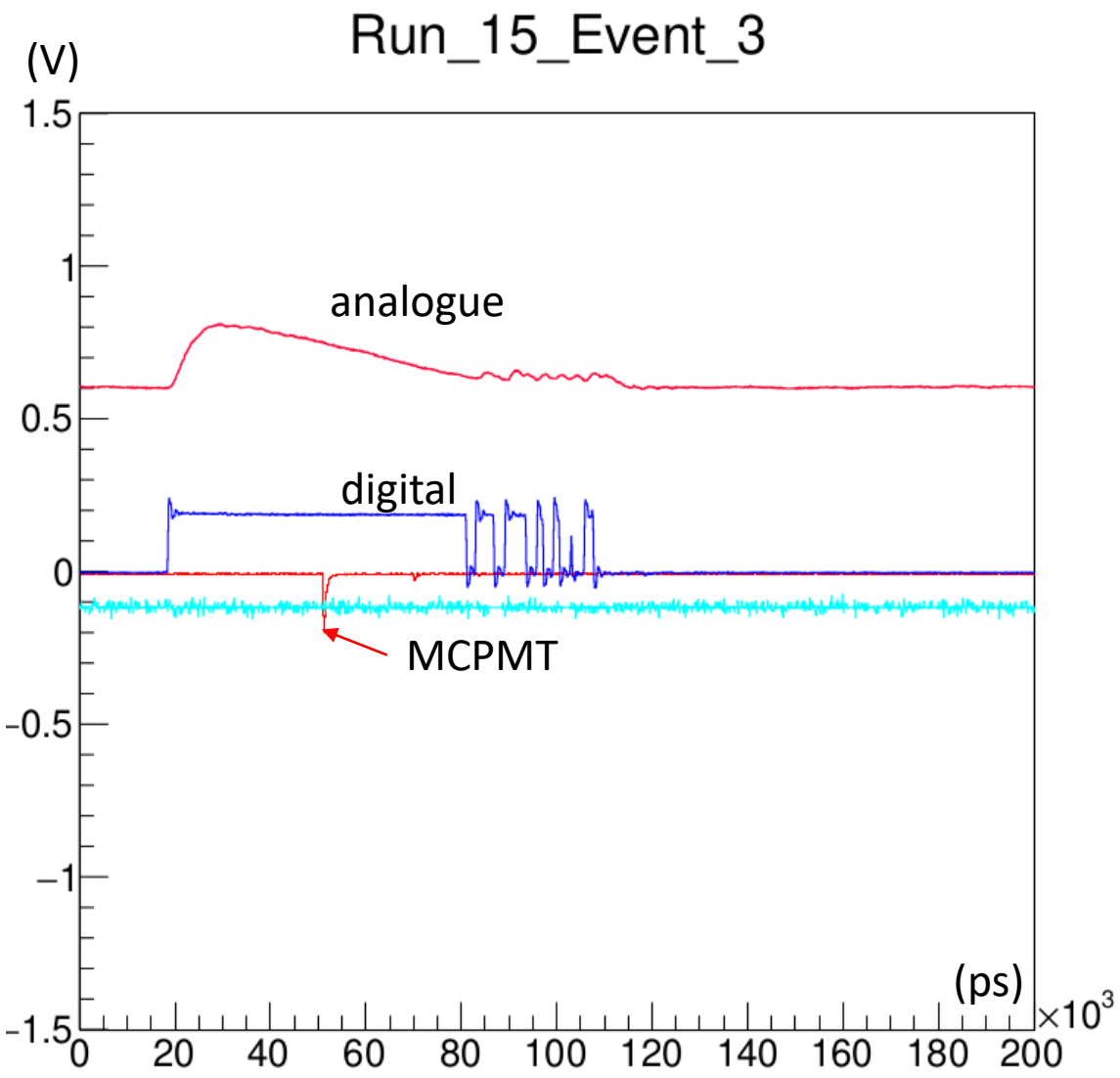
Time ref: MCPMT (Hamamatsu R3809U-50) owned by RD51

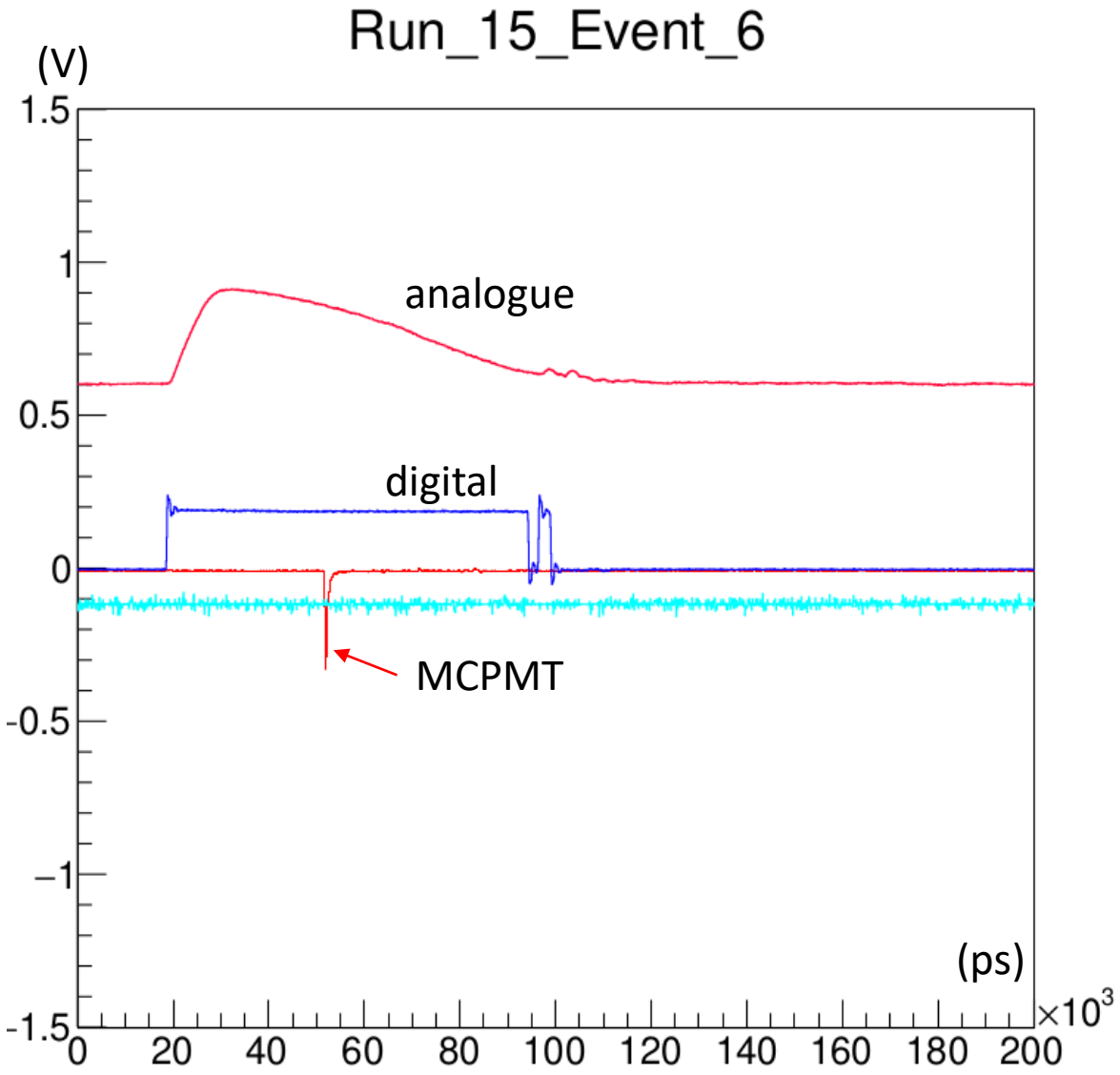


Several passive splits changing with time…
Not so easy to follow the thing and also changes with HV on MCPMT which impact time resolution of our reference.

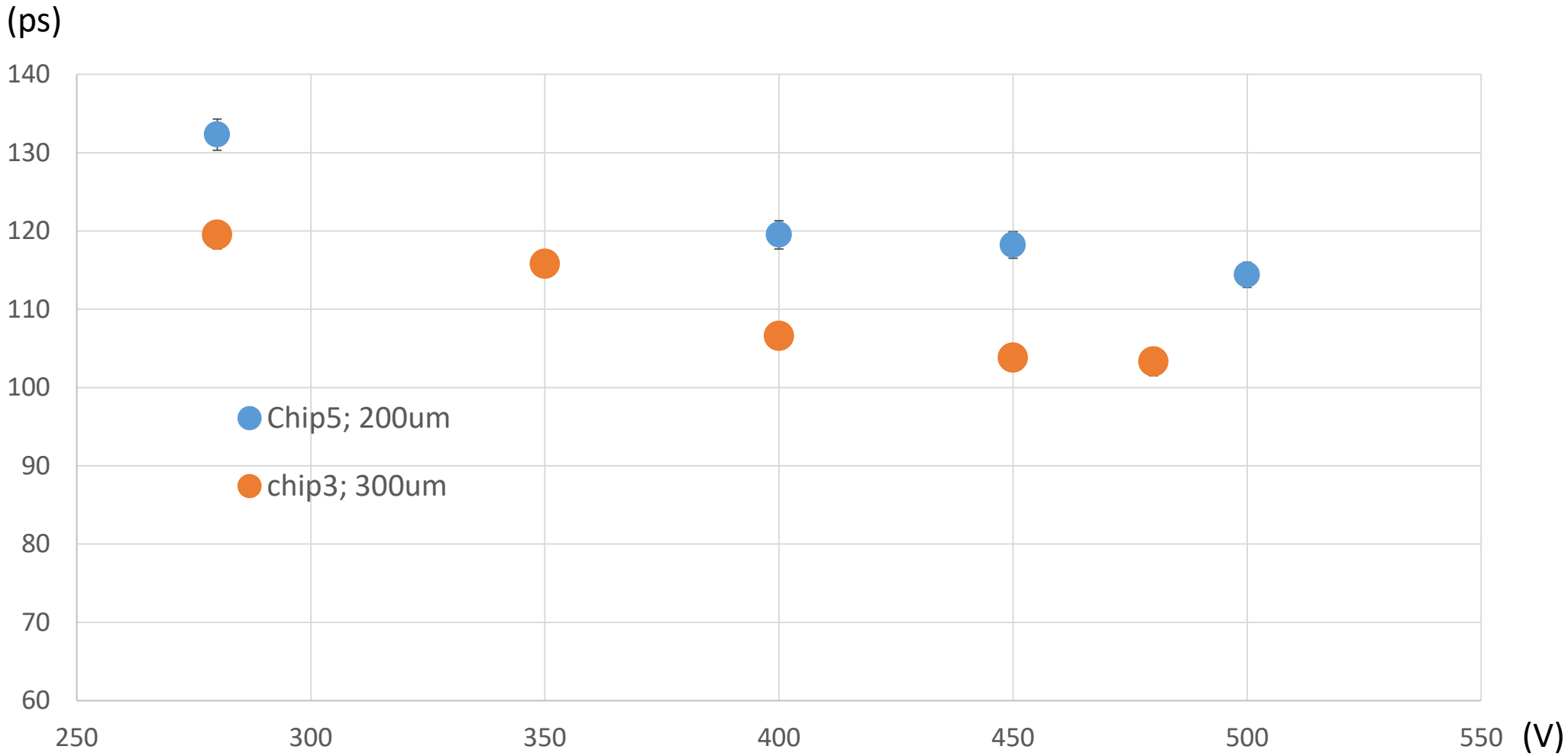


Typical events:

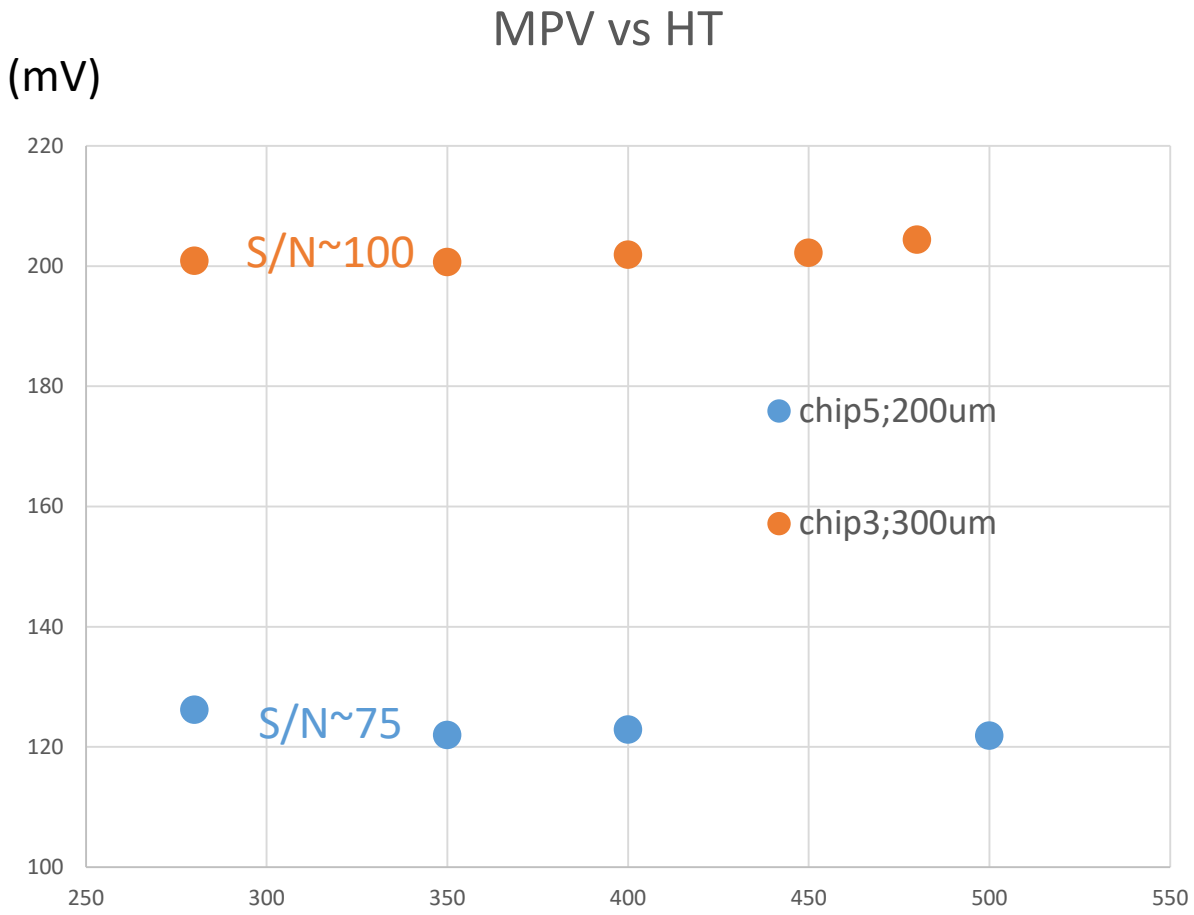


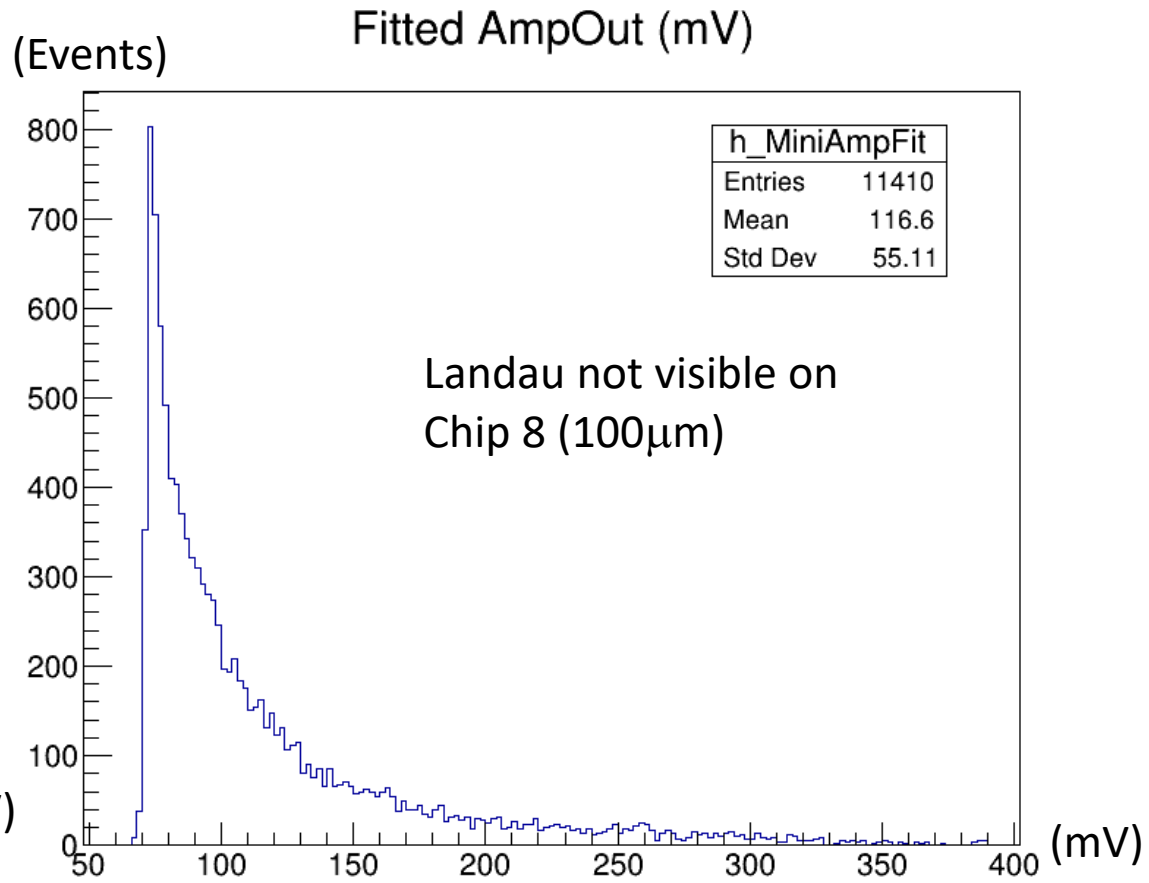


Pixel 7 Resolution versus HT

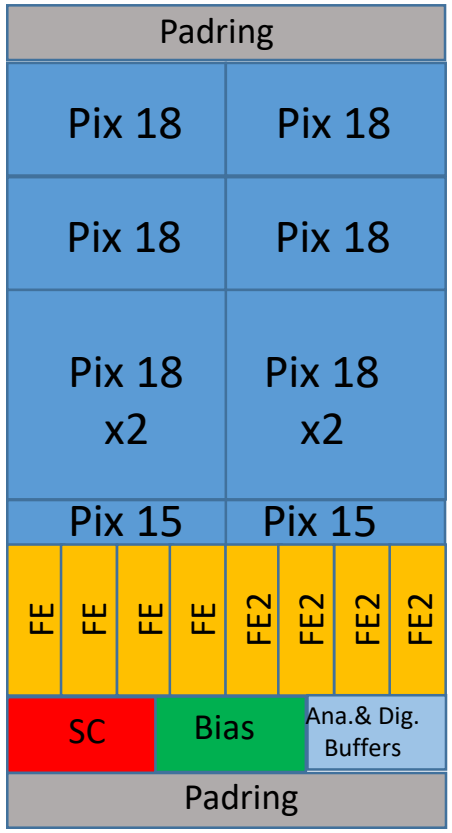


Pixel 8


MPV vs HT
(mV)
220
200
180
160
140
120
100
250
300
350
400
450
500
550
(V)
S/N~100
S/N~75
chip5;200um
chip3;300um


Fitted AmpOut (mV)
(Events)
h_MiniAmpFit
Entries 11410
Mean 116.6
Std Dev 55.11
Landau not visible on
Chip 8 (100µm)
800
700
600
500
400
300
200
100
0
50
100
150
200
250
300
350
400
(mV)

MiniCACTUS V2?



Ideas of Yavuz

FE : Préampli + Discri de MiniCACTUS
FE2 : Préampli de MiniCACTUS + Nouveau Discri différentiel avec hystérésis

Améliorations possibles :

- Séparation des caissons DNW des buffers CMOS
- Conversion LVDS en sortie des buffers CMOS (actuellement dans le pad LVDS)
- Amélioration du DAC d'ajustement des discriùinateurs (4bits→ 5bits)
- Retour aux anneaux de garde de CACTUS