Contribution ID: **68** Type: **Oral presentation**

CSM FPGA Irradiation Test at LANSCE for the HL-LHC ATLAS Muon Spectrometer Upgrade

Saturday, 9 April 2022 15:40 (20 minutes)

The increased radiation environment and data rate for the High Luminosity Large Hadron Collider (HL-LHC) require upgrades to the readout electronics for the Muon Spectrometer (MS) electronics. In this talk, I will present ongoing irradiation studies of a custom-built front-end electronics board, the chamber service module (CSM), which is responsible for multiplexing data read out from on-detector electronics as well as passing configuration information to them. An important component of the CSM is a Field-programmable gate array (FPGA), specifically using the FPGA Artix7 xc7a35T, which is responsible for fanout of configuration and control information for 18 mezzanine cards. The Artix-7 is a commercial component with a history of meeting our radiation specifications. The specific model used in the CSM was tested in a radiation hard environment with an average flux 103 higher than ATLAS (6.02E+3 n/cm^2/s vs 1.3E+6 n/cm^2/s). Preliminary results show that the LANSCE Single Event Upset (SEU) test approximately had 3 years of ATLAS in comparison with ˜ 1.9E+11n/cm^2/y fluence (MDT CSM Requirement) and accumulated 18 SEU errors for two boards.

Career stage

Graduate student

Author: GUHIT, Jem Aizen Mendiola (University of Michigan (US))

Co-authors: GUO, Yuxiang (University of Michigan (US)); HU, Xueye (University of Michigan (US)); SCHWARZ, Thomas Andrew (University of Michigan (US)); XIAO, Xiong (University of Michigan (US))

Presenter: GUHIT, Jem Aizen Mendiola (University of Michigan (US))

Session Classification: Instrumentation II