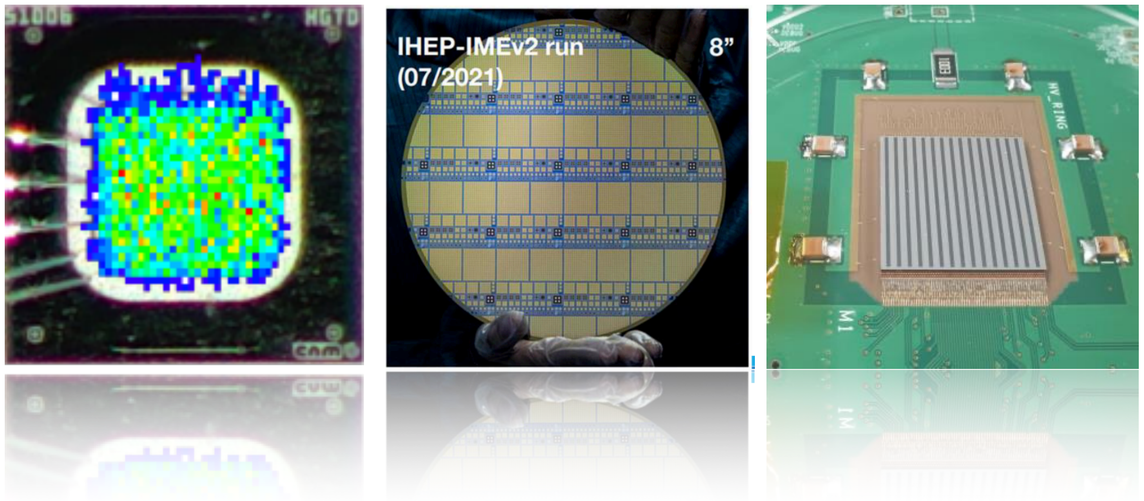
A High Granularity Timing Detector for the ATLAS Phase-II upgrade

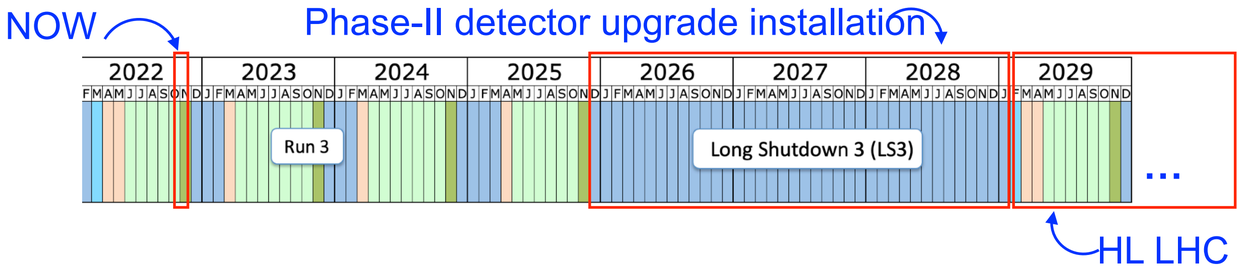
Mengqing Wu *(Radboud University & Nikhef)*
On behalf of the ATLAS HGTD group

Vertex 2022, Tateyama, Oct 24-28 2022



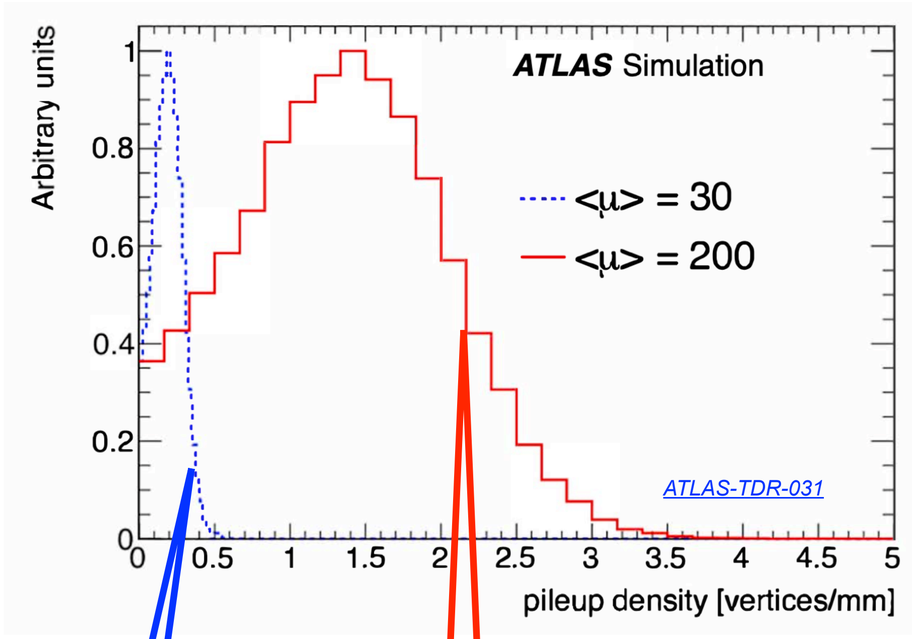
Radboud University Nikhef ATLAS EXPERIMENT

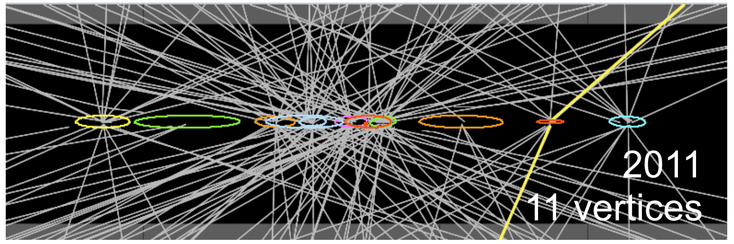
Detector upgrade requirements towards HL-LHC

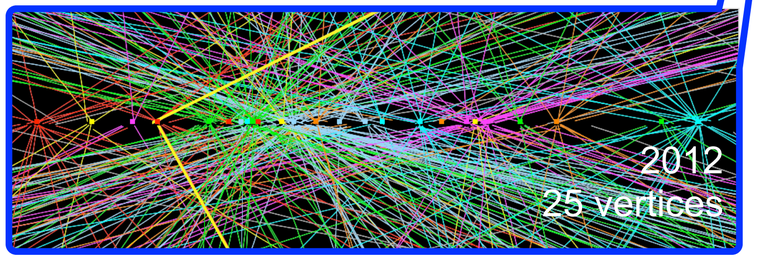


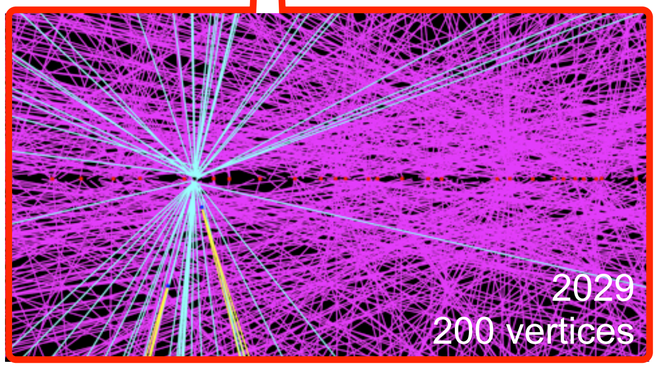
HL-LHC: instantaneous luminosity **5 times higher**, giving a total integrated luminosity of up to 4 ab^{-1}

- Up to 200 inelastic pp collisions (pile-up) on average per bunch crossing ➔ motivates not only finer spatial measurements but also **timing measurements**
- Higher radiation requirement ➔ detector radiation hardness increased by an order of magnitude









Exploit the 4th dimension: time

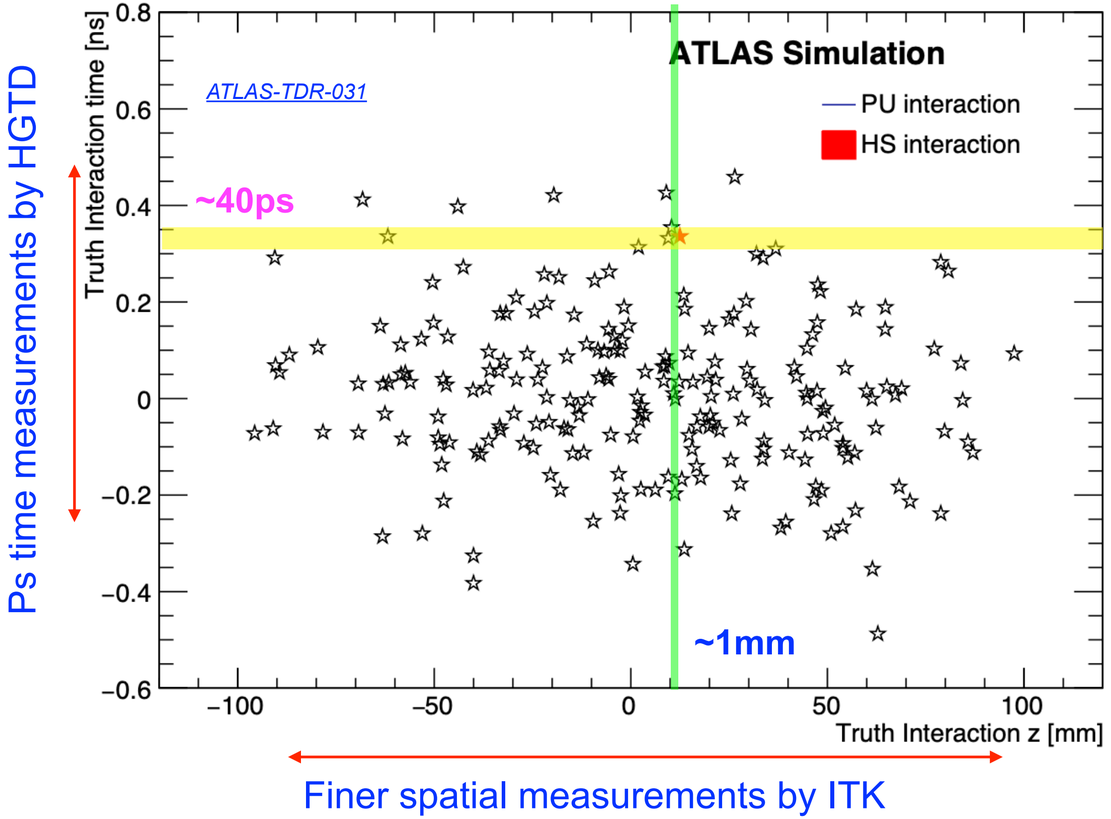
Interactions spread not only in z but also in t (RMS ~ 175 ps), at least for tracks in **high |η| region**, requiring

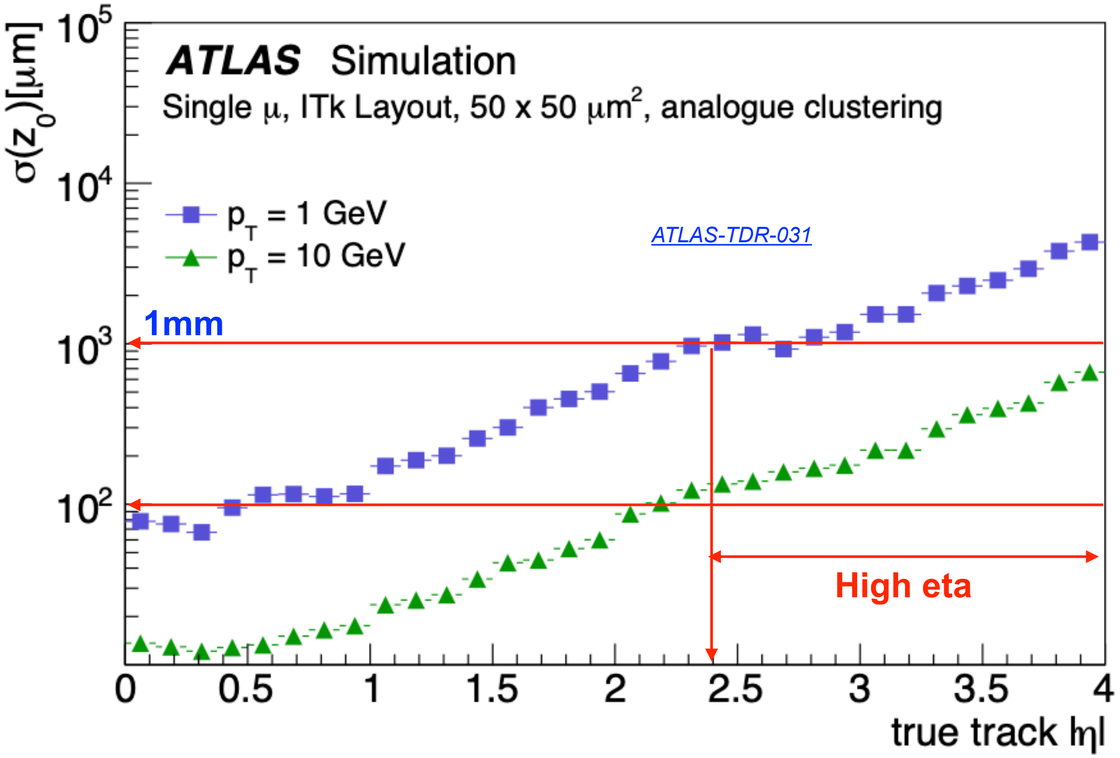
- σ_t << 175ps, and HGTD aims at **< 50ps**

➔ pile-up suppression by **a factor of ~6**

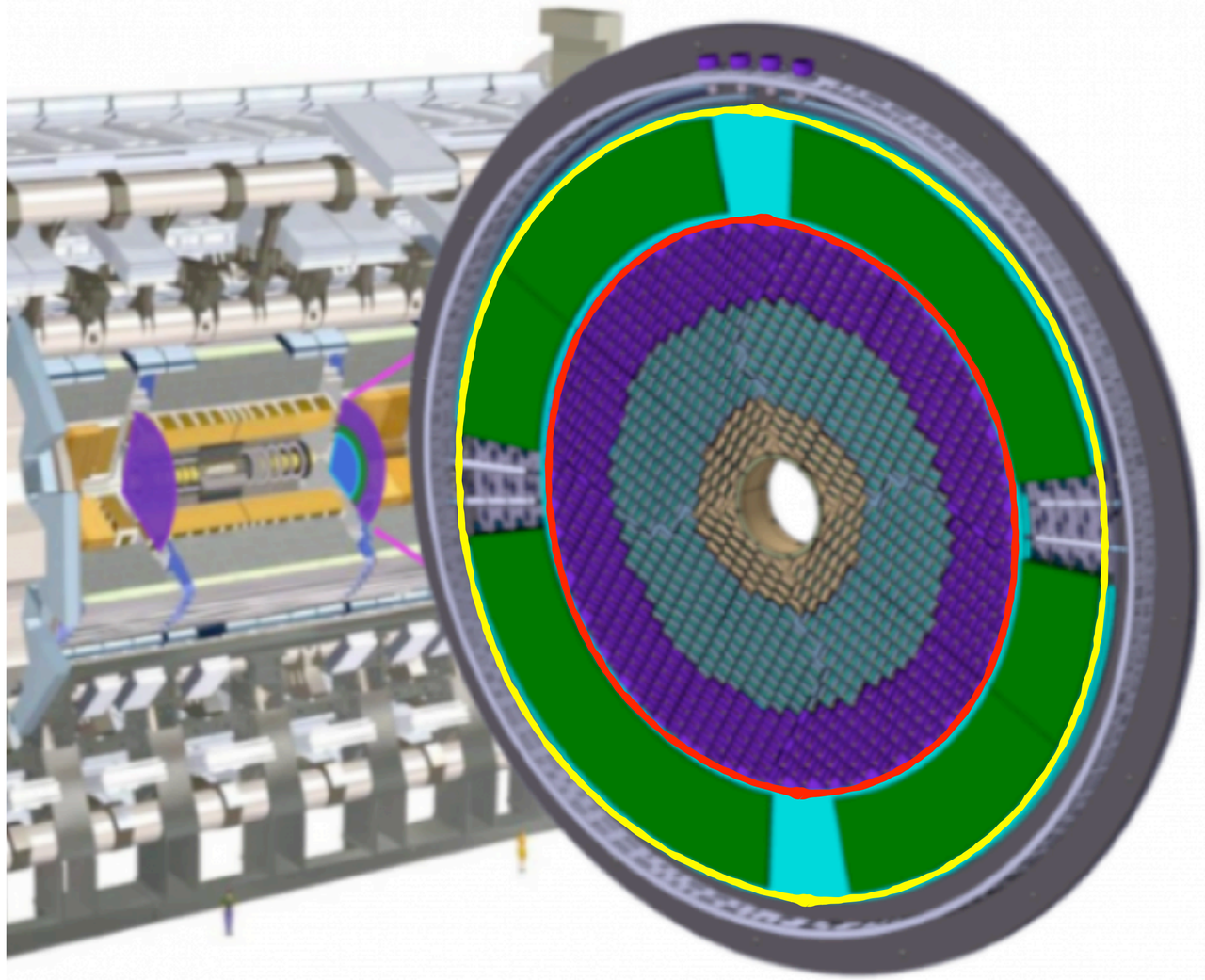
➔ impact on pile-up rejection, track/jet reconstruction

Critical to success of the physics programme



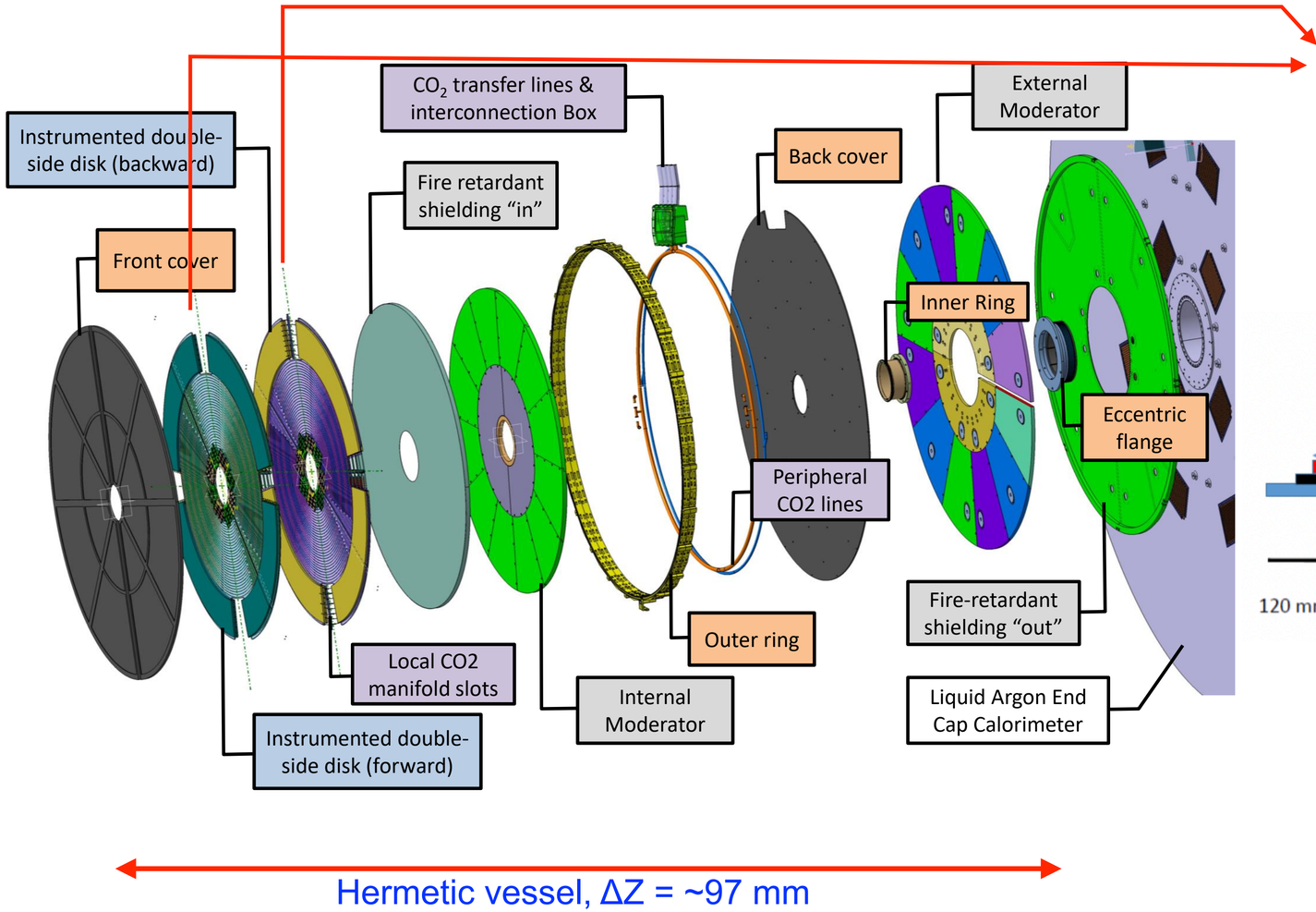


High Granularity Timing Detector

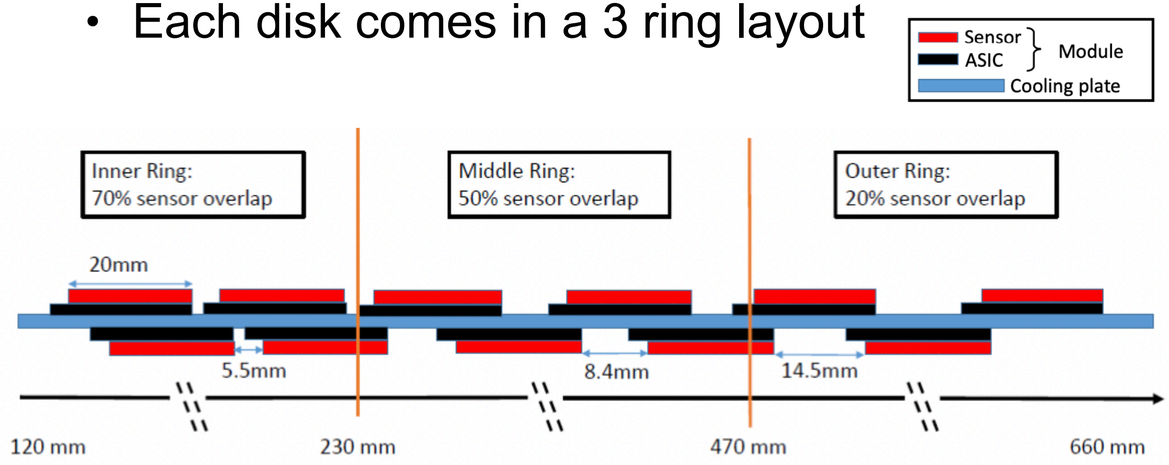


- Pixel detector with coarse spatial resolution but **highly precise time** measurements
  - Time resolution per track (hit):
    - 30-50 ps (35-70ps)
  - Luminosity measurements, bunch by bunch, i.e. 40MHz readout
    - Goal for HL-LHC: 1% luminosity uncertainty
  - Approved by CERN LHCC in Sep 2019
- Two HGTD end-up disks installed in the gap between barrel and end-cap calorimeter
- $z \sim \pm 3.5$m from the nominal interaction point
- Total radius: 11 cm < R < 100 cm
- Active region covering:
  - $2.4 < \eta < 4.0$, 12 cm< R < 64 cm
- Radiation hardness requirements:
  2.5×10^{15} n_{eq}/cm^2 (w/ Safety Factor=1.5)
  or 2 MGy (w/ SF=2.25)

Detector Vessel

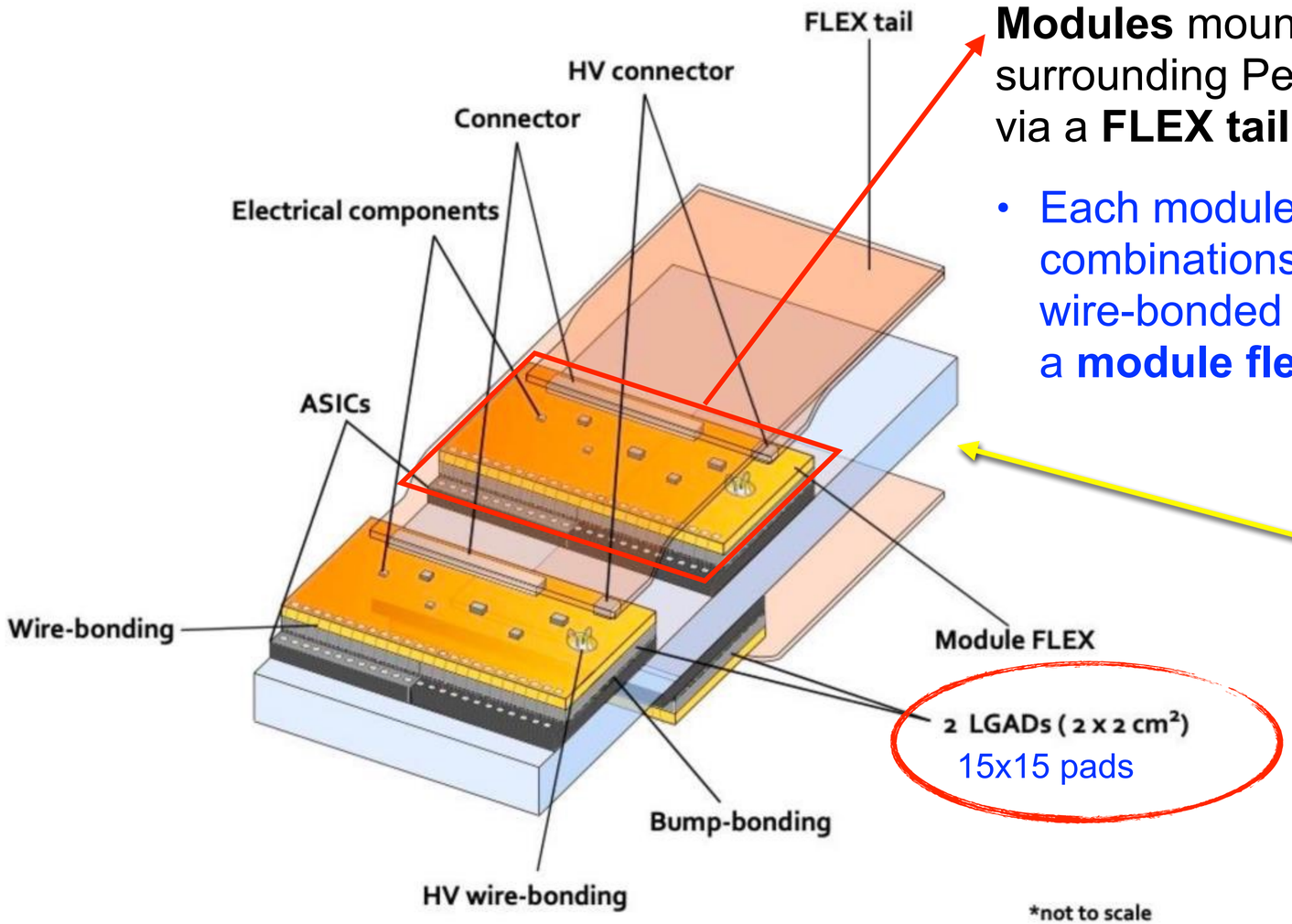


- Each vessel has two instrumented disks with double-sided layers
- Each disk comes in a 3 ring layout



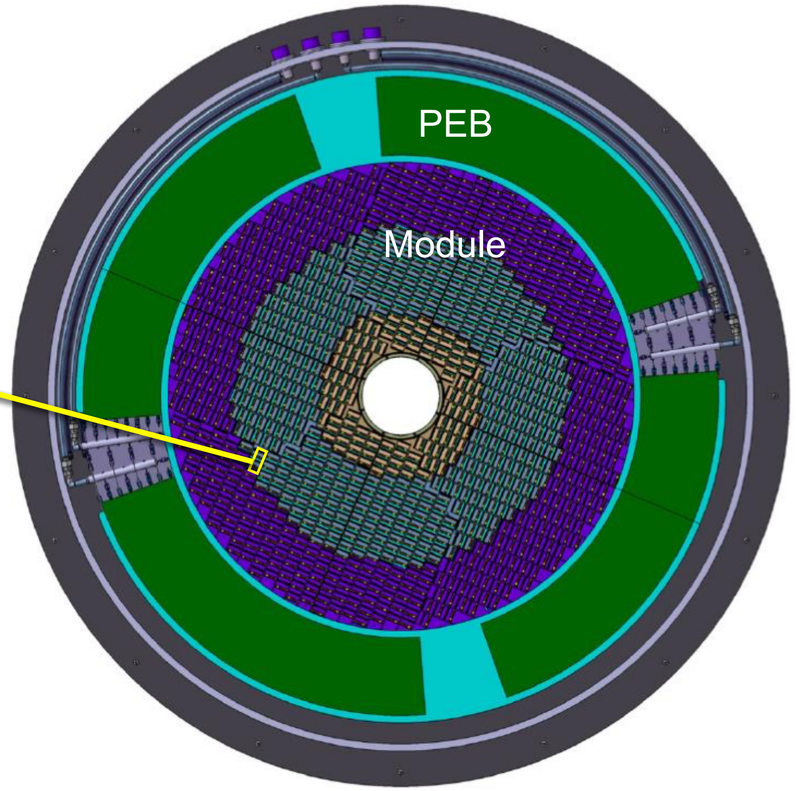
- In total: 8032 modules
  ➔ 6.4 m^2, 3.6M channels

Detector Module



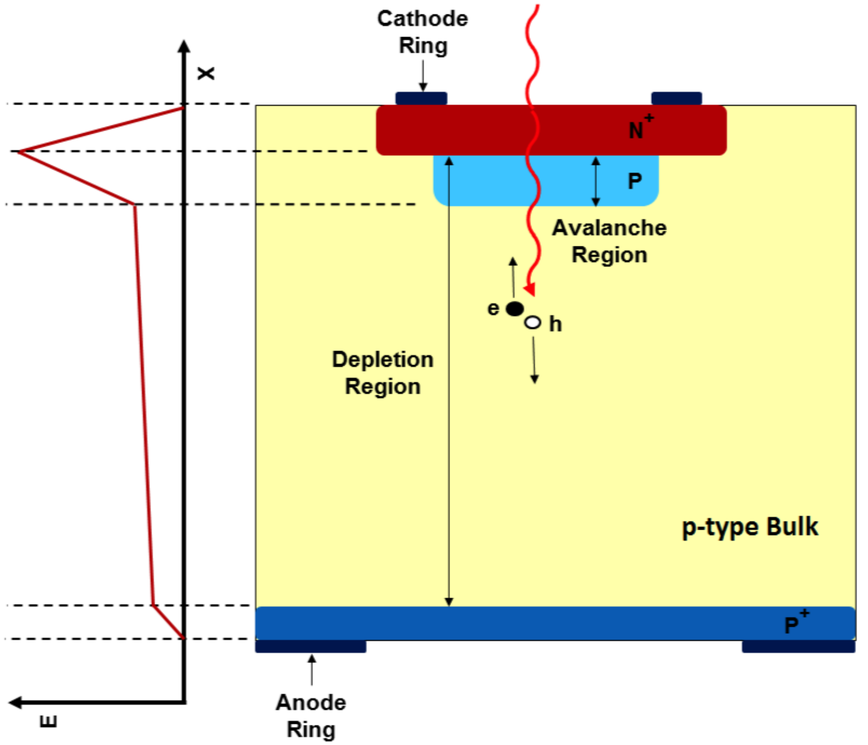
Modules mounted on cooling plate, connected to the surrounding Peripheral Electronics Boards (**PEB**s) via a **FLEX tail** cable

- Each module consists of two bump-bonded **sensor** + **ASIC** combinations, glued and wire-bonded to a **module flex**



Sensors: Low Gain Avalanche Diode

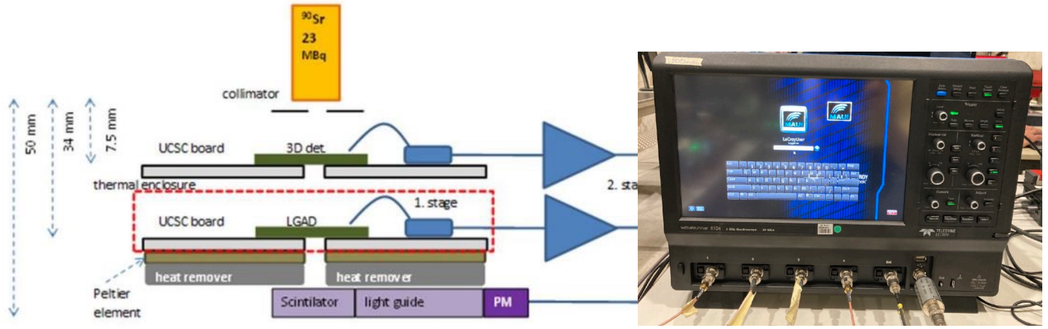
- Low Gain Avalanche Diodes
  - Compared to APD and SiPM, LGAD has modest gain of 10-50
  - High drift velocity, thin active layer — favoured for fast timing
- LGAD for HGTD:
  - 50 μm thick
    - Compromise between Landau fluctuations contributing to the time resolution, charge/bias property etc.
  - Pad size 1.3x1.3 mm^2
    - Compromise between rise time, capacitance, occupancy, fill factor…
  - Signal level: 10fC (w/ 20 gain) before and 4fC (w/ 8 gain) after irradiation

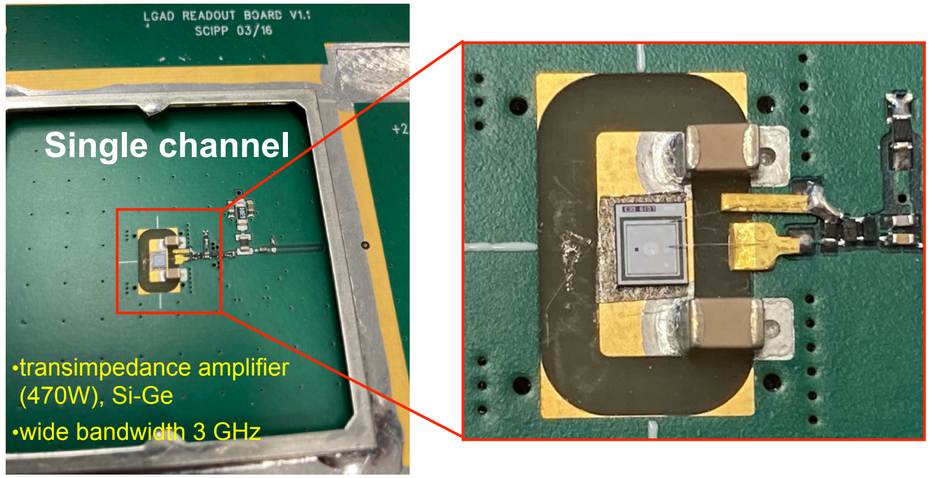


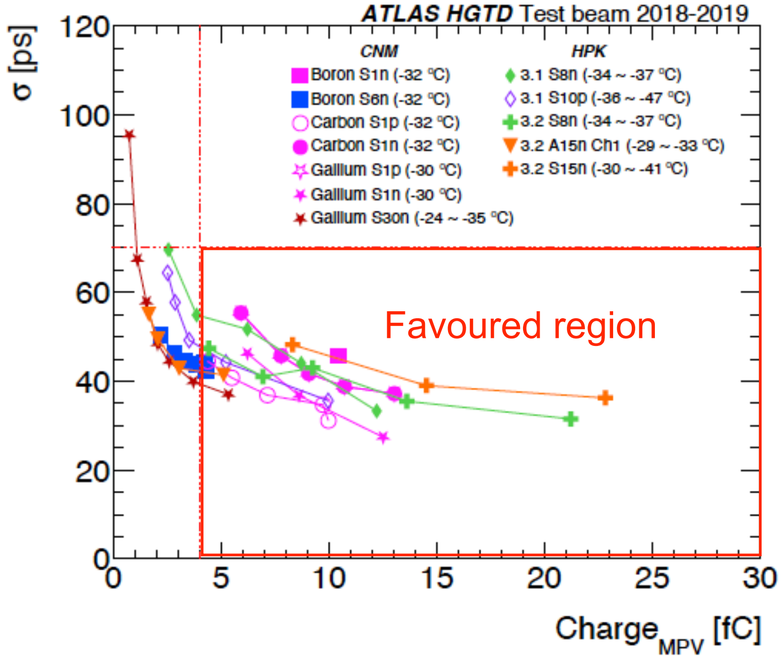
Thorough studies carried out with small prototypes and full size sensors, only selected examples shown here

Measuring the sensor performance

- UCSC boards widely used in the lab and at the test beam
  - Versions of 1 or 4 channels for single and 2x2 pad(s) prototypes
  - Help to explore the sensor limits without ASICs
- HGTD Test Beam paper summarising 2018-2019 beam test results: C. Agapopoulou et al 2022 JINST 17 P09026
- Latest Test Beam results see Valentina's talk "Performance studies of the Low Gain Avalanche Detectors for the ATLAS High Granularity Timing Detector in beam tests", today 9:15

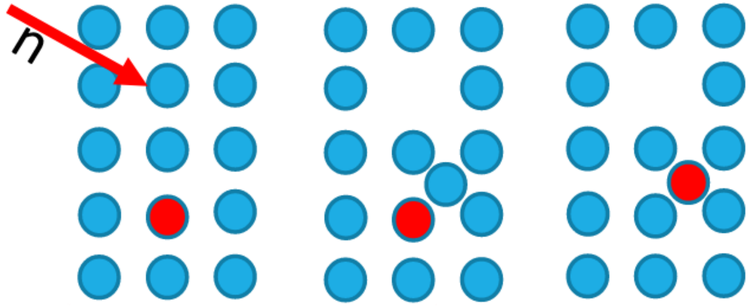


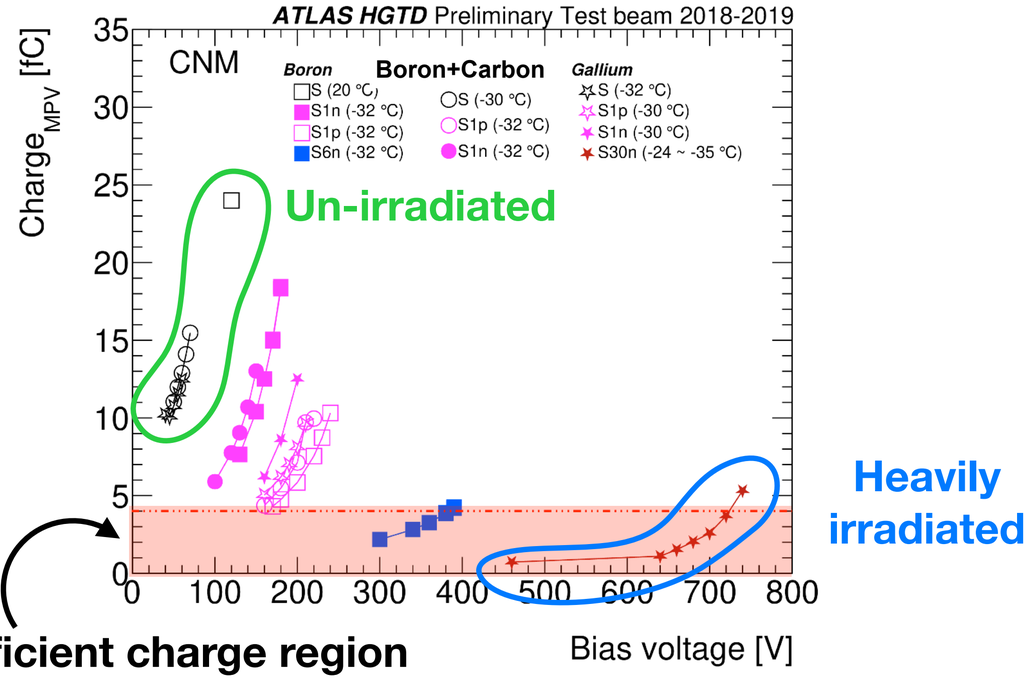




Irradiation damage on the LGAD sensors

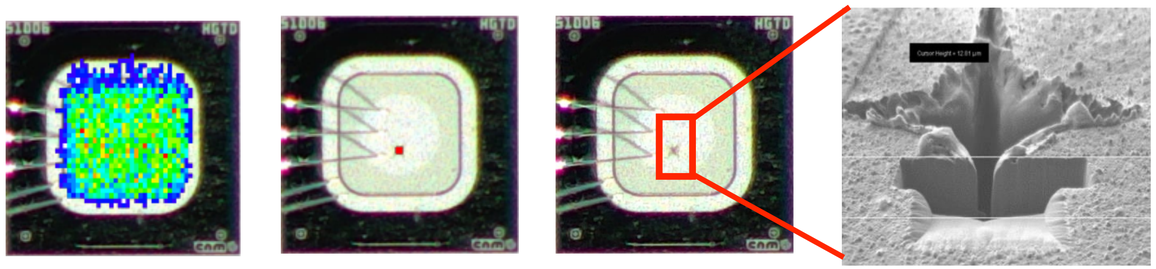
- HGTD targets at 70ps (hit) time resolution after 2.5×10^{15} n_{eq}/cm^2 **full radiation**
- Gain layer is the key property of the Low Gain Avalanche Diode contributing to S/N, timing and efficiency
  - Different gain layer designs (thickness, doping) studied using full radiation as reference
  - Gain layer doping affected by irradiation from the **"acceptor removal"** process (i.e. removal of the acceptor from its substitutional lattice site)
  - To recover the gain: **higher bias voltage is needed**

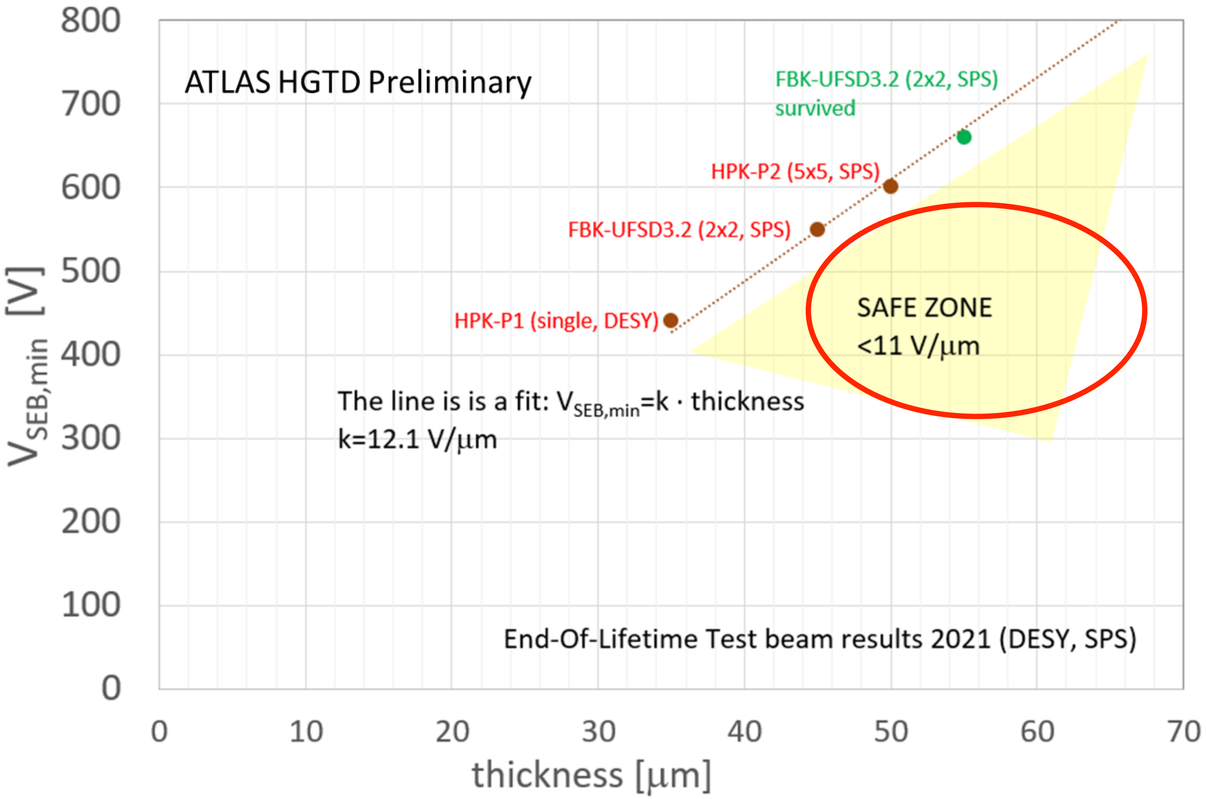




Single Event Burnout

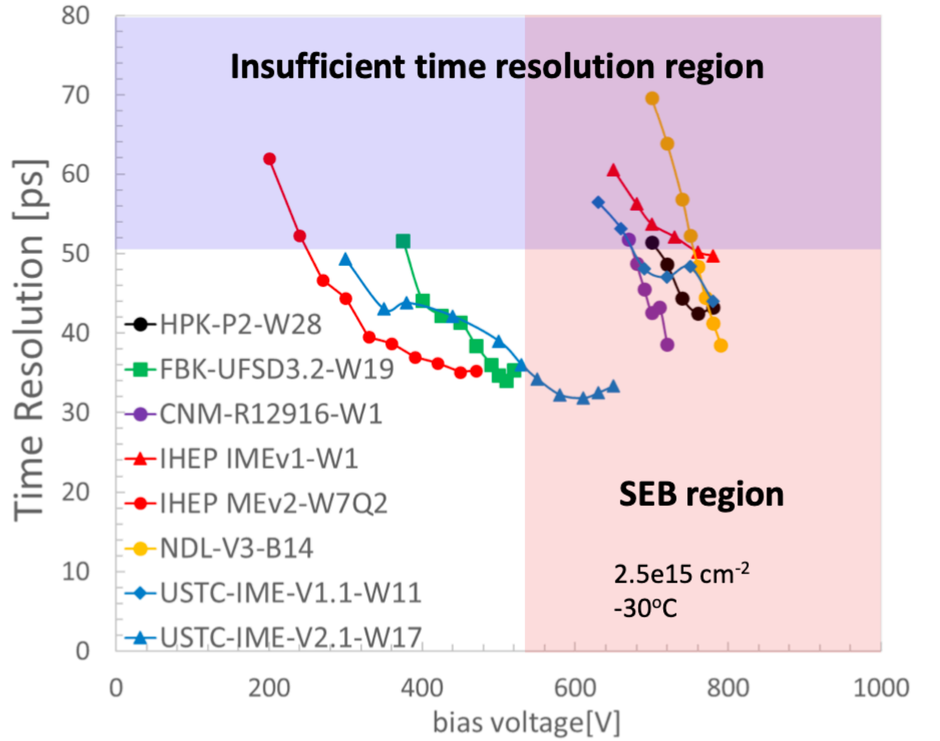
- Single Event Burnout (SEB) - when heavily irradiated sensors (~end-of-life 2.5e15 n_{eq}*cm^{-2}) operated with high bias voltage
  - Not a problem if operated with lower voltage!
  - A single particle which deposits enough energy (~tens MeV) causes: conductive path leading to destructive breakdown
    - Confirmed & cross checked with R&D at CMS and RD50
  - Bias voltage safe from SEB: **< 11V/µm (i.e. <~550V for 50µm)**

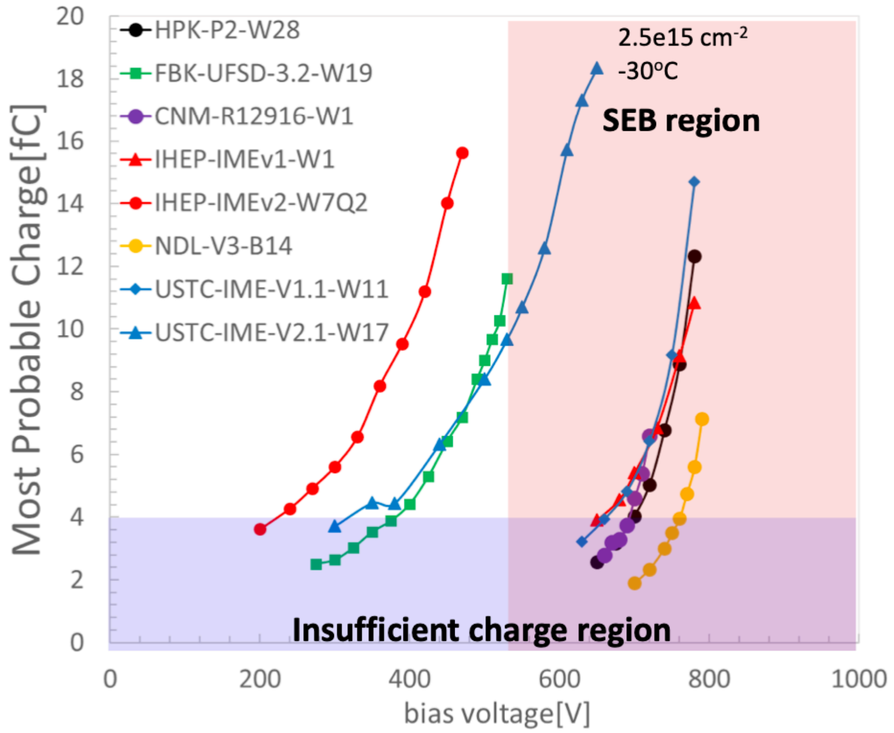




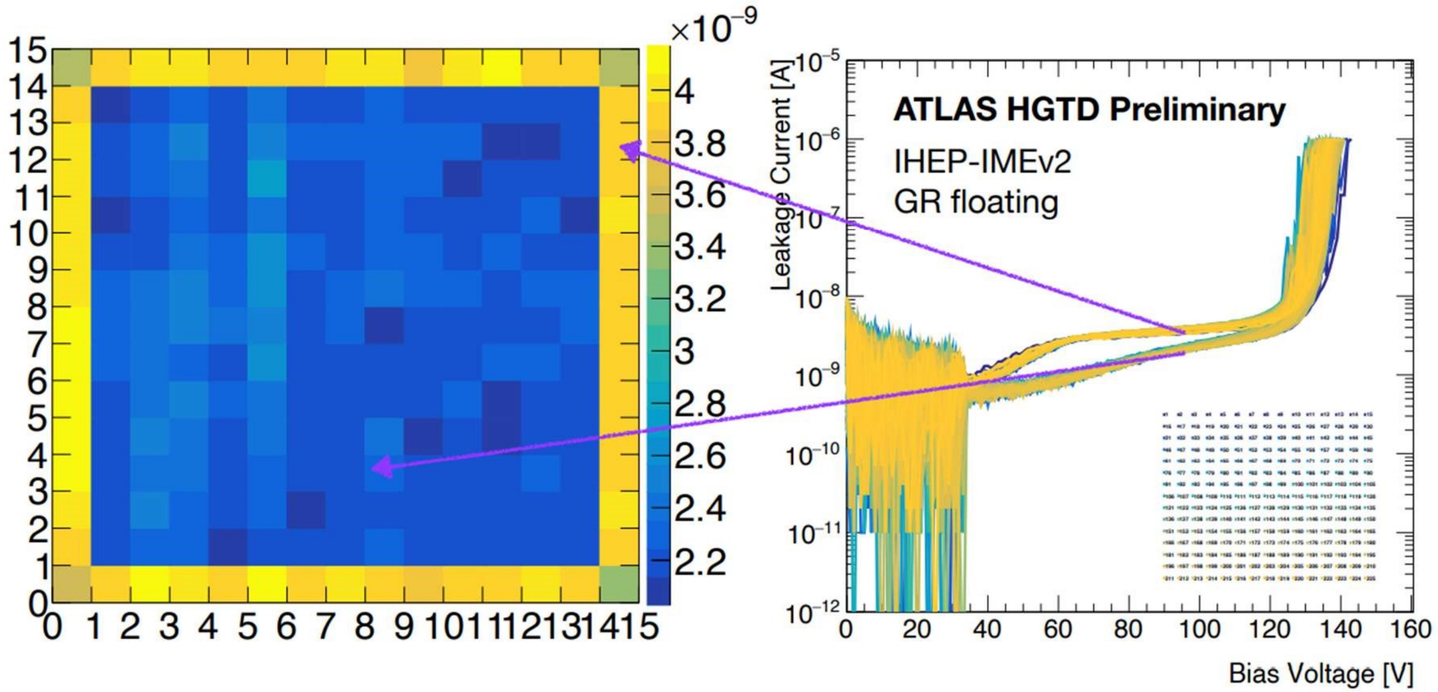
Carbon enriched gain layer design

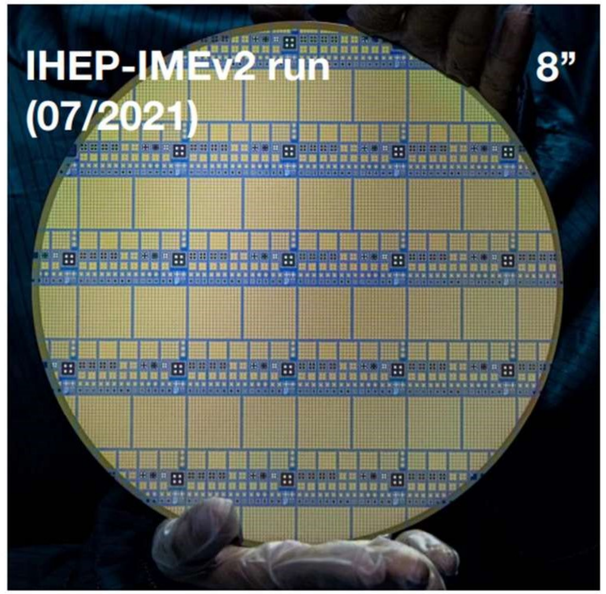
- Defect engineering: Carbon enrichment reduces “removal speed”
  - Carbon enriched gain layer (C-GL) design
  - Only C-GL modules left in the safe white region
- **All C-GL sensors reached specification requirements!**
  - Below shows results from measurements using Sr90 in the lab, sensor irradiated with max. fluence
  - Confirmed by TB data (SPS TB 2021 & DESY 2022)





Full size sensor prototypes



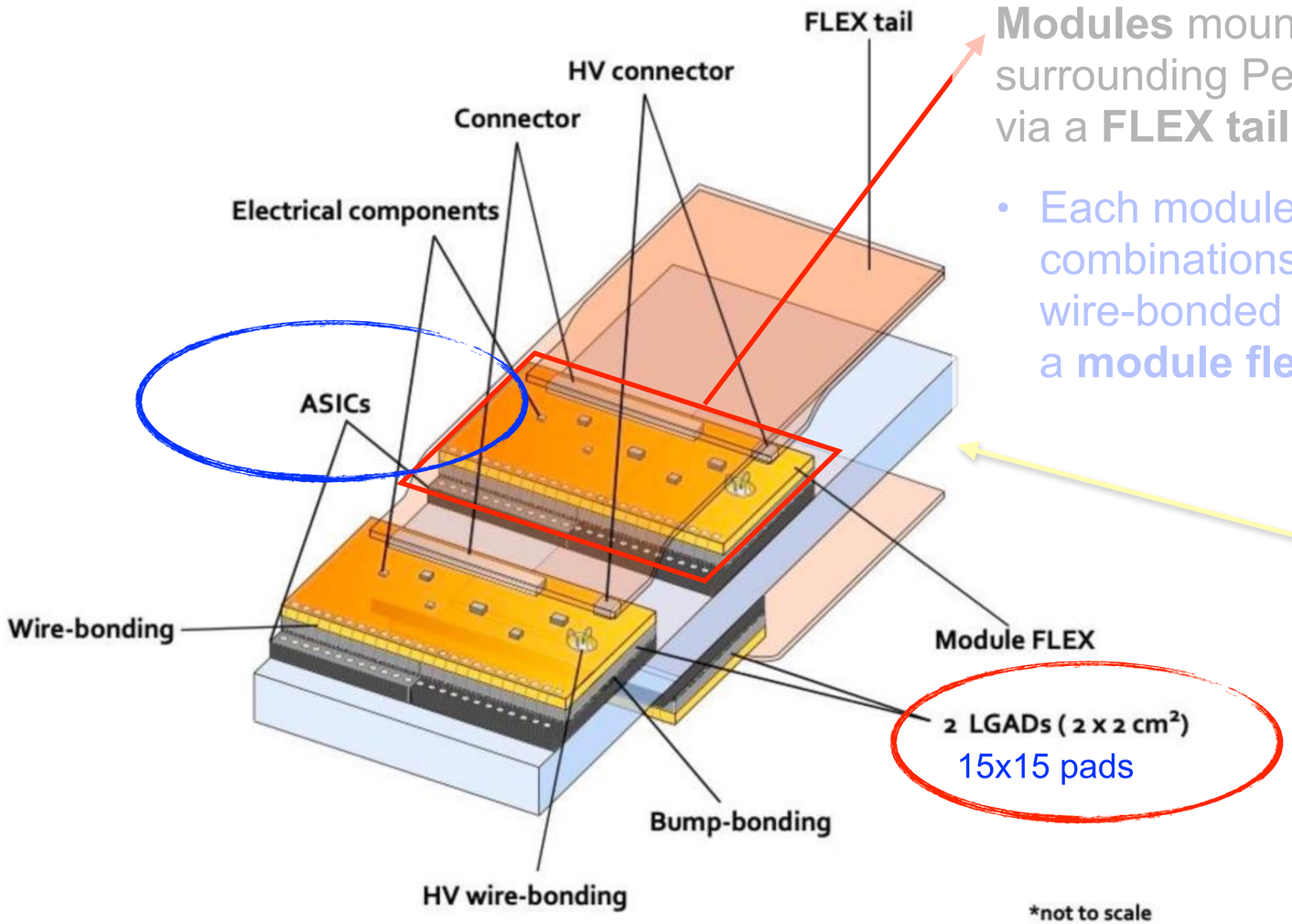


- Good uniformity of full size sensor prototypes (15*15 pads)
  - Sensors from various vendors: HPK, IME, FBK and CNM
- Example shown here from IME
  - electrical properties shown here, satisfying the required specifications.

More before sensor (pre)production

- ☑ QA/QC procedures both have been proposed
- ☐ Vendor verification

Detector Module



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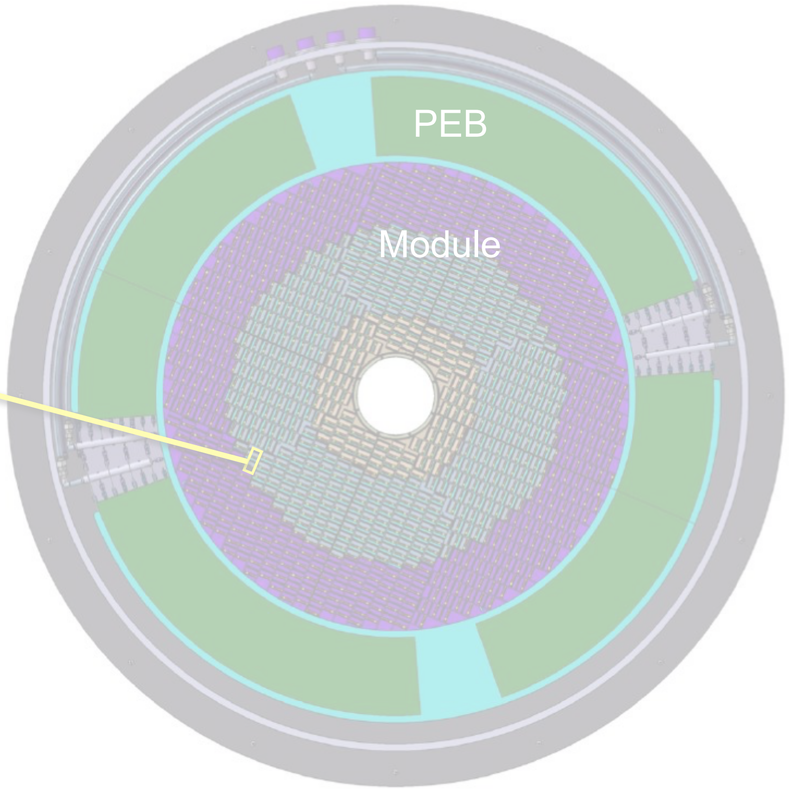
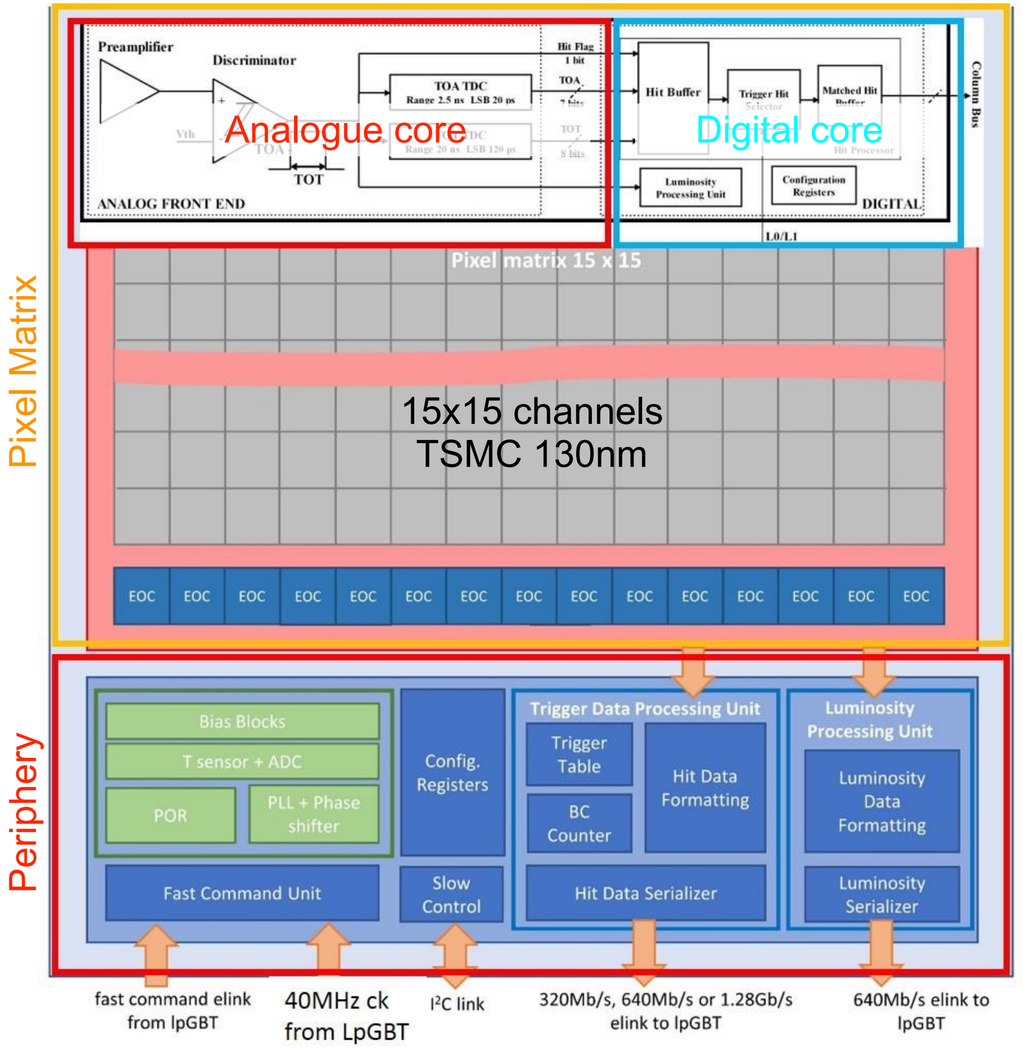


ATLAS LGAD Timing Integrated Readout Chip (ALTIROC)

ALTIROC, TSMC 130 nm CMOS,

Output two data paths:

- **Timing data**: Time of arrival (TOA) + time over threshold (TOT) data per channel, data stored in one local memory until L1A; requiring:
  - Jitter < 25ps @ 10fC / 65ps @ 4fC
  - Discriminator threshold min. 2fC
  - Integrated temperature measurement + calibration between fills to maintain resolution at system level
  - Low power: <1.2W/chip (TDC at 10% occupancy) to satisfy cooling budget
- **Luminosity**: per sensor hit multiplicity readout at 40MHz (used only in outer ring)



ALTIROC R&D Roadmap

- **ALTIROC0**: version 0 ASIC, **preamplifier + discriminator** waveform sampling on the oscilloscope
- **ALTIROC1**: 5x5 array with **complete analogue** front-end (discriminator, **TOA, TOT**)
- **ALTIROC2**: **first** 15x15 full scale prototype, **first** digital module, with almost complete functionalities
  - **new territory in HEP:** first full scale bump-bondable 1GHz front-ends to readout 4 pF LGAD pixels
  - **Main goal: demonstrate the functionality/performance** of the ASIC (time resolution + luminosity counting) **alone & assembled with a sensor**

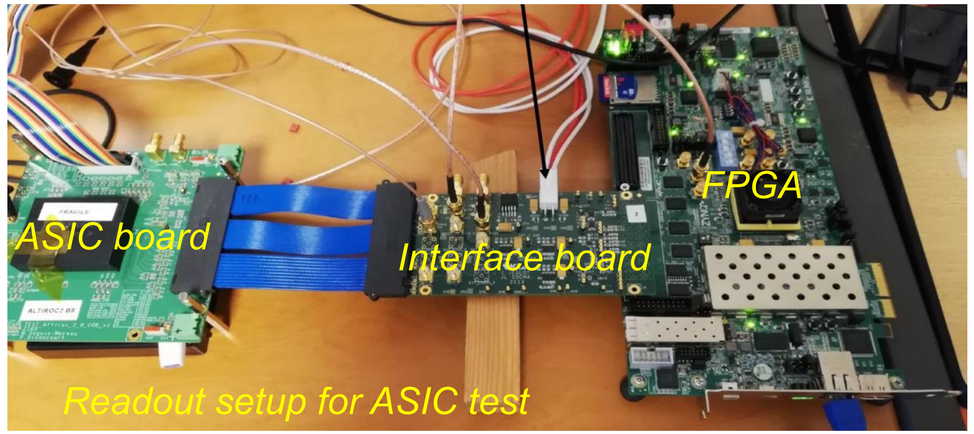
Only selected example performance shown here

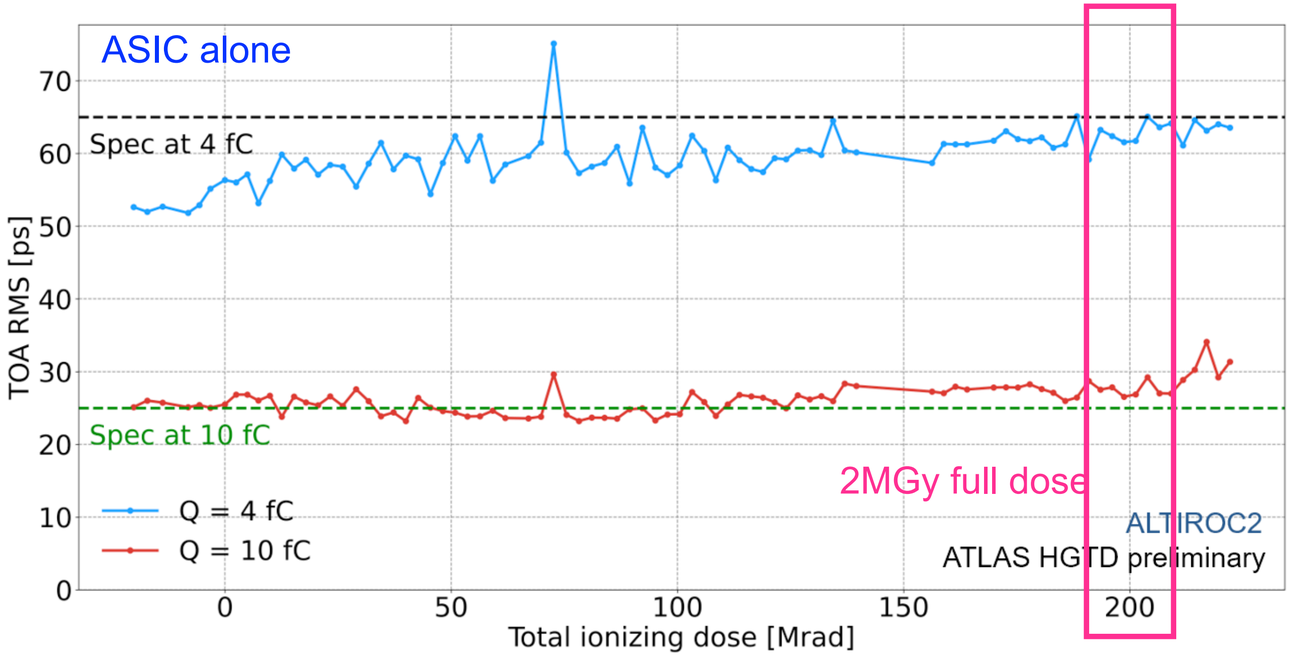
- Preliminary Design Review (PDR) on Oct 18

ASIC: ALTIROC2 performance

- Tested **with and without** full size sensor prototype
- Intensive tests prove it to be fully functional
  → thus used for module assembly tests and demonstrator tests
  - Close to specification as ASIC alone:
    meets the specs with one activated column ON at a time
  - Additional noise found in ASIC+LGAD assembly **- understood**:
    - Due to parasitic inductances separating sensor/preamp grounds.
    - Noise get amplified 10 times more than ASIC alone
    - **Close to spec** 2.6fC min. threshold **achieved**
- Radiation influence studied
  - Jitter stays stable with the increasing Total ionising does (TID).

More details see a talk @ TWEPP2022





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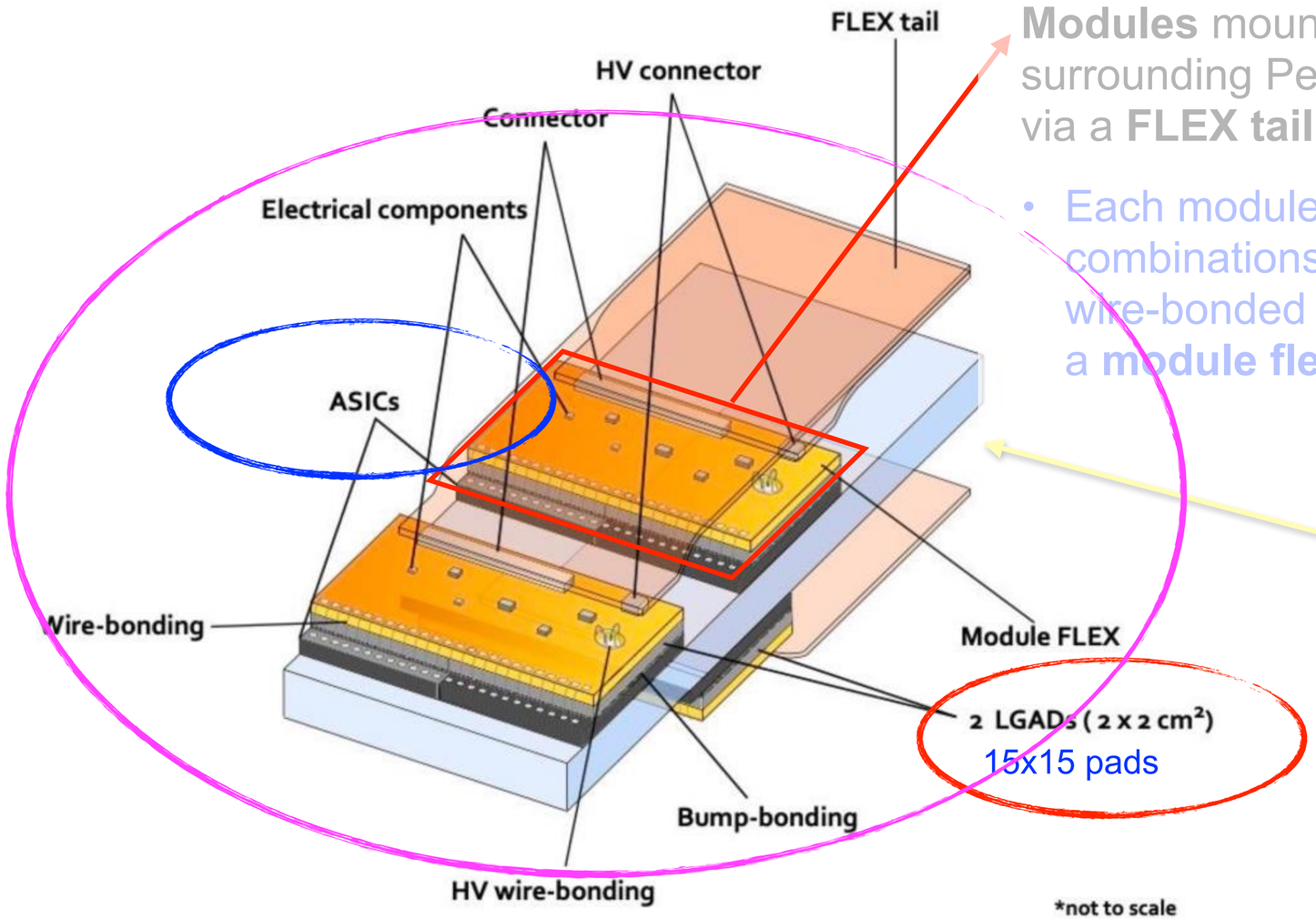
- Preliminary Design Review (PDR) on Oct 18
- **ALTIROC3**:
  - Number of improvements based on studies on ALTIROC2, including higher redundancy to improve robustness against single event effects, choice of the pre-amplifier etc.
  - Submission to foundry ~ Nov 2022 - to arrive at CERN early **Feb 2023**
- **ALTIROC-A** - pre-production ASIC
  - Design to start in **April 2023**
- Final Design Review (FDR) planned in **Oct 2023**

Detector Module



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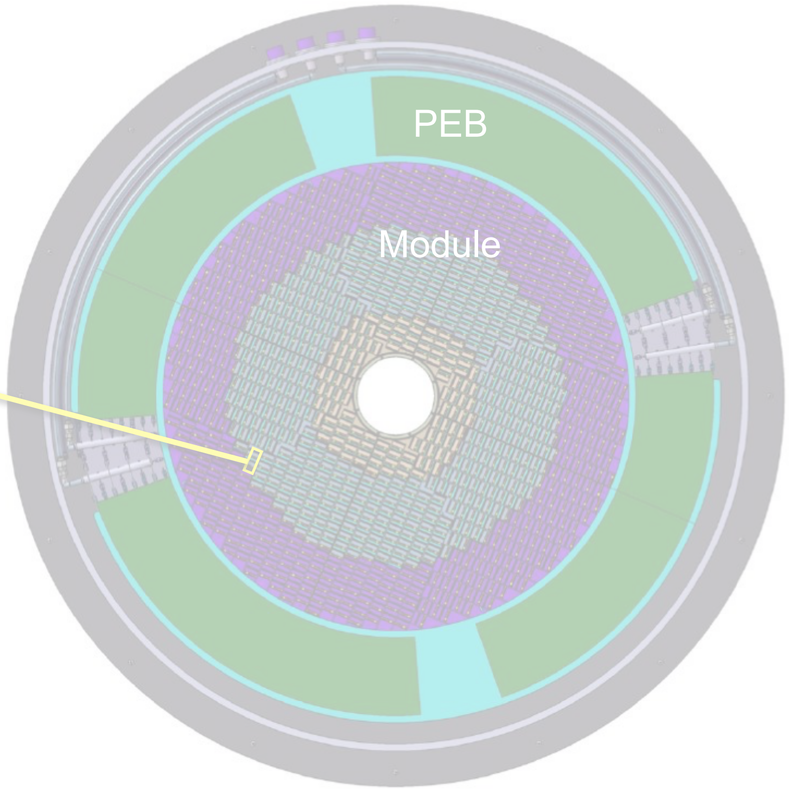


Sensor + ALTIROC2: Hybridisation

Testing hybrid prototype (full size sensor + ALTIROC2)

✓ 15 (Spain) +40 (China) +30 (Germany) hybrids produced

✓ **Bump-bonding connectivity**: validated with x-ray

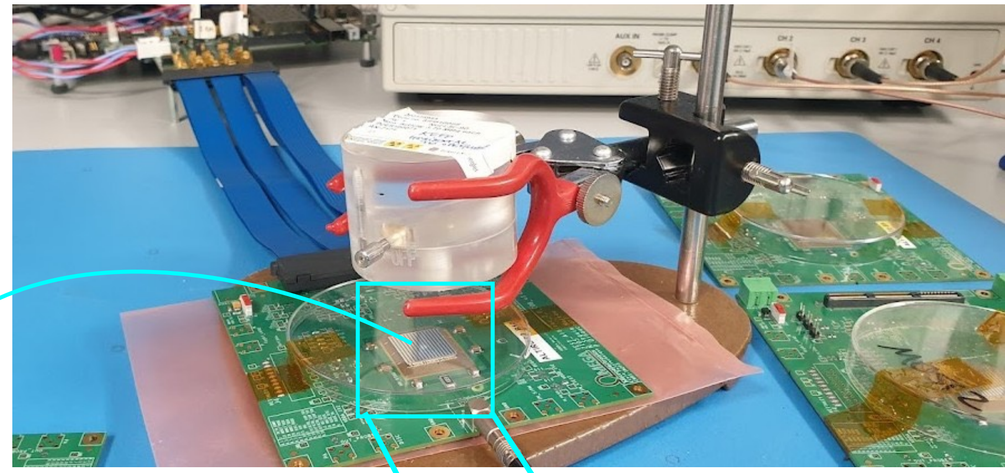
✓ **Good agreement** of break-down voltage and bulk current

✓ **Functionality** confirmed with Sr90 source tests in the lab

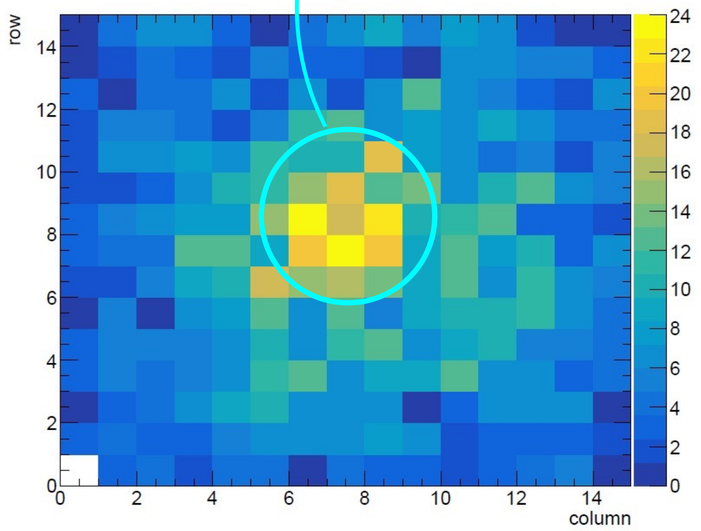
- ☐ To be further confirmed with beam tests

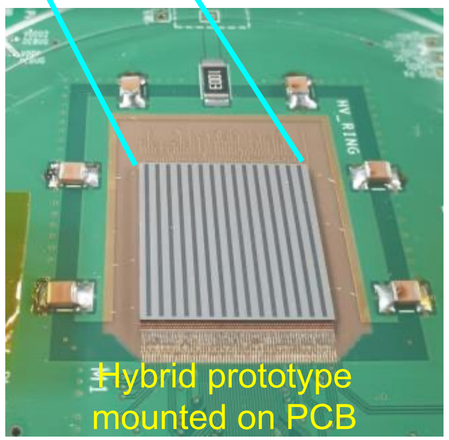
Work in progress **before (pre)production**:

- Beam tests in July and Sep 2022 at CERN, analyses ongoing
- Next beam test at CERN: Oct 19 - Nov 2



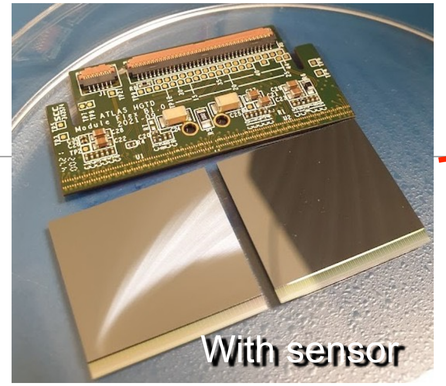
Reflecting where the source pointed



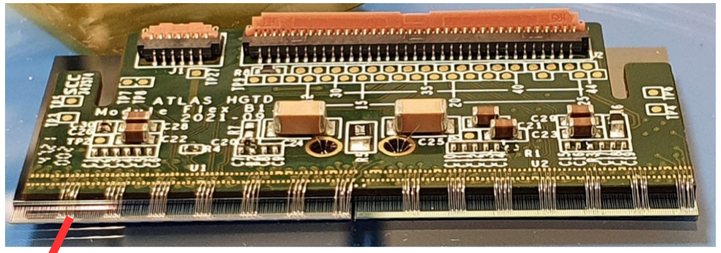


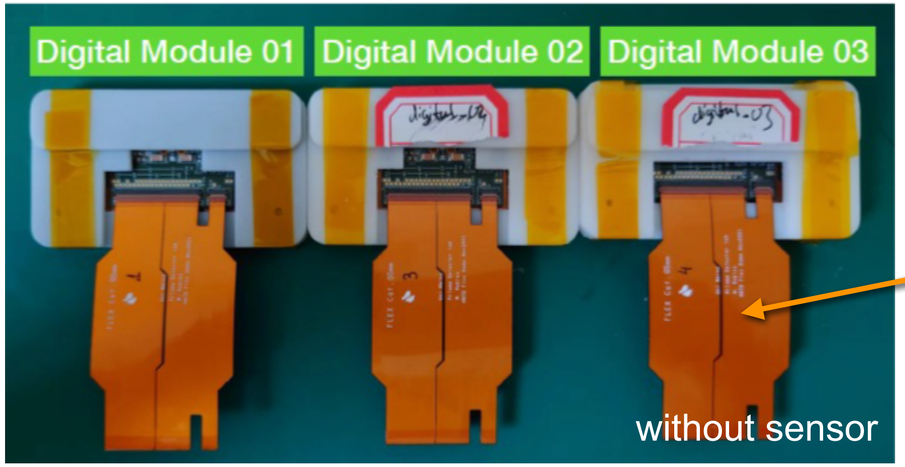
Module Assembly

- In total 8032 modules, each 2x4 cm2
  - Five full modules produced for tests
  - more without sensors (digital module) for DAQ chain tests
- Dedicated tools developed
  - Bending the flex, aligning and placing the hybrids on the flex, and gluing the assembly
- Module-level test system developed
  - An adapter card produced and successfully tested

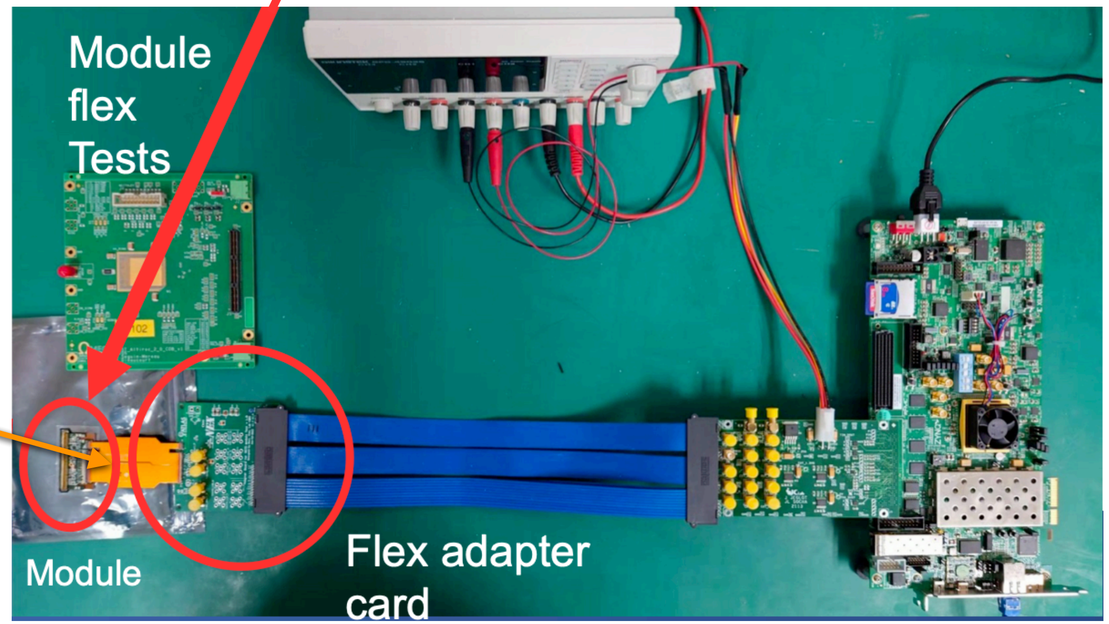


glue+
wire-bonds



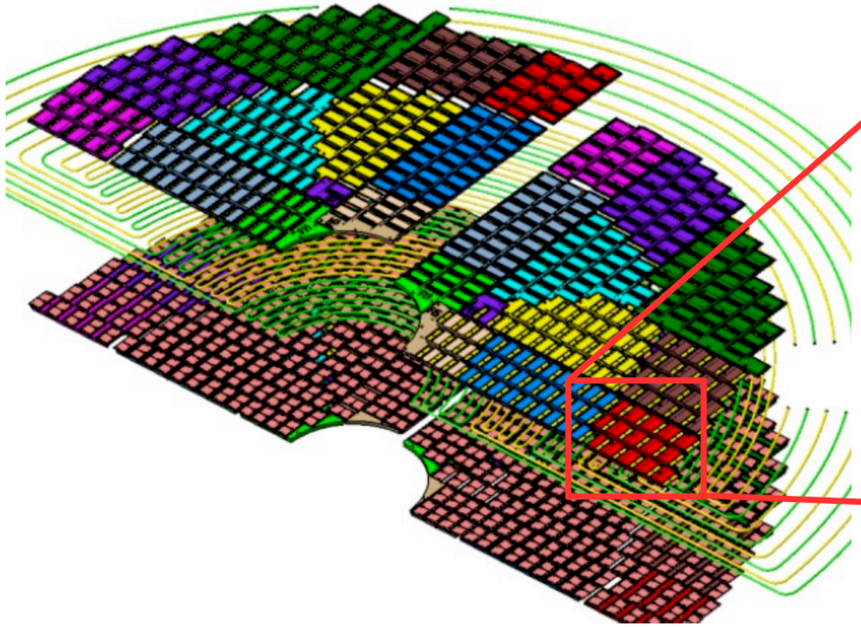


Flex tail

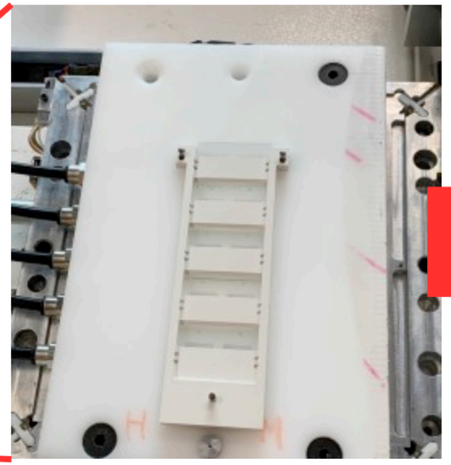


Detector Units

12x2 DUs per quarter
(on both sides)



Detector Unit



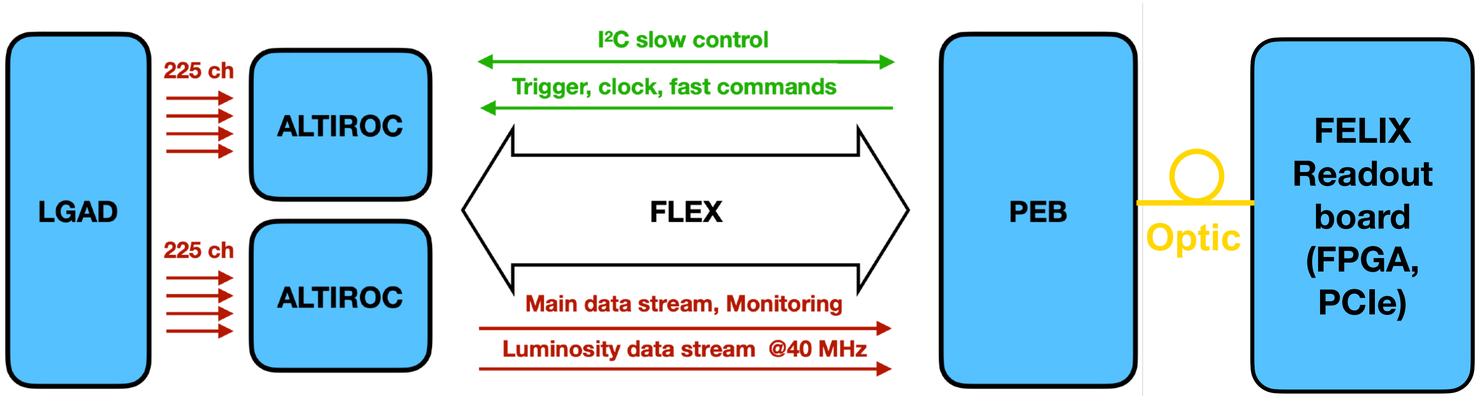
Loaded
Detector Unit

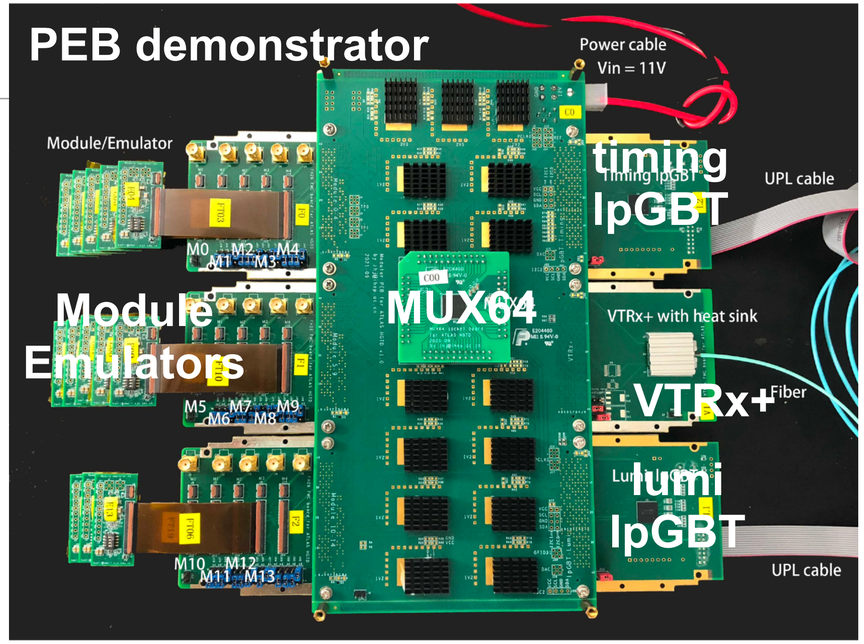
Dummy parts used for tests

- Module layout converging
- Flatness critical parameter to ensure contact of modules with cooling plate
- Various materials investigated
- Various companies contacted, in-house production not excluded
- Early prototypes for heater and demonstrator tests produced and tested

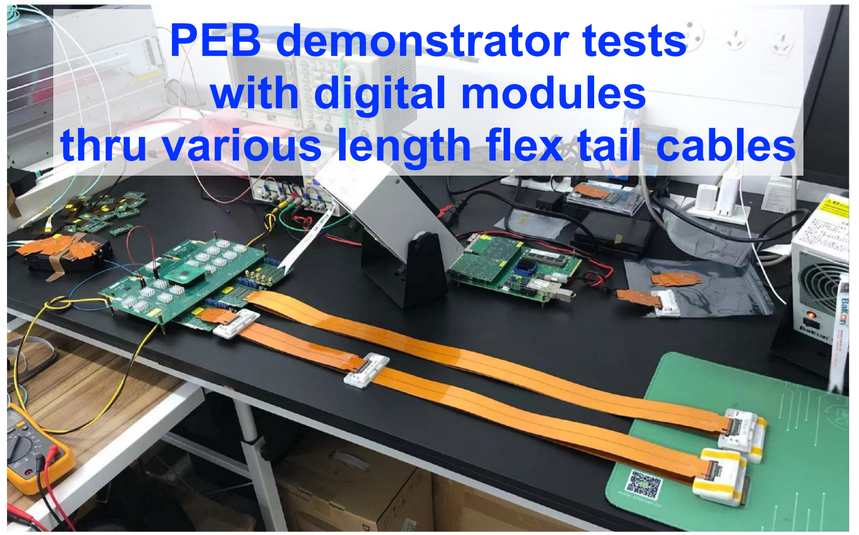
384 Detector Units, in 24 different shapes
Loading assemblies to detector units happens on the same site

Peripheral Electronic Board (PEB)



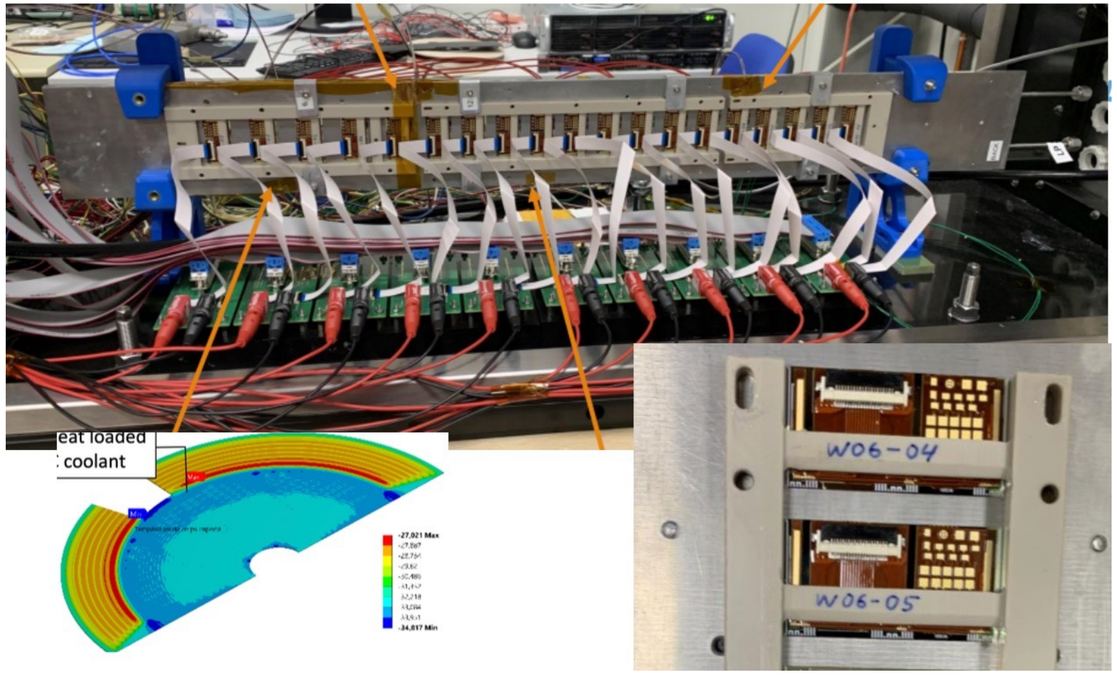


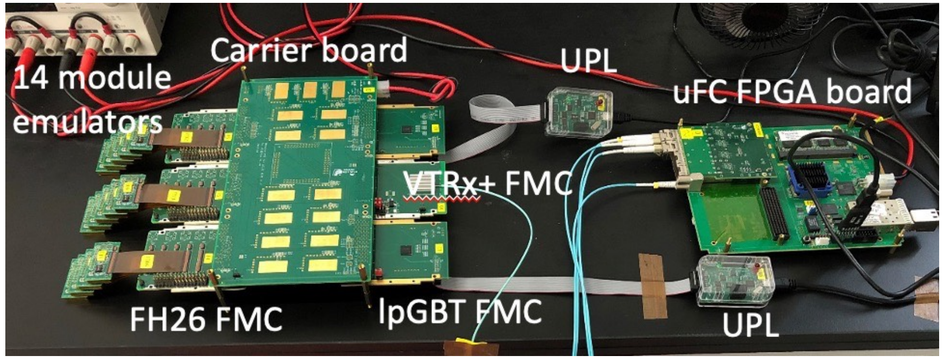
- Intensive work on characterising all individual components on its prototypes
  - DCDC converter bPOL12V - in depth investigated regarding space constraints, power efficiency
  - Intense tests communications via lpGBT with the FELIX readout card
    - First digital module data successfully dumped through FELIX early Oct.
  - MUX64: analogue multiplexer (for monitoring ASIC power supply and temperature)



Demonstrator

- Heater demonstrator
  - 19 silicon heaters mounted on a silicon stave
  - Representing modules dissipating heat
  - On the cooling plate (CO_2 cooling)

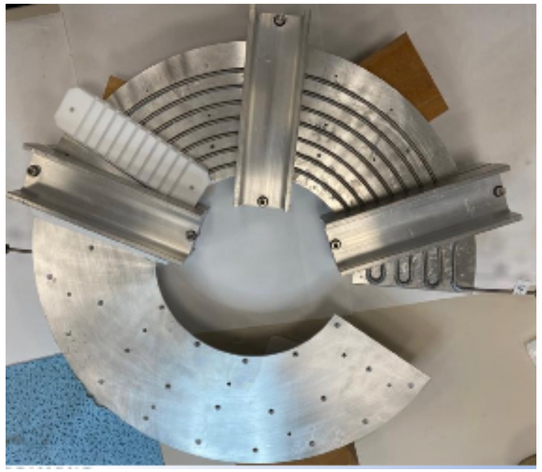




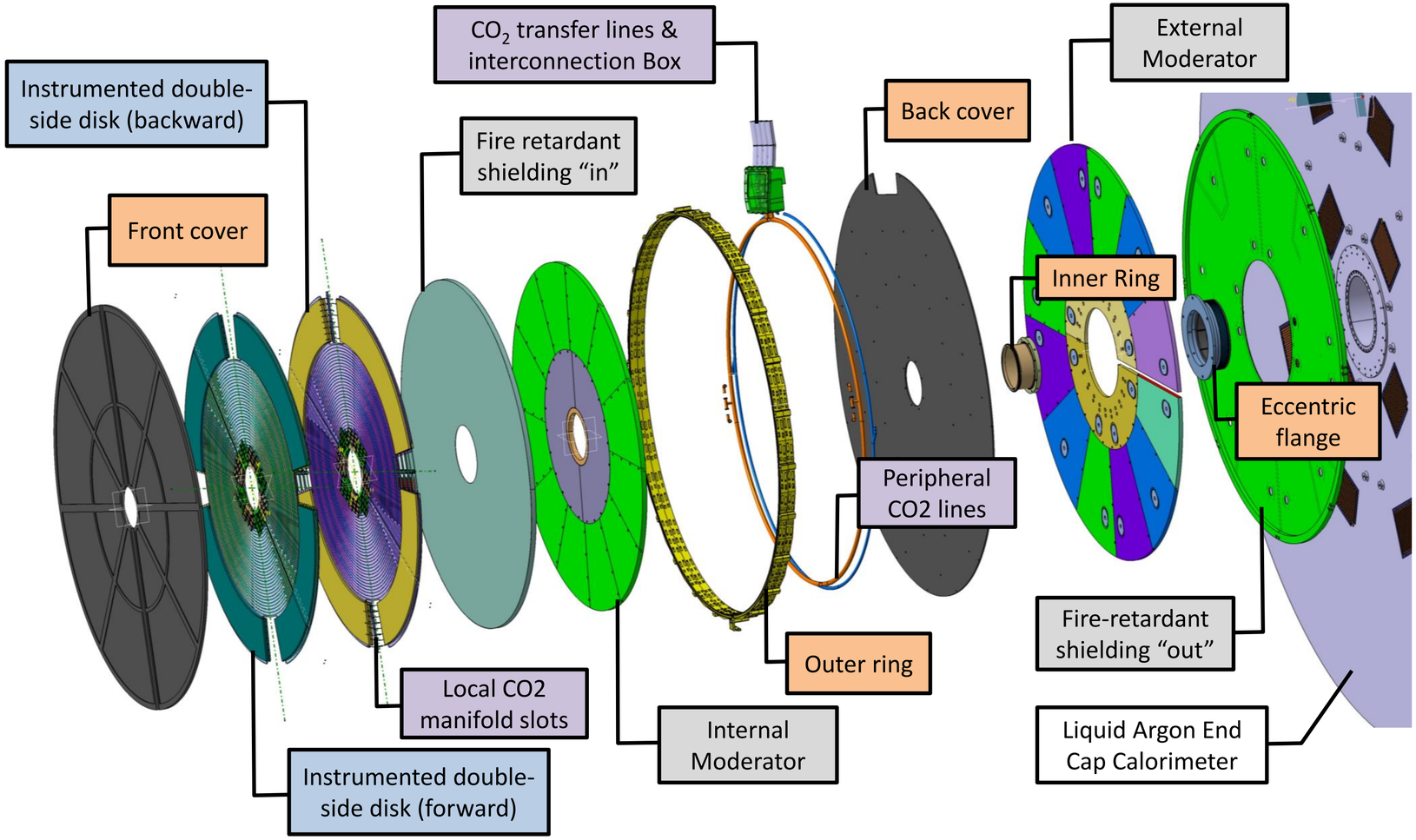
- DAQ Modular PEB demonstrator
  - 4 copies across institutes working on various aspects (firmware, software, system tests, luminosity etc.)
  - A mini full chain readout demonstrator, from module emulator boards to FELIX board
  - Support up to 14 modules with two lpGBTs and one VTRx+
  - Latest update:
    - Timing data can reach up to the **benchmark bandwidth 320Mbps** with **14 modules** fully loaded
    - Luminosity data can reach the **required 640 Mbps** with **7 modules** loaded
    - Various copies upgraded to digital modules with ALTIROC2 for firmware and software development

HGTD Mechanics and service

- Specifications on Hermetic vessel and on-detector cooling defined - next week review the preliminary design
- Cooling plate with CO2 loops design and prototyping in good progress
- Outer ring in progress: Challenging tight junction design with lots of feed-throughs



Prototype of cooling plate



Conclusion and outlook

- The HGTD will yield track time measurements with a time resolution of 30-50 ps in the forward region 2.4-4
  - Expect important benefits from suppression of pile-up tracks and forward jets, and more potential in object identification
- Great progress has been made in developing the LGAD sensors and the ALTIROC readout ASICs
  - Good progress in LGAD design fulfilling the radiation hardness requirements
    - Carbon enriched LGADs fulfil the radiation hardness requirements up to 2.5e15 n_{eq}/cm^2
  - ALTIROC2 (first full size prototype) tested, so far all blocks functional and performed as expected
    - ALTIROC3 submission expected in November
- Stay tuned for the next milestones:
  - 2023: many critical elements (Sensor ASIC and PEB) move to the pre-production phase
  - 2024: module and detector units pre-production start
  - 2025-2026: HGTD-A, HGTD-C vessels integration

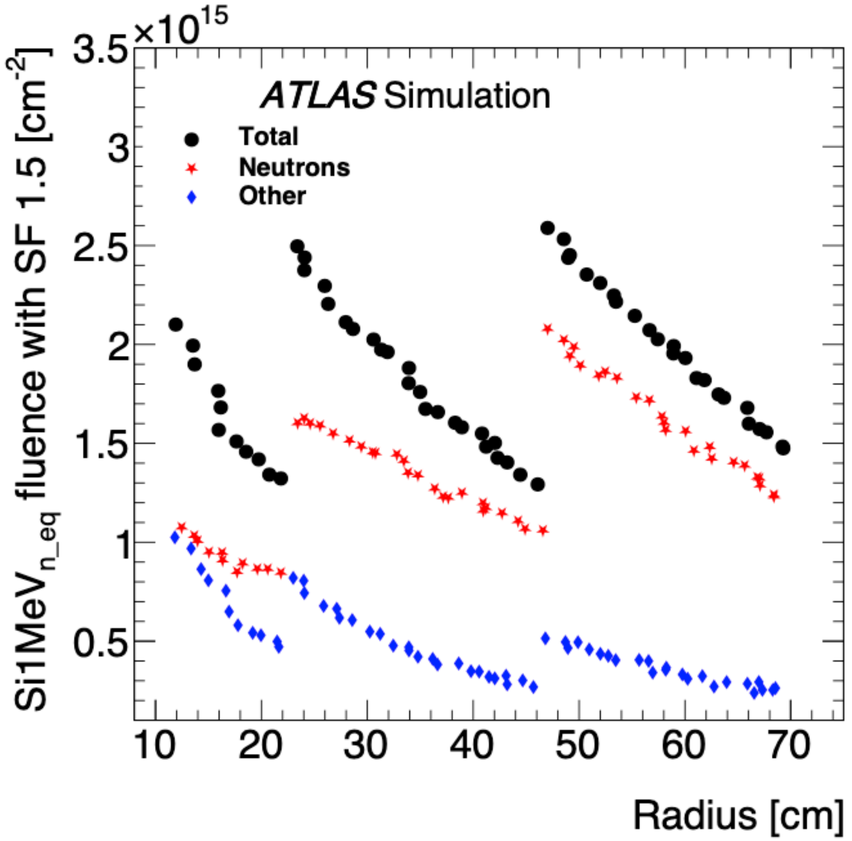
Backup

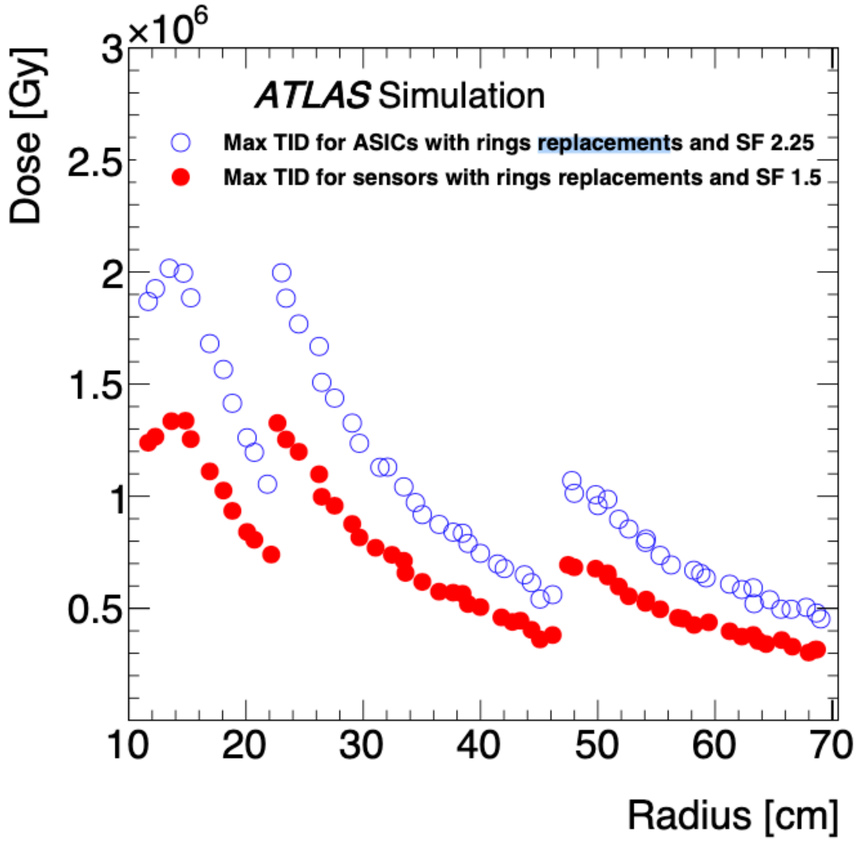
You’ve got one

Replacement plan

- Inner rings replace every 1000 fb^{-1} (3 times in total);
- middle ring every 2000 fb^{-1} (1 time)
- outer ring kept the same

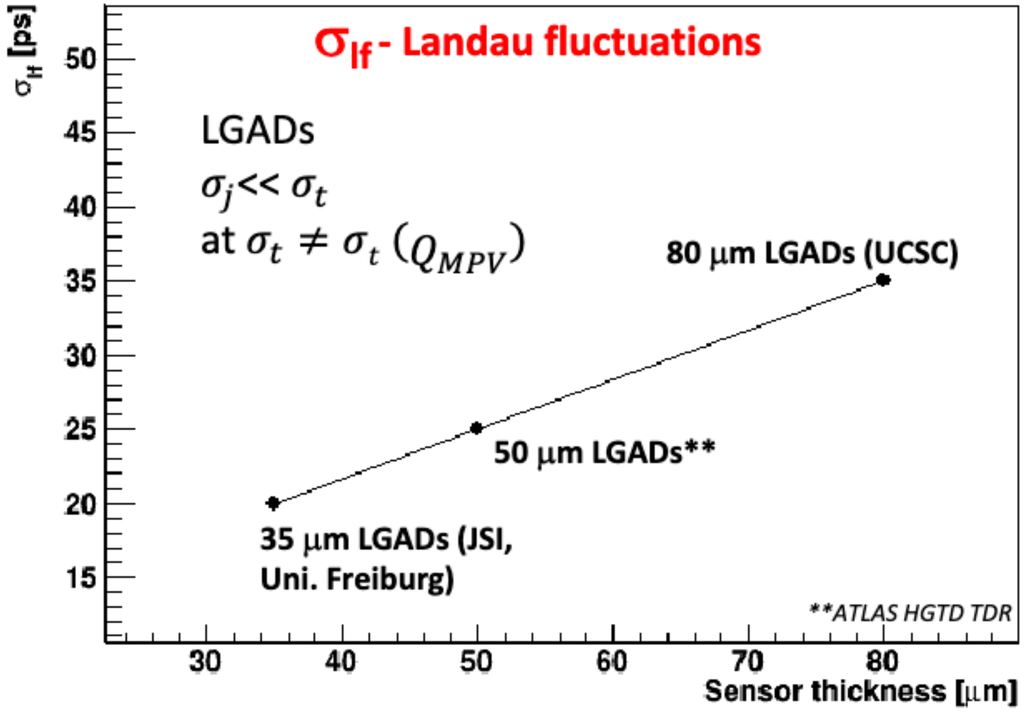
➔To not exceed 2 MGy and 2.5 × 1015 neq/cm2





Choice of detector geometry

Slide from G. Kramberger



$$\sigma_t^2 = \sigma_j^2 + \sigma_{tw}^2 + \sigma_{TDC}^2$$

time res. — noise jitter — time walk — TDC

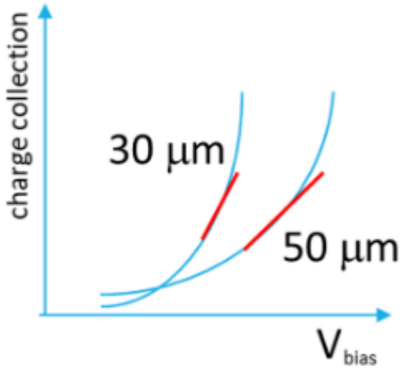
$$\sigma_j = \frac{\sigma_n}{\left|\frac{dV}{dt}\right|} \approx \frac{\sigma_n}{\left|\frac{S}{\tau_p}\right|} = \frac{\tau_p}{S/N}$$

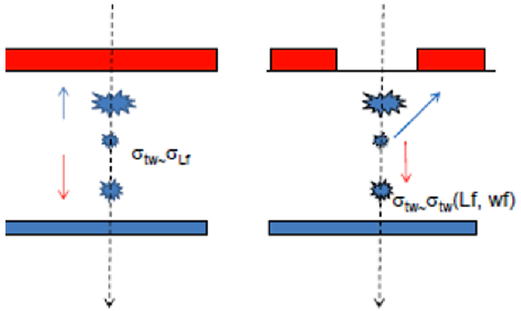
Active thickness ~50 (+/-5) μm

- large capacitance (noise) can be offset by gain -> good S/N
- In order to reach the desired time resolution the thickness is limited to <80 μm (Landau fluctuations)
- thinner sensors have steeper Q-V (difficult to control the bias voltage over a single module)

Cell size 1.3x1.3 mm² determines:

- capacitance (dominated by capacitance to the back, inter-pixel capacitance ~0.5 pF – measured and shown at PDR)
- assures that weighting field is 1/thickness and that the role in contribution to the time walk is negligible – dominated by the σ_{lf}
- pixel hit occupancy and fill factor (indirectly)

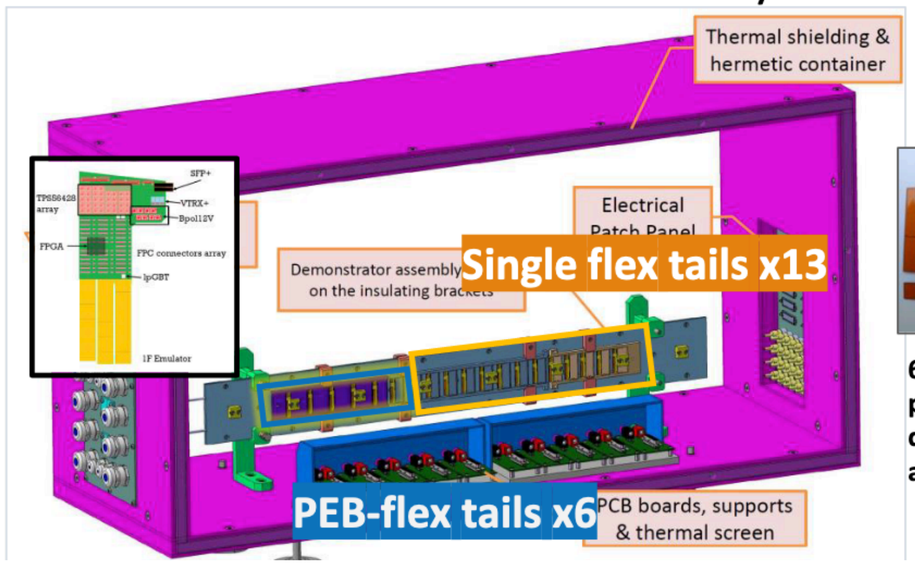


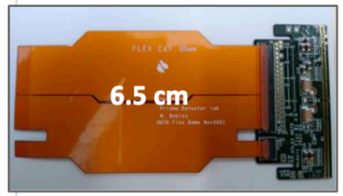


Flex cable tail status

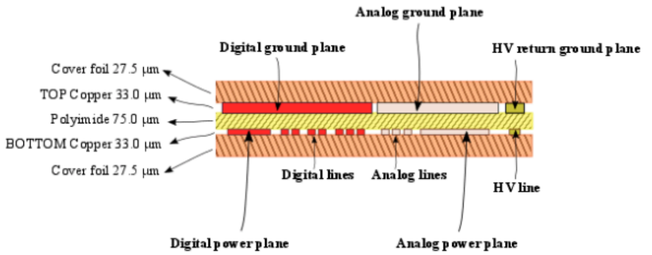
Slide from M. Robles-Manzano

- Flex cable tail for the demonstrator was designed based on previous flex PCB
  - **13 different lengths** defined by the position of the connector on the module loaded on the support unit and the connector on the PEB: **90 pieces**
  - Additional length (65 mm long) for testing purposes on sites (module qualification): **40 pieces**
  - **Flex cable tails manufactured** by same company

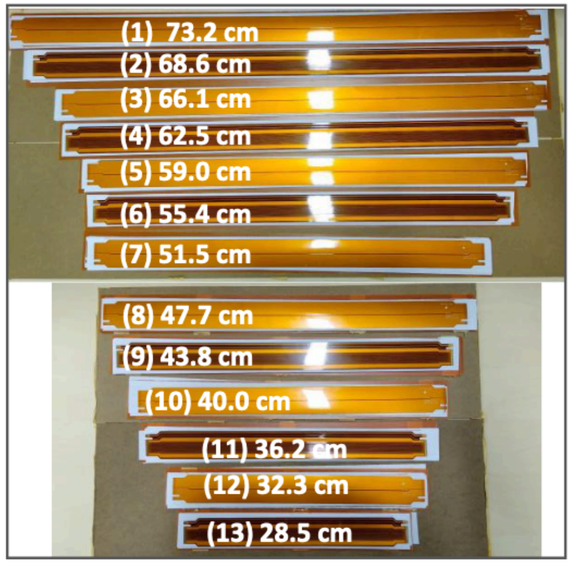




6.5 cm long flex cable tail prototype for the demonstrator attatched to a module flex prototype



Flex cable tail prototype stackup



Flex cable tail prototypes for the demonstrator 13 lengths : 73.2-28.5 cm long (longest and shortest length)