Science & Technology Facilities Council
Rutherford Appleton Laboratory

University of BRISTOL

CMS

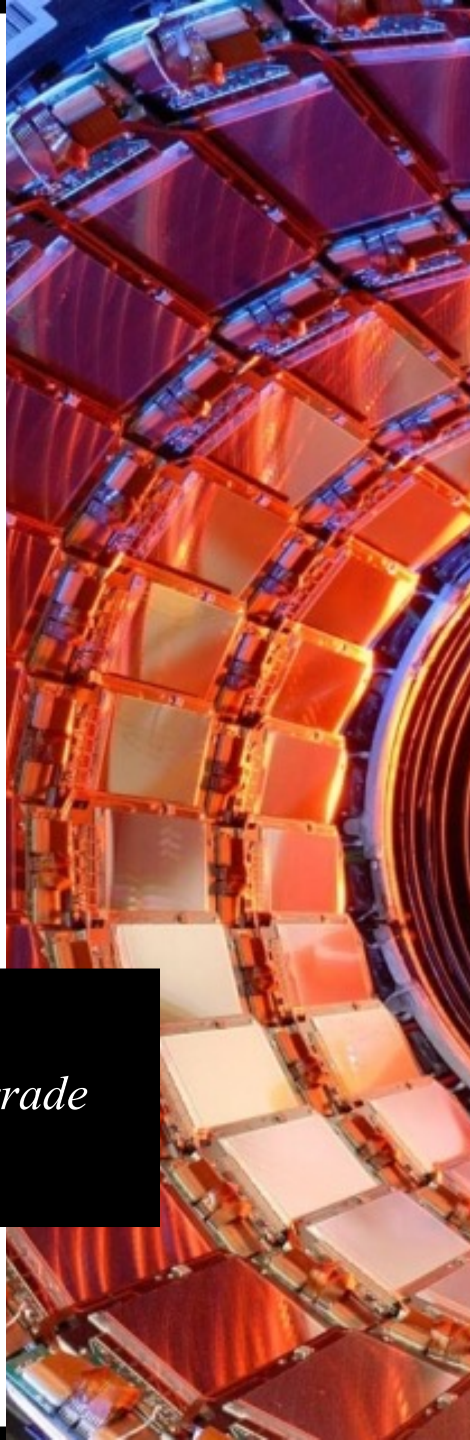
MEI-LI
HOLMBERG

LEVEL-1 TRACK FINDER

for the CMS HL-LHC upgrade

VERTEX 2022

24 OCTOBER
2022



OVERVIEW

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- Outer Tracker HL-LHC Upgrade
- Track Finder Hardware
- Track Finding Algorithm
  - Overview
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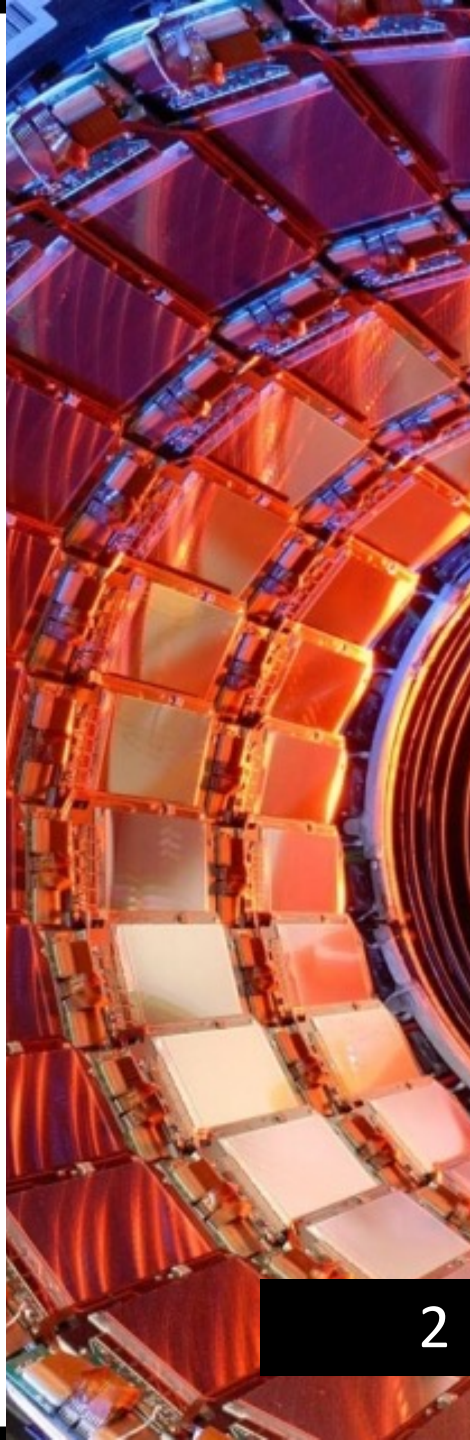
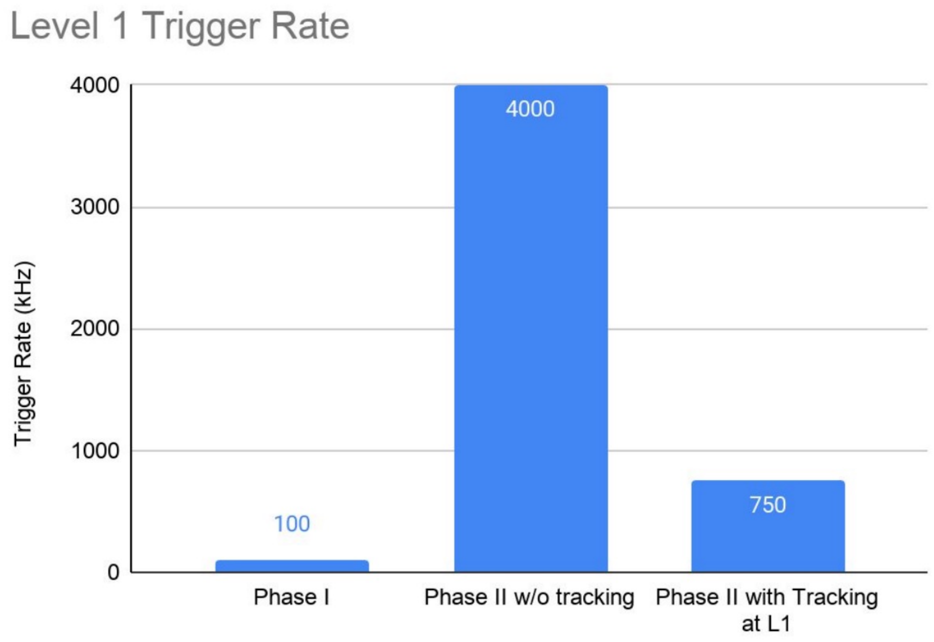
  - Project Design
- Algorithm Testing
  - Skinny Chain
  - Barrel-Only chain
- Summary



INTRODUCTION

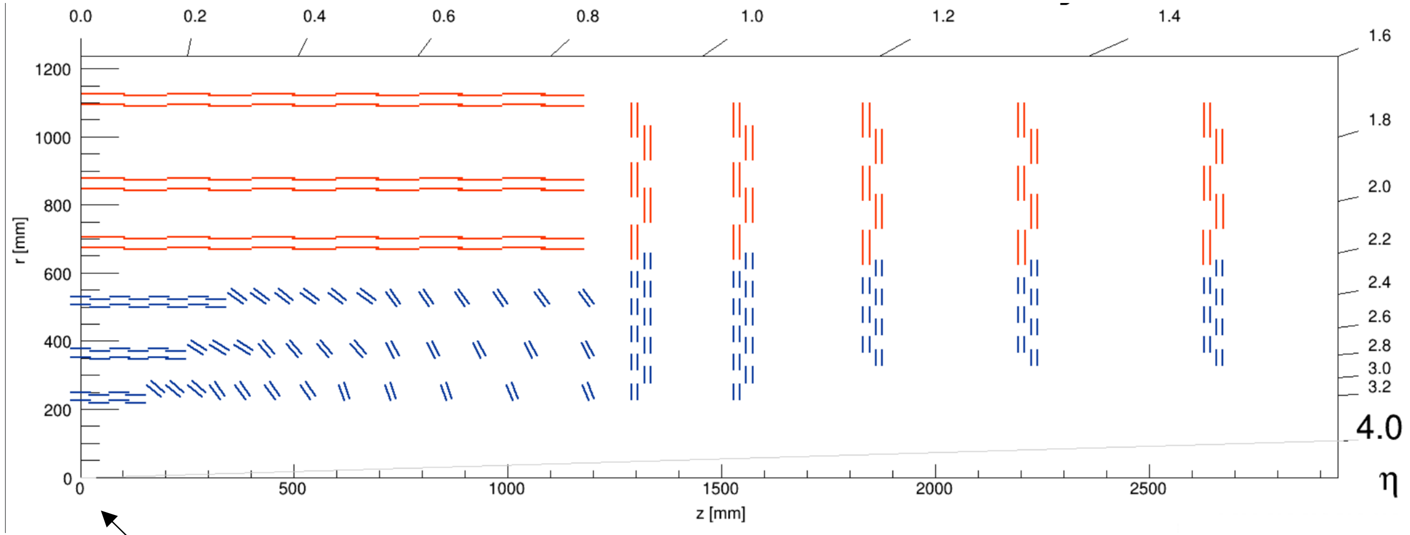
- High-Luminosity LHC (HL-LHC) will increase the number of simultaneous proton-proton collisions
- CMS Trigger Systems select interesting events
  - Level-1 Trigger (L1T) and High Level Trigger (HLT)
- CMS will include particle tracks from the Outer Tracker at the L1 Trigger
  - Mainly used for vertexing
  - Reduces L1 trigger rate from 4000 kHz to 750 kHz
- Track Finder reconstructs particle tracks every bunch crossing (40 MHz)
  - Track p_T > 2 GeV
  - ~200 tracks per event
  - Targeting 4 μs



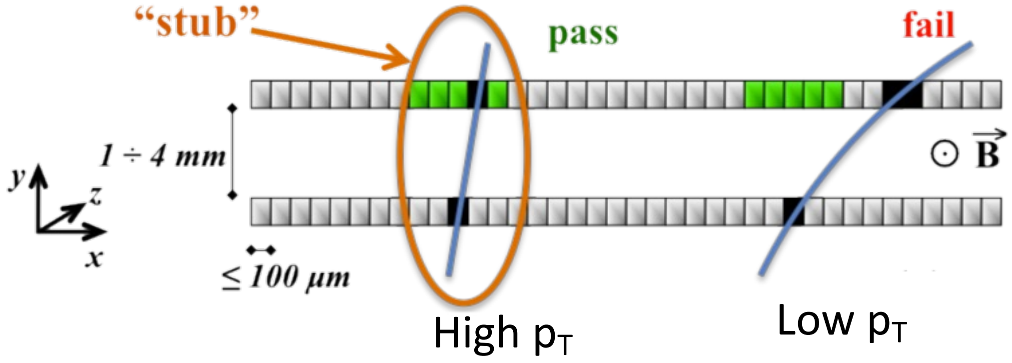
L1 TRACK FINDER

OUTER TRACKER HL-LHC UPGRADE

- L1 tracks uses data from the silicon Outer Tracker only
- New Outer Tracker will consist of 6 barrel layers and 5 disks on each side
- Outer tracker sensor filtering
  - Transmits hits from p_T > 2 GeV charged particles: Stubs
  - Reduces data rate to the Track Finder by a factor ~20



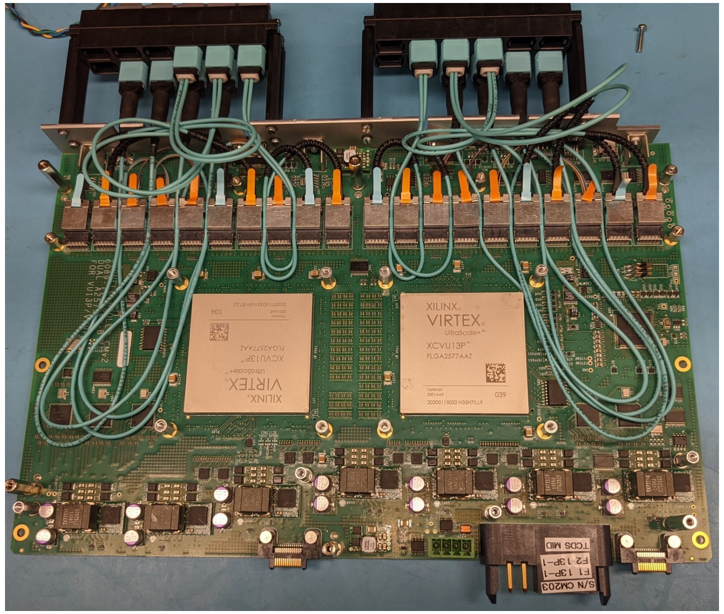
Interaction point

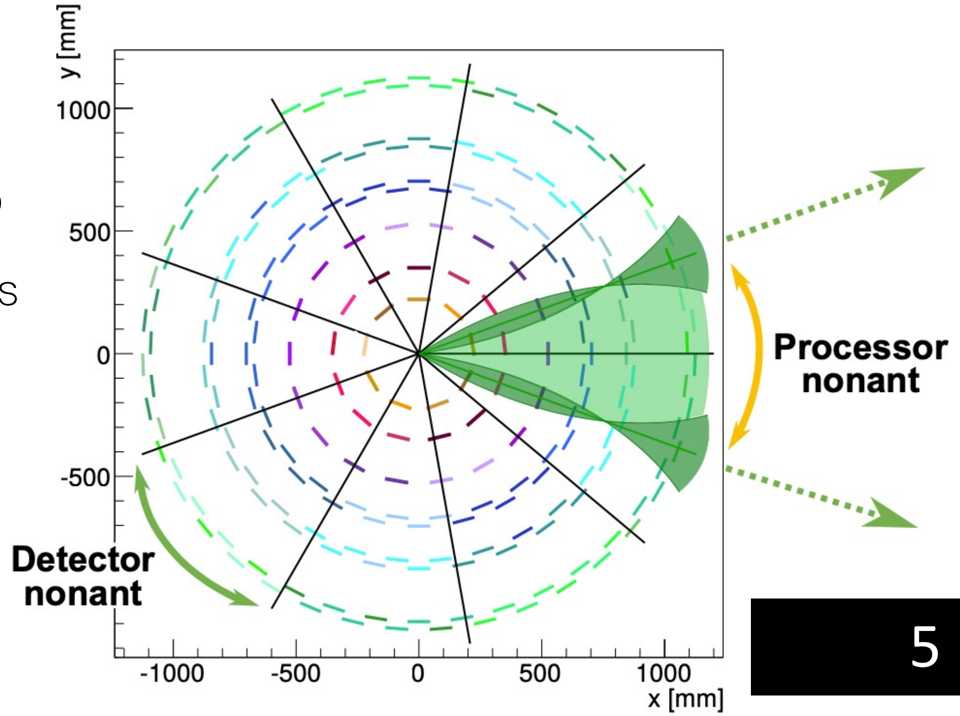


L1 TRACK FINDER

HARDWARE

- Track finding algorithm is being implemented on FPGAs
  - Very fast and programmable integrated circuits
  - Firmware programmed using a hardware description language (HDL) and high-level synthesis (HLS)
  - Two VU13P FPGAs mounted on each Track Finder (TF) board
- The Track Finder is split into 9 equally sized sectors in φ
  - 18 TF boards per sector (nonant), each processing different events
  - Data at the borders is copied to both neighbouring sectors
- No communication between sectors is necessary
  - Processes can run in parallel

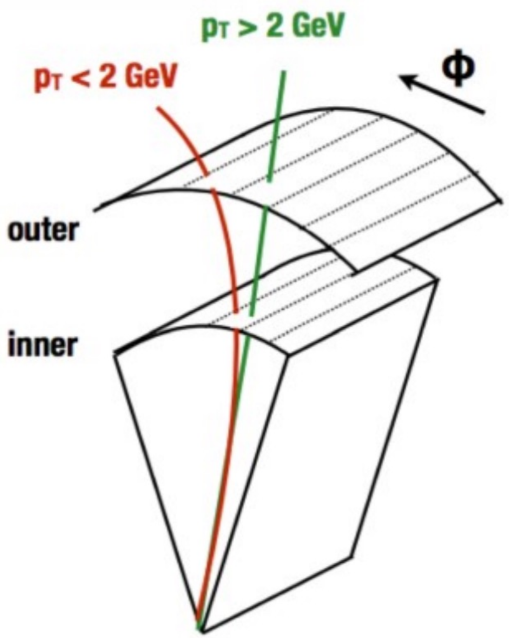


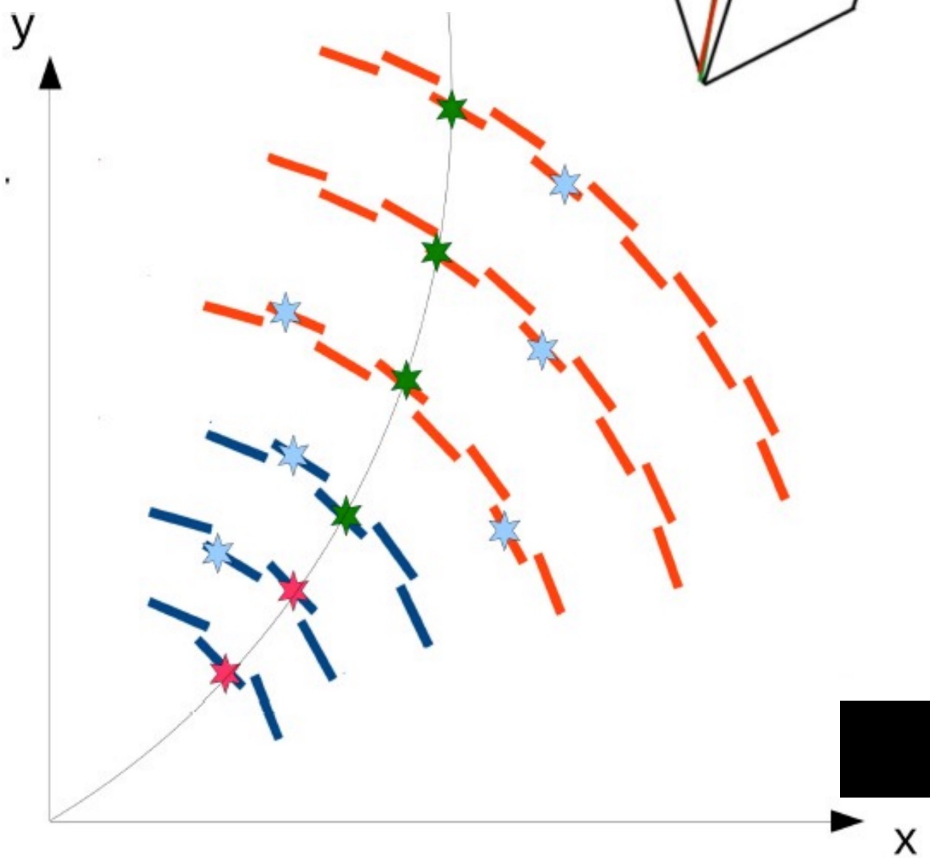


TRACK FINDING ALGORITHM

OVERVIEW

1. Sort stubs into smaller regions in φ
   - Reduces combinatorics in upcoming steps
2. Take two stubs in adjacent layers and estimate track parameters
3. Project potential track to other layers
4. Look for stubs close to the track in the other layers
   - Reject tracks if not enough layers with matching stubs were found
5. Remove duplicate tracks
6. Use stubs and track candidate to calculate final track parameters
   - Using a Kalman Filter

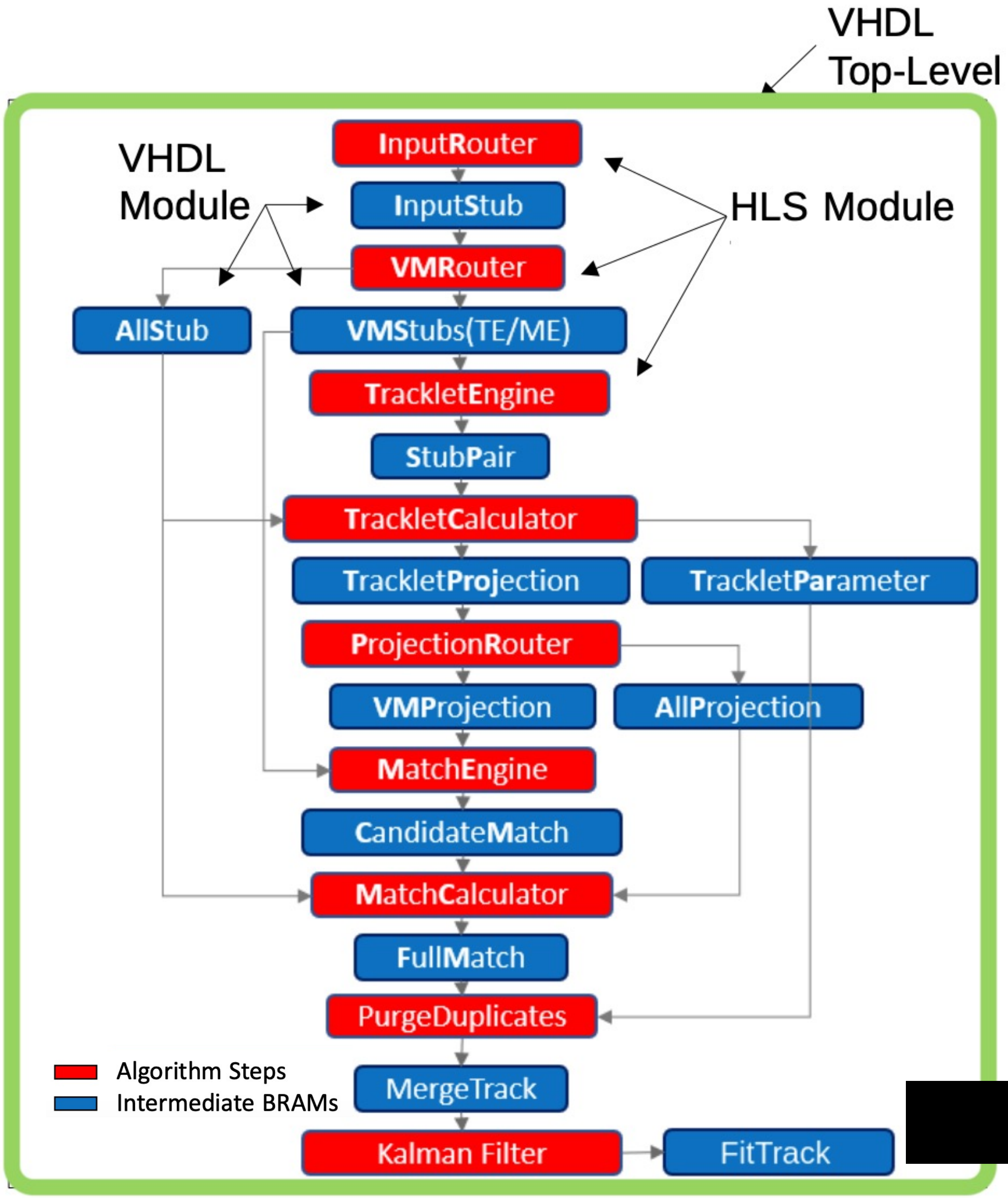




TRACK FINDING ALGORITHM

PROJECT DESIGN

- Algorithm is split up into multiple modules
  - Each processing module is implemented separately using HLS (except Kalman Filter)
  - A module processes one event at a time
- Memories temporarily store the output of each module
  - Implemented in VHDL
- Top-level function connects the whole chain
  - Implemented in VHDL
- 240 MHz FPGA clock

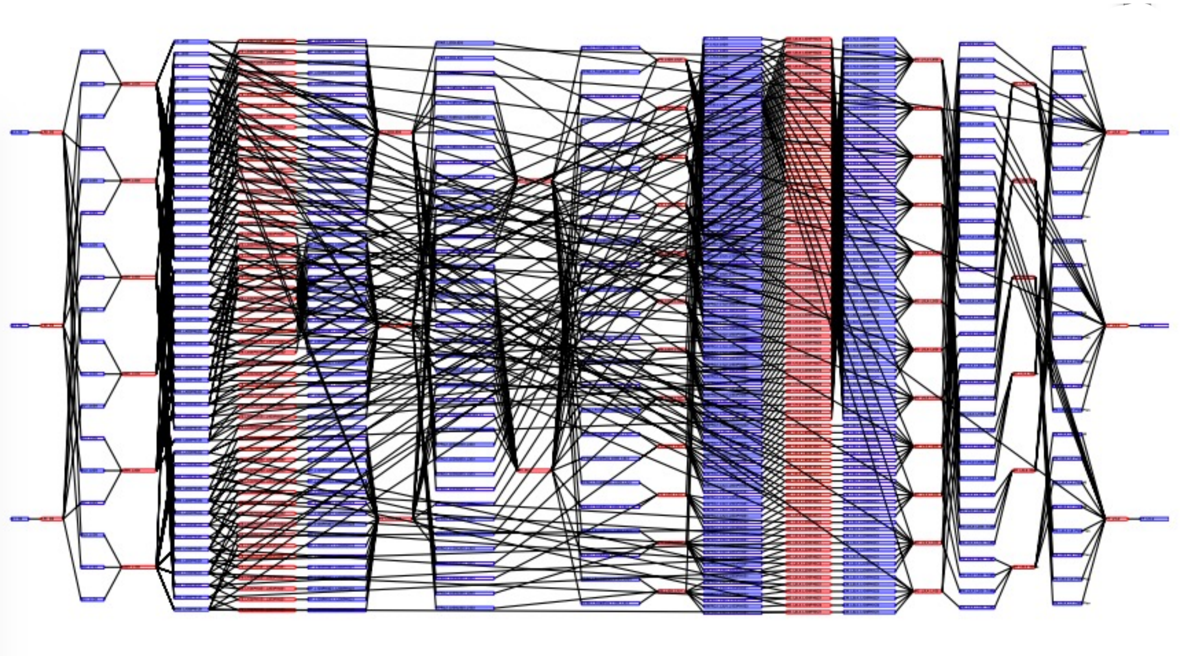


TRACK FINDING ALGORITHM

PROJECT DESIGN

- Multiple versions of each processing module work in parallel
- Scripts create and synthesise the processing modules
- VHDL top-level that connects all the modules is written by a python script

Stubs in



Tracks out

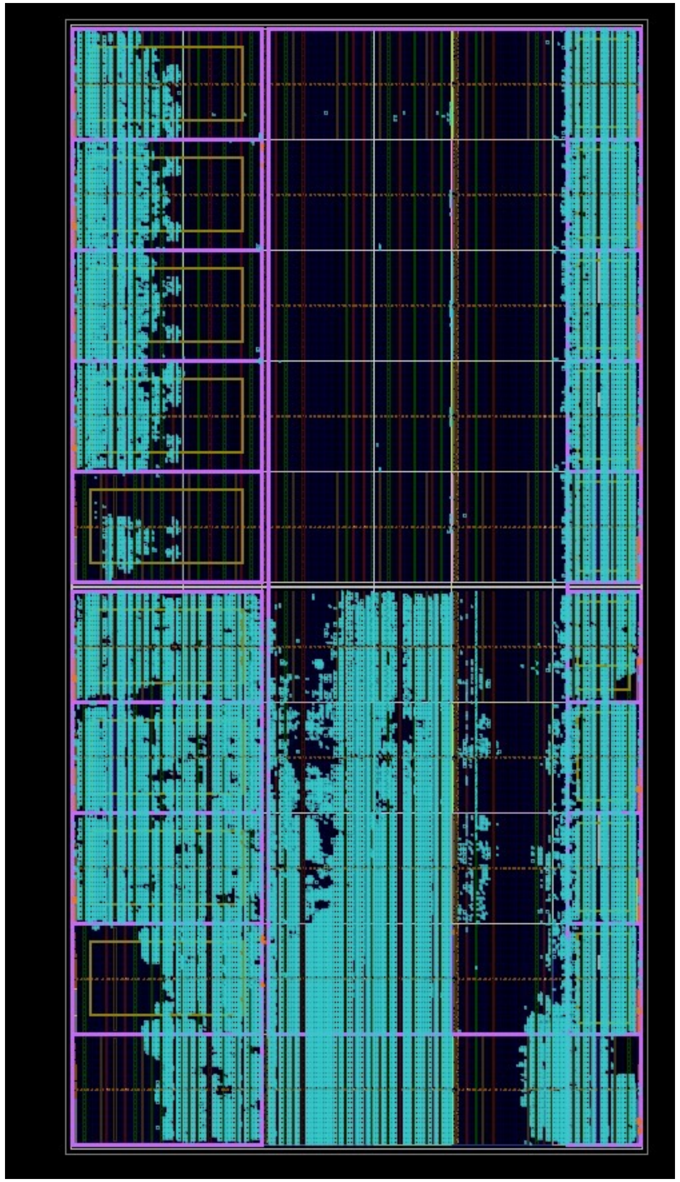
Algorithm Steps
Intermediate BRAMs

ALGORITHM TESTING

SKINNY CHAIN

- Firmware processing modules pass HLS simulations when run separately
  - Does not mean the full chain will work out of the box
- Implemented and tested a small slice of the algorithm
  - ~4% of the full project
  - Did not include the Duplicate Removal modules
- Ran hardware simulations using 1000 events*
  - 98% of events match emulation
  - Debugging in process
- Ran in hardware

*ttbar 200 pileup



Skinny chain
VU7P FPGA Floorplan

ALGORITHM TESTING

BARREL-ONLY CHAIN

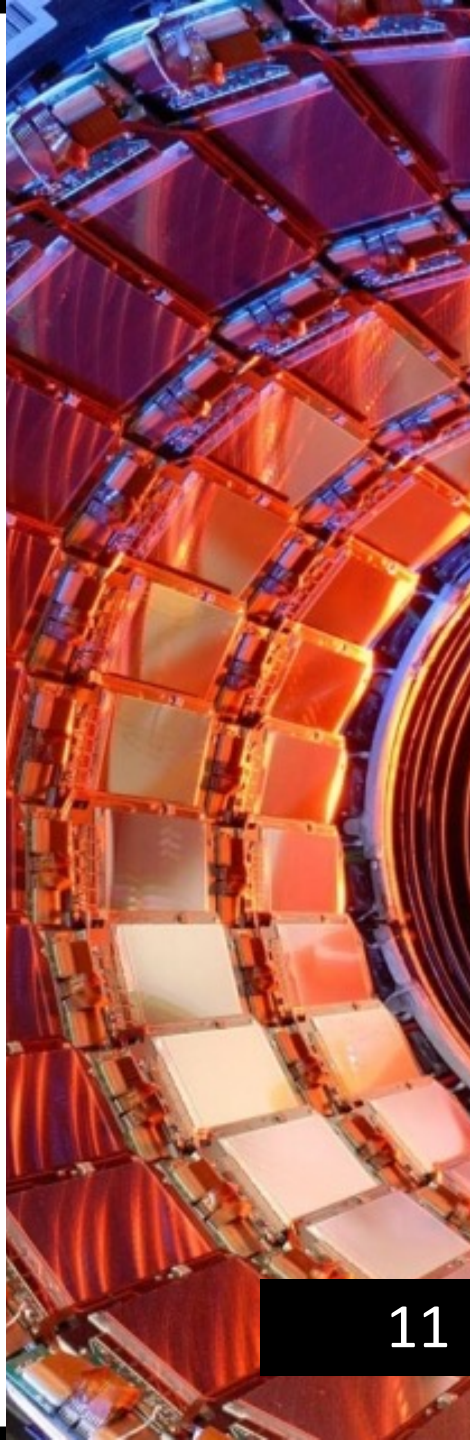
- Implement a chain with all the processing modules for the barrel layers
  - Using a single VU13P FPGA (final project will use two VU13Ps)
  - 2/3 of the full project
  - Does not include the Duplicate Removal modules and the Kalman Filter
- Preliminary resource usage estimation
  - Needs to be optimized
- Good progress towards meeting timing
  - Congestion on the FPGA
- No simulations yet

Preliminary Resource Usage

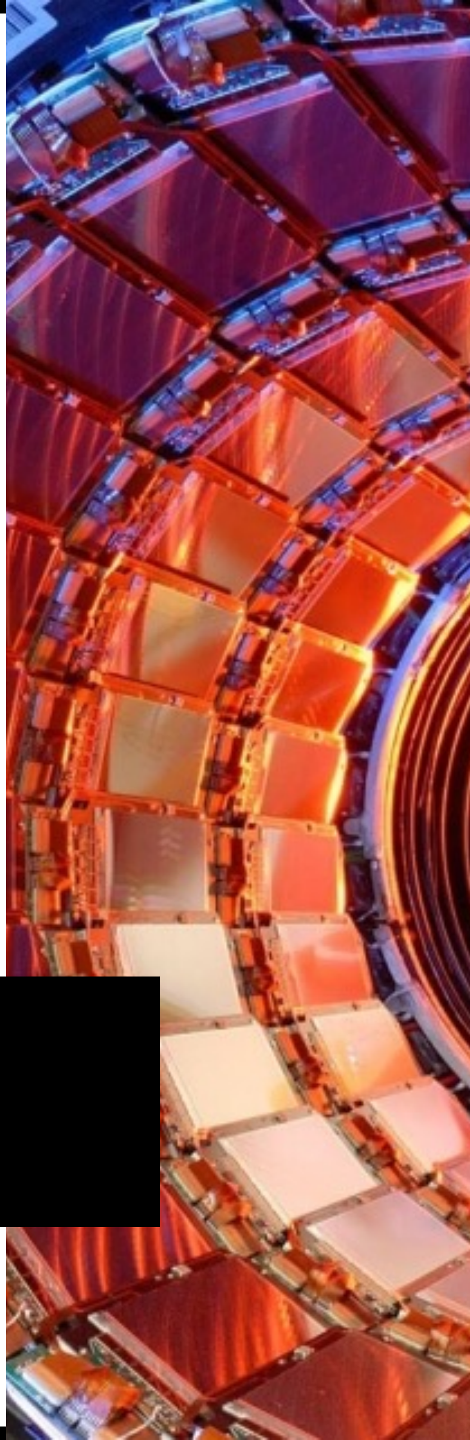
	BRAM_18K	DSP48E	FF	LUT	URAM
Total	2732	1176	1278914	711720	224
Available (VU13P)	5376	12288	3456000	1728000	1280
Utilization (%)	**50.8**	**9.6**	**37.0**	**41.2**	**17.5**

SUMMARY

- L1 Track Finding at CMS is necessary to reduce the L1 trigger rate to an acceptable level
- Algorithm modules have been individually tested
  - Pass simulations
  - Meet timing requirements
- Skinny chain has been successfully run on hardware
  - Debug the few inconsistent outputs
- Barrel-Only chain has been synthesised
  - Optimise resource usage and fix timing issues
- Scale the chain up to the full project in the future



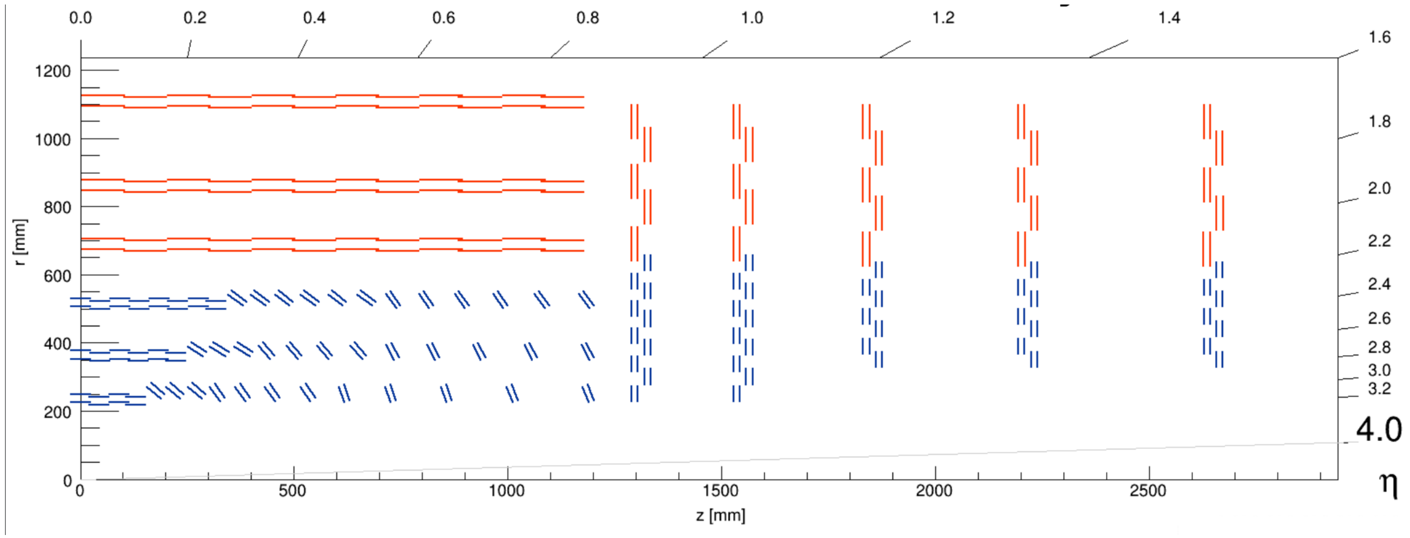
BACKUP SLIDES

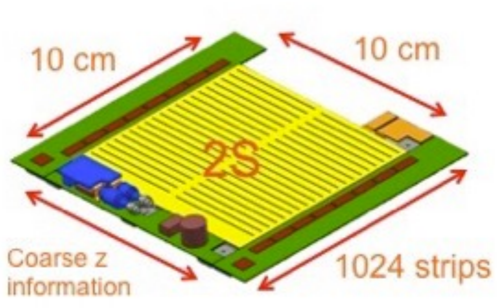


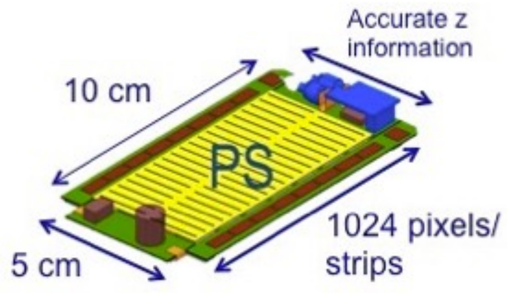
OUTER TRACKER

TWO-STRIP AND PIXEL-STRIP MODULES

- Two types of sensor pair modules are used for the new Outer Tracker
- Two–Strip (2S) modules
  - Accurate information in φ but coarse in z
- Pixel–Strip (PS) modules
  - Accurate information in both φ and z

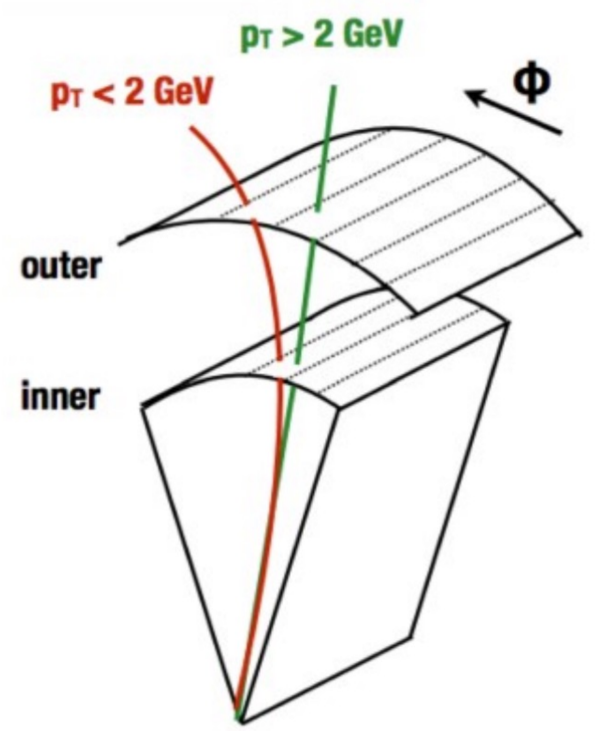




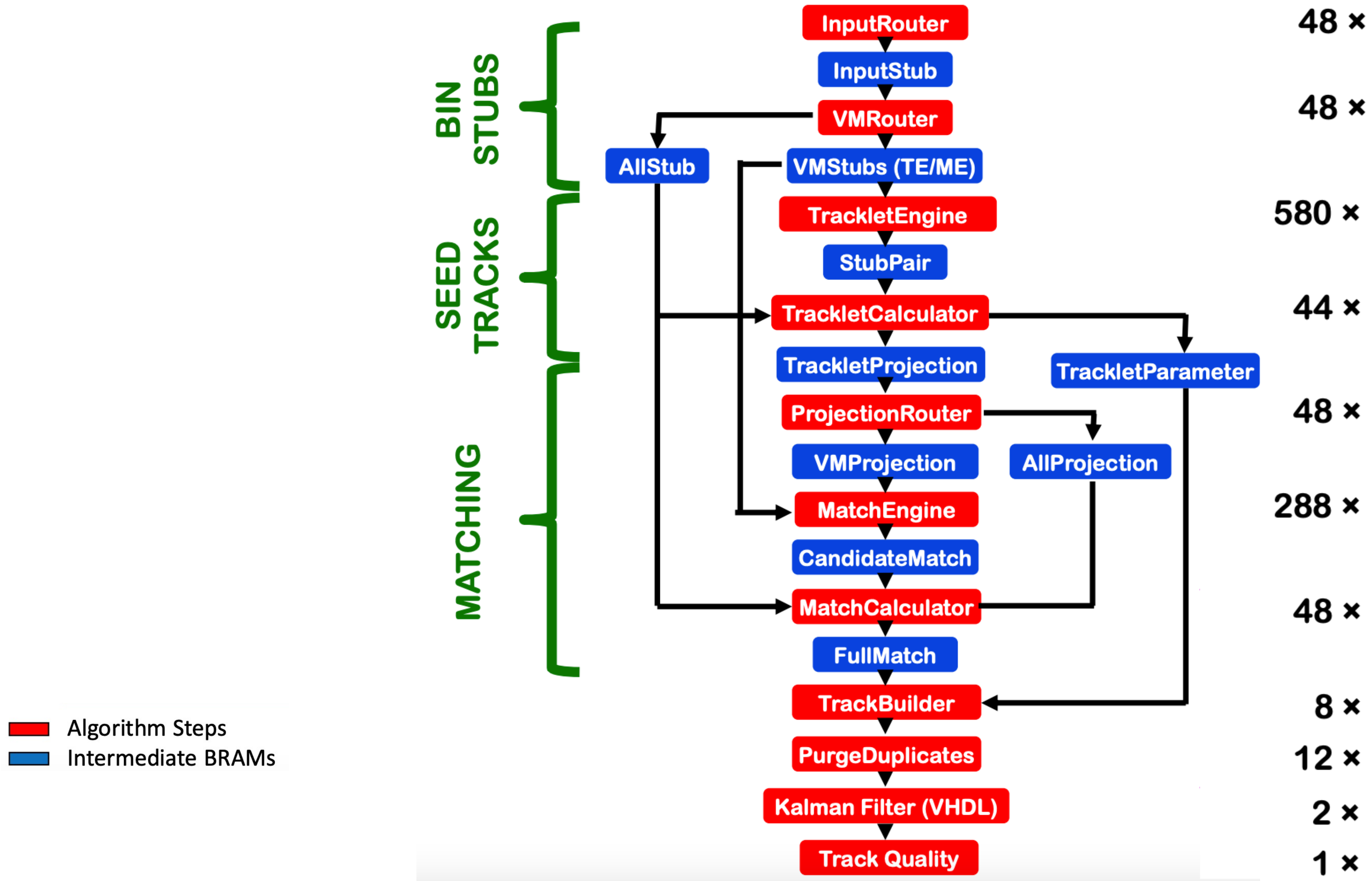


VIRTUAL MODULES

- Taking any two adjacent stubs in the first algorithm step results in large number of combinatorics
  - Inefficient as we are only interested in $p_T > 2$ GeV tracks
- Split each sector layers into slices in φ: Virtual Modules (VMs)
- Stubs in an inner layer VM are only compatible with some outer layer VMs
- In firmware the VMs are implemented as separate memories
  - Avoid having to go through lots of irrelevant stubs
- The VMRouter routes the stubs to the correct VM



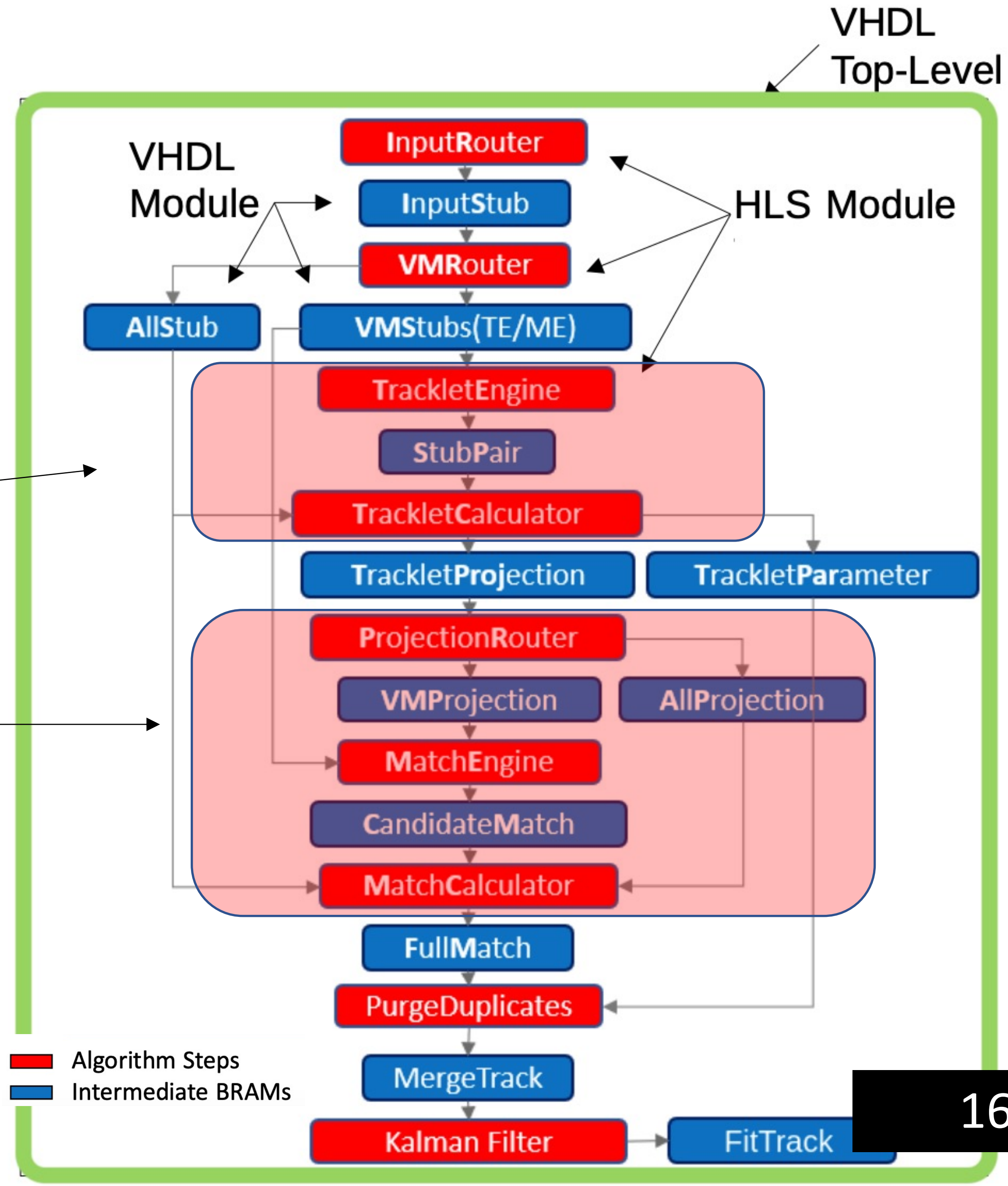
PROJECT DESIGN – NUMBER OF MODULES PER NONANT



TRACK FINDING ALGORITHM

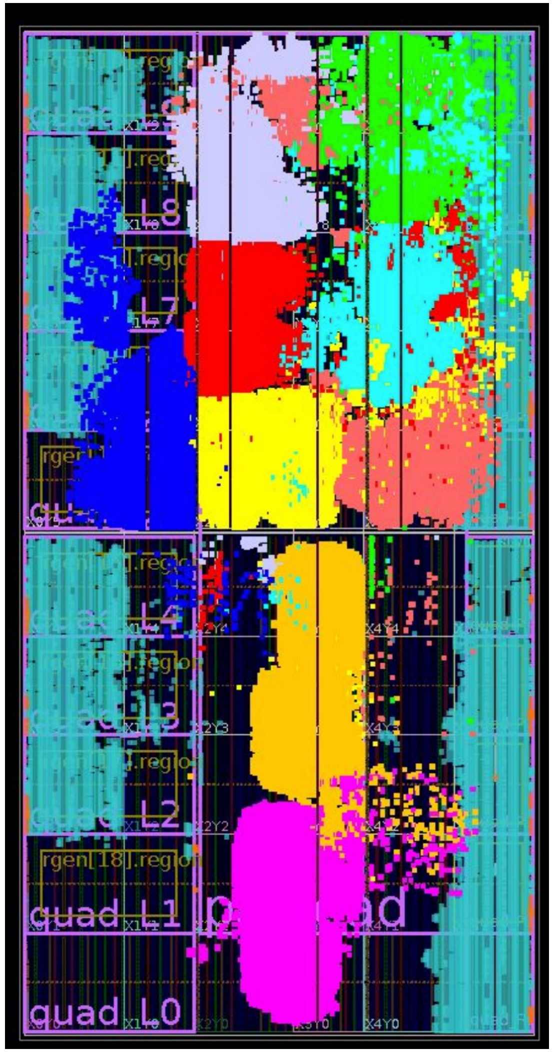
COMBINED MODULES

- Some modules can be combined to save time
  - Can also save resources as it reduces the number of intermediate memories
- Tracklet Processor
  - Tracklet Engine, Tracklet Calculator
- Match Processor
  - Projection Router, Match Engine, Match Calculator
- The track finding algorithm is moving towards using the combined modules
  - Combined modules implemented for barrel layers
  - A small combined module chain has been simulated but fails timing

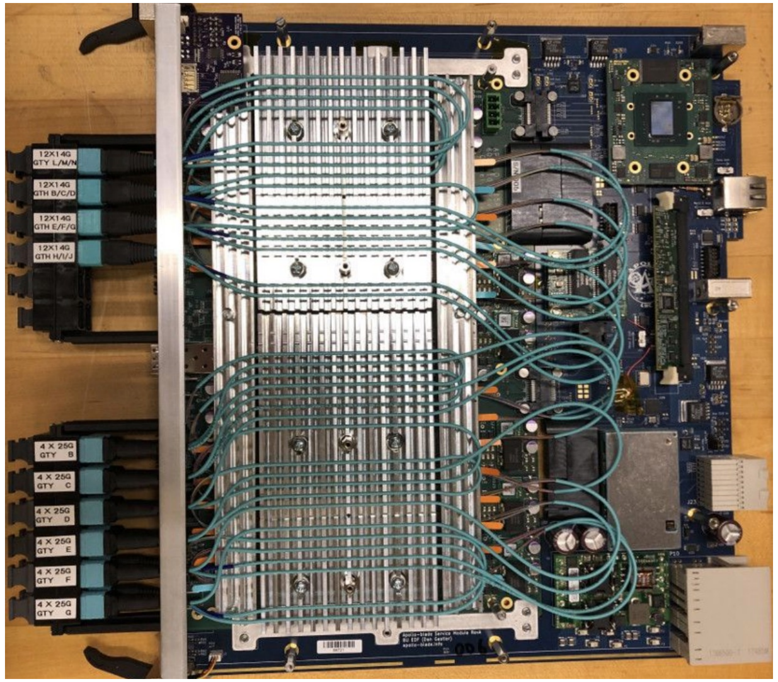


COMMISSIONING & TESTING

- Tested skinny chain on hardware
  - Successfully…
  - Some inconsistencies in output
- Tested communication between L1 subsystems
  - TF Board and Vertexing Board
  - Only the last step of TF algorithm (Kalman Filter Out)
  - High speed fibre optics



9 Kalman Filter Out
VU7P FPGA Floorplan



Track Finder Board