

Performance evaluation of newly developed front-end ASIC for Belle II Silicon Vertex Detector upgrade

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on behalf of the Belle II TFP-SVD project

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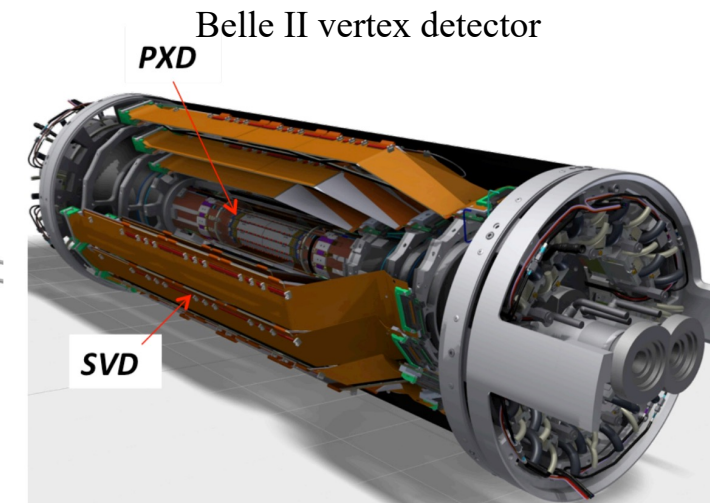
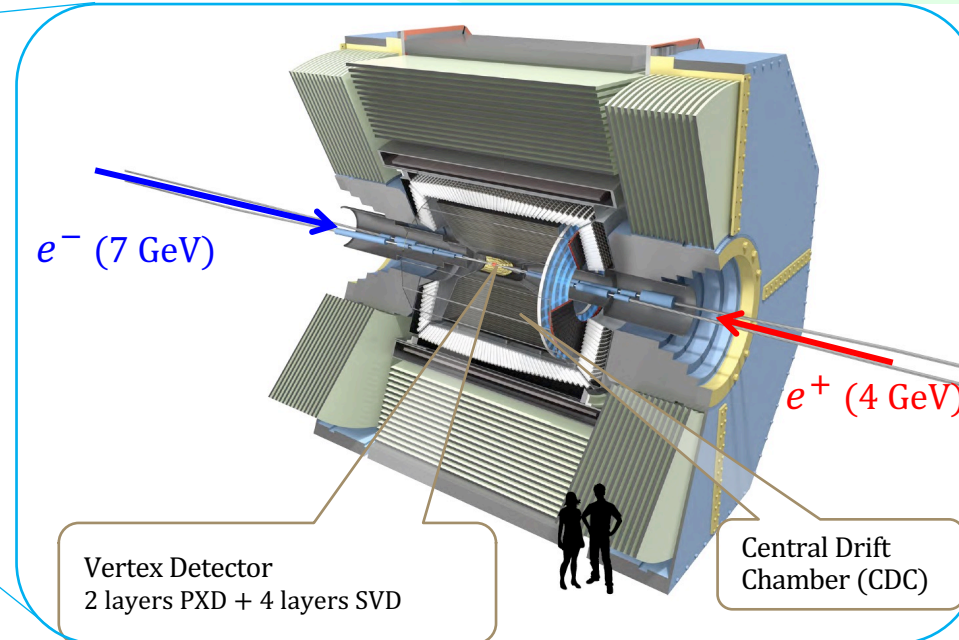
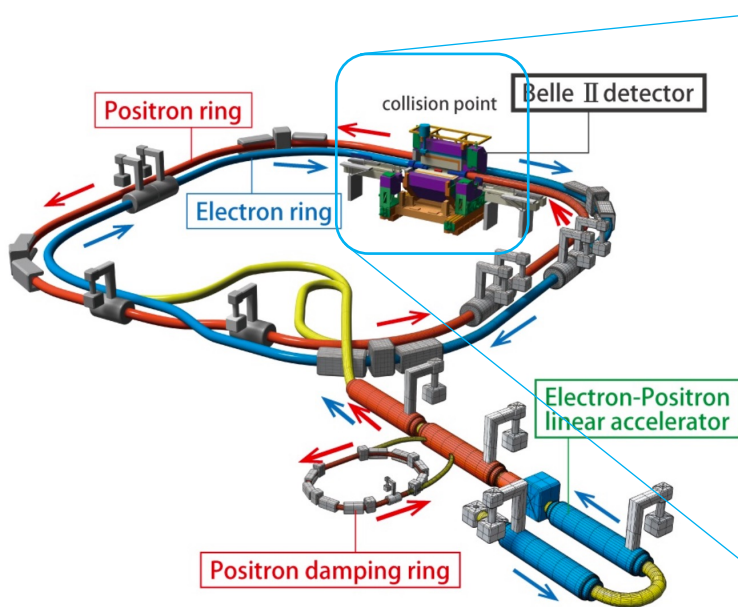
Introduction

See talk in the morning by [A. Bolz](#) and [K. Kang](#) for the current PXD and SVD!
See previous talk "[The vertex detector upgrade of the Belle II experiment](#)" by Tsuboyama-san for the general status of VXD upgrade!

- SuperKEKB
 - e^+e^- collider
 - Target luminosity: $6 \times 10^{35} \text{ cm}^{-2} \text{ s}^{-1}$
 - $0.47 \times 10^{35} \text{ cm}^{-2} \text{ s}^{-1}$ achieved in 2022 run
- Belle II vertex detector:
 - PXD: inner 2-layer Silicon pixel detector
 - SVD: outer 4-layer Silicon strip detector

Thin Fine-pitch SVD (TFP-SVD) project

- Upgrade of the SVD
 - Improve momentum resolution for low momentum tracks due to smaller material budget
- Replace inner layers of the gas drift chamber (CDC) with silicon detector
 - Improve background tolerance

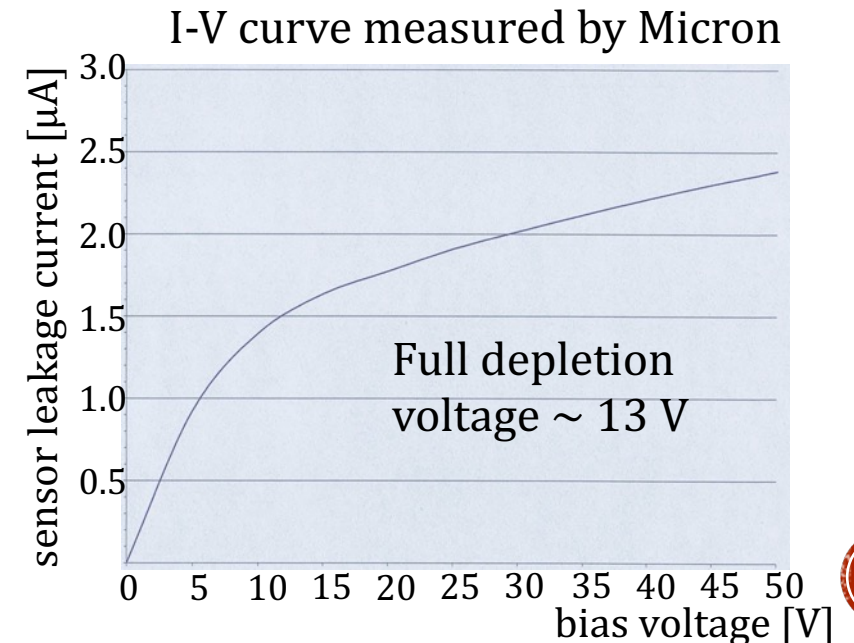
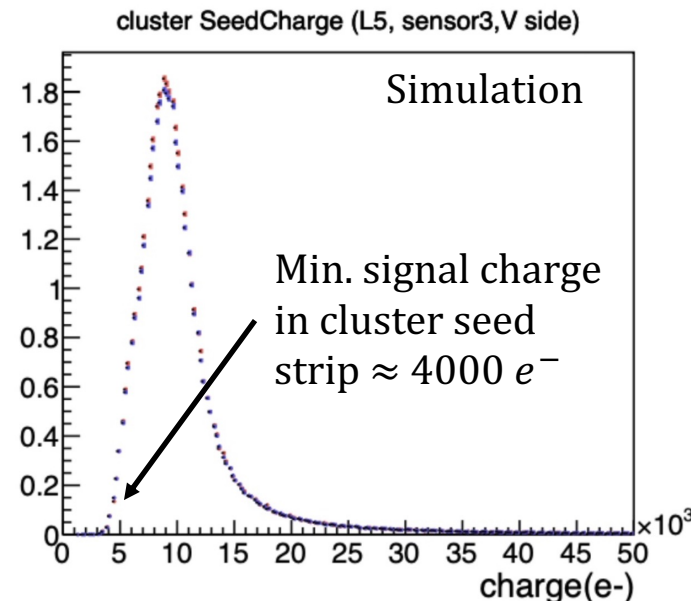
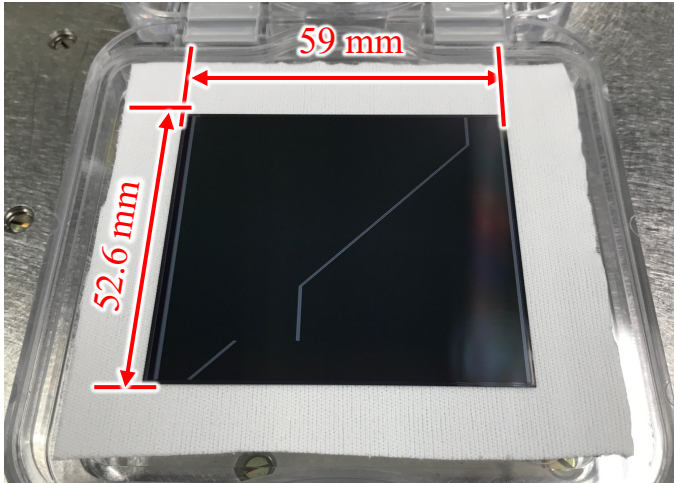


Prototype sensor: TFP-DSSD

- Double-sided Silicon Strip Detector (DSSD) sensor
 - Manufactured by Micron Semiconductor (UK)
- Target sensor size: 96 mm × 109 mm
 - Expect $C_{det} \approx 14 \sim 16$ pF
- **Lower thickness and Finer pitch**
 - Smaller material budget
 - Better position resolution
- Smaller signal charge requires low-noise readout ASIC

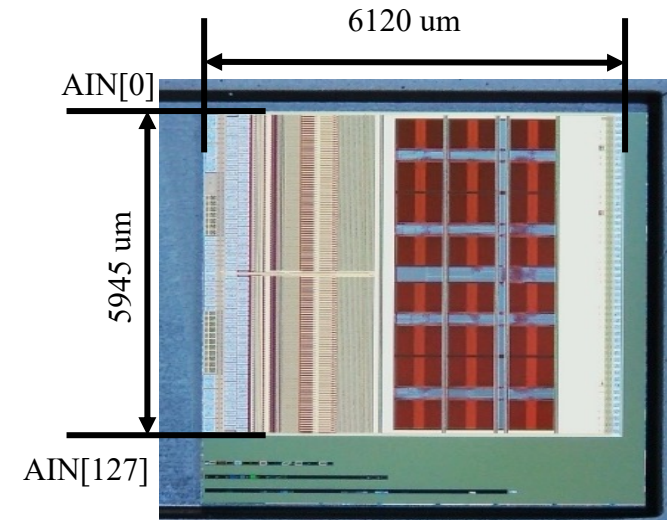
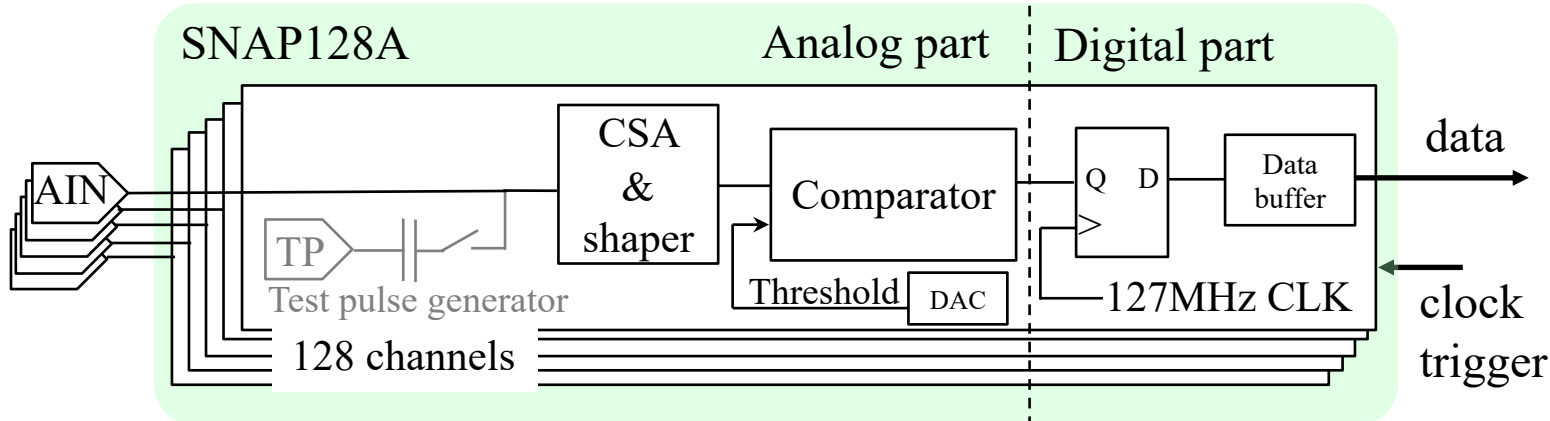
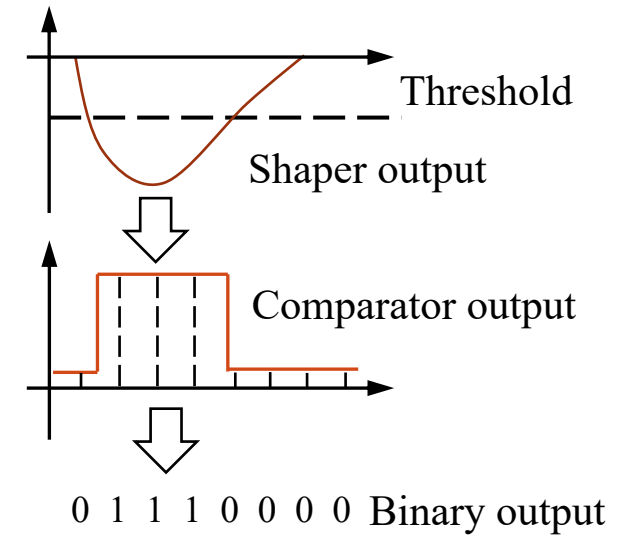
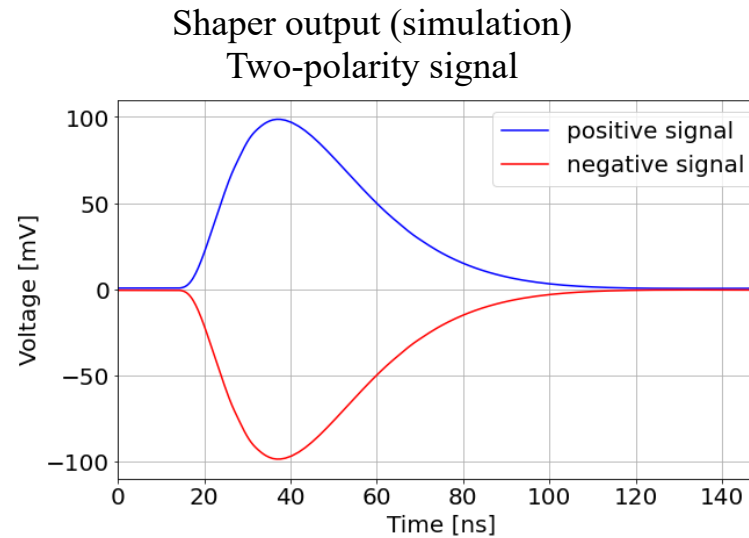
	Thickness	Readout strip pitch (P/N side)
Current DSSD (Large Rectangular)	320 μm	75/240 μm
TFP-DSSD (target)	140 μm	75/85 μm

Prototype DSSD sensor



Front-end ASIC: SNAP128A

- Designed by E-sys group in KEK
 - 180 nm CMOS technology by Silterra
- 128 input channels/chip
- Capability of processing both positive and negative signals
- Binary hit information readout
- 127MHz sampling frequency
- Power consumption: 330 mW/chip



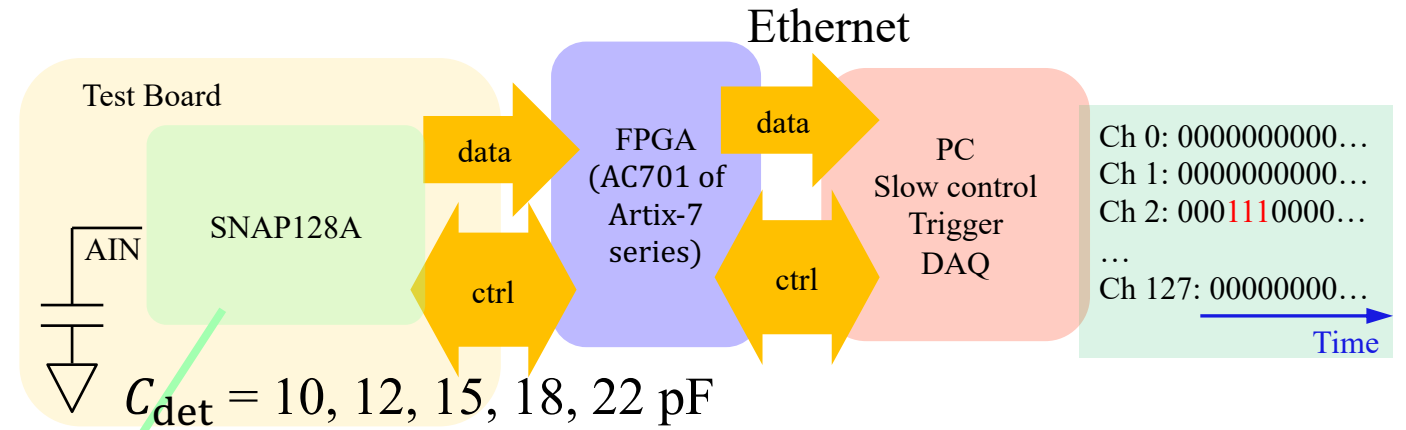
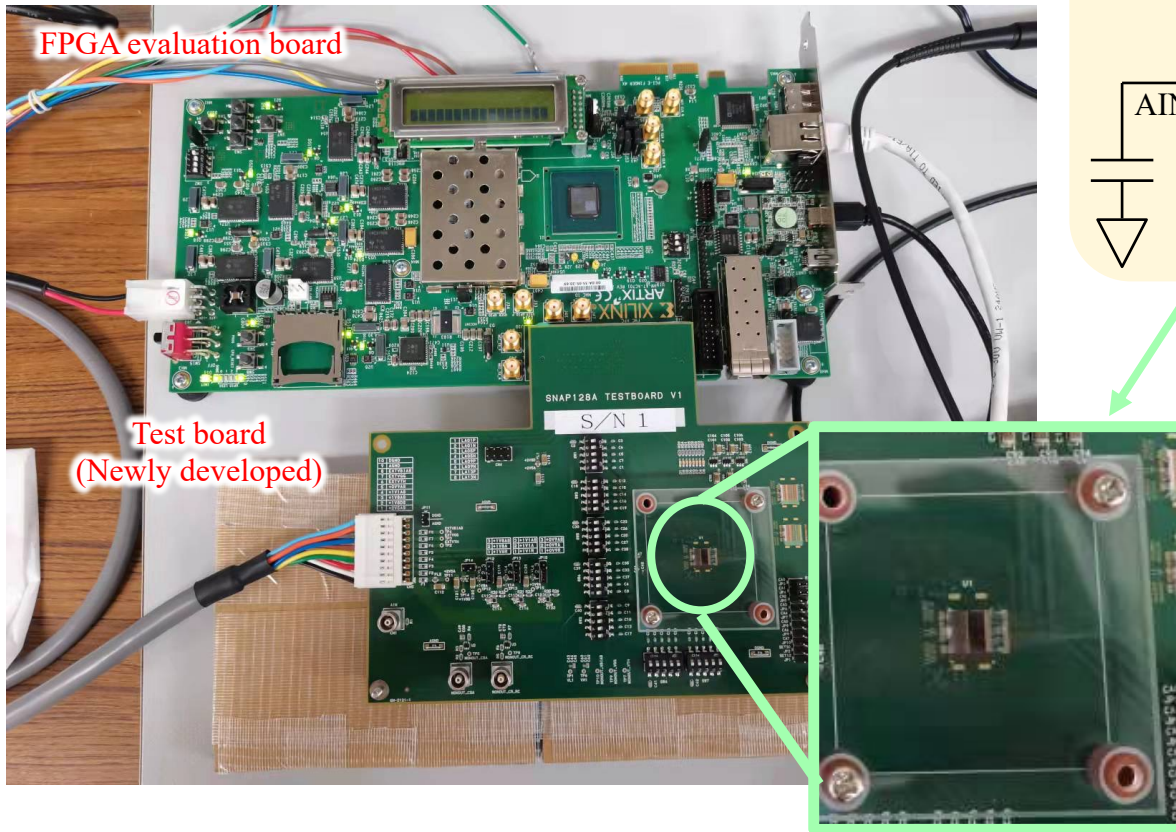
Prototype front-end ASIC
(SNAP128A)

SNAP128A evaluation: check points

1. **Pulse width of shaper output < 100 ns**
 - Required by the suppression signal pile-up rate to 5% @ 10 MHz/cm² hit-rate (SVD inner most layer)
2. **Noise $< 800 e^-$**
 - To apply a cut threshold $> 5 \times$ noise, with min. signal charge on cluster seed strip being 4000 e^-
3. **Verify above properties for both positive and negative signals**

SNAP128A evaluation system

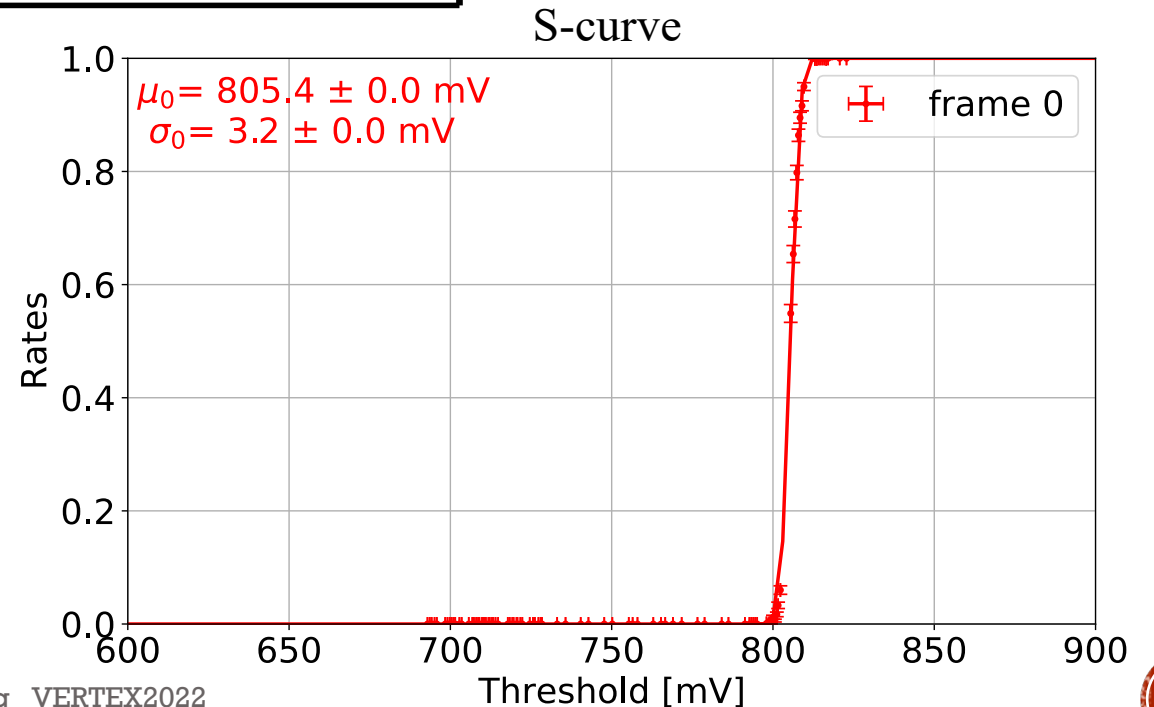
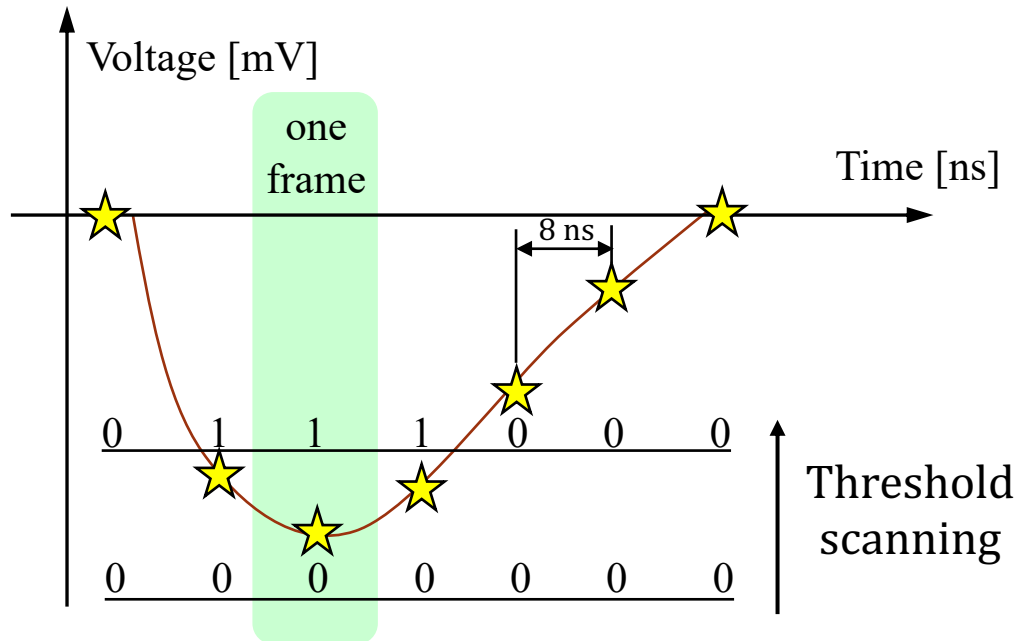
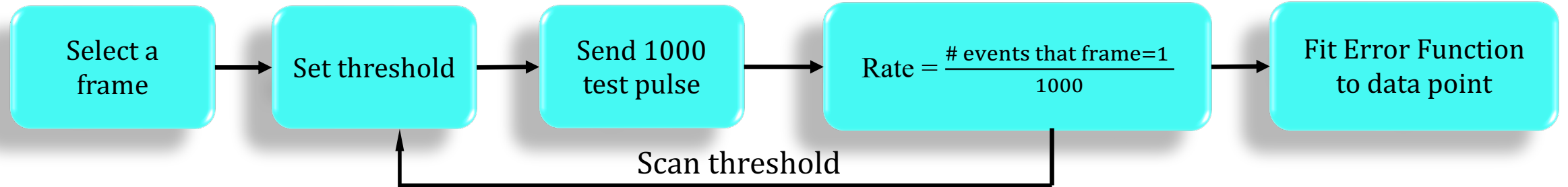
- Evaluation system developed



- Reconstruct waveform using binary hit information
 - Necessary for pulse width, noise measurement
- Chip response at different detector capacitance

Waveform reconstruction using binary data (1)

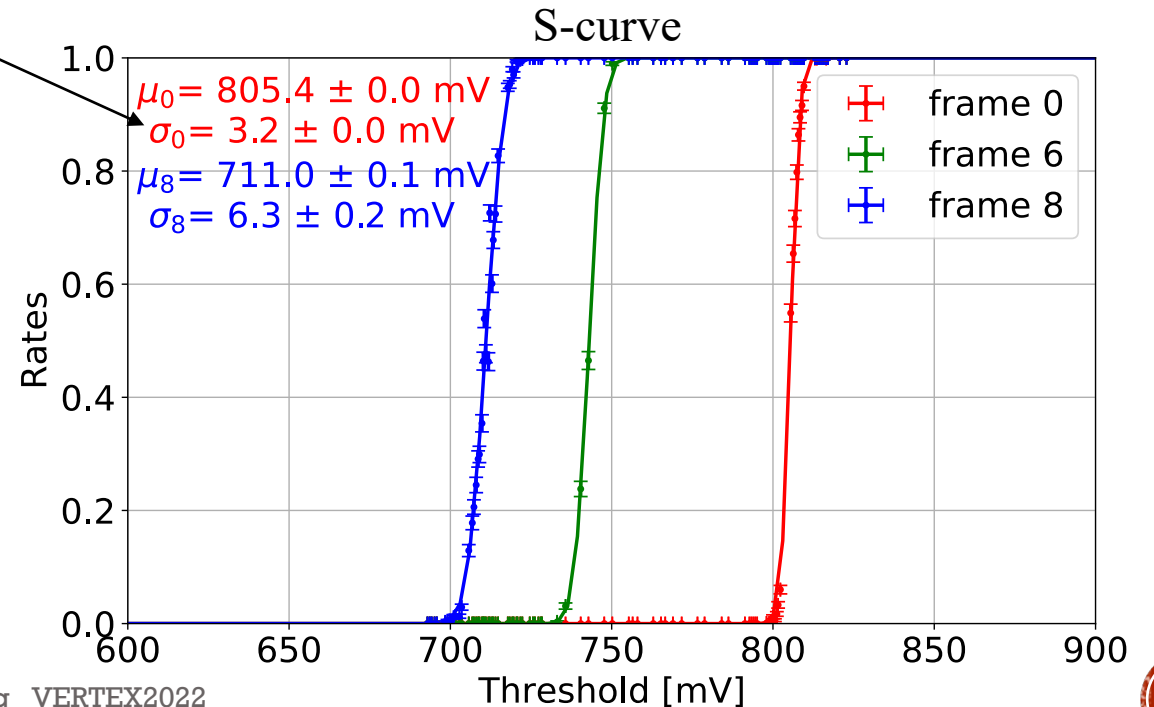
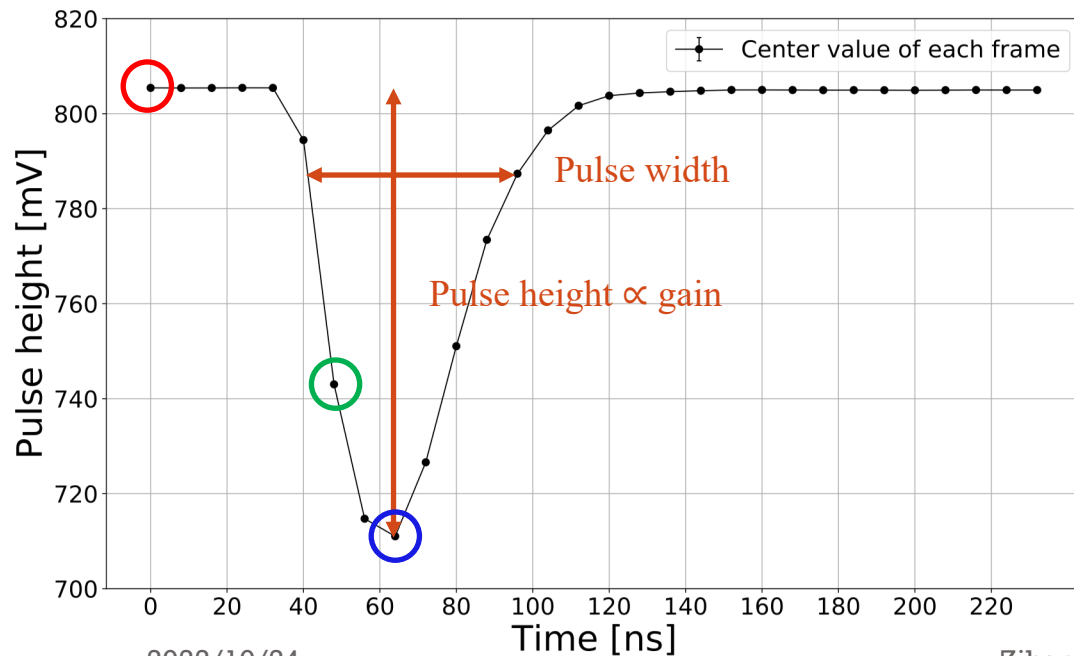
- Waveform reconstructed by measuring the pulse height at each frame
- Average voltage and standard deviation of each frame measured by the S-curve method



Waveform reconstruction using binary data (2)

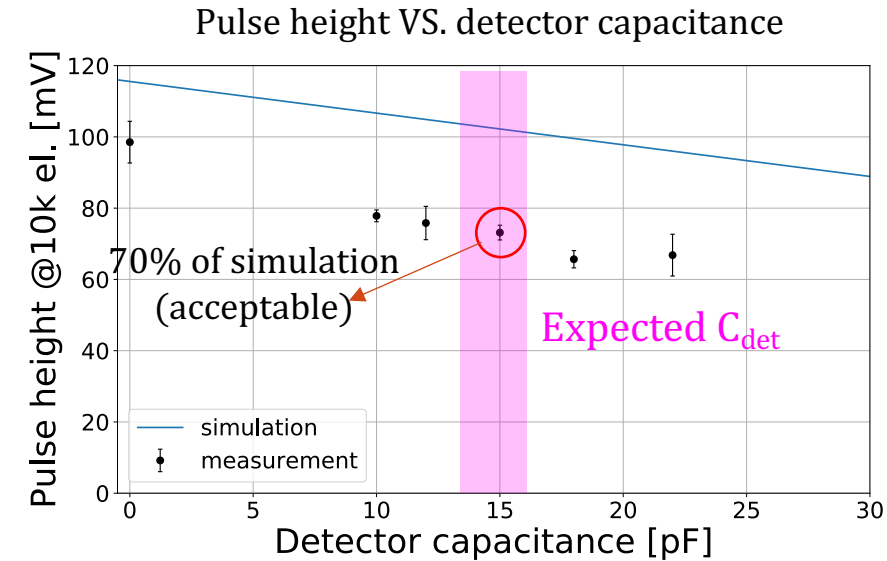
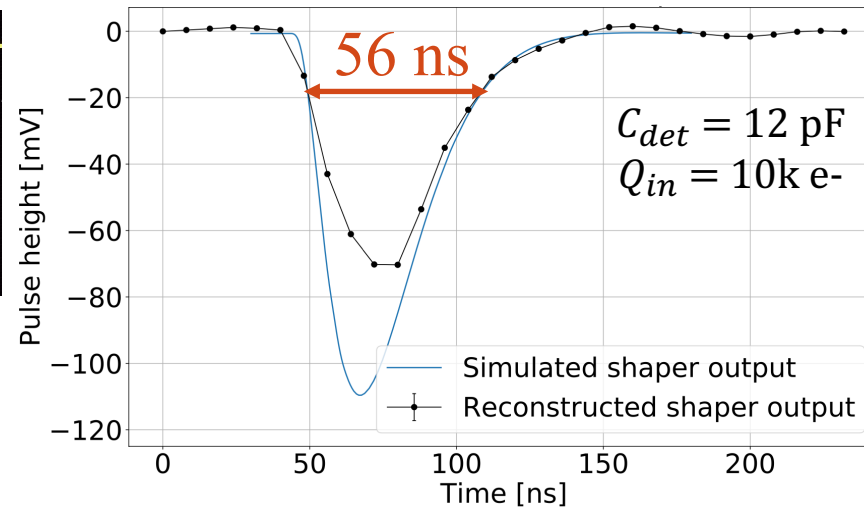
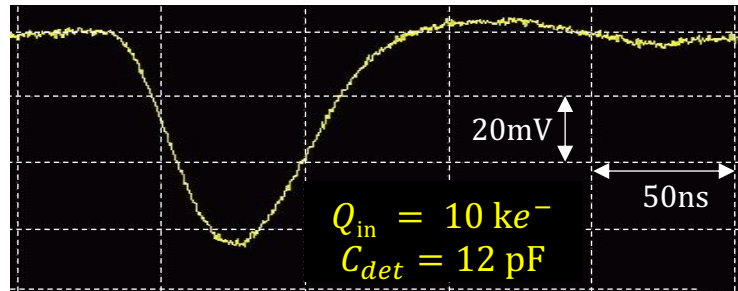
Measurement items

- Pulse width = time range @ $\frac{1}{4}$ pulse height
- Gain = pulse height / input charge
- Noise [e^-] = σ_0/Gain



Negative signal waveform

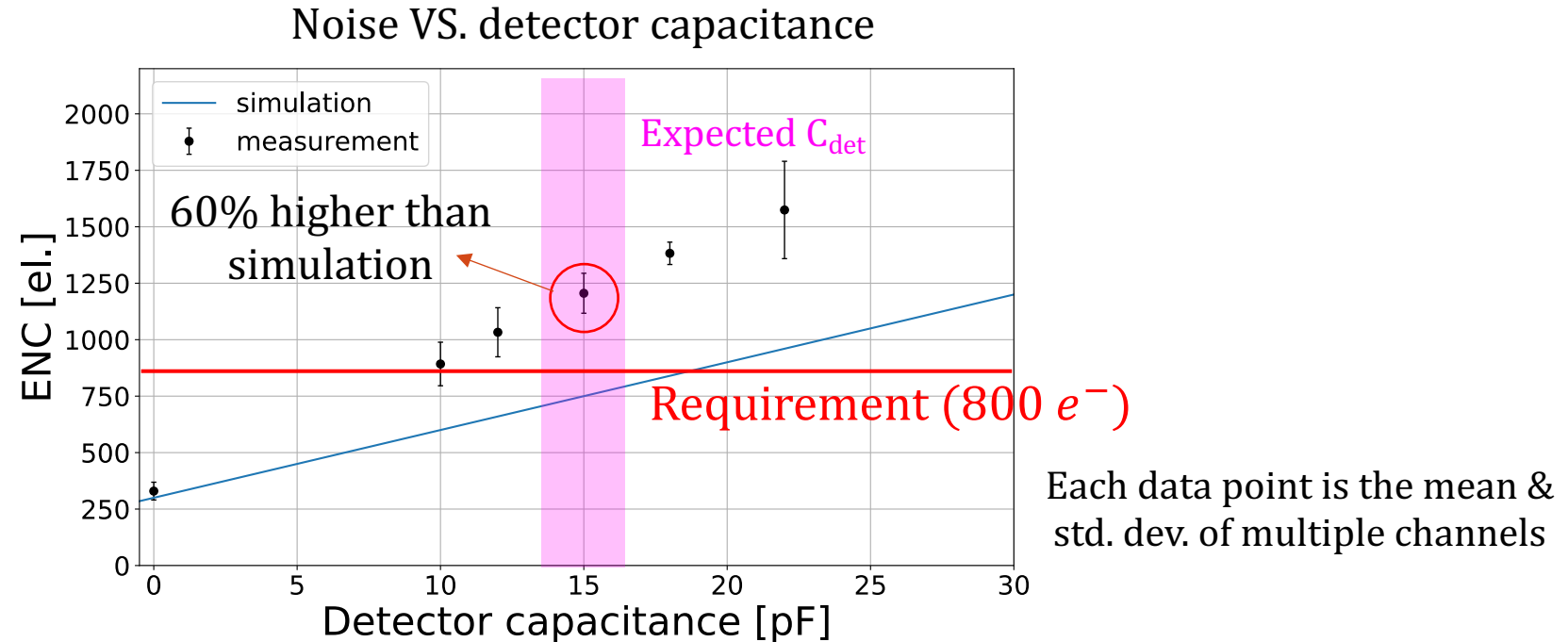
Shaper output @ oscilloscope



Each data point is the mean & std. dev. of multiple channels

- Reconstructed waveform is consistent with oscilloscope observation and similar to simulation
- Pulse width $\sim 56 \text{ ns}$, meets our requirement ($<100 \text{ ns}$)
- Pulse height is about 70% of simulation but acceptable

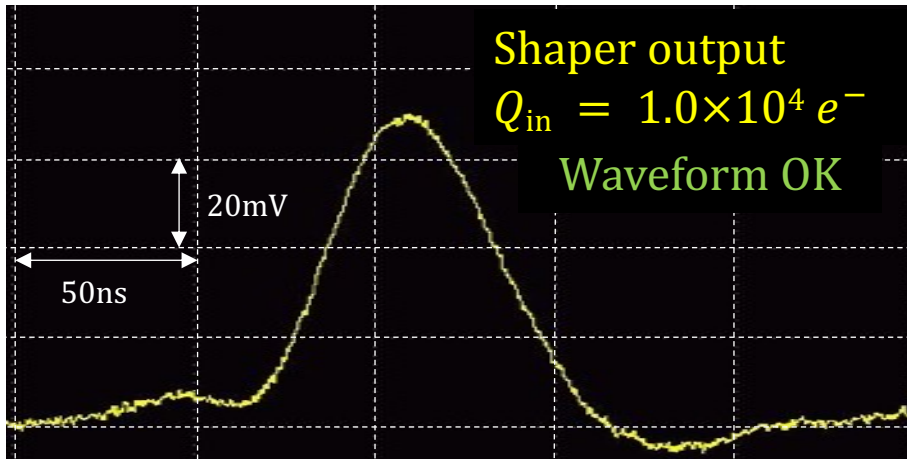
Noise measurement for negative signal



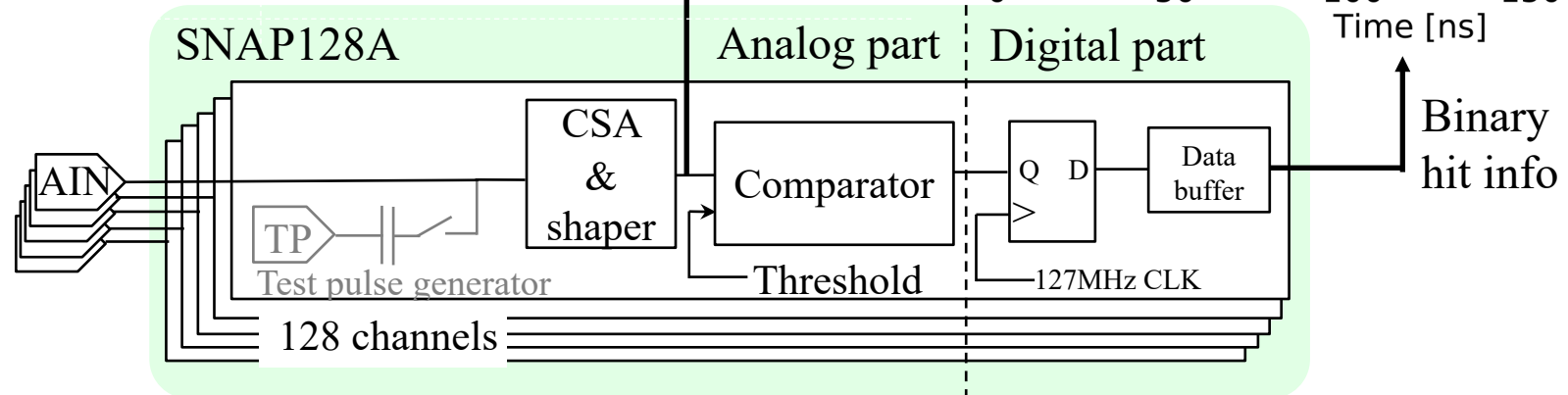
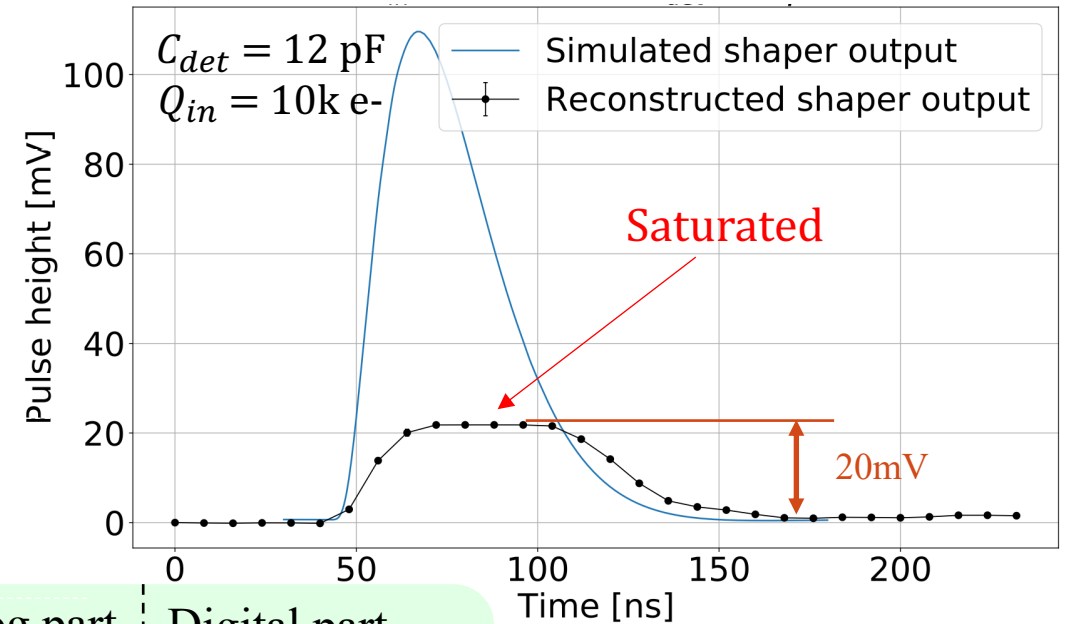
- 85 channels of one chip measured
- Possible sources of inconsistency between data and simulation:
 - Parasitic capacitance ($\sim 3\text{pF}$) on the test board layout
 - Possible noise on DAC reference voltage

Reconstruction of positive signal

Before comparator



After comparator



- Saturation in Comparator
 - Smaller working range for positive signal is confirmed in simulation

Prospects of SNAP64B

- To improve the performance, next prototype SNAP64B is under development
 - Manufacturer changed to TSMC

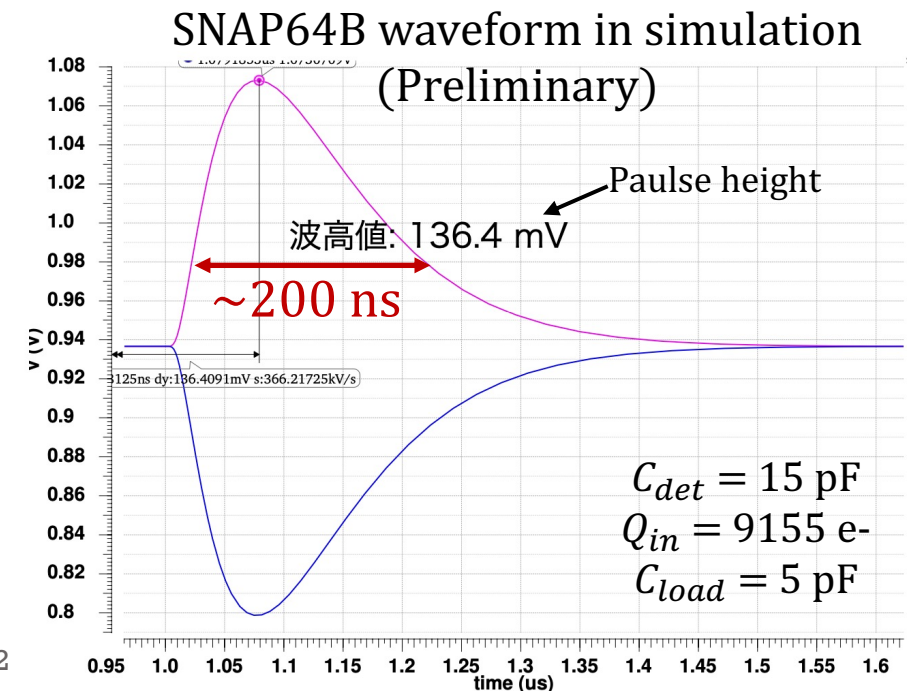
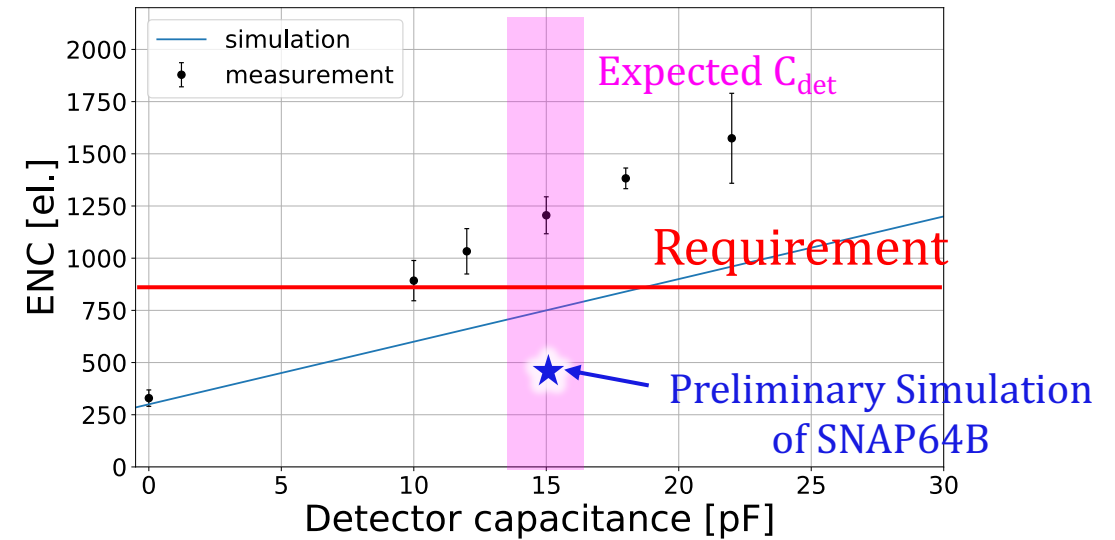
Noise

- Relaxing shaping time to improve the noise level
- Use low noise supply for DAC reference voltage

Positive signal saturation

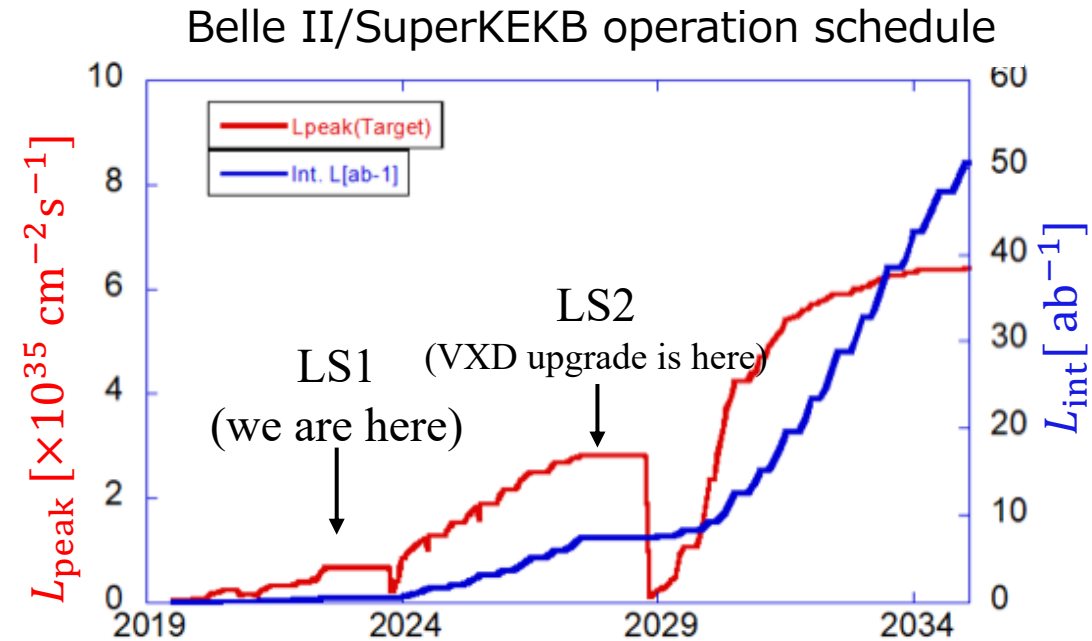
- Expand dynamic working range of the comparator (under development)

Next prototype will be submitted in this December!



Summary

- Achievements so far
 - Evaluation system works
 - Negative signal performance evaluated
 - Pulse width meets requirement
- Next version of SNAP will be submitted in this December
 - Noise level to be improved by enlarging pulse width
 - Saturation can be avoided by expanding working range of the comparator
- Aiming the installation of TFP-SVD during long shutdown 2 of SuperKEKB



BACK UP

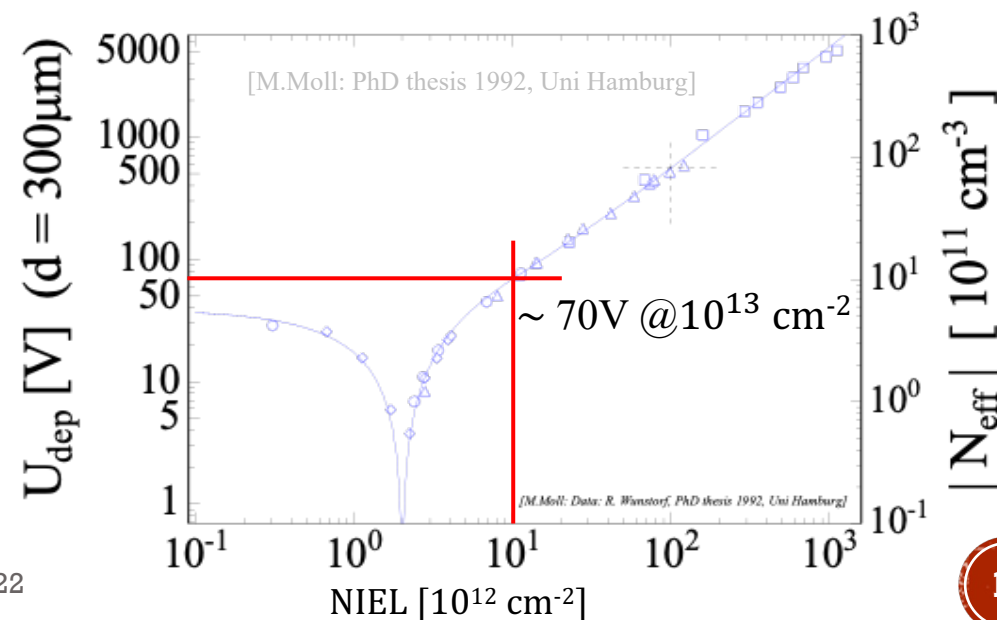
Belle II vertex detector upgrade project

SVD Beam background status @ target luminosity

- Motivation of vertex detector upgrade
 - **Better vertex & momentum resolution**
 - Especially for K_S & low momentum tracks
 - **Higher beam background tolerance**
 - Eating up safety factors according to simulation
 - Increasing depletion voltage due to NIEL
 - **Higher hit rate tolerance**
 - Avoid possible signal pile-up at target luminosity
- Thin/fine-pitch SVD (TFP-SVD) project is an upgrade plan of SVD (Silicon strip detector)

	Expected at target luminosity*	Limits	Safety factor
Layer-3 occupancy	$\sim 3\%$	$\sim 3\%$	~ 1
NIEL	$7 \times 10^{12} \text{ cm}^{-2}$	$\sim 10^{13} \text{ cm}^{-2}$	~ 1

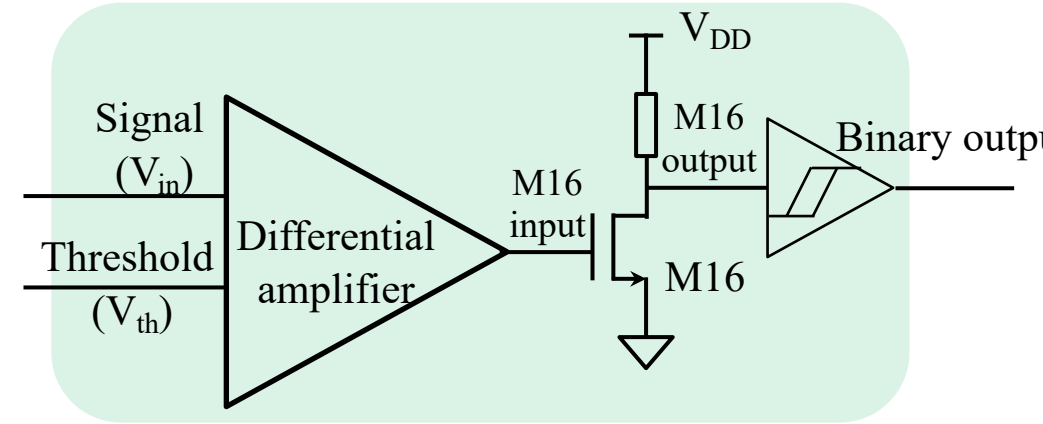
*: Large uncertainty due to injection background and collimator setting difference



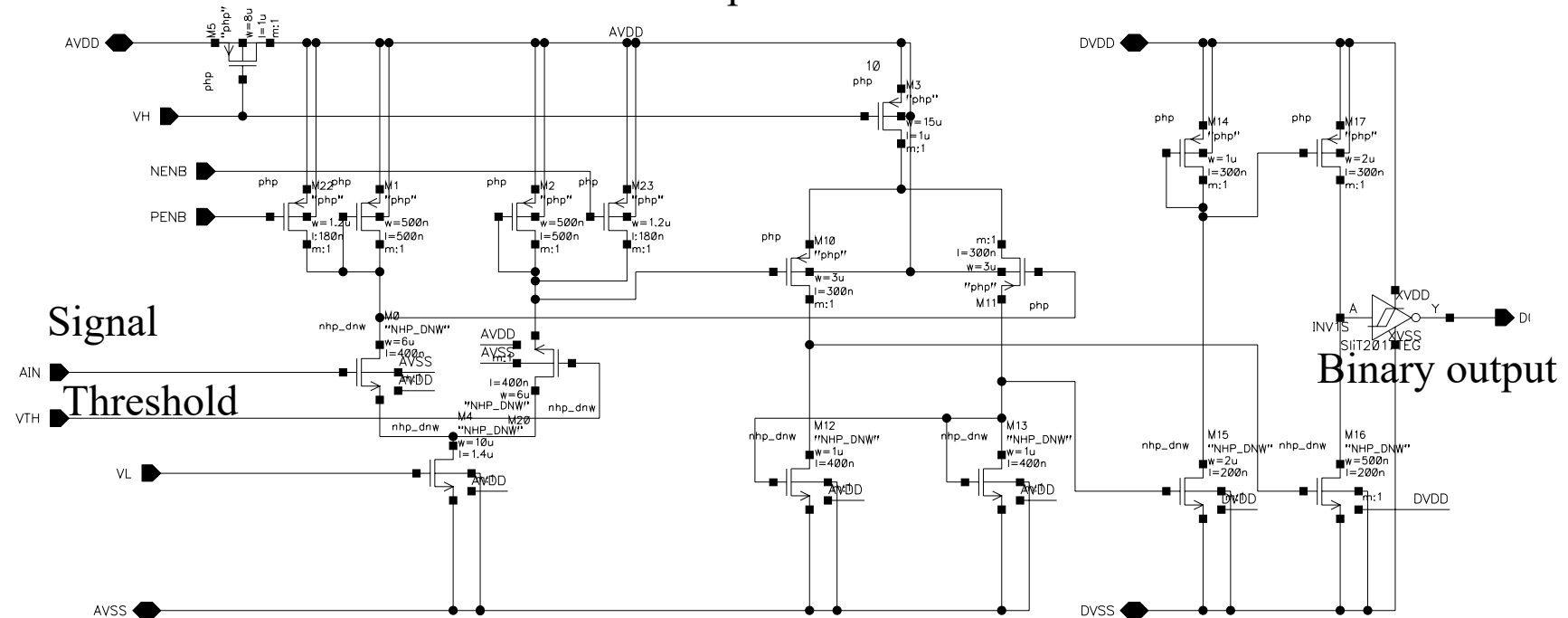
Comparator simulation

- Software: cadence virtuoso IC617
- Simulate the behavior of each transistor in the Comparator

Block diagram of Comparator

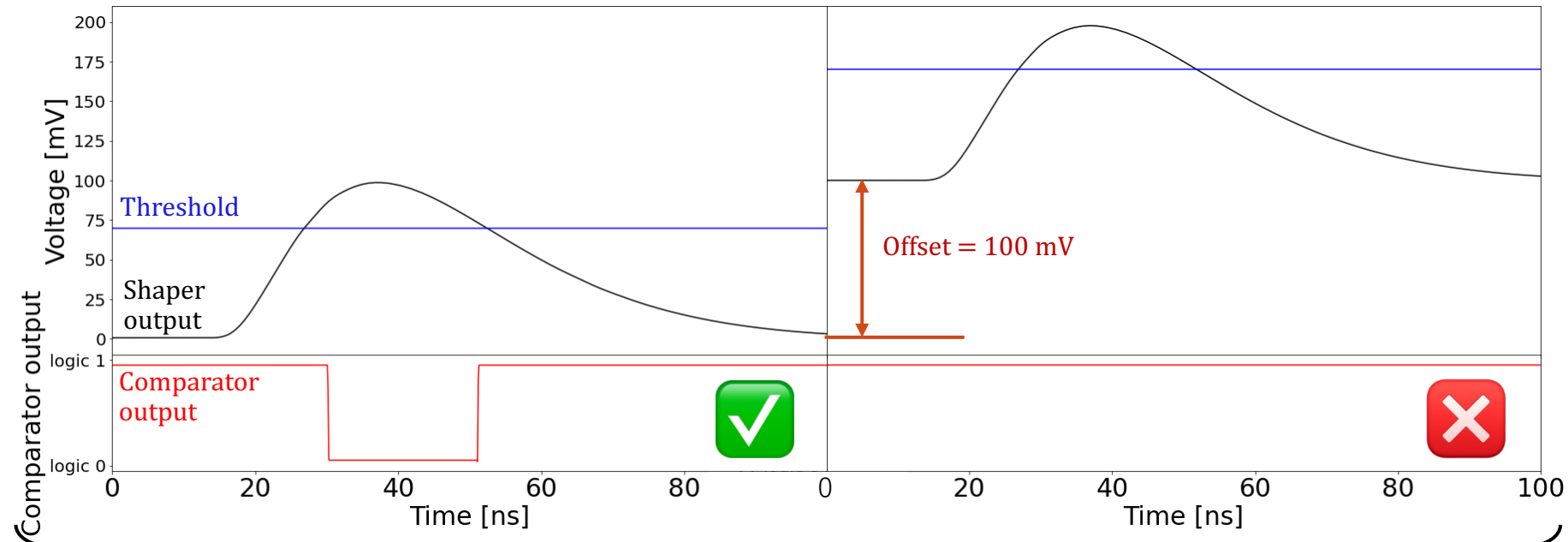


Schematic of Comparator

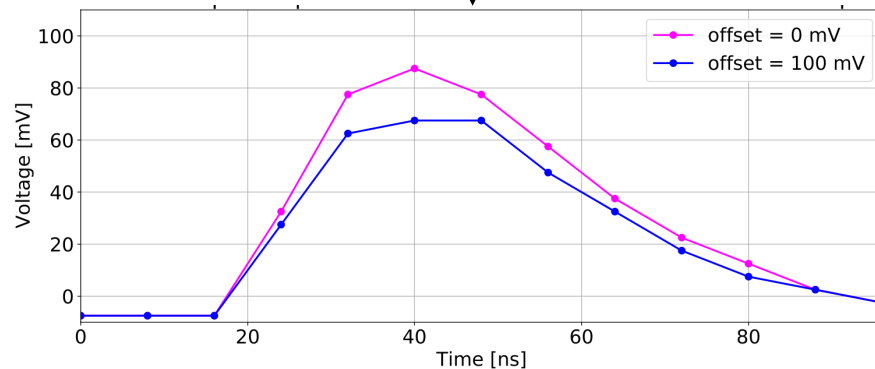


Simulation of Comparator reaction

Simulation environment:
cadence virtuoso IC617

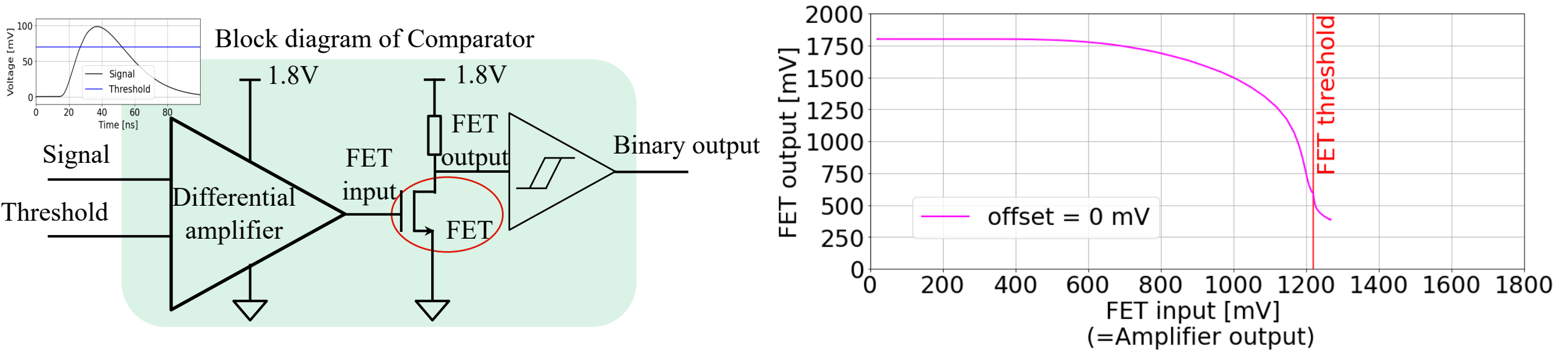


Waveform reconstruction by threshold scanning



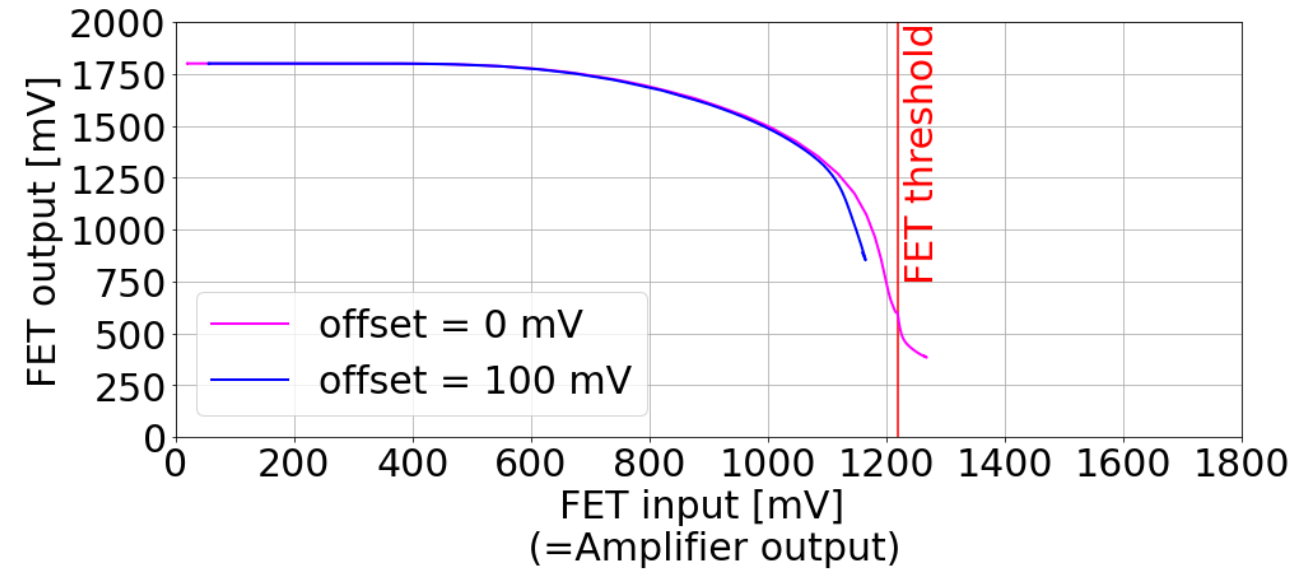
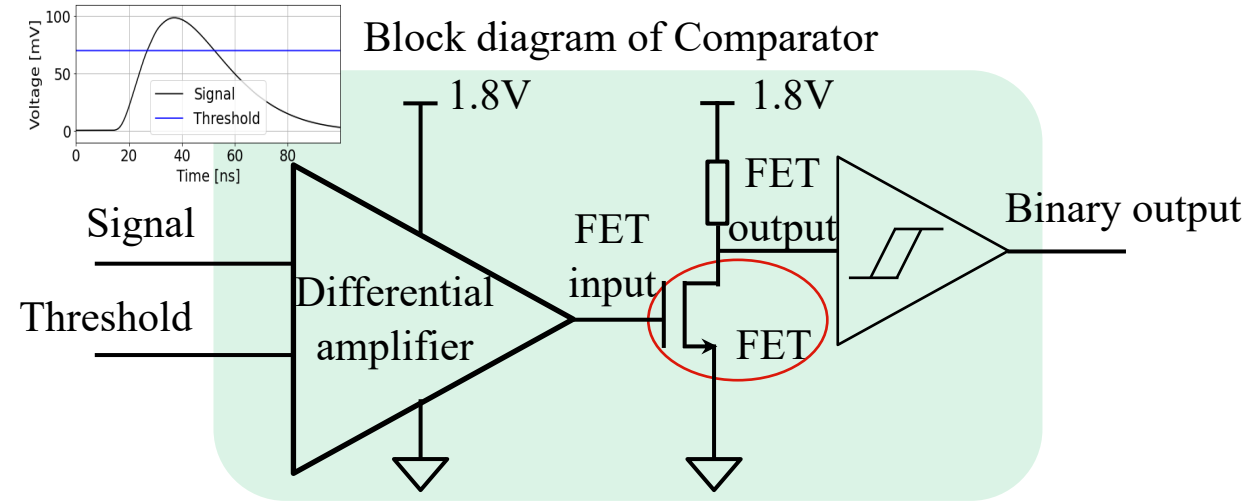
- Direct reason of saturation: no logic 0 output from comparator when shaper output is over threshold
- With offset, saturation reproduced in simulation

Mechanism of saturation and solutions



- Comparator outputs 0 when amplifier output $>$ FET threshold
- Maximum amplifier output is too close to FET threshold:
 - Maximum amplifier output didn't reach 1.8 V
 - FET threshold is too high (0.9 V is preferred)

Mechanism of saturation and solutions



■ Problems:

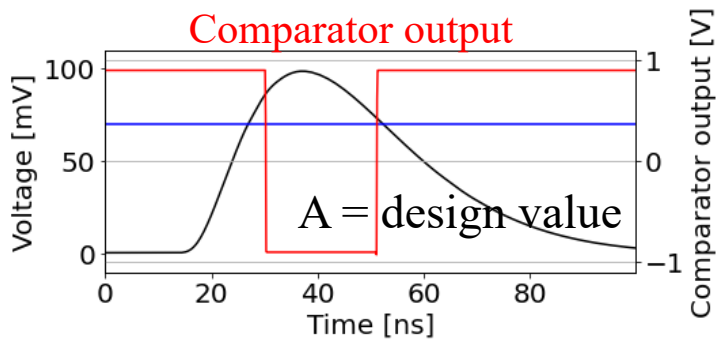
- Maximum amplifier output didn't reach 1.8 V
- FET threshold is too high (0.9 V is preferred)
- Larger offset results in smaller amplification in the amplifier

■ Solutions:

- Raise amplification factor of the amplifier
- Reduce the FET threshold to 0.9 V

Mechanism of signal saturation

No saturation



With saturation

