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[B06] Performance evaluation of front-end ASIC and DSSD sensor for Belle II Silicon Vertex Detector upgrade

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The Belle II Vertex Detector (VXD), which is located around the beam pipe, is one of key sub-detectors in the Belle II experiment that determines the vertex positions. To improve the tolerance for the beam background and reduce the material budget in the outer layers of the VXD, a new silicon strip detector, Thin and Fine-Pitch Silicon Vertex Detector (TFP-SVD), is proposed as a candidate for the VXD upgrade. A new Double-sided Silicon Strip Detector (DSSD), TFP-DSSD, and a new front-end ASIC, SNAP128, are being developed in the TFP-SVD project.

TFP-DSSD sensor is characterized by thin thickness down to 140 um with strip pitch of 75(85) um for P(N) side. These properties reduce the material budget and hit rate per strip due to smaller covered area. The new SNAP128 ASIC is designed in 180 nm CMOS technology and has 128 input channels per chip. The input signal in each channel is processed by preamplifier, shaper and discriminator with the binary output sampled by 127MHz clock. The shaper output has a short pulse width of about 60 ns, which helps reducing signal pile-up at high hit-rate.

This presentation reports the first performance evaluation of the prototype ASIC and sensor. For the ASIC, we report the measurement of the noise level, power consumption, and waveform of shaper output. We confirmed the basic functionality of SNAP128, and that the power consumption and analog pulse width meets the design requirements. Also, we found two major issues. The first one is that the discriminator circuit gets saturated when processing positive signals. The second one is that the noise at the target detector capacitance (15 pF) is about $1200\ e^-$, over the design limit of $800\ e^-$. Possible solutions to these two issues are discussed in this presentation.

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