Design and performance of the Monopix2 reticle-scale DMAPS

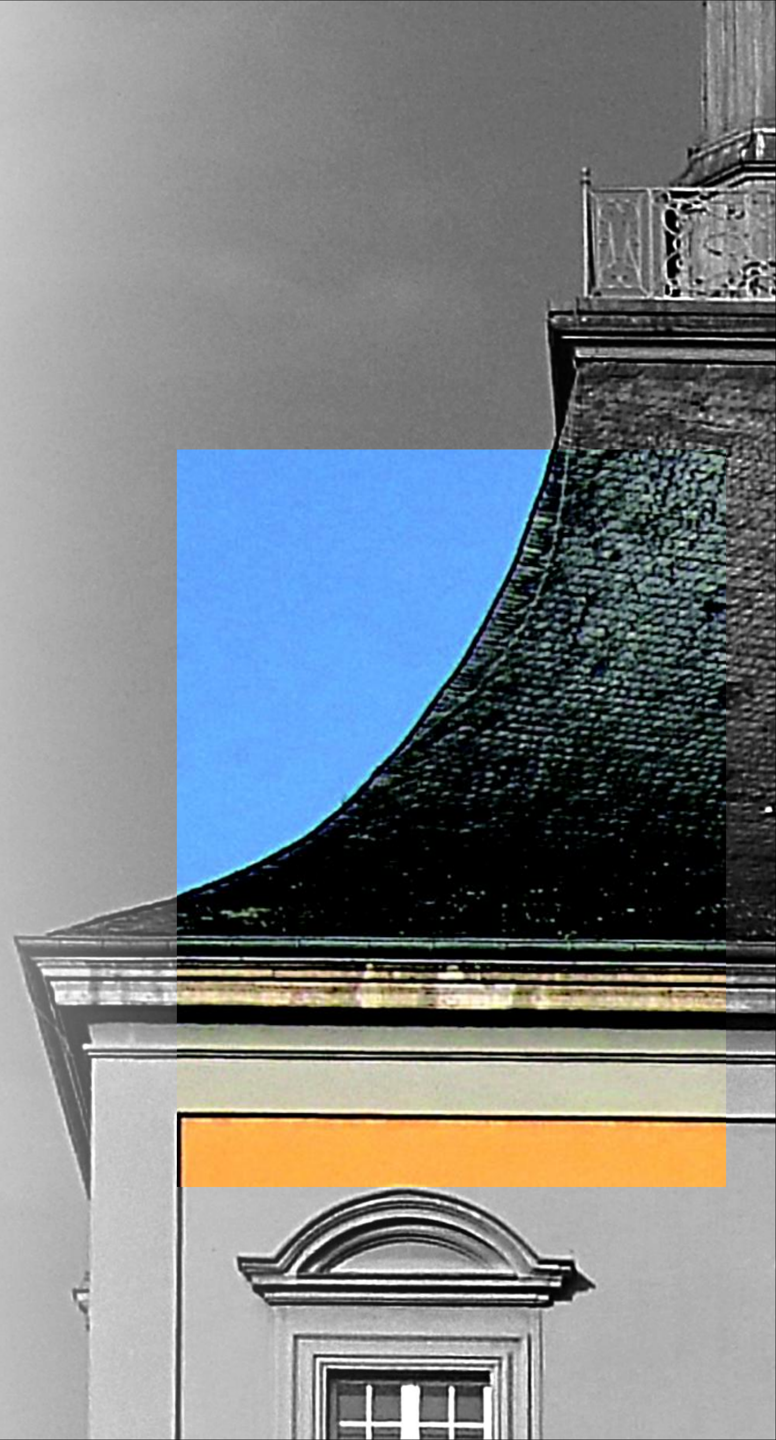
Ivan Caicedo*, C. Bespin, J. Dingfelder, T. Hemperek, T. Hirono, F. Huegging, H. Krueger, K. Moustakas, P. Rymaszewski, L. Schall, T. Wang, N. Wermes, S. Zhang
(University of Bonn)

M. Barbero, P. Barrillon, P. Breugnon, P Chabrillat, N. Destaing, A. Habib, P. Pangaud, A. Rozanov
(Aix Marseille University, CNRS/IN2P3, CPPM)

Y. Degerli, F. Guilloux, P. Schwemling (IRFU CEA-Saclay)

I. Berdalovic, R. Cardella, L. Flores, C. Marin, H. Pernegger, F. Piro, P. Riedler, W. Snoeys (CERN)

*caicedo@physik.uni-bonn.de

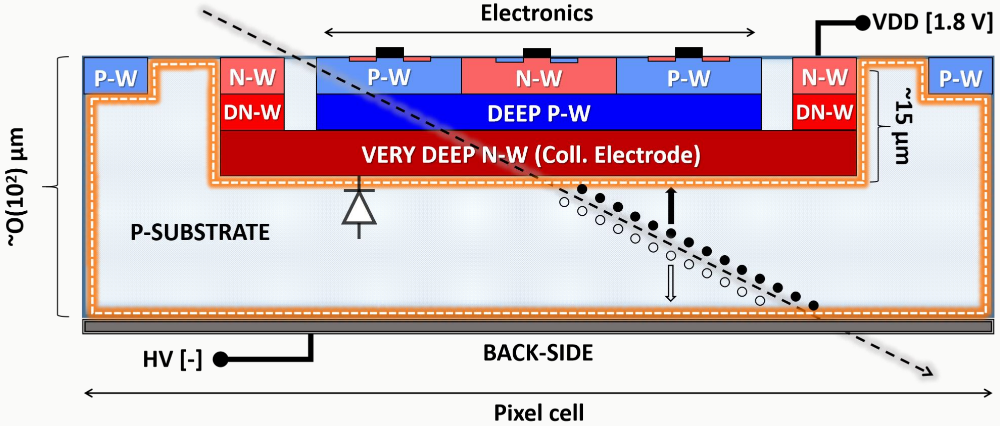


DEPLETED MONOLITHIC ACTIVE PIXEL SENSORS (DMAPS)

- Commercial CMOS processes: Multiple wells to shield electronics.
- Considerable depleted regions in highly resistive substrates: Fast charge collection by drift.

"Large Electrode" design

Large collecting well containing all in-pixel electronics

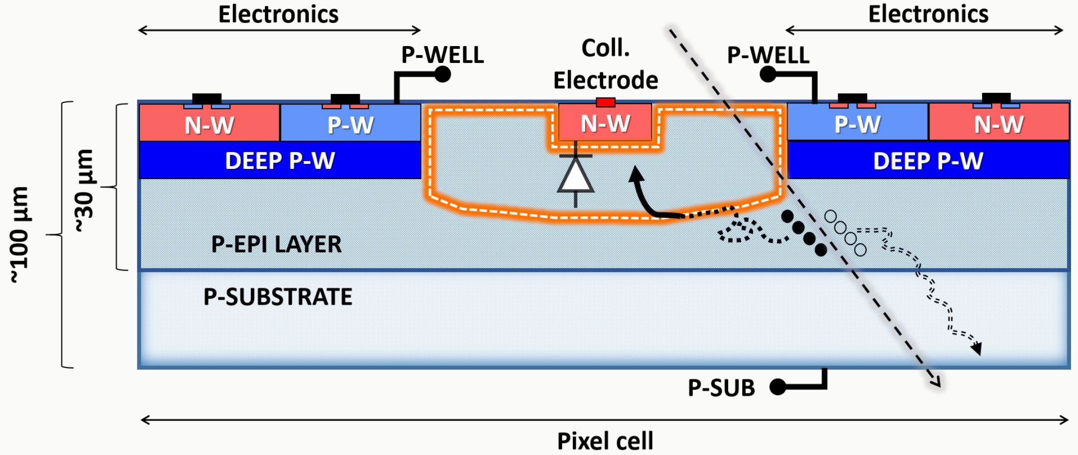


PROS: Short drift distances, strong E-field (Rad-hard).
CONS: Large sensor capacitance, high analog power.

---> Requires design efforts to optimize timing and minimize cross-coupling into the collection node.

"Small Electrode" design

Small collecting well separate from in-pixel electronics



PROS: Small sensor capacitance, low power and noise.
CONS: Weak electrical field compromises rad-hardness.

---> Requires process modifications and small pixel pitch to optimize charge collection.

DMAPS FOR HIGH ENERGY COLLIDER EXPERIMENTS

Taking the requirements of future HEP experiments as benchmark:

	ITk Outer Layer	Belle II VTX
Occupancy	1 MHz/mm^2	1.5 MHz/mm^2
Time Res.	25 ns	O(100) ns
NIEL	10^{15} n_{eq}/cm^2	5×10^{14} n_{eq}/cm^2
TID	80 Mrad	100 Mrad
Area	O(10m^2)	O(3m^2)

DMAPS would offer:

- Reduced material budget compared to hybrids.
- Cheaper and less complex module production.

The Monopix DMAPS developments

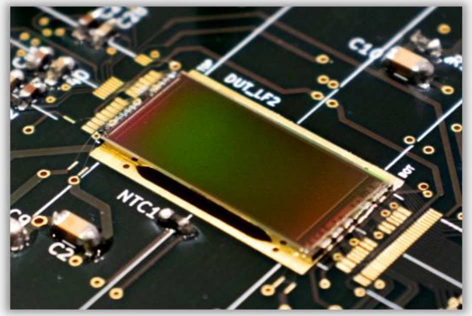
Column-Drain ("FE-I3 like") synchronous R/O architecture and fast front-end implementations

+

Design optimization to preserve charge collection after irradiation

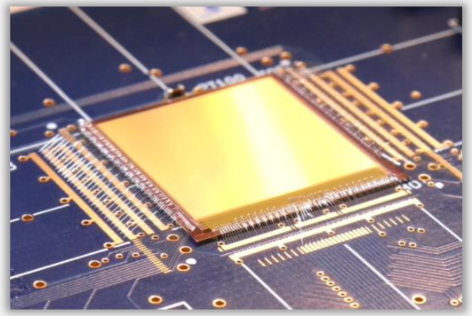
LF-Monopix:

Large electrode DMAPS in LFoundry 150 nm CMOS



TJ-Monopix:

Small electrode DMAPS in Tower 180 nm CMOS



THE LF-MONOPIX PROTOTYPES

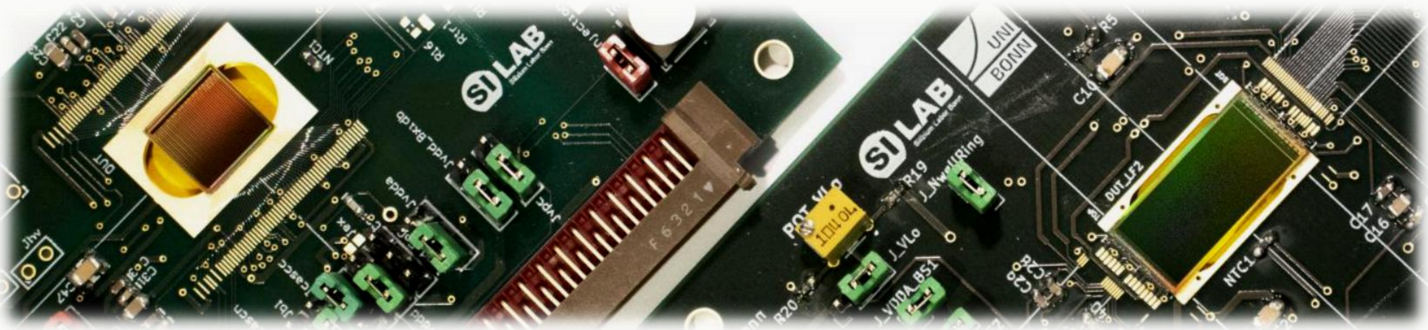
Barbero et al. https://doi.org/10.1088/1748-0221/15/05/P05013
Dingfelder et al. https://doi.org/10.1016/j.nima.2022.166747

LFoundry
150 nm CMOS
process

Silizium Labor Bonn

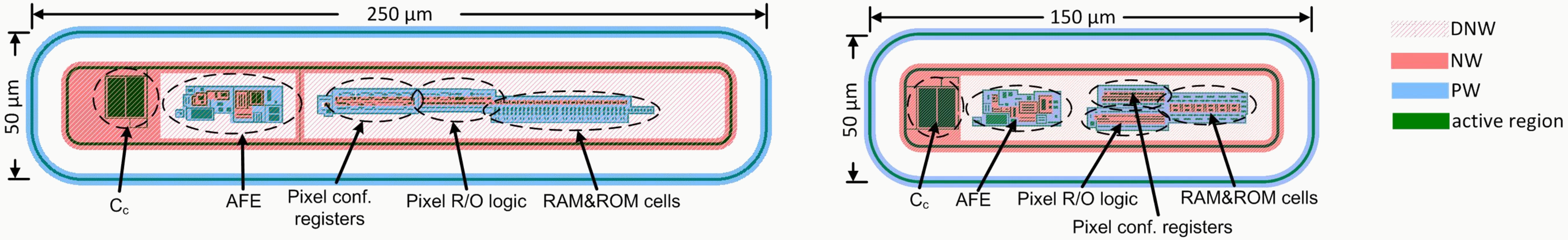
LF-Monopix1
(Mar 2017)

LF-Monopix2
(Feb 2021)



- **Full-size (~cm²) large electrode DMAPS.**
- **Functional column-drain R/O architecture.**
- **In-pixel electronics in >2 kΩ-cm resistive substrates.**

Pixel layouts
(Top view):

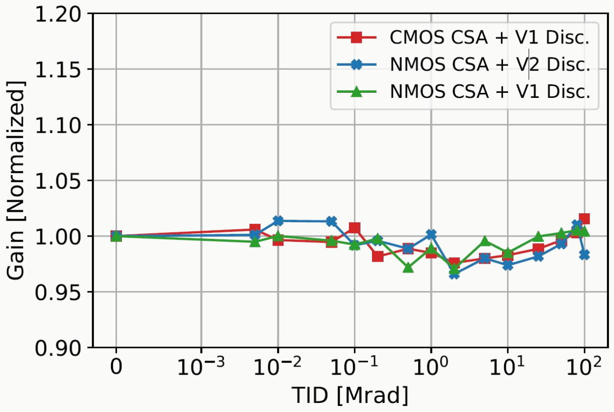


DAQ system: Bonn's Multi-I/O 3 ("MIO3") and General Purpose Analog Card ("GPAC")

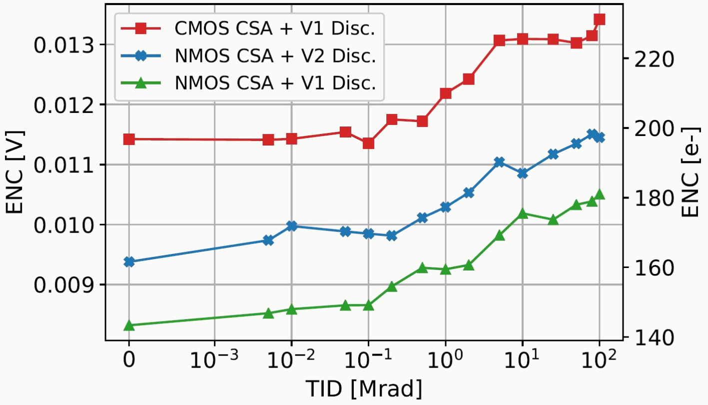
LF-MONOPIX1: RADIATION HARDNESS

TID up to 100 Mrad

- **Relative Gain variation:** <3%



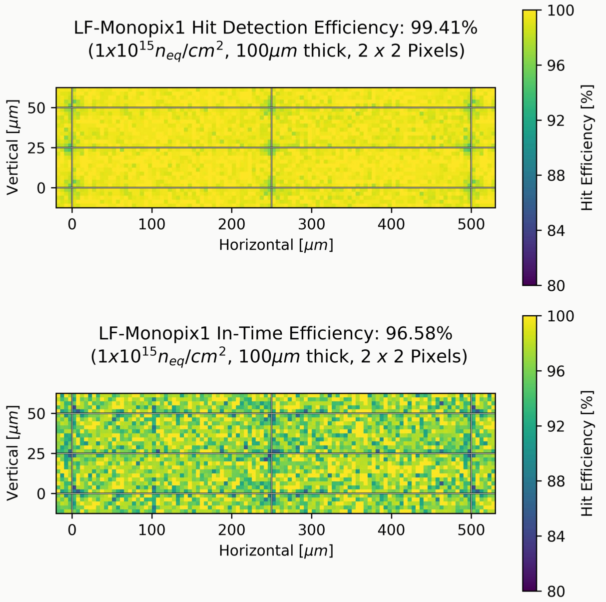
- **ENC increase:** NMOS CSA (25%), CMOS CSA (15%)

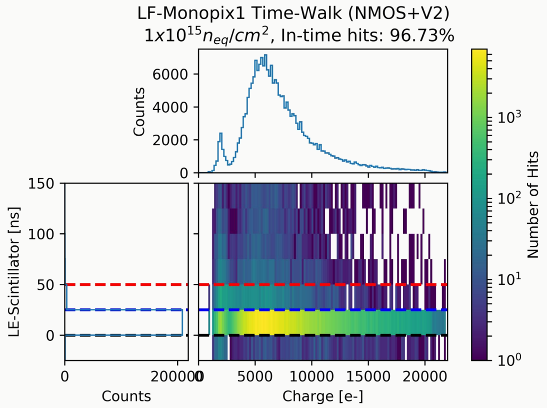


NIEL up to 1x10^{15} N_{eq}/cm^2

- **Hit efficiency:** ~99.4% (in-time: ~96.6%)

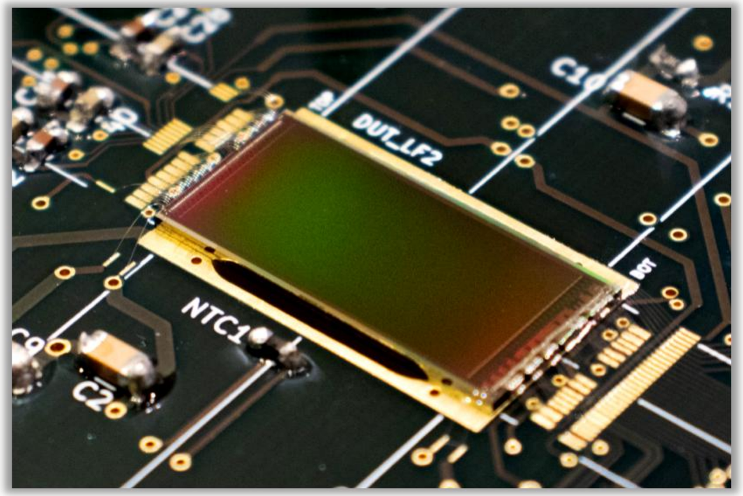
(100 µm thick | Bias: 150V | Threshold: 2336±262 e$^-$ | Noise Occ. < 10^{-7})

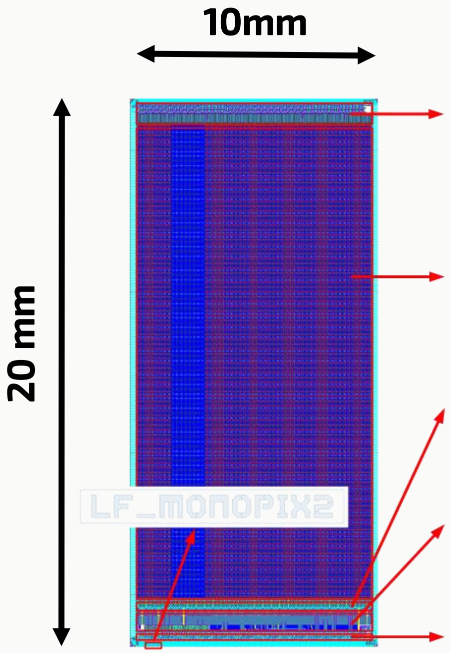




Caicedo et al. http://10.1016/j.nima.2022.167224

LF-MONOPIX2





- Smaller pixel pitch than LF-M1: **50 x 150 µm²**
  → Reduced C_{det} (~250 fF)
  ergo: lower noise & power
- Larger pixel array (**340 rows x 56 cols**)
- 40 MHz / 160 MHz CMOS or LVDS serial output.
- Timestamping: **6-bit LE/TE (ToT) @ 25 ns**
- Analog power: ~30 µW/pixel **(400 mW/cm²)**
- New injection & HitOr circuitry: **Digital, at pixel level**

Column-drain R/O in a **1.7 centimeter long column**, with **full in-pixel electronics** ☑

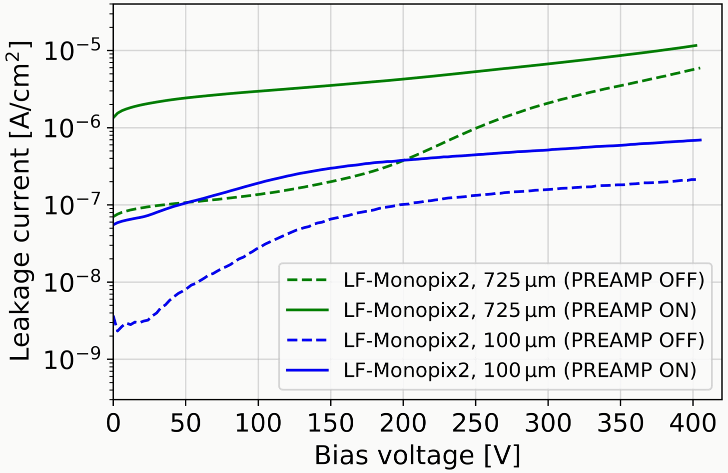
Improved pixel layout for **further cross-coupling mitigation** ☑

The chip inherited the fastest rad-hard front-end
(CSA with NMOS input transistor
+
fast discriminator)

Some additional new features to be tested:

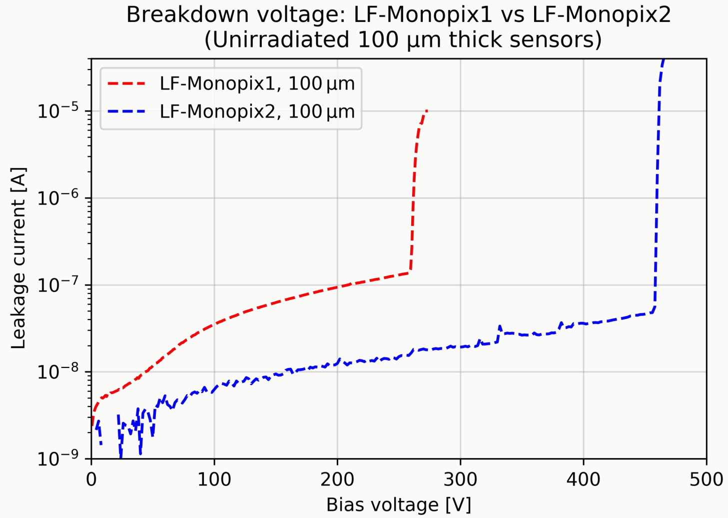
- Improved range of tuning circuitry
  - Benefits of smaller C_f (1.5 fF)
- Slightly modified CSA versions

LEAKAGE AND BREAKDOWN IN LF-MONOPIX2



Succesful wafer thinning and back-side processing

- Leakage current: <1 µA/cm²
- No early breakdown

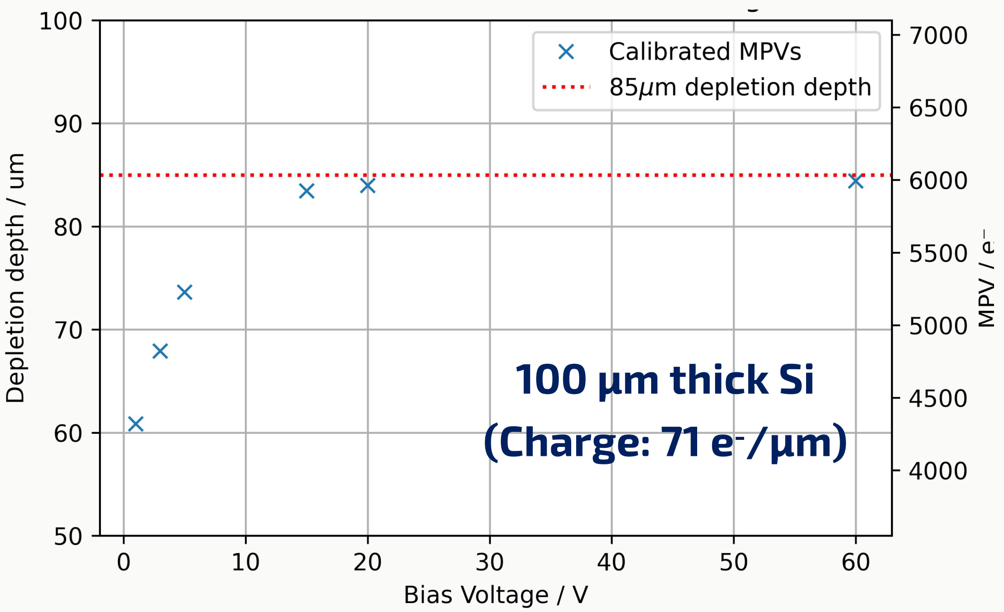


Improved breakdown voltage in LF-Monopix2

(~460V)

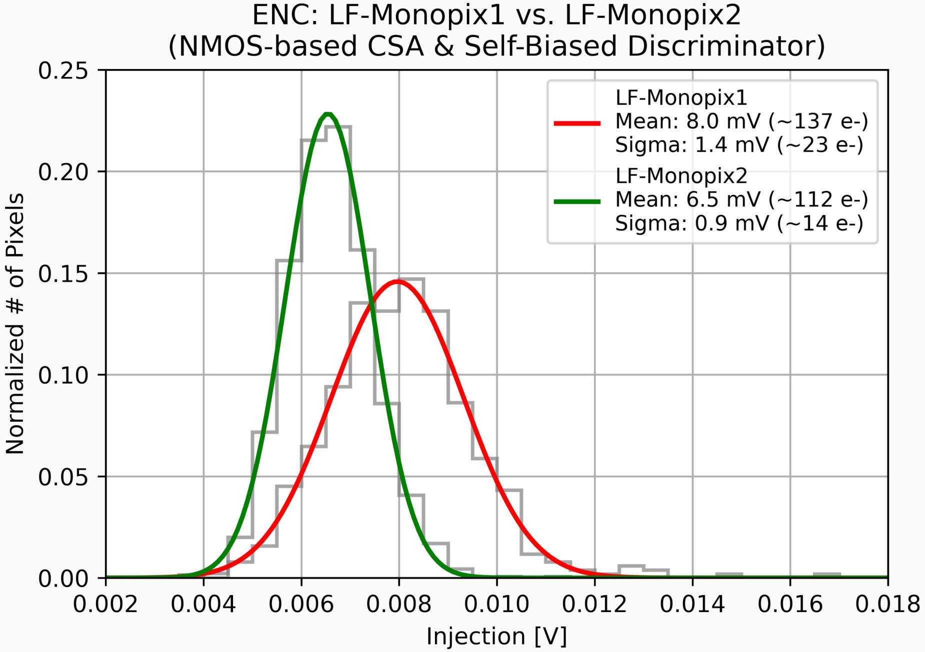
due to guard-ring optimization

The breakdown voltage is large enough to fully deplete 100 µm thick chips



LF-MONOPIX2: ENC & GAIN

ENC from LF-Monopix1 to LF-Monopix2:

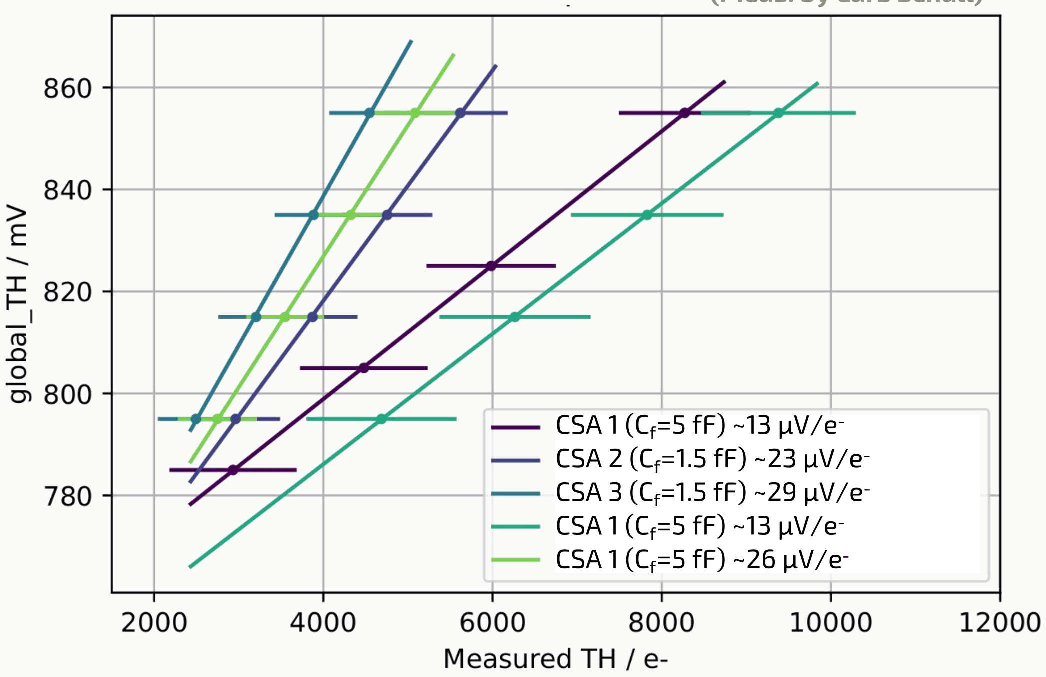


Decrease of ~20-30% in mean ENC and dispersion for the same front-end implementation

(As expected from reduced pixel pitch ~ C_d)

Gain calculated out of multiple untuned threshold scans:

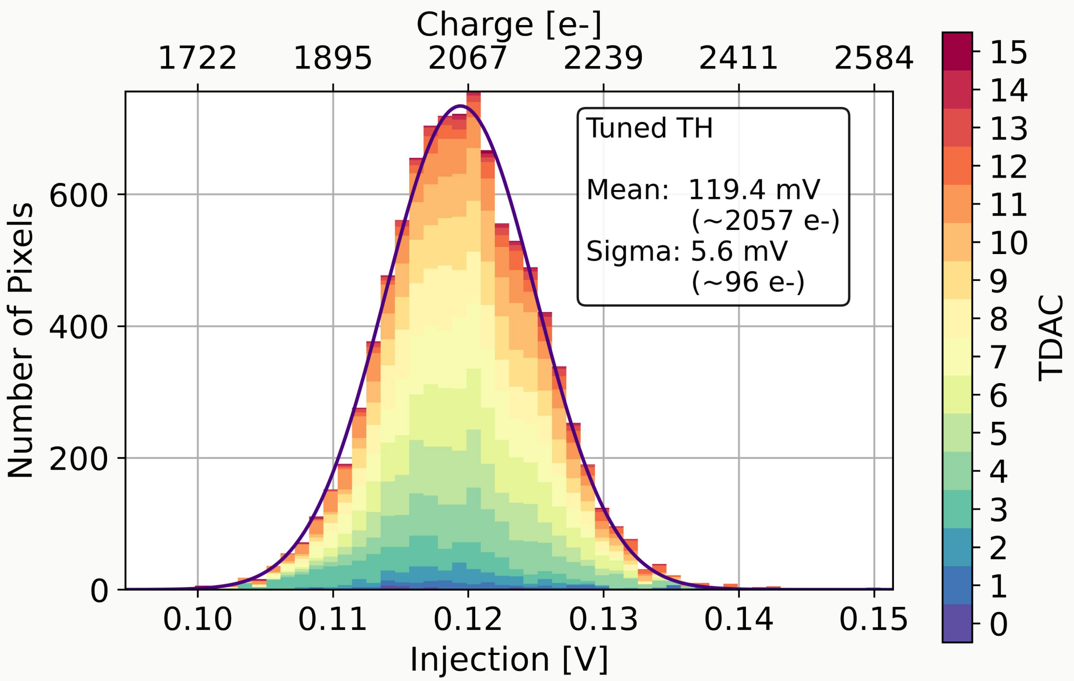
(Meas. by Lars Schall)



- Very linear CSA response
- Both old and new CSAs benefit from a smaller C_f

LF-MONOPIX2: TUNED FRONT-END PERFORMANCE

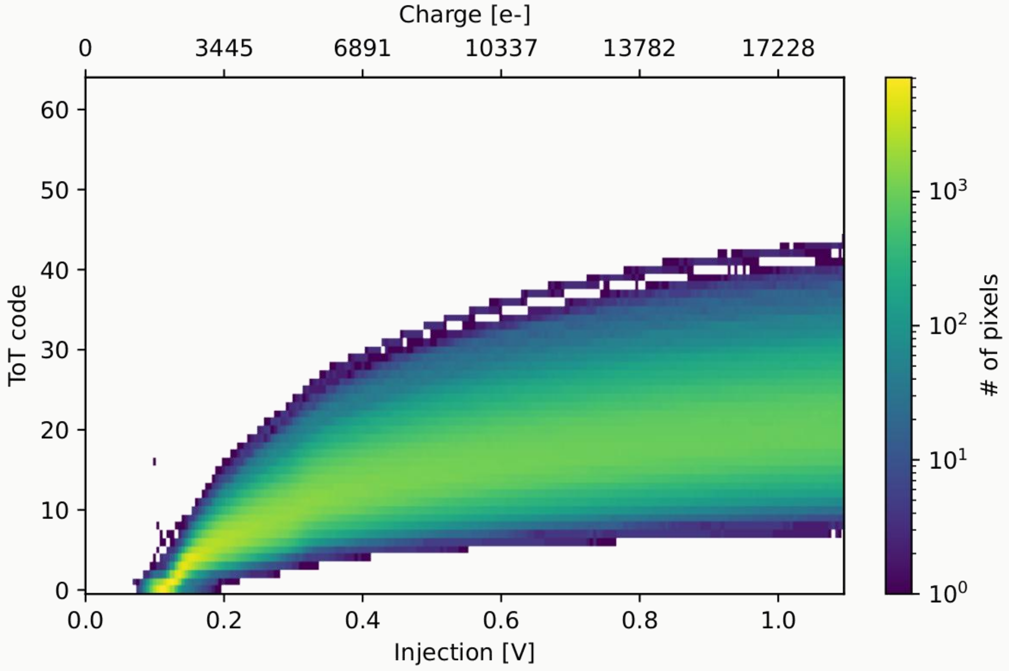
Threshold dispersion tuned through of a 4-bit current DAC (per pixel) :



- **Tuned threshold dispersion ~100e-**
  - Normally distributed TDAC values
- Only 1/3 of the maximum TDAC bias current

Correct ToT response for different charges

The dispersion in ToT was intentional (Low V_{fb}), for better charge sampling

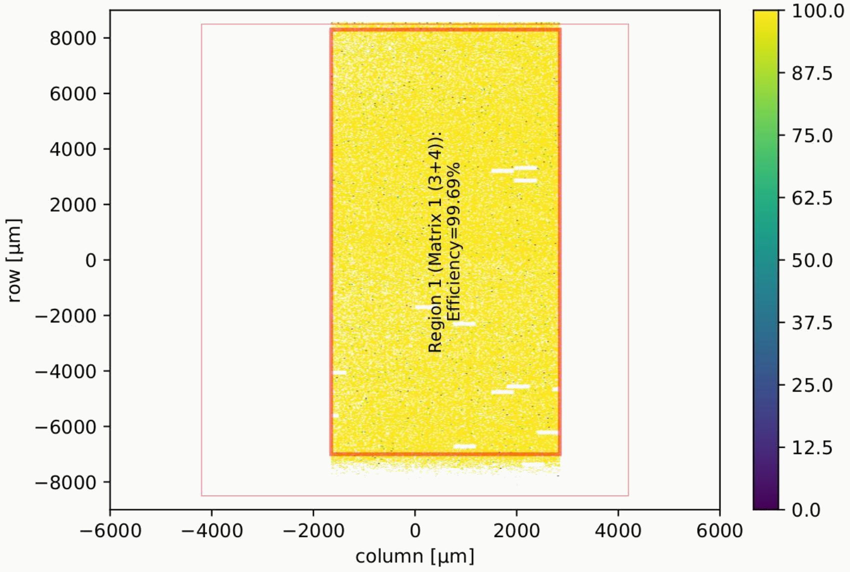


LF-MONOPIX2: HIT & IN-TIME EFFICIENCY

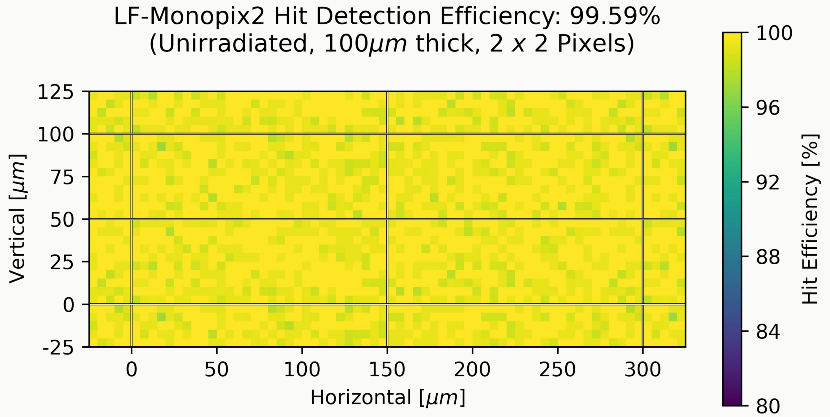
- **Unirradiated chip exposed to 5 GeV e- @ DESY**

(100 µm thick | Bias: 60V | Mean threshold ~2ke- | Noise Occ. < 10^{-7})

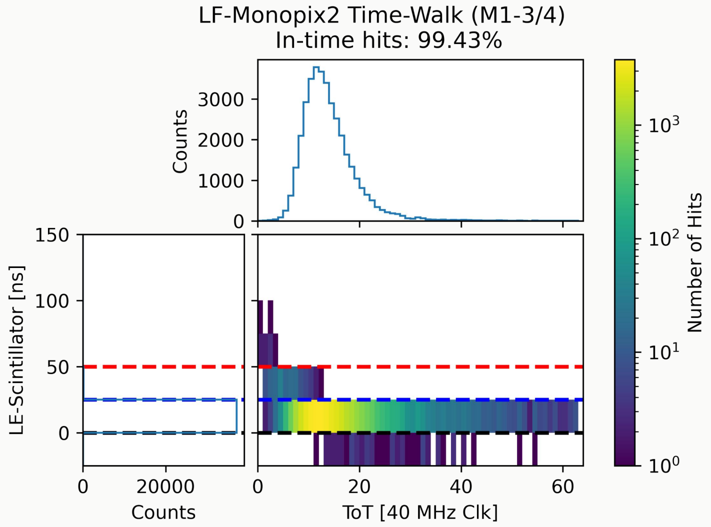
Efficiency map of the full matrix



Efficiency projected onto a 2x2 pixel array

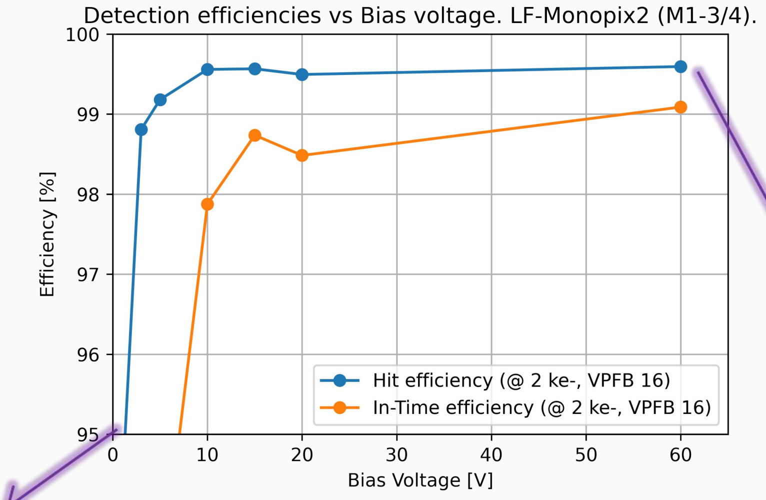


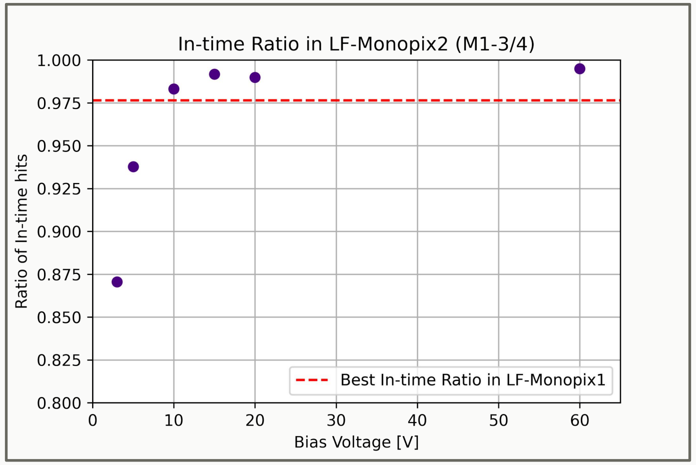
Time-walk distribution of seed pixels in efficient events

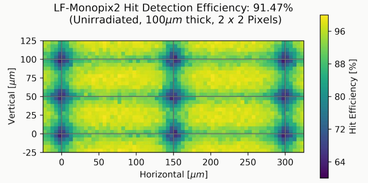


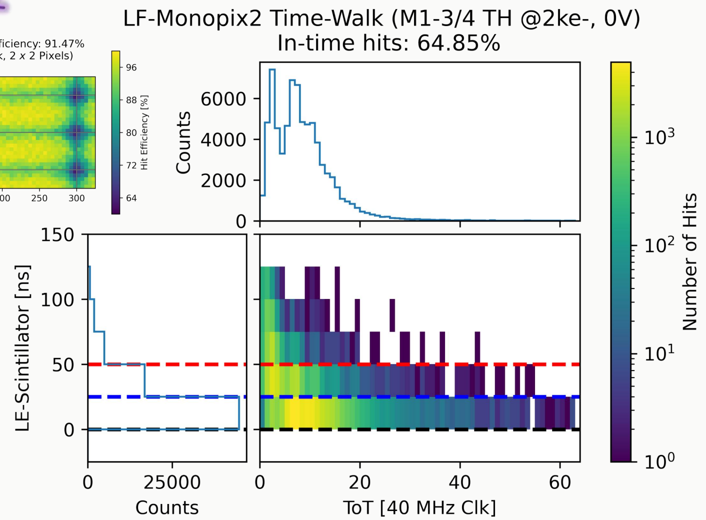
- **Hit detection efficiency and in-time events >99%**
- **~2.5% improvement in in-time efficiency (at the same threshold) with respect to LF-M1**

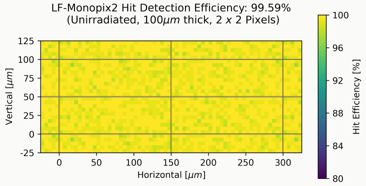
LF-MONOPIX2: EFFICIENCY VS BIAS VOLTAGE

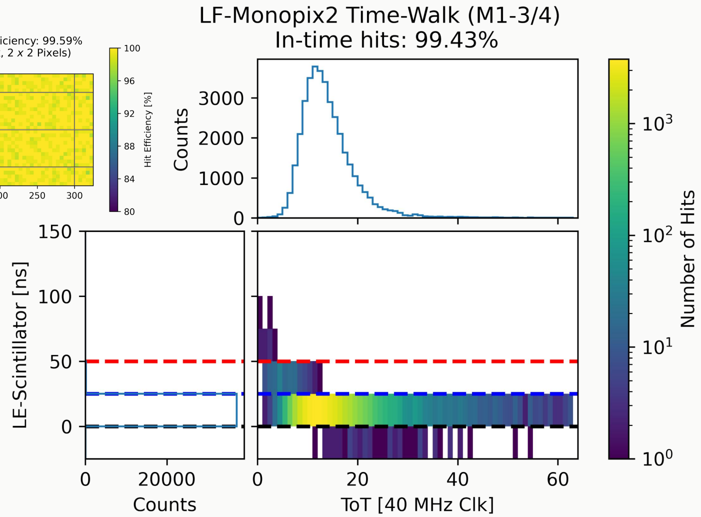






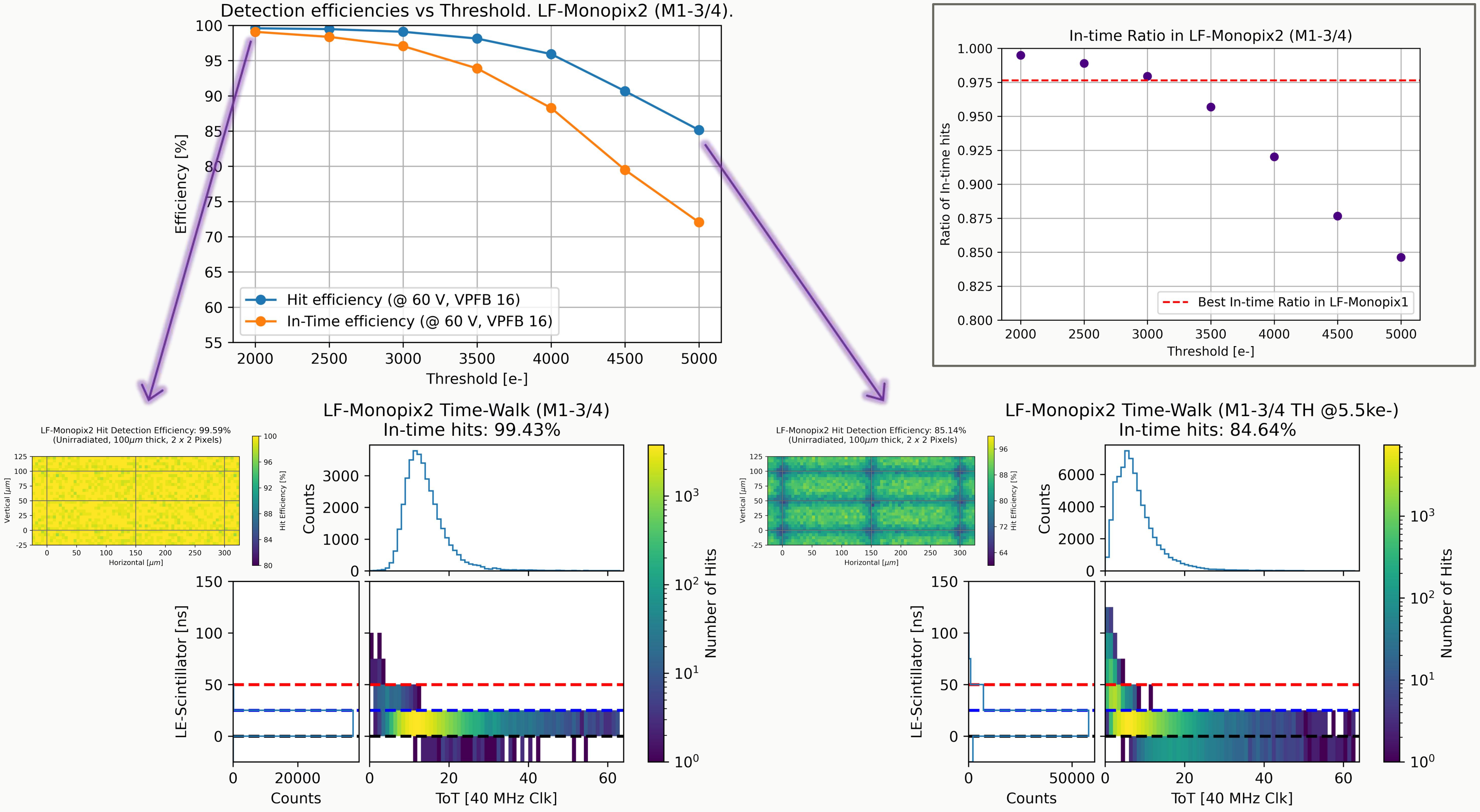






- **Expected drop in overall hit and in-time efficiency as the MIP signal shrinks with the depleted region**
- **Lowest efficiency at the pixel edges** (charge sharing)

LF-MONOPIX2: EFFICIENCY VS THRESHOLD



- **Expected uniform drop in hit efficiency as the threshold increases**

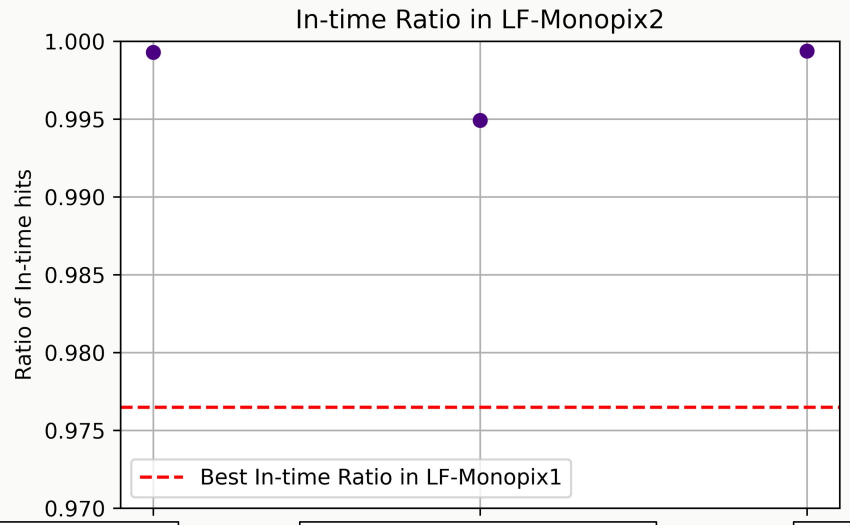
- **Threshold dependency of the front-end timing performance**

(Designed for a threshold ~1.5ke$^-$ and a signal ~6 ke$^-$)

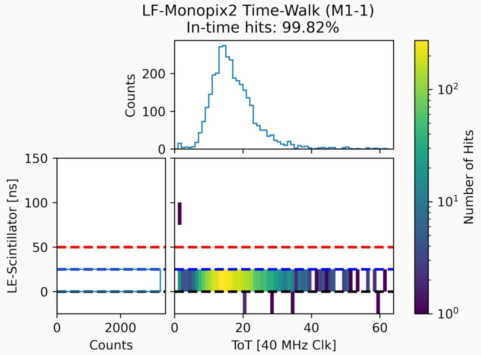
LF-MONOPIX2: TIMING VS FEEDBACK CAPACITANCE

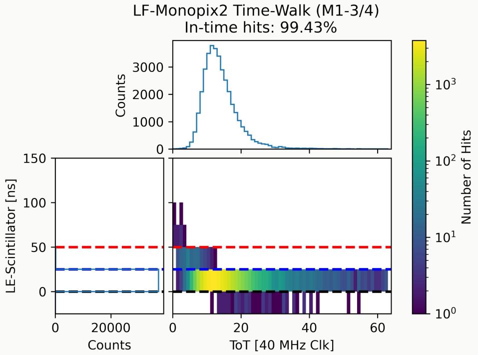
The increase in gain results in all efficient events detected within 25 ns

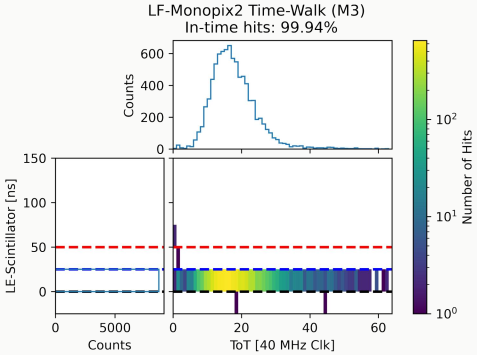
(Bias: 60V |
Mean threshold ~2ke)



CSA 1 (C_f=1.5 fF)	CSA 1 (C_f=5 fF)	CSA 3 (C_f=1.5 fF)





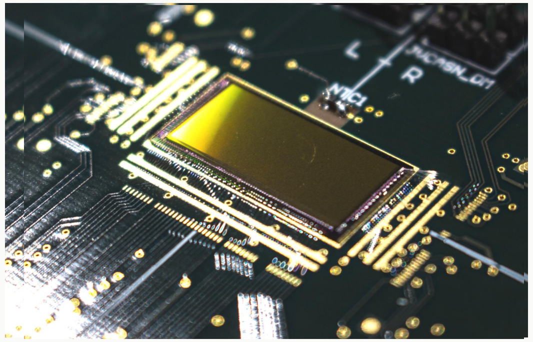


THE TJ-MONOPIX PROTOTYPES

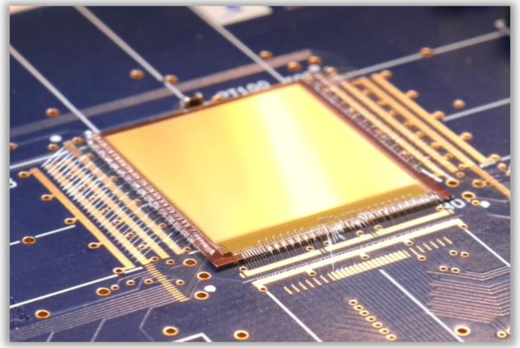
K. Moustakas https://hdl.handle.net/20.500.11811/9315
Dingfelder et al. https://doi.org/10.1016/j.nima.2022.166747

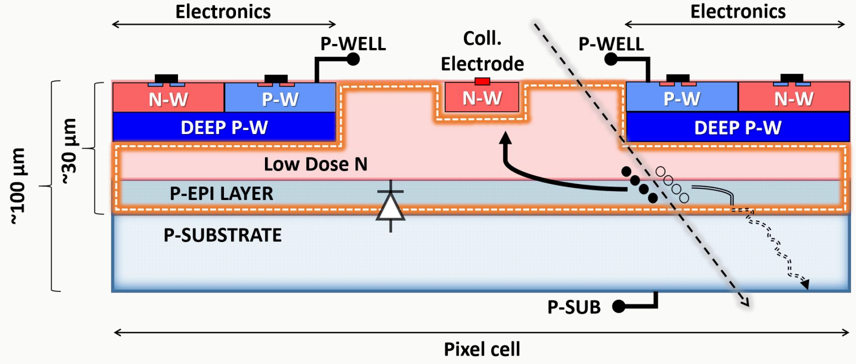
Tower
180 nm CMOS
process

TJ-Monopix1
(Mar. 2018)



TJ-Monopix2
(Mar. 2021)





In both chips:
Uniform depletion through the addition of a low dose n-type layer + further process modifications

Snoeys et al. https://doi.org/10.1016/j.nima.2017.07.046

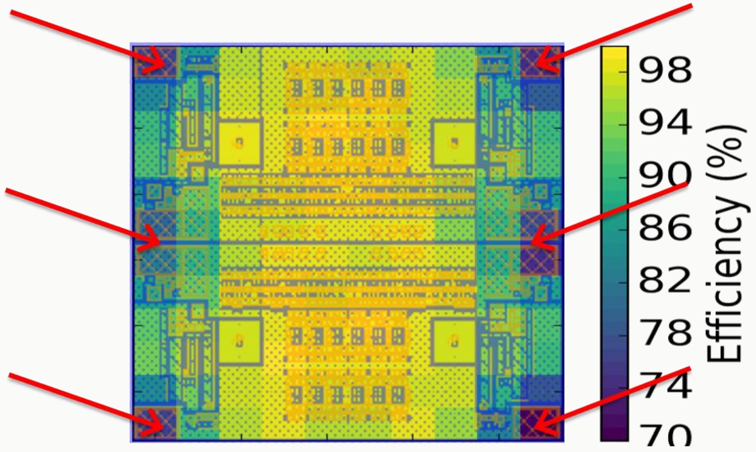
- **Full-size (~cm²) small electrode DMAPS**
- **Functional column-drain R/O architecture**
- **In-pixel electronics in ~1 kΩ-cm resistive epi-layer or Czochralski substrate**
- **Low power front-end design based on ALPIDE**

DAQ systems: Bonn's MIO3 + GPAC or BDAQ (RD-53A/B testing readout board)

TJ-MONOPIX1: PROCESS WITH N-LAYER ONLY

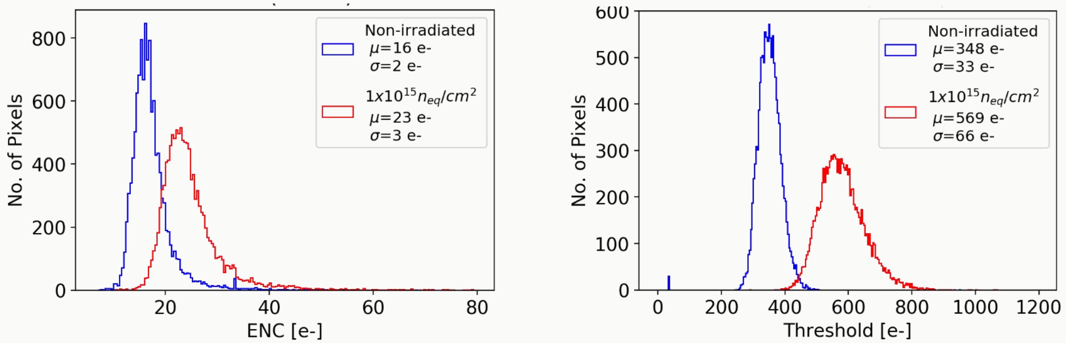
The first design of TJ-Monopix1 (2018) added only a continuous n-layer for uniform depletion

Worked well except for charges created at the pixel corners, where the lateral component of the electric field was not strong enough to drive them to the collection node

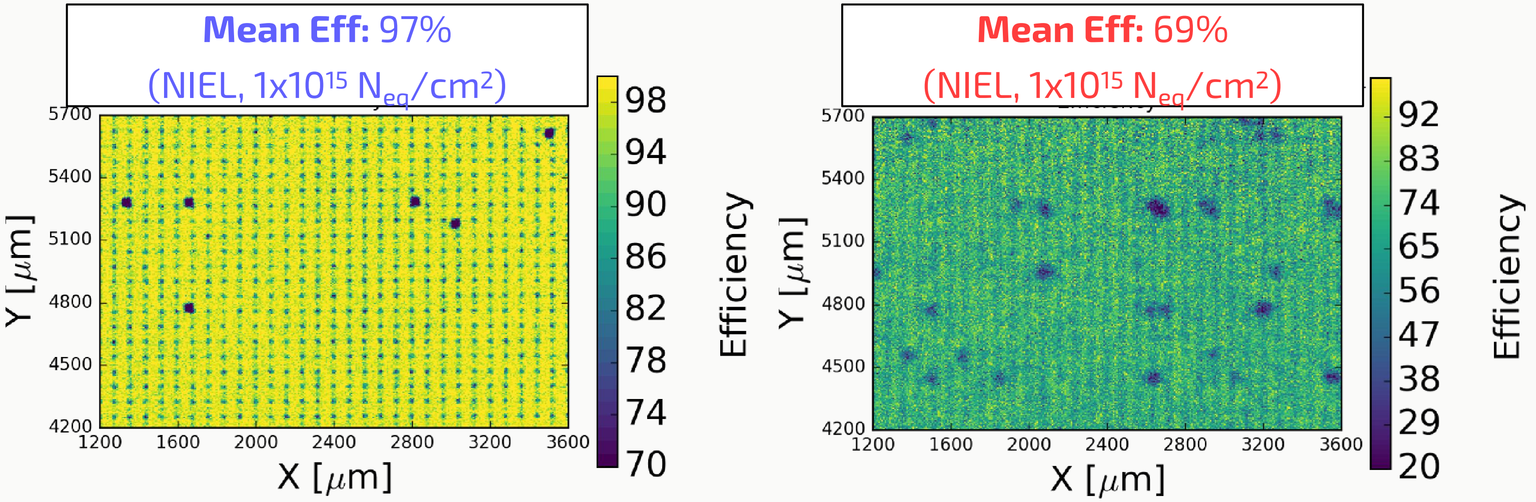


Caicedo et al. https://doi.org/10.1088/1748-0221/14/06/C06006

In addition to that, an asymmetric ENC distribution limited the minimum operational threshold (RTS noise)



Resulting in low hit detection efficiencies:

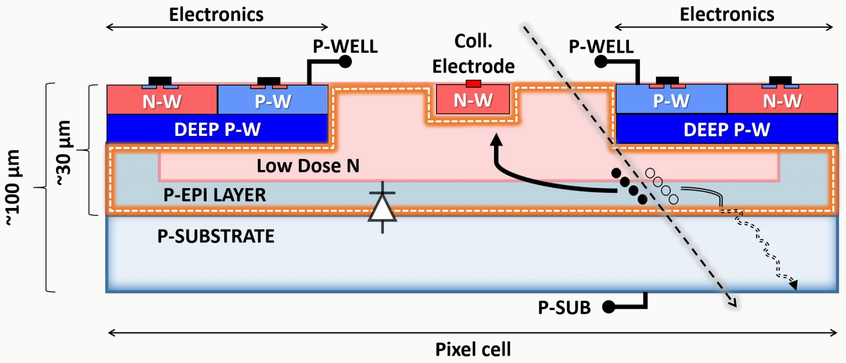


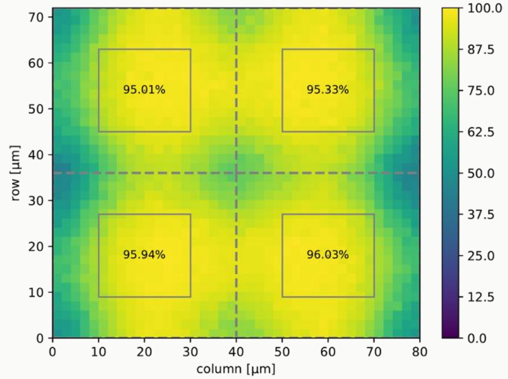
TJ-MONOPIX1: IMPROVEMENT OF CHARGE COLLECTION

- **Additional process modifications** (gap in n-layer or additional p-typle implant) → Improve lateral field at pixel corners.
    - **Czochralski substrates instead of epi-layer** → Larger depleted volume (and therefore, larger signal MPV)

Two designs were neutron-irradiated and tested in beam (NIEL, 1x10^{15} N$_{eq}$/cm^2)

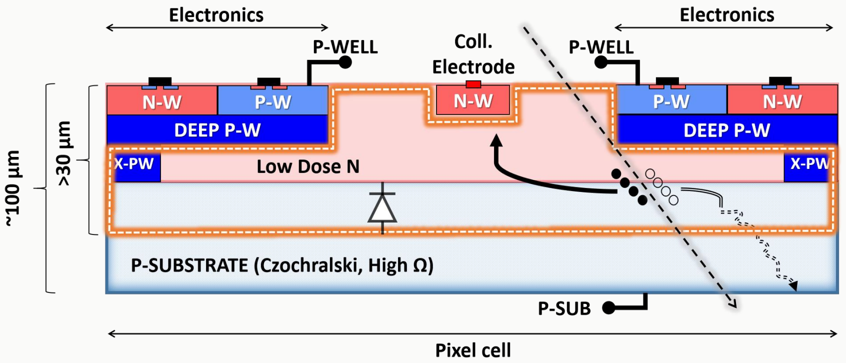
Epi-layer + gap in n-layer

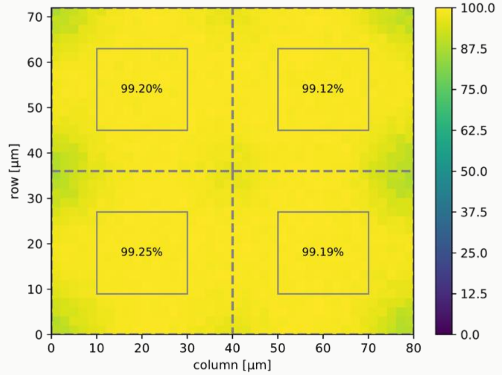




Mean efficiency: 87.1% (Threshold ~500e$^-$)

Cz substrate + Extra p-well



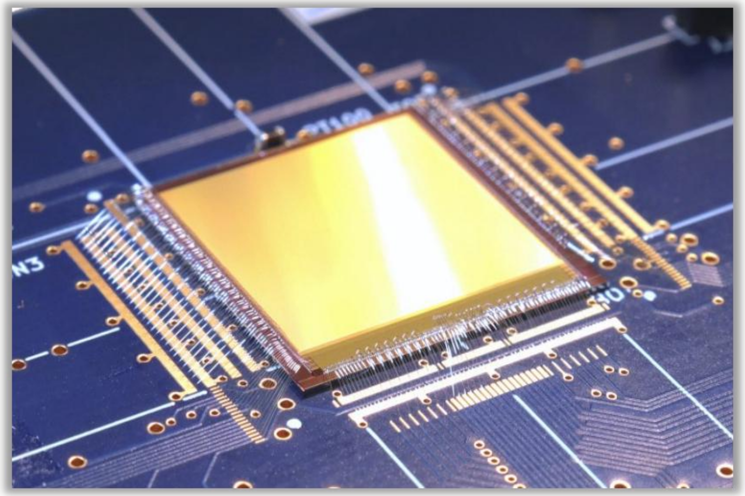


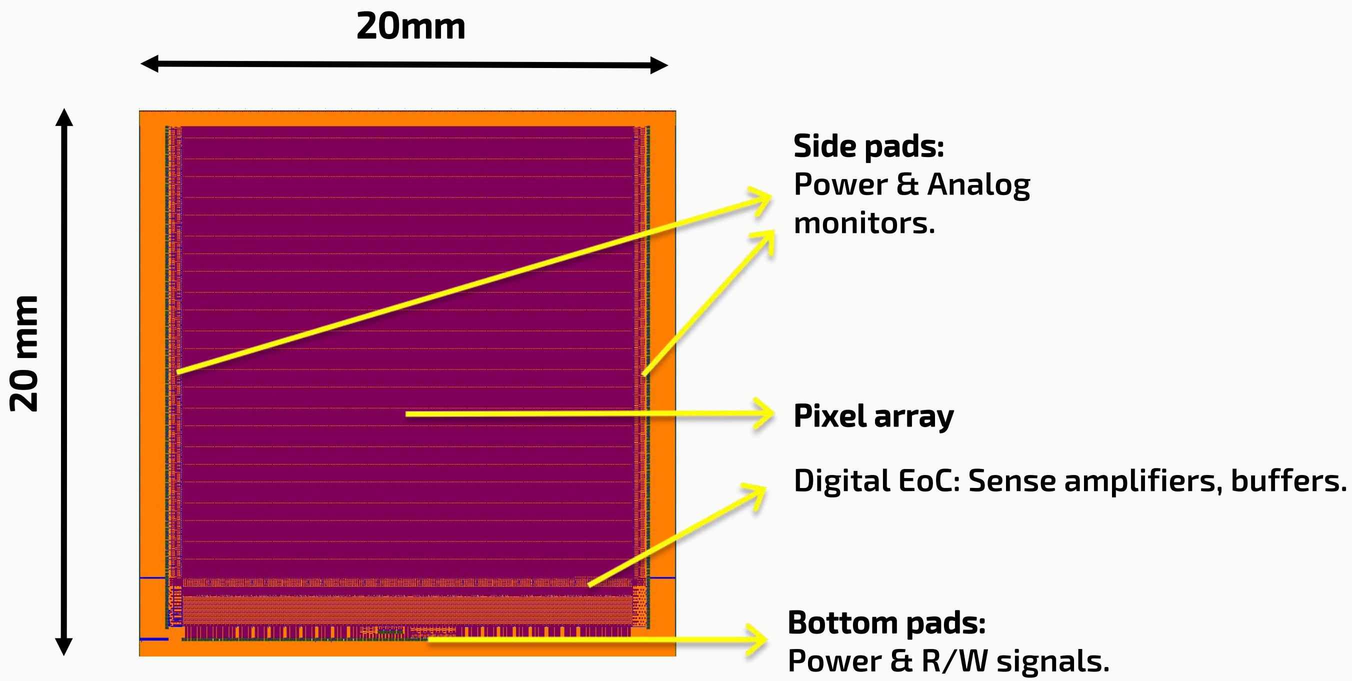
Mean efficiency: 98.6% (Threshold ~490e$^-$)

Münker et al. https://doi.org/10.1088/1748-0221/14/05/C05013
Pernegger et al. https://doi.org/10.1016/j.nima.2020.164381

Bespin et al. https://doi.org/10.1016/j.nima.2022.167189

TJ-MONOPIX2





- <u>Smaller pixel pitch than TJ-M1</u>: **33 x 33 µm²**
  → Shorter drift paths for charges created at the pixel edges
- Larger pixel array (**512 rows x 512 cols**)
- 160 MHz/320 MHz LVDS serial lines
- Timestamping: **7-bit LE/TE (ToT) @ 25 ns**
- Analog power: ~1 µW/pixel **(90 mW/cm²)**
- Local pixel tuning: **3-bits**
- Command decoder in periphery (RD-53B)

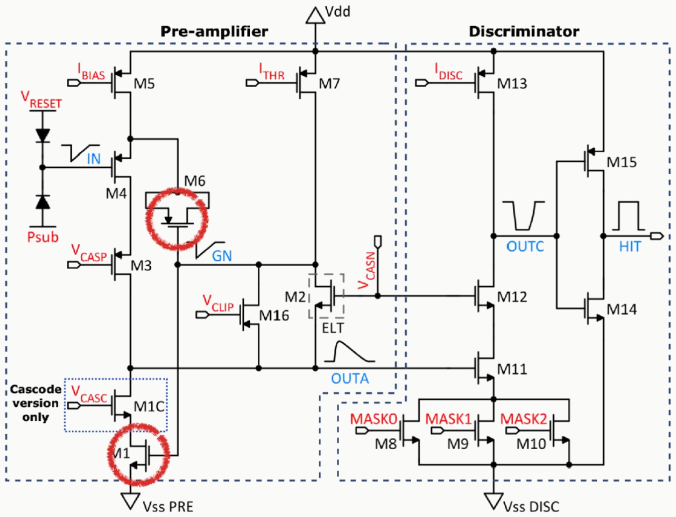
Column-drain R/O in a **1.7 centimeter long column**, with **full in-pixel electronics**
☑

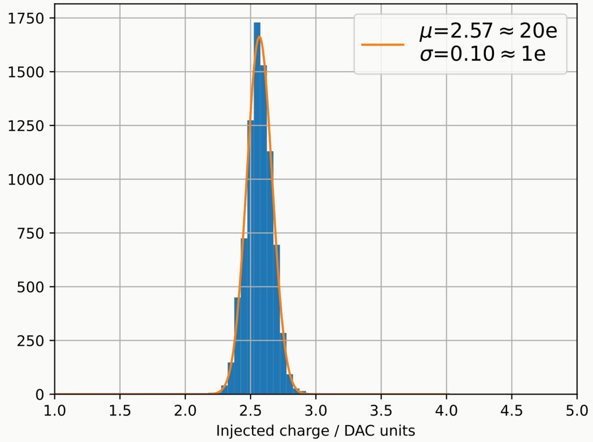
Modified front-end to reduce RTS tail in ENC
→ Lower minimum threshold
☑

TJ-MONOPIX2: FRONT-END ENC AND TUNING

Front-end with larger transistor size

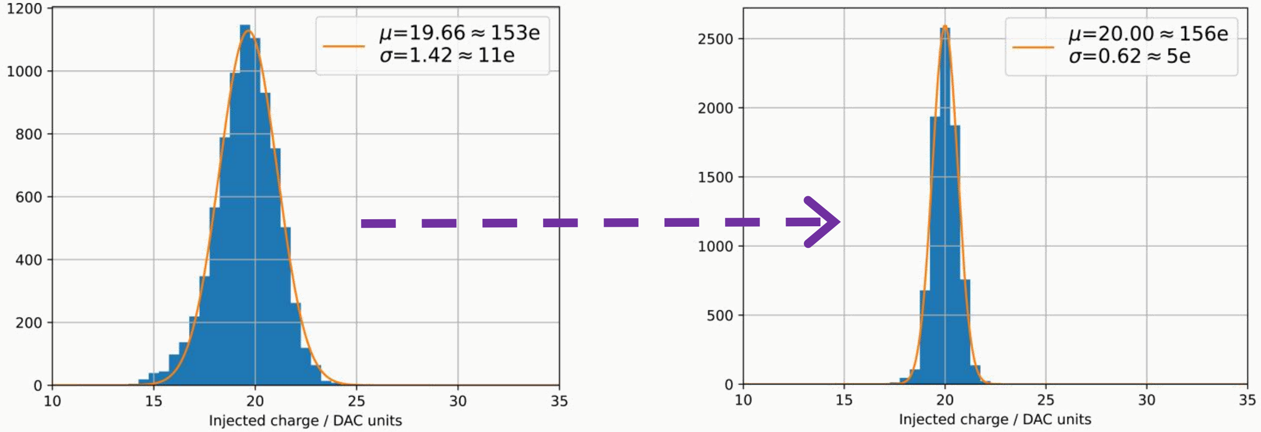
- Increase gain
- Normally-distributed ENC





Improved thresold distibution

- Mean value of ~150e⁻
- Dispersion reduced by half after tuning



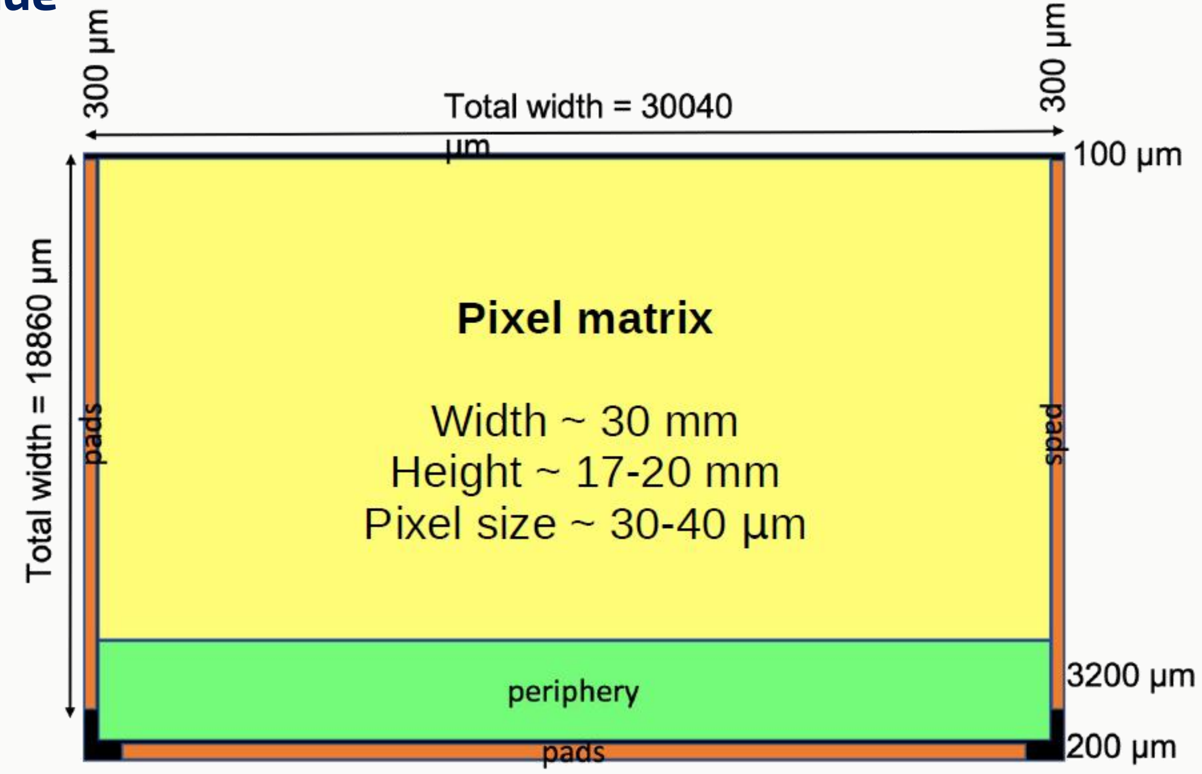
Bespin et al. https://doi.org/10.1016/j.nima.2022.167189

OBELIX

Proposed DMAPS design for the BELLE2 VTX Upgrade

Based on the design of TJ-Monopix2

- Increased matrix size 3x2 cm^2
- Larger pixel pitch ~40 µm
- 7-bit ToT information
- Integrate trigger logic and data formatting circuitry
- Shorter "time window" than current PXD:
  - 40 MHz clock
  - Consider 4 clock cycles around trigger
- Improve powering scheme for optimized distribution across larger matrix



Joint design between:

U. Bergamo, Bonn, Dortmund, CPPM-Marseille, INFN-Pavia, IPHC-Strasbourg, IFIC-CSIC-UV-Valencia, HEPHY-Vienna.

PERFORMANCE OVERVIEW

	LF-Monopix1	LF-Monopix2	TJ-Monopix1	TJ-Monopix2
CMOS process	LFoundry 150 nm		Tower 180 nm	
DMAPS type	Large collection electrode		Small collection electrode	
P-type substrate	CZ (>2 kΩ-cm)		Epi-layer (~1 kΩ-cm) | CZ (>1 kΩ-cm)	
Signal MPV [ke$^-$]	6 (85 µm)		Epi: 2 (30 µm) | CZ: >2 (>30 µm)	
Pixel pitch [µm^2]	250 x 50	150 x 50	36 x 40	33 x 33
Column length [mm]	6.5	17	8	17
Analog power [µW/pixel (mW/cm^2)]	~50 (400)	~30 (400)	~1 (90)	~1 (90)
ENC [e$^-$]	150-200	90-130	~20 + RTS noise	20 (expect: 10-15)
TH. minimum [e$^-$]	1500	1000	350	150 (expect: 100)
TH. Dispersion [e$^-$]	600-1000 → (T) 100	450-900 → (T) 100	35	10 → (T) 5
Max. Bias Voltage [V]	~270	~460	50	50
Irrad Level **Hit (in-time) Efficiency [%]**	NIEL, 1x10^{15} N_{eq}/cm^2 [TH~2.3 ke$^-$] 99.4 (~97)	Unirradiated [TH~2 ke-] 99.6 (>99)	NIEL, 1x10^{15} N_{eq}/cm^2 [500 e$^-$] Epi: 87.1 | CZ: 98.6	TBA soon... (expect: >99)

CONCLUSIONS & OUTLOOK

LF- and TJ- Monopix:

- DMAPS in large and small electrode designs
- Fully functional column-drain read-out architecture at a reticle-size scale
- All signal processing and R/O electronics placed within the pixel volume
- Radiation-hard up to the requirements of current and future HEP experiments

- **LF-Monopix2 outlook:**
  - Test beam (Nov. 2022) for proton irradiated samples ($1\text{x}10^{15}$ N_{eq}/cm^2)
- **TJ-Monopix2 outlook:**
  - Test beam (Nov. 2022) for unirradiated samples
  - Planned neutron irradiation in JSI-Lubljana up to $5\text{x}10^{14}$ N_{eq}/cm^2, and test beams in Spring 2023.
  - Test of new back-side processed wafers → Possible improvement in field uniformity
  - Design of a new application-specific chip for the BELLE2 VTX Upgrade

Thank you for your attention

Questions?

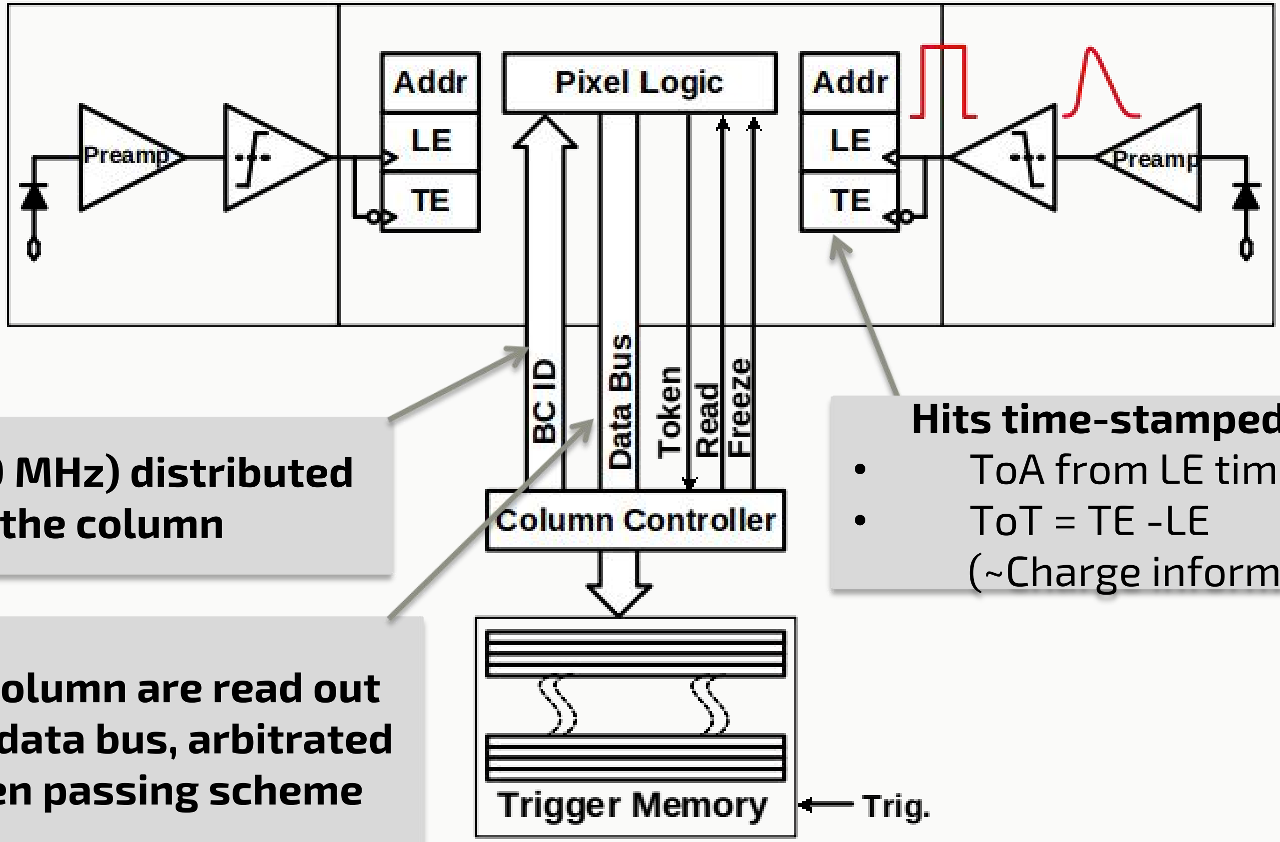
This project has received funding from the Deutsche Forschungsgemeinschaft DFG (grant WE 976/4-1), the German Federal Ministry of Education and Research BMBF (grant 05H21PDRD1) and the European Union's Horizon 2020 Research and Innovation programme under grant agreements No. 675587 (STREAM), 654168 (AIDA-2020) and 101004761 (AIDA-Innova).

The measurements leading to these results have partially been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF) and the E3 beam-line at the electron accelerator ELSA operated by the university of Bonn.

Backup slides…

COLUMN-DRAIN R/O ARCHITECTURE

Why? Sufficient rate capability with affordable in-pixel logic density for CMOS pixels



BC ID (40 MHz) distributed in the column

Hits in the column are read out on a shared data bus, arbitrated by the token passing scheme

Hits time-stamped in pixel
- ToA from LE time stamp
- ToT = TE -LE (~Charge information)

Column-drain has already proven to be capable to handle the hit rates of the current inner ATLAS pixel layers (FE-I3)

☑

Simulation studies for the outmost HL-LHC pixel layers agree

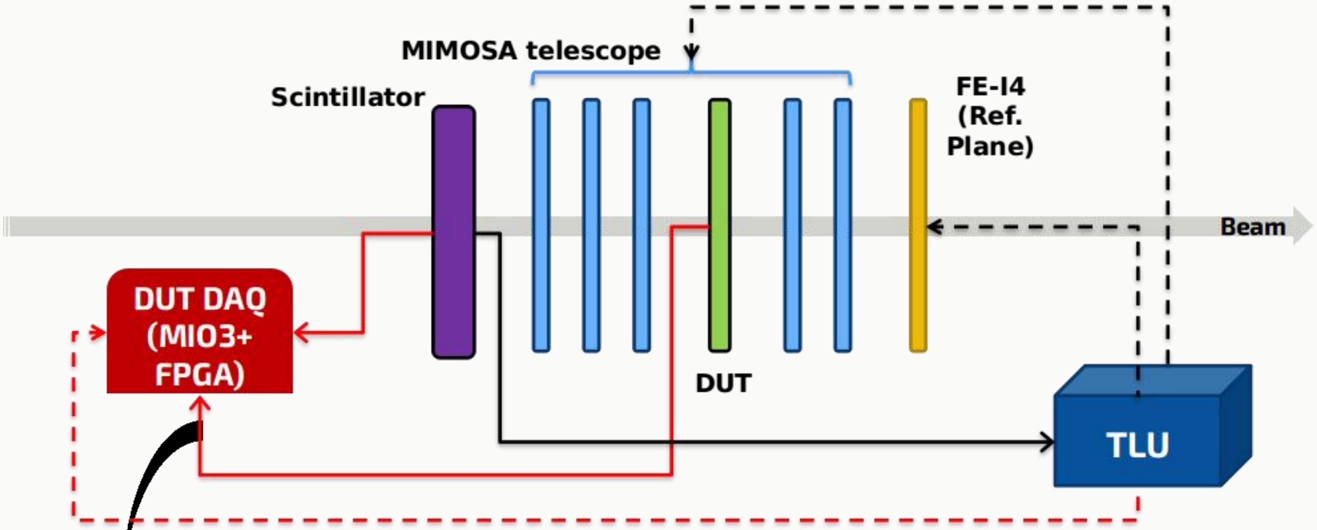
☑

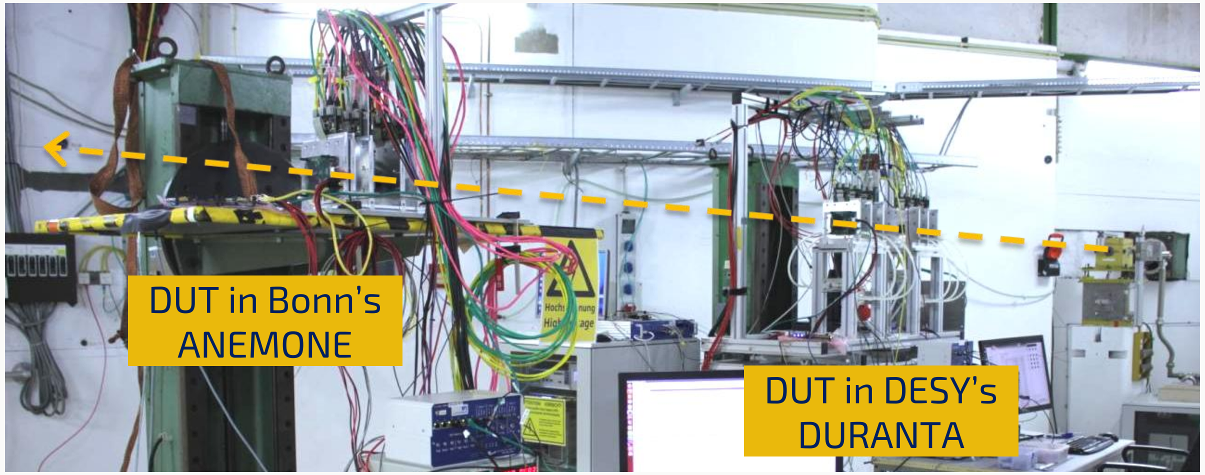
TB DATA ACQUISITION

Telescope setup:

- 1 LF/TJ-Monopix DUT
  (100 µm thickness)
- 5/6 MIMOSA26 tracking planes
- 1 FE-I4 timing reference plane.
- Triggered by a plastic scintillator.

Beam: ELSA (2.5 GeV e^-) or DESY (5 GeV e^-)





Scintillator and TLU timestamps sampled with a **640 MHz** clock in the MIO3 FPGA.

TB data analysis carried out using Bonn's BTA:

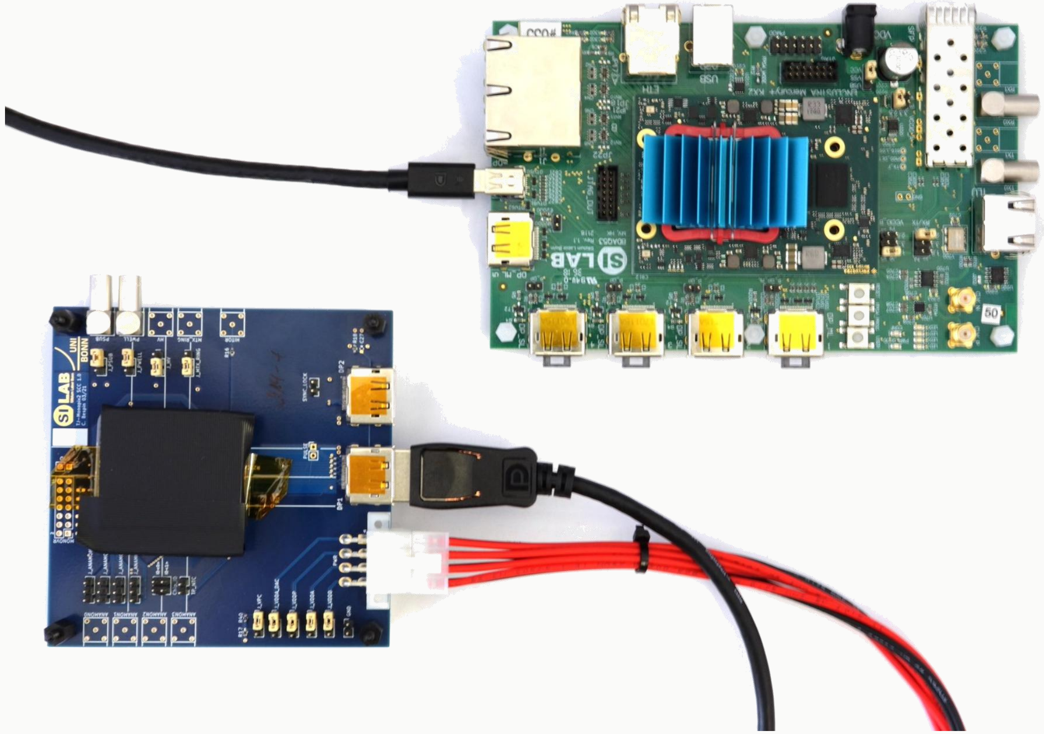
https://github.com/SiLab-Bonn/beam_telescope_analysis

TJ-MONOPIX2: READ-OUT SYSTEM

DAQ System based on the bdaq53 (RD-53A/B testing) readout board

https://gitlab.cern.ch/silab/bdaq53/-/wikis/home

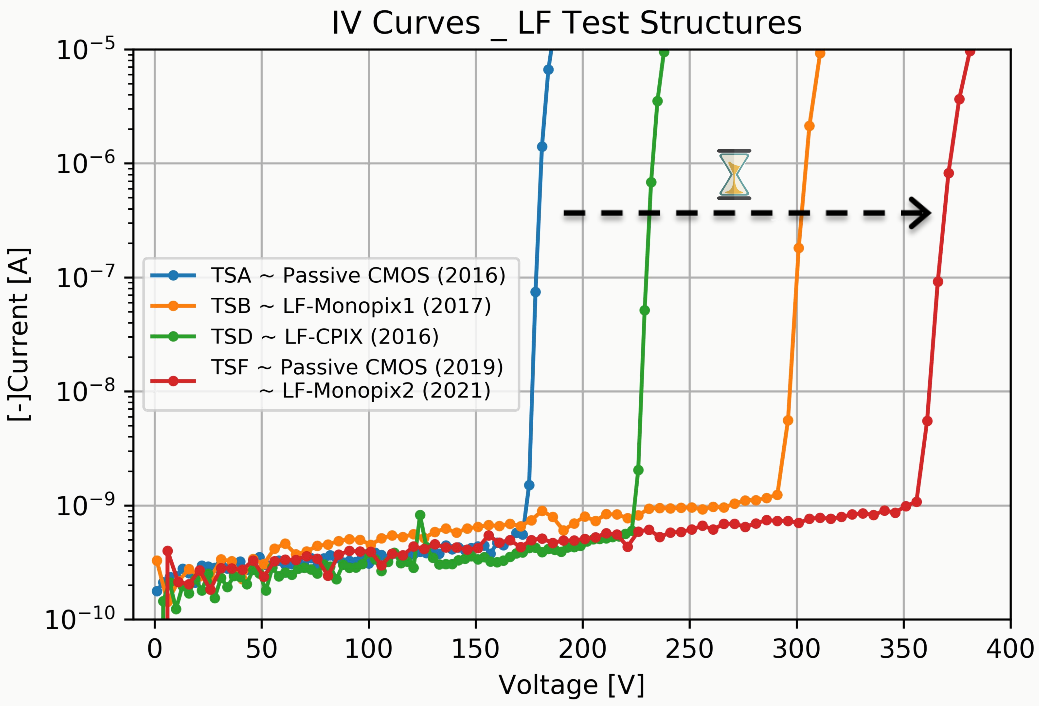
- „Standalone" DUT carrier PCB connected with DP cable to readout board
- Suited to handle all of TJ-Monopix2 LVDS I/O lines
  - Custom board for Kintex 7 series FPGA
- Readout board connected to PC with 1 Gbit/s ethernet
- Portable setup for irradiations, beam test, etc



BREAKDOWN IMPROVEMENT IN LFOUNDRY SENSORS

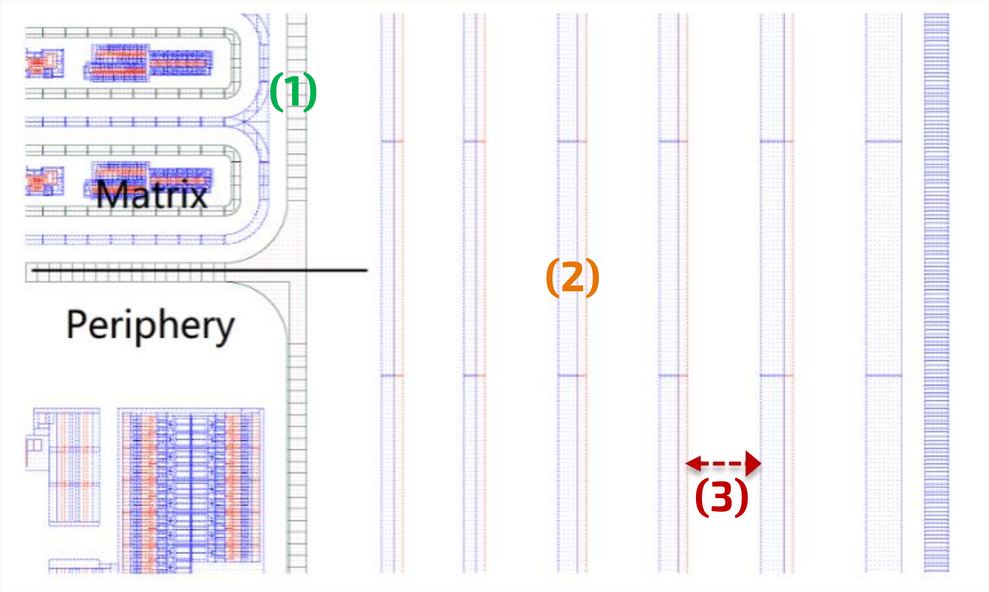
We are able to deplete large volumes in the LF-Monopix and LF Passive CMOS sensors:

HR substrate + <u>Large breakdown voltages</u>



Improvement of breakdown voltage achieved by:

- Adding Deep N-well on innermost n-ring **(1)**
- P+N combination in guard-rings **(2)**
- Reduction of guard-ring number -> Increase in spacing **(3)**

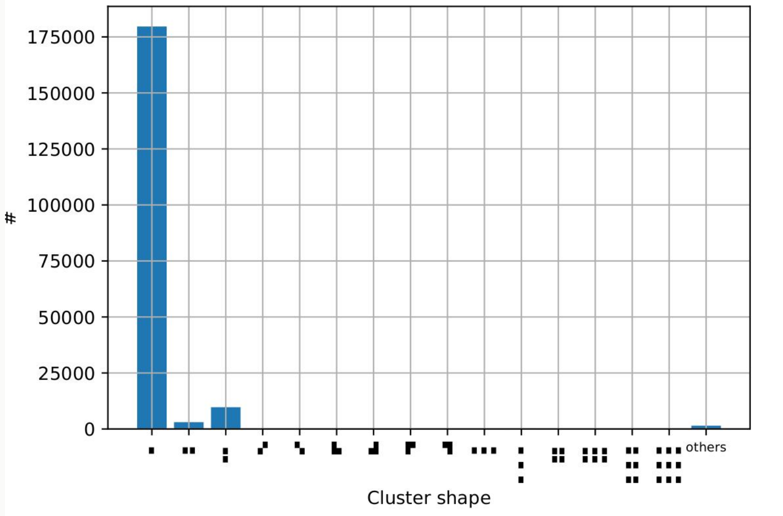


What to try next?...

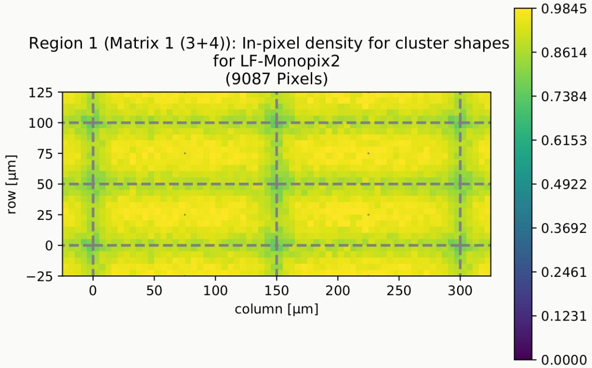
LF-MONOPIX2 TEST BEAM: QUALITY CHECK

Cluster size distributions

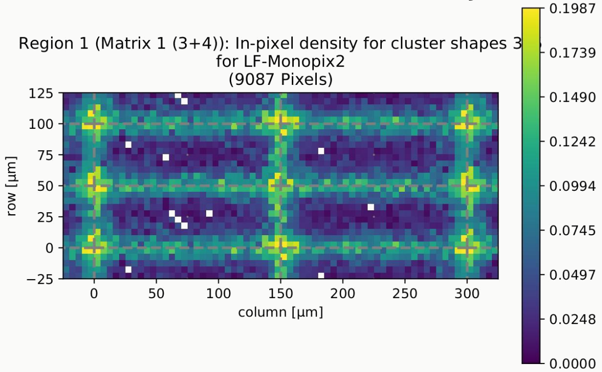
(Depleted 100 µm thick sensor)



Cluster size 1 density



Cluster size 2 &3 density



Residual distributions