CMS Inner Tracker status and performance

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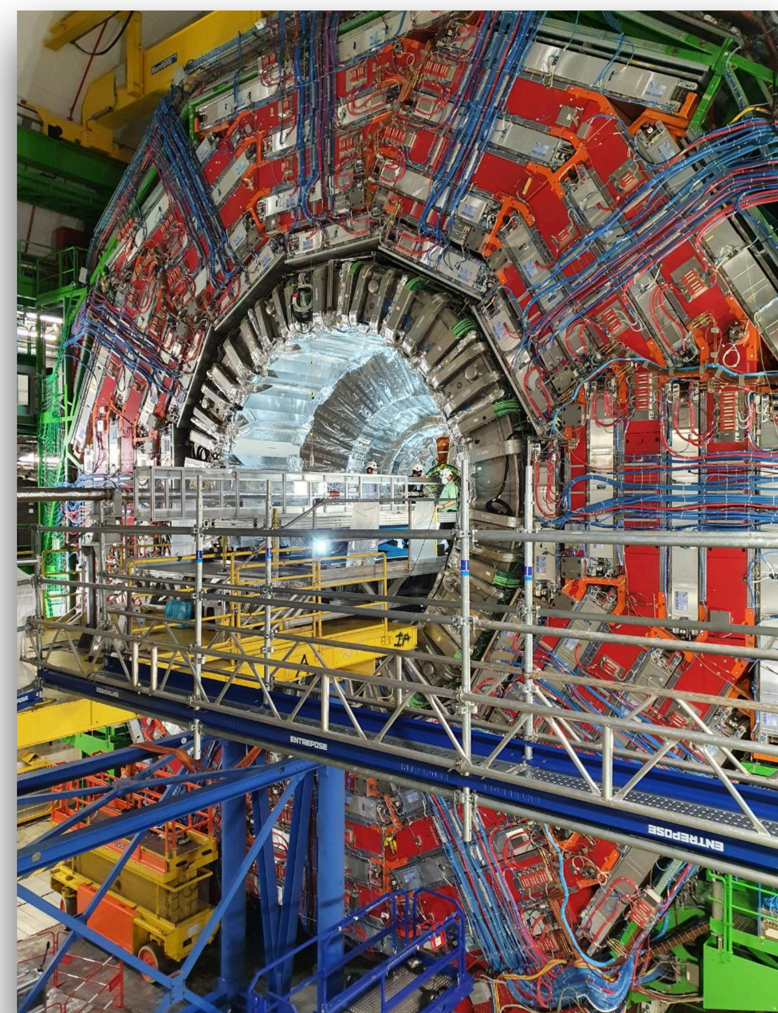
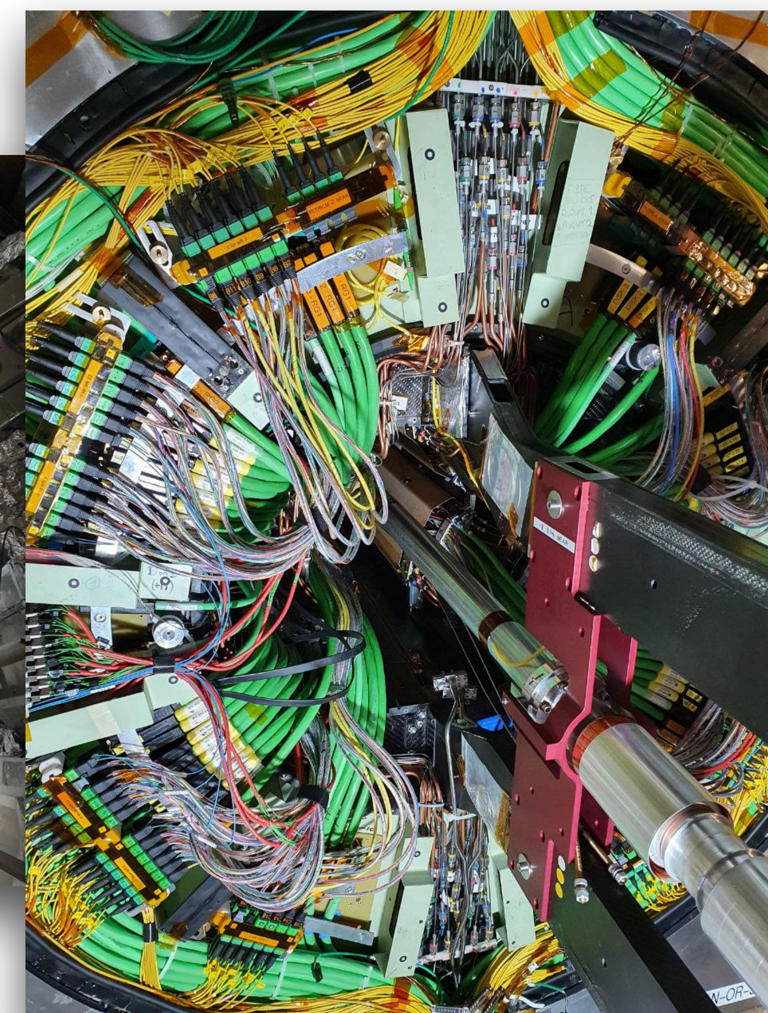
on behalf of the CMS Collaboration

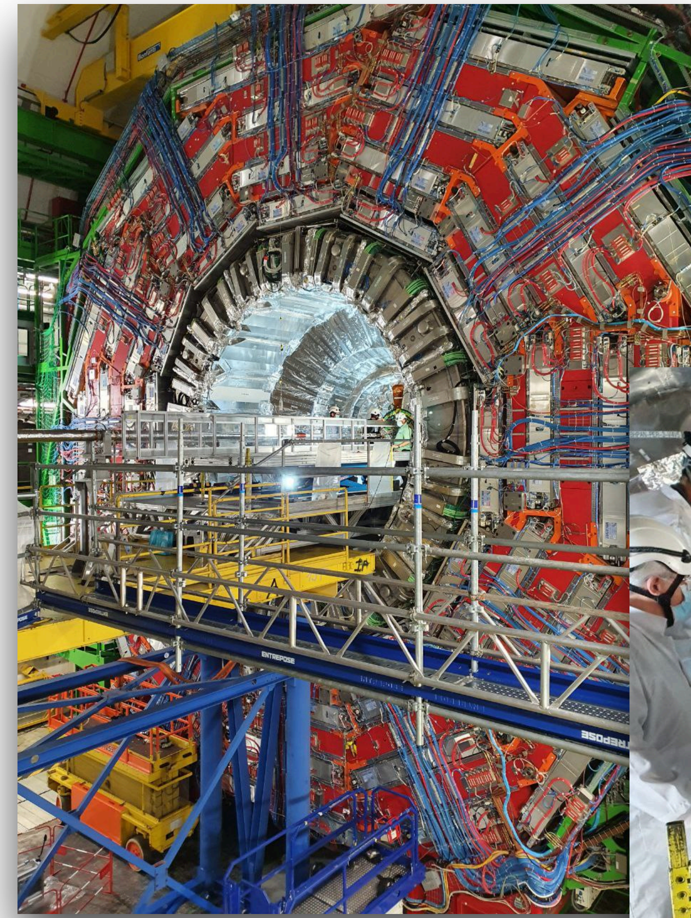
VERTEX 2022
24 October 2022

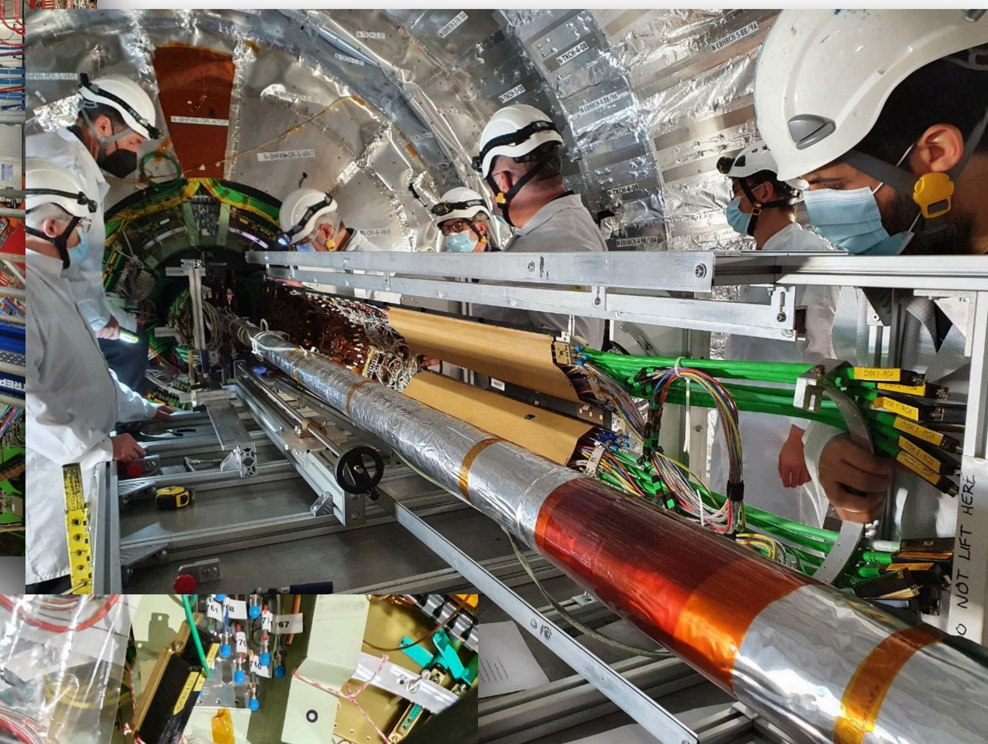




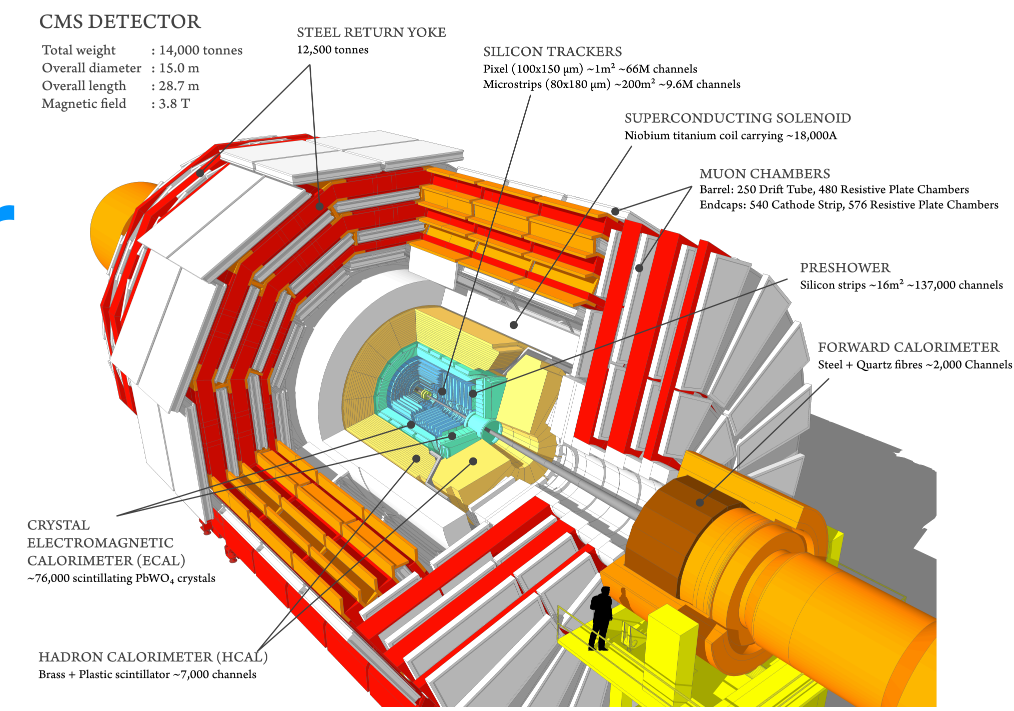
Overview

- **CMS Pixel detector**
- **LS2 activities:**
  - refurbishment
  - installation
  - commissioning
  - Pilot Beam test
- **Start of Run 3:**
  - 900 GeV collisions
  - 13.6 TeV collisions
  - first performance



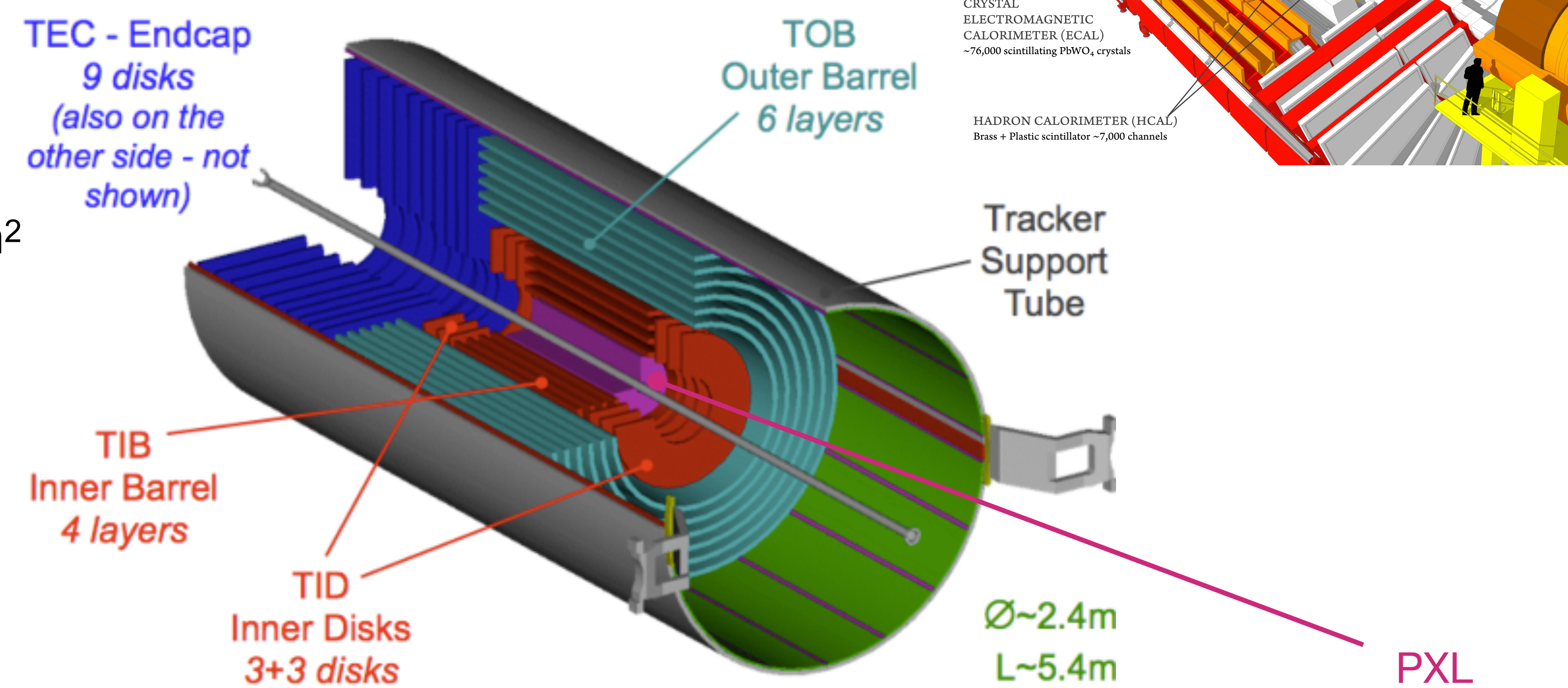


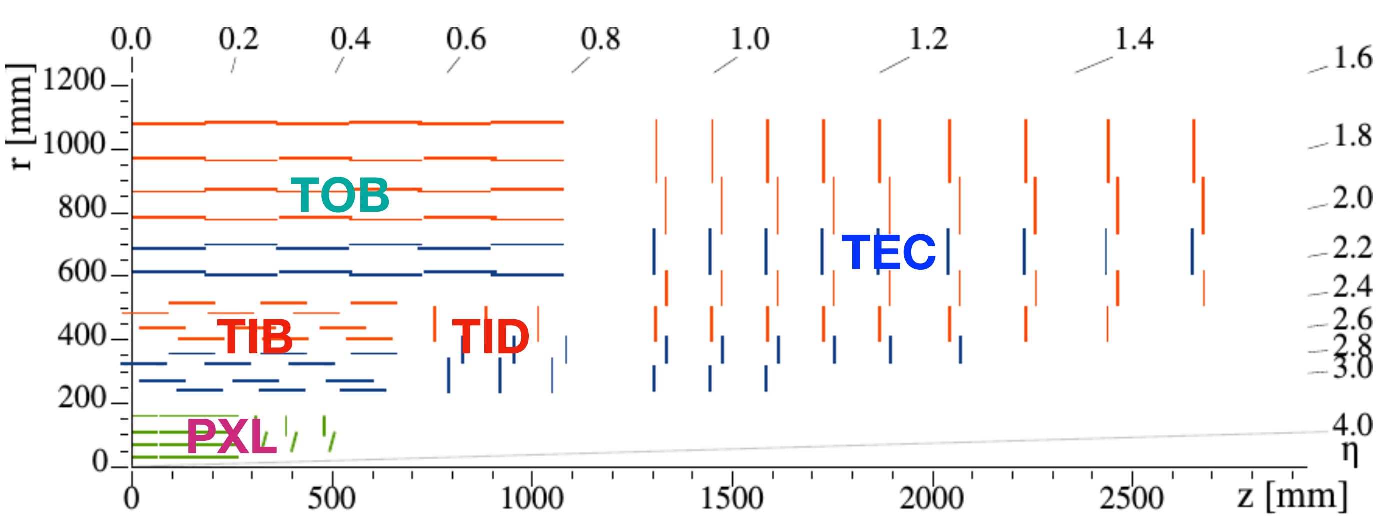
CMS Tracker detector

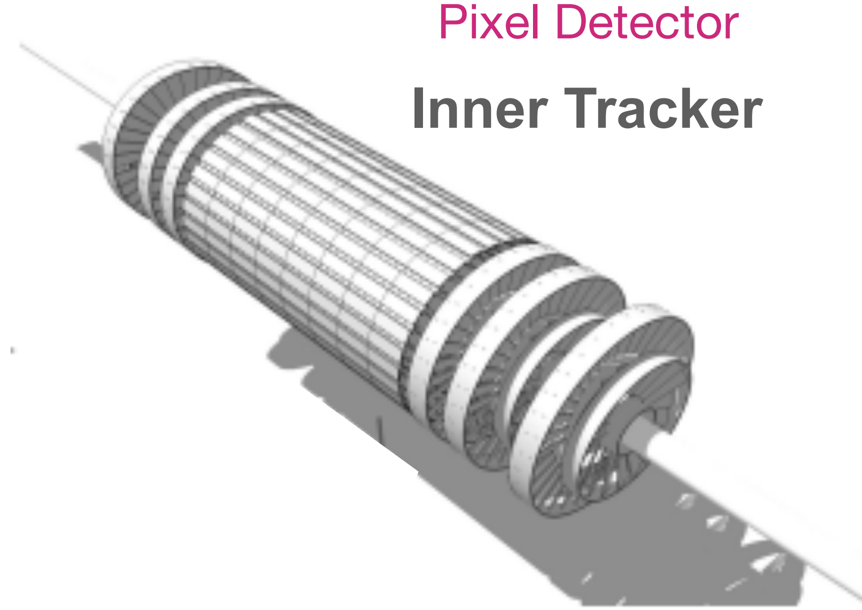


Outer Tracker = Strips Tracker

- TIB, TID, TOB, TEC
- active material ~200 m^2
- ~10M electronic channels
- see [Suvankar's talk]() for details



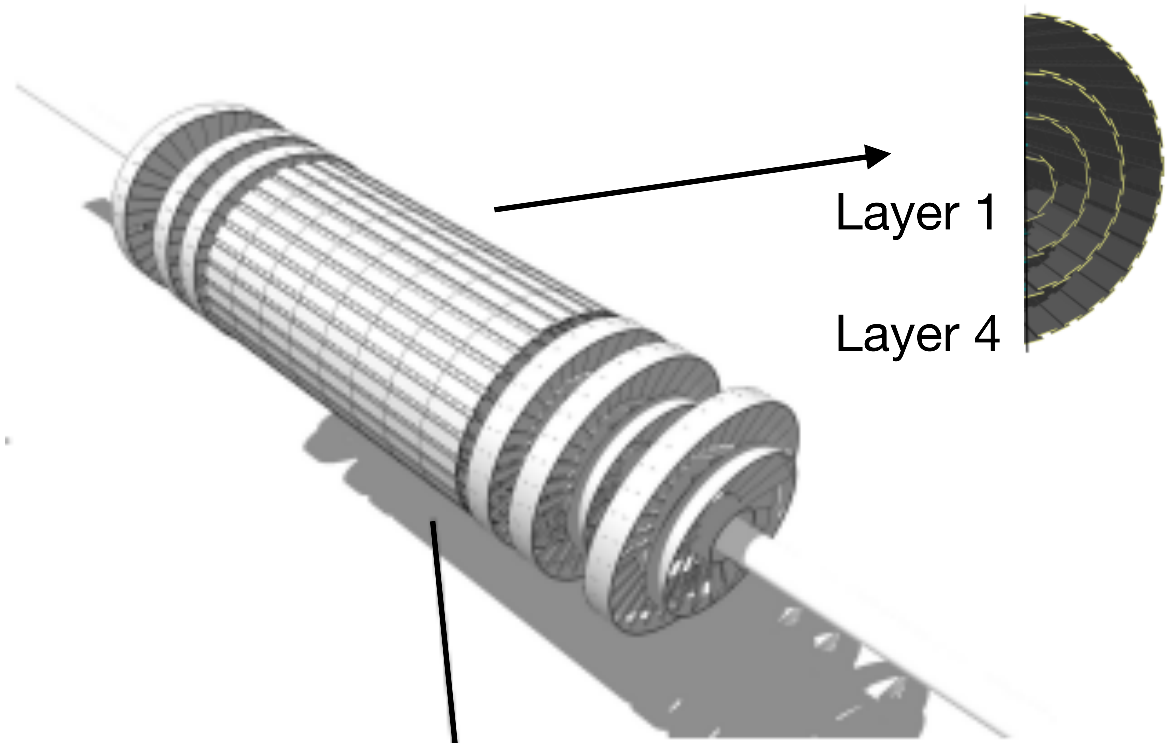


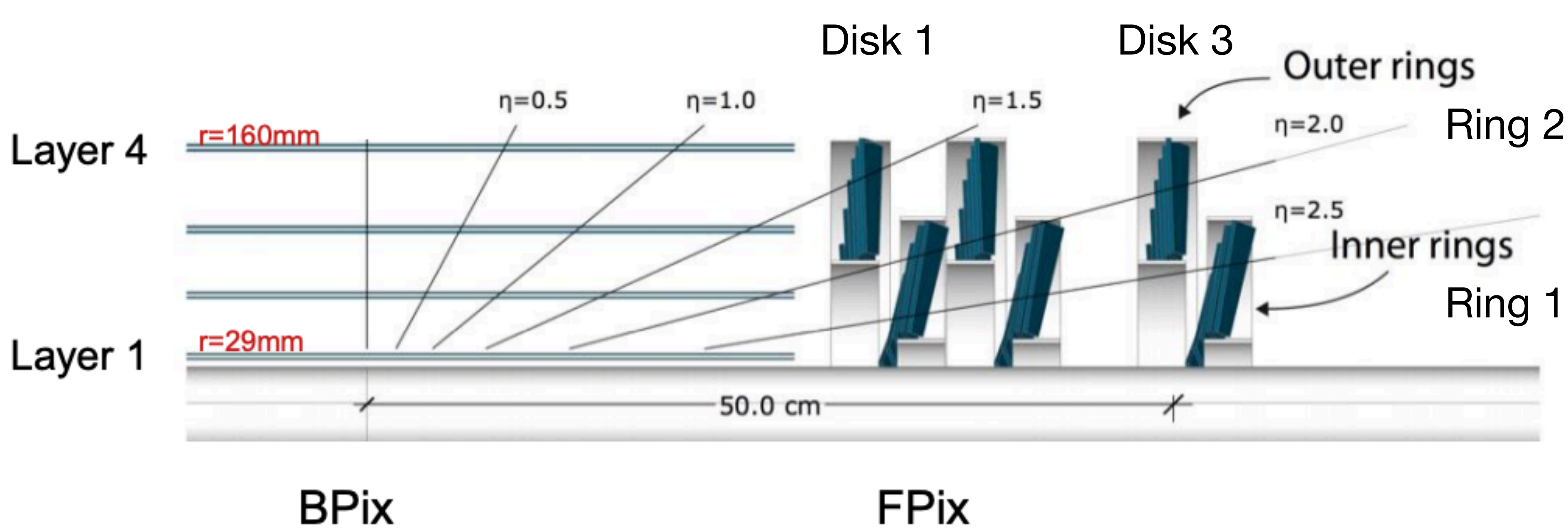


Inner Tracker

Pixel Phase-1 detector

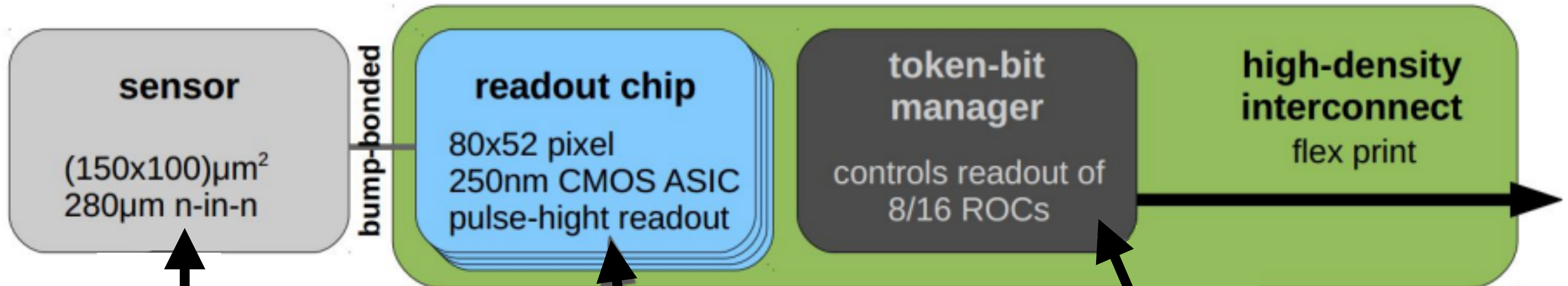
- Installed in winter 2016-2017
- ~124M channels in ~1.9 m^2
- 4 hit coverage up to η = 3
- **Barrel Pixel (BPix): 4 layers**
- **Forward Pixel (FPix): 3 disks * 2 rings**





Pixel modules

All components suited for high integrated and instantaneous luminosities

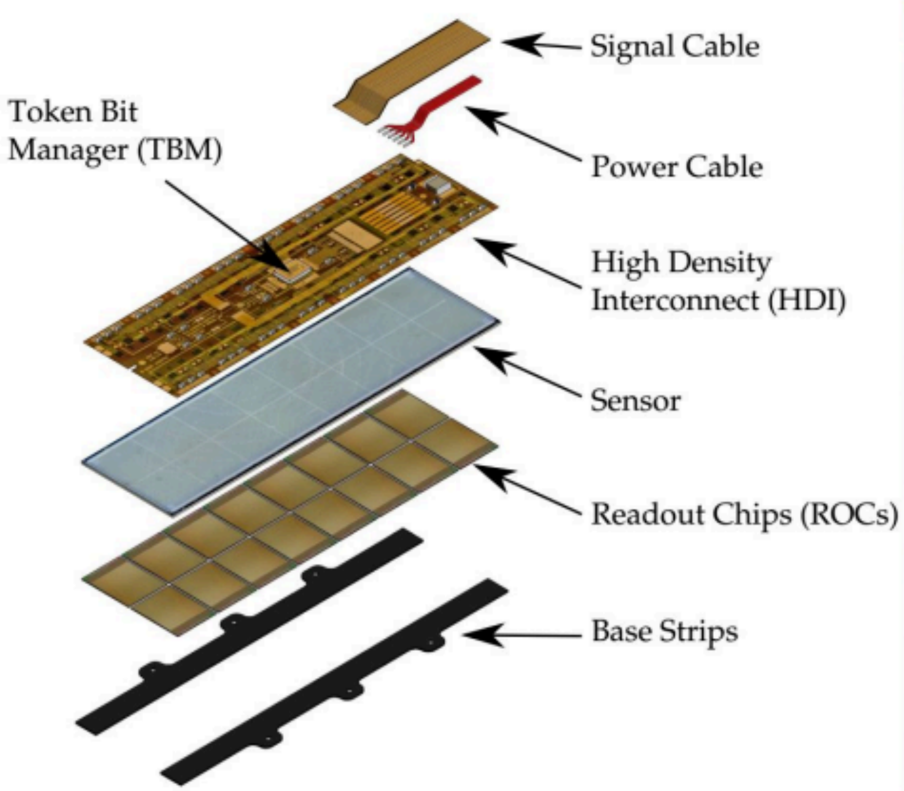


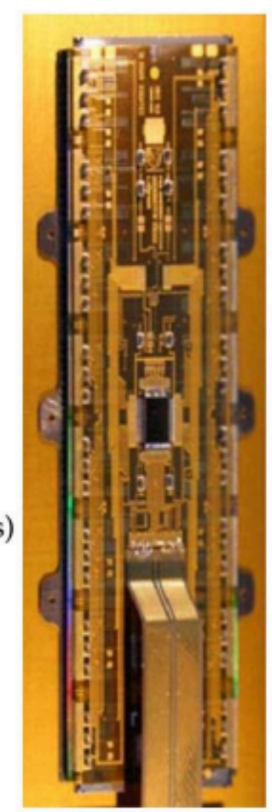
Unchanged compared to Phase-0 detector (2009-2016)

- **New digital TBM** with 160Mbit/s digital coding
- Old TBM: 40MHz analog coding
- Module out-bound data stream: 400Mbit/s

- **PSI46dig**
  - same architecture as Phase 0
  - digital readout and double column drain
  - >90% efficiency up to 400MHz hit rate

- **PROC600**
  - dedicated for Layer 1
  - dynamic cluster drain
  - >90% efficiency up to 600MHz hit rate



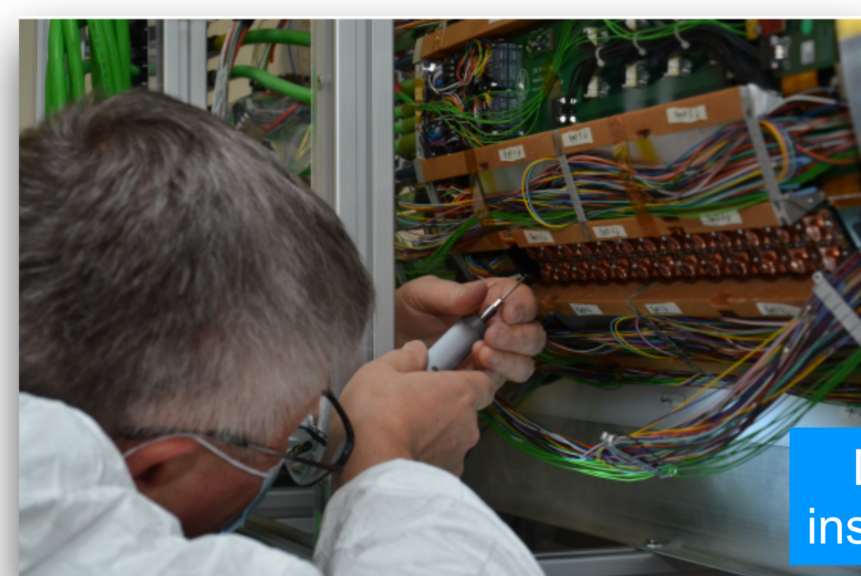


Refurbishment during LS2

- **Detector was extracted from underground cavern** at the end of Run 2 (early 2019)
  - **kept cold and dry** in boxes to protect the silicon sensors

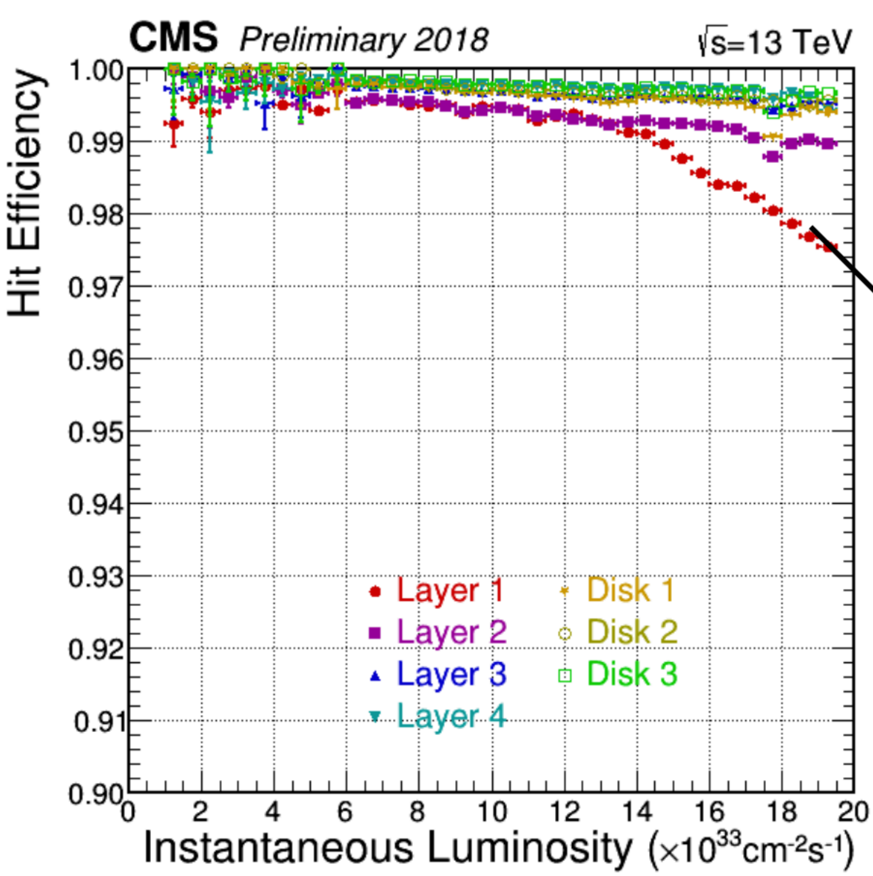
- **Refurbishment work during Long Shutdown 2 (LS2):**
  - install new Layer 1
  - replace accessible modules in Layer 2 damaged by HV ON / LV OFF condition in 2017 (DCDC-damaged modules)
  - install new DCDC converters in both BPix and FPix
  - consolidate FPix CO_2 cooling connection
  - replace FPix filter boards for better HV granularity
  - test detector in warm and cold temperatures in cleanroom

1/4 FPix in cold box

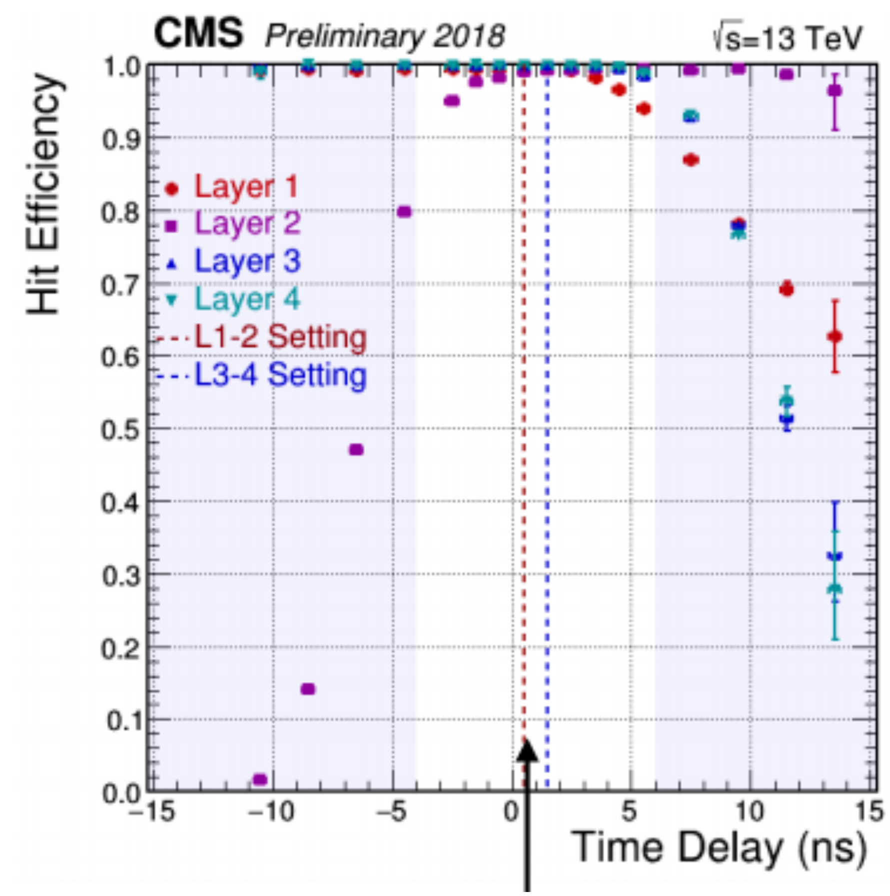

DCDC installation

New Layer 1

- We needed a new Layer 1 after Run 2.. so we made it better!
- **New readout chip (PROC600v4)**
  - fix dynamic inefficiency issue
  - reduce crosstalk noise
- **New Token-Bit-Manager (TBM10d)** with delay and power reset option
- **New HDI design** to eliminate HV issues



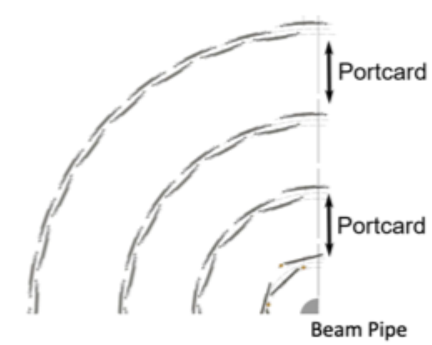
Dynamic inefficiency addressed in new ROC



Optimal range very narrow and efficiency on the edge for Layer 1+2

New TBM10d allows a relative delay of Layer 1 w.r.t. Layer 2

In old modules, 1 common setting for Layer 1 and Layer 2 because they shared same delay chip (portcard)

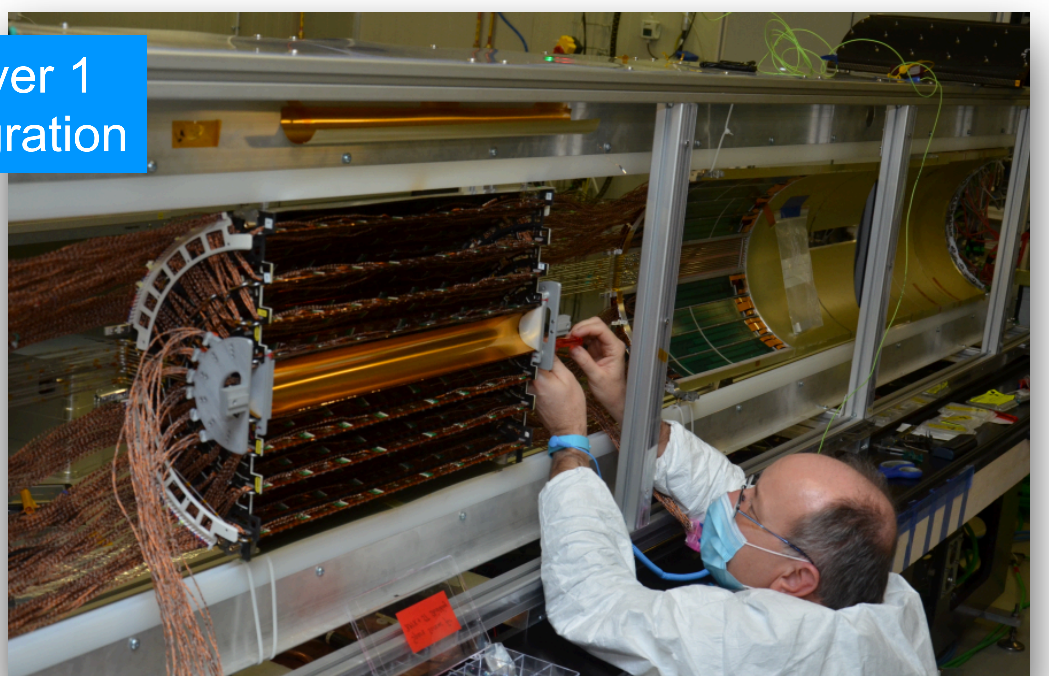


Layer 1 and 2 work

- **Installed new Layer 1 modules:**
  - delivered to CERN at the end of October 2020, after work at PSI
  - tested after unpacking (post-transportation) at beginning of 2021
    - overall ~6 weeks of delay w.r.t. the original plan due to the Covid situation
  - integrated with all cabling and cooling connections
- **Replaced 8 (out of 10) modules in Layer 2 damaged by HV ON / LV OFF condition**
  - 2 not accessible (facing outwards)

Final work at PSI

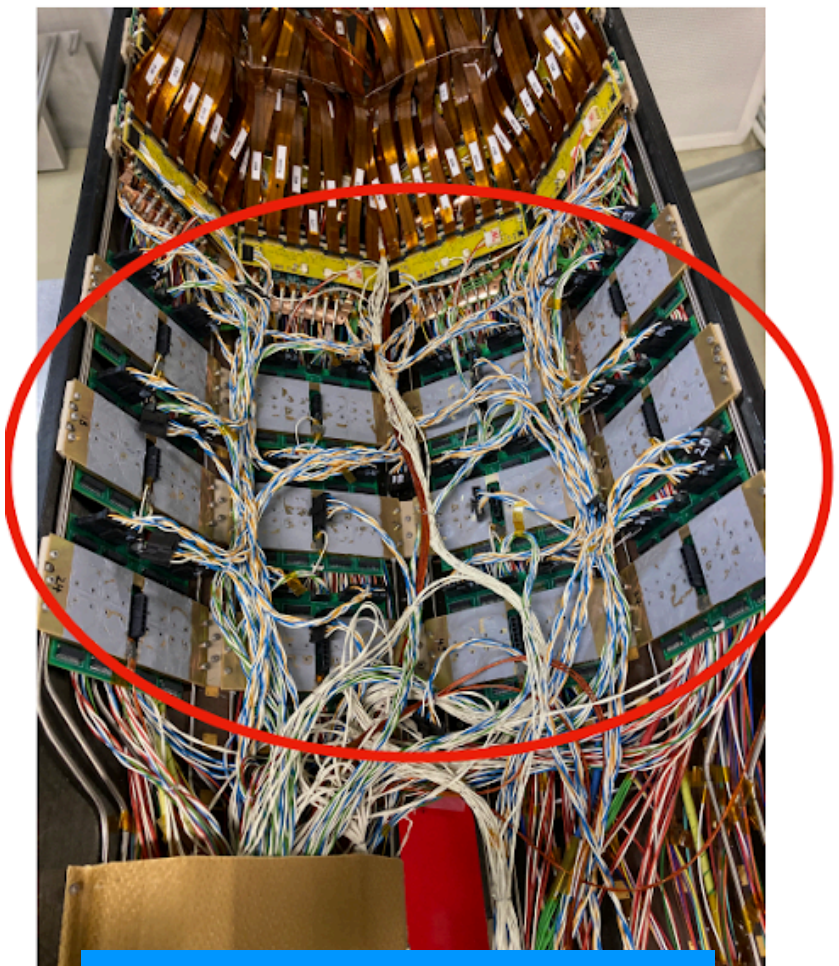
Delivery to P5



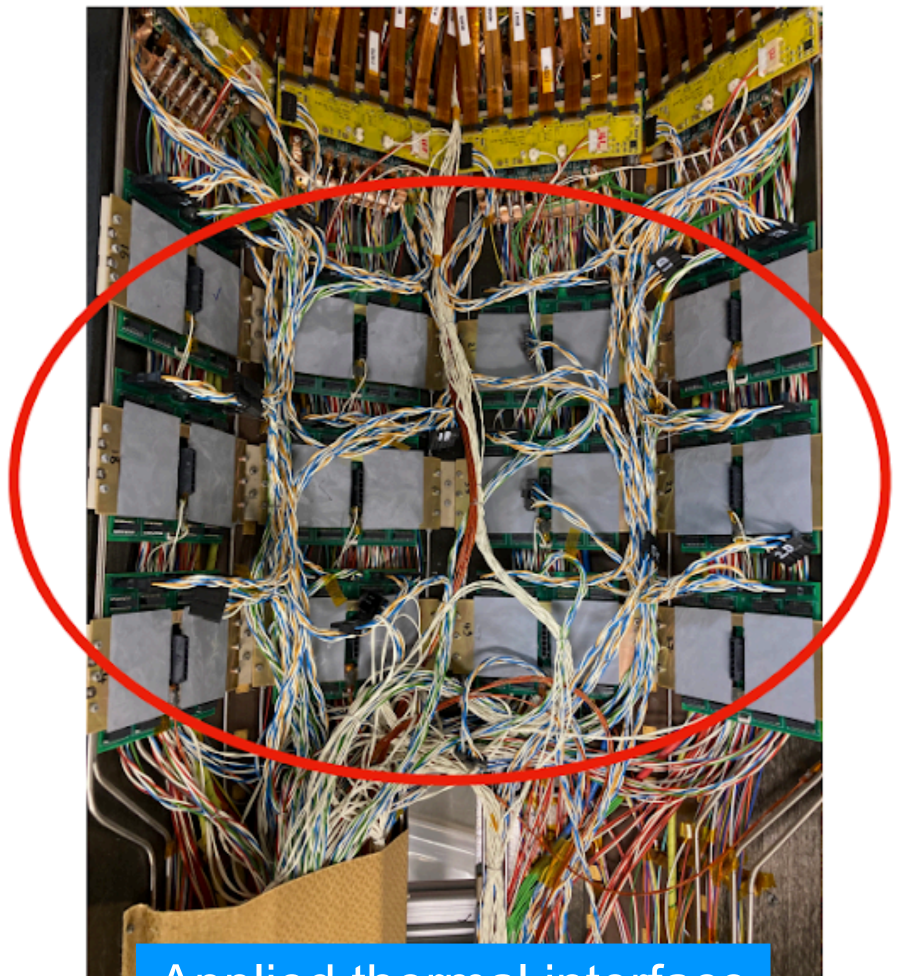
Layer 1 integration

Layer 1 cabling

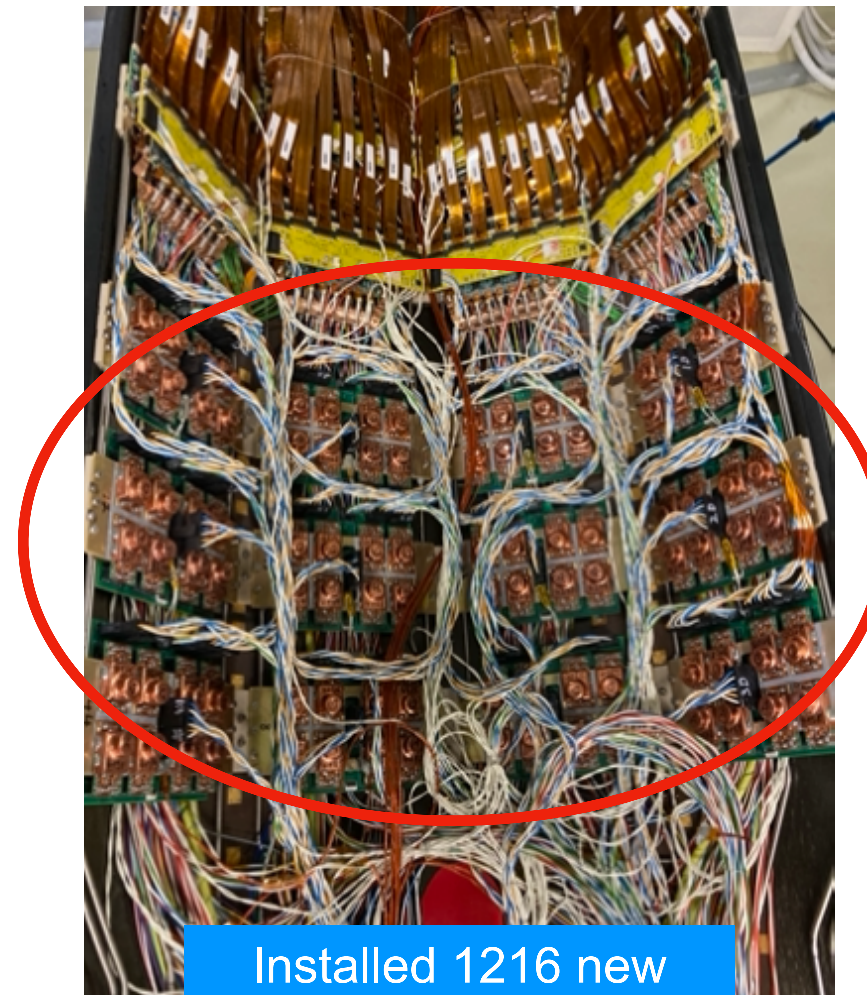
DCDCs replacement



Extracted old converters



Applied thermal interface film for better contact



Installed 1216 new DCDC converters for Run 3 detector

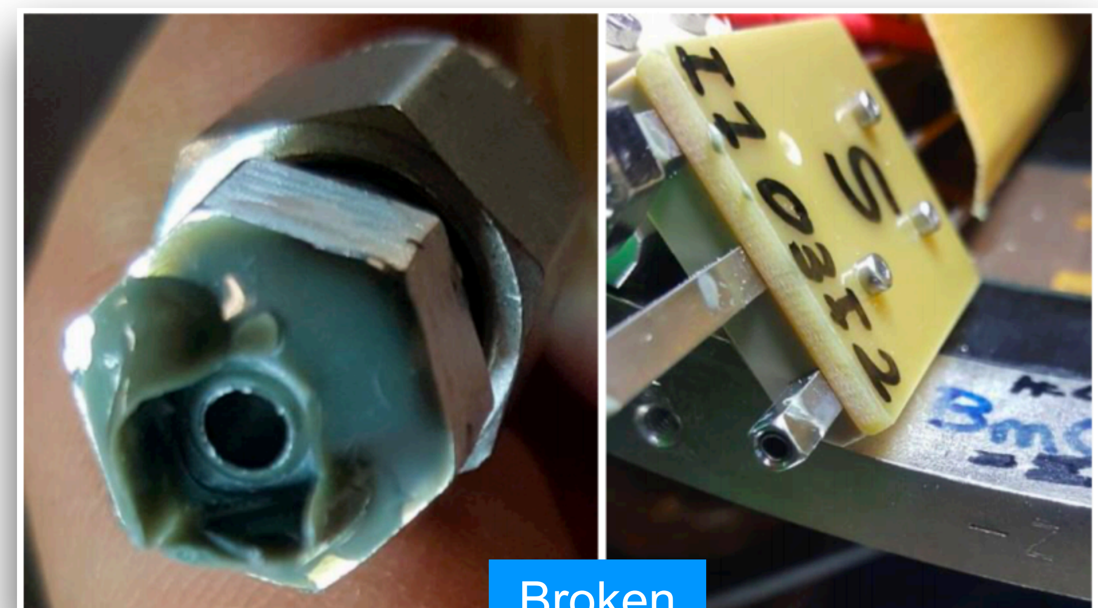
All DCDC converters have been replaced with the new production: revised ASIC (FEAST v2.3) to fix failure mechanism in disabled state

Type	Required
2.4 V (= Analog)	608
3.3 V (=Digital, BPix)	320
3.5 V (=Digital, FPix & BPix L2)	288

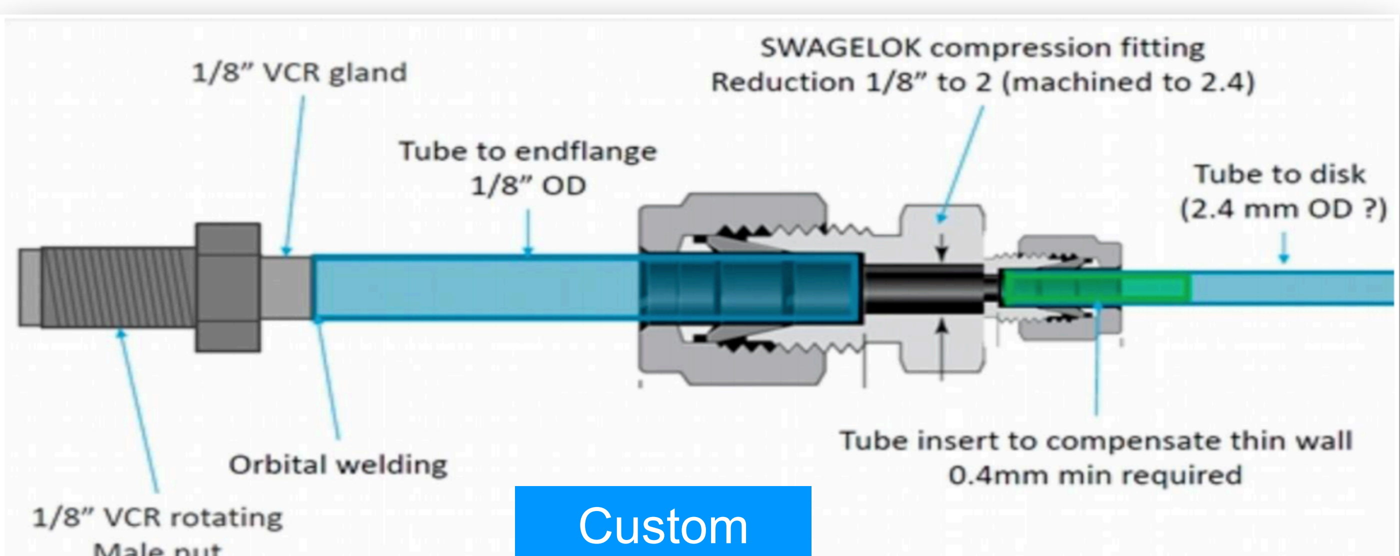
FPix cooling connections

- **Inlets with fixed nut directly welded to cooling pipes**
    - glue meant to reduce mechanical stress
    - minimal mechanical torque needed to break off the nut
- **High risk to damage the 24 connections during handling**
    - one broke during lab checkout
- **To ensure operational stability, introduced rotating nut and custom VCR fitting**

CO_2 cooling inlets

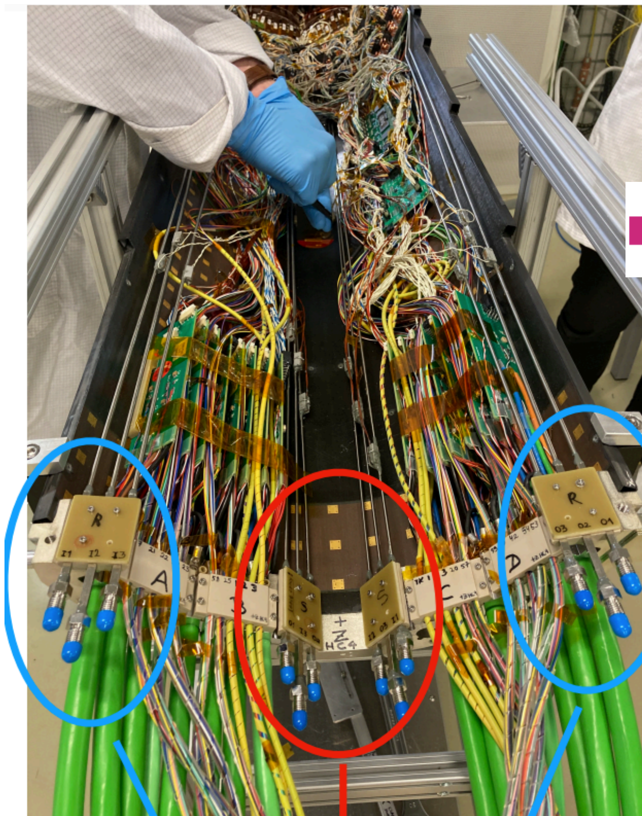


Broken inlet



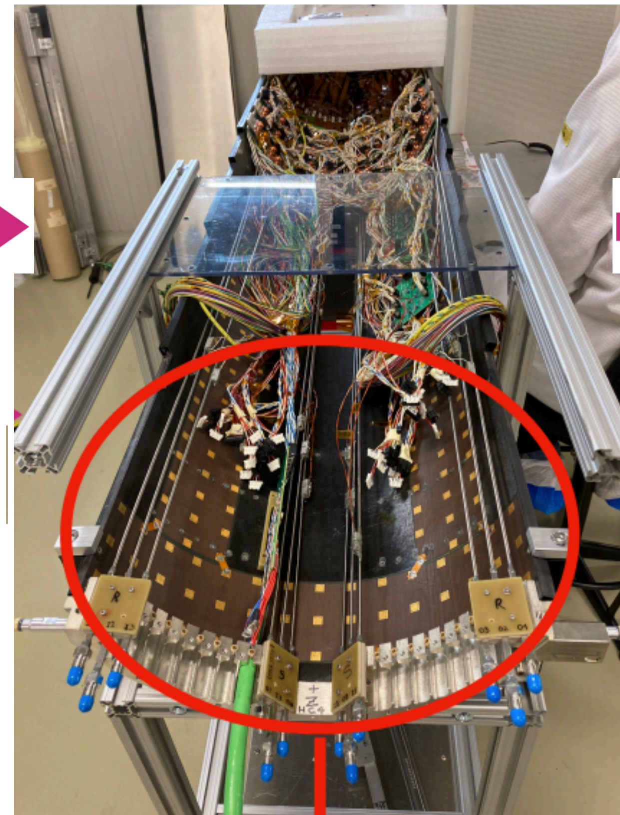
Custom VCR fitting solution

FPix cooling pipe repair

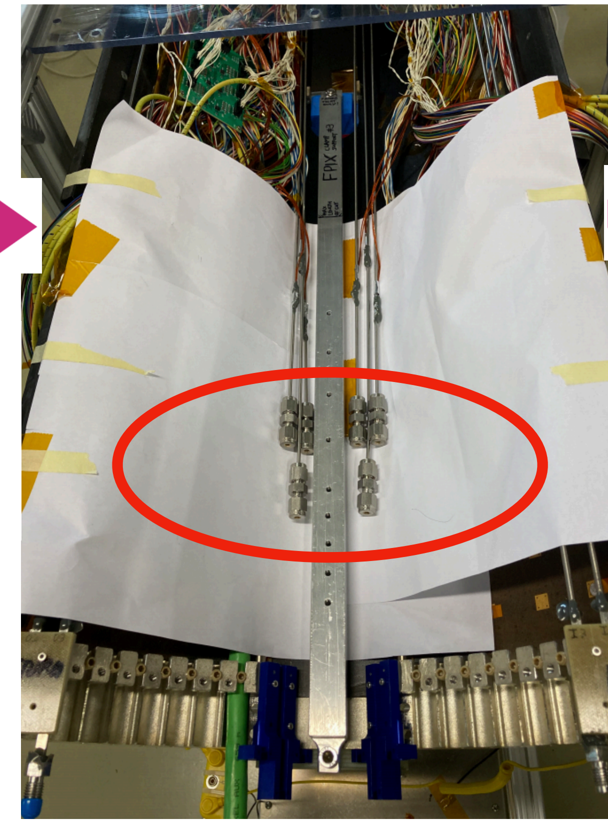


Cooling Inlets

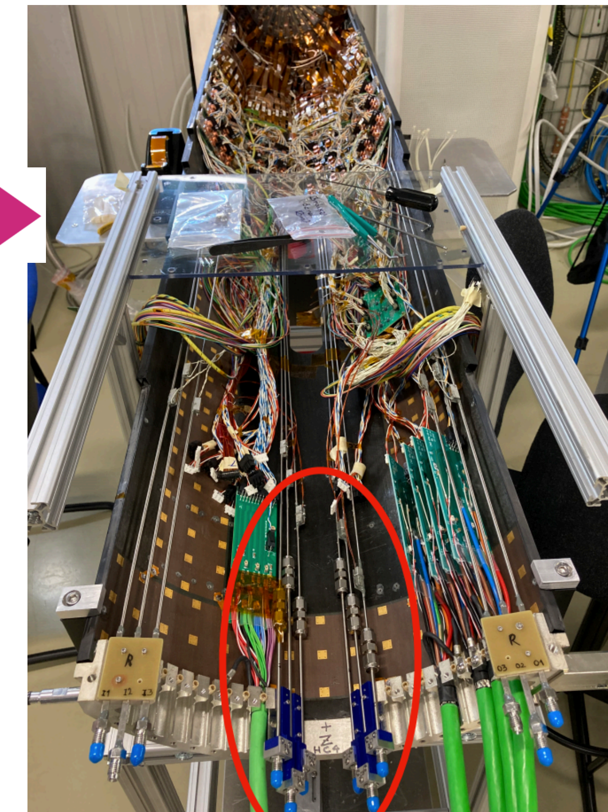
Cooling Outlets



removed old filter boards to clear area for cooling repair



cooling repair in progress with custom VCR fittings

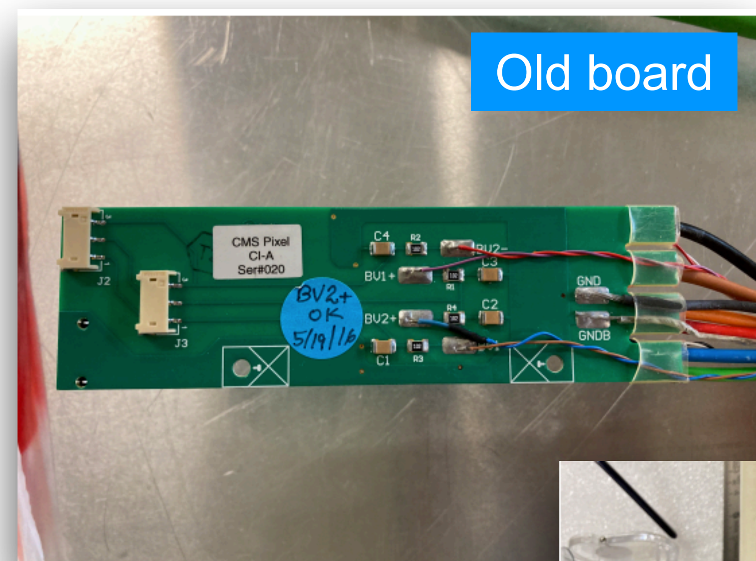


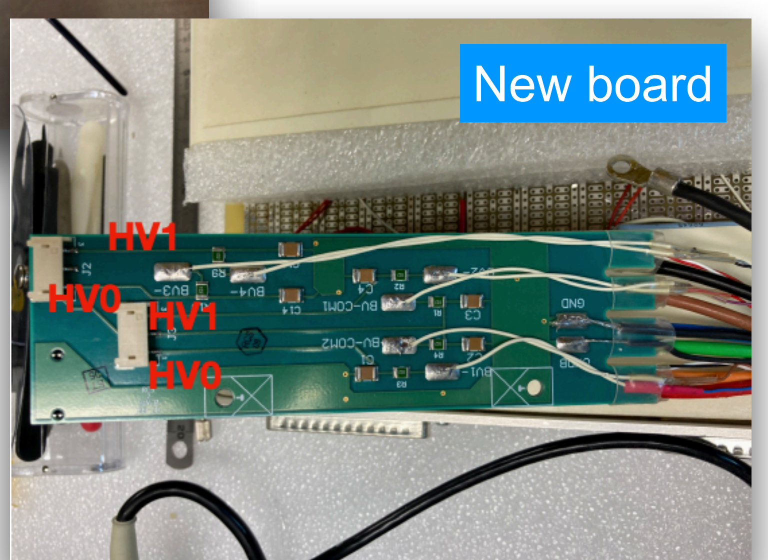
repair done with newly installed supply inlets with redesigned mounts

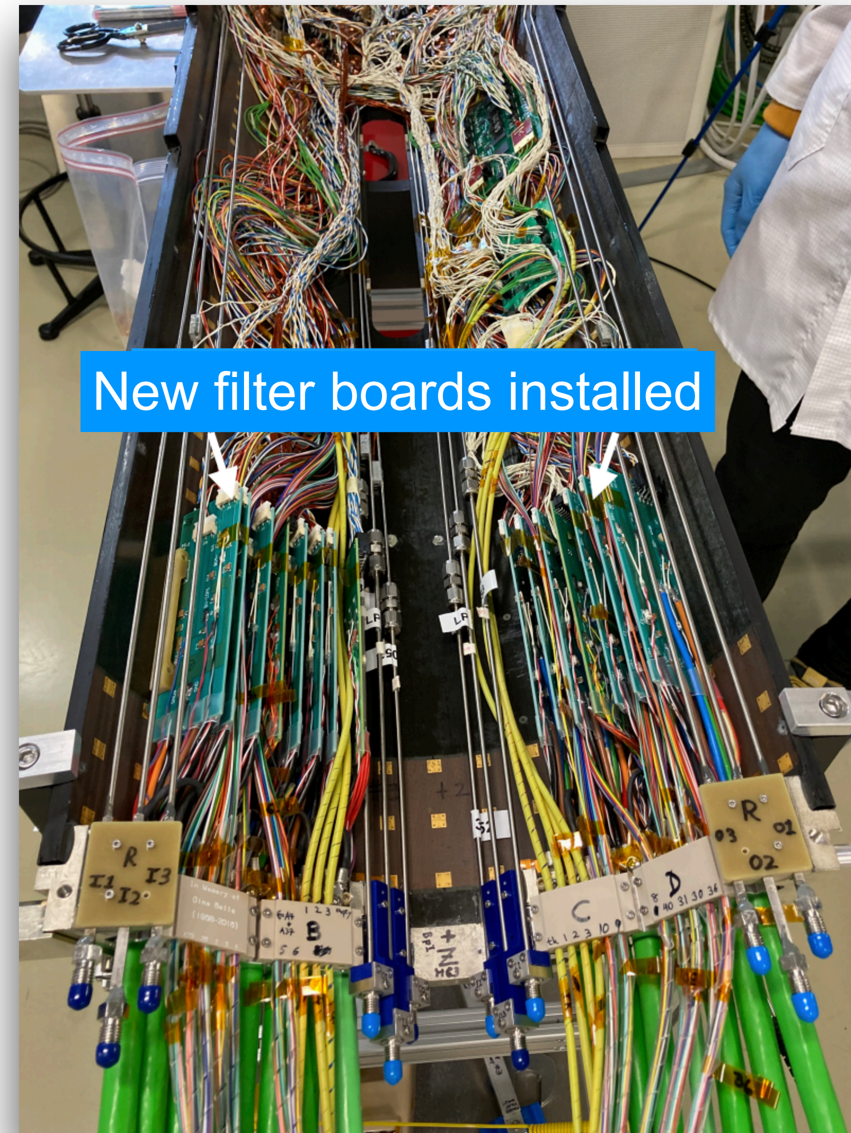
All cooling inlets have been refitted with custom Swagelok fitting and new mounts for the supply lines with rotating nut for strain relief

FPix filter board replacement

- **New filter boards have 4 independent HV lines (instead of 2) per power group to improve HV granularity**
- Tested 4 HV lines up to 800 V and common ground



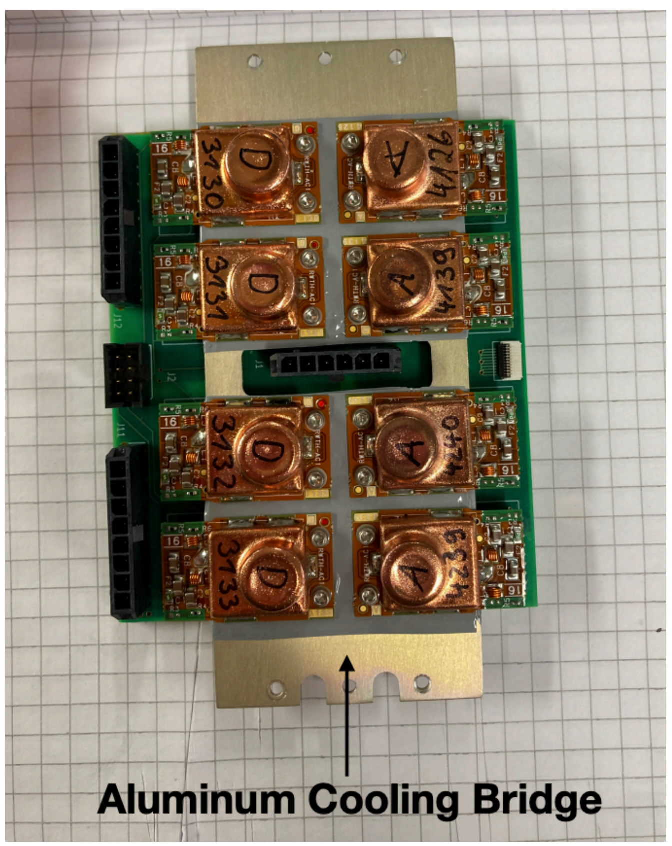


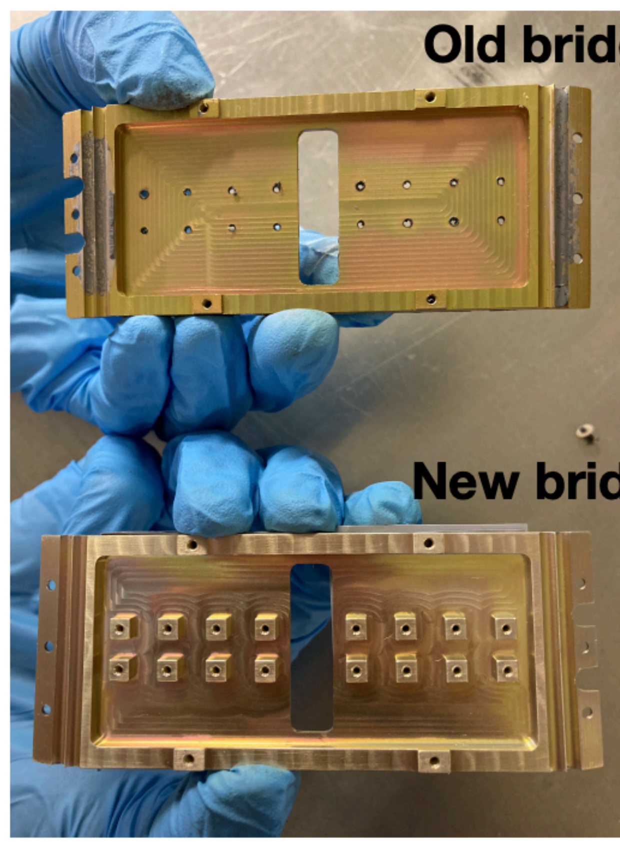


12 module power filter boards per 1/4 FPix

Other FPix refurbishment

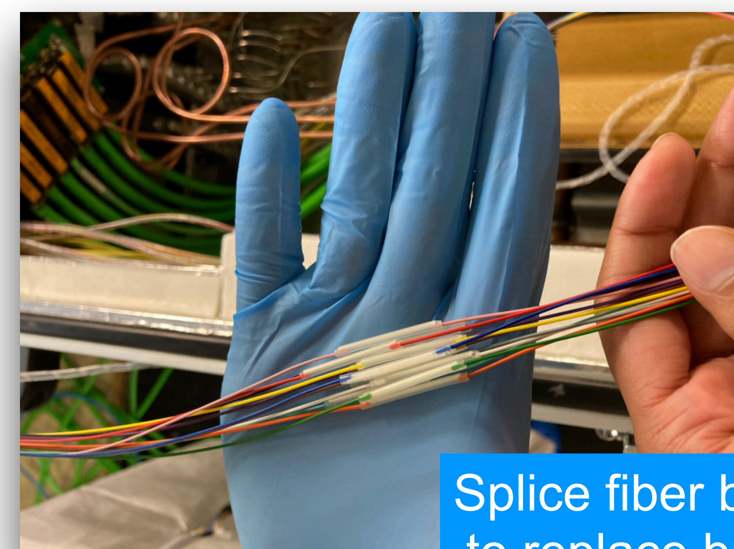
- **Repaired broken FED fiber bundle (MTP) connector**
- **Replaced DCDC cooling bridges for better thermal contact** - DONE only when deemed necessary





Better thread better thermal contact between DCDC and cooling bridge

Broken FED bundle connector



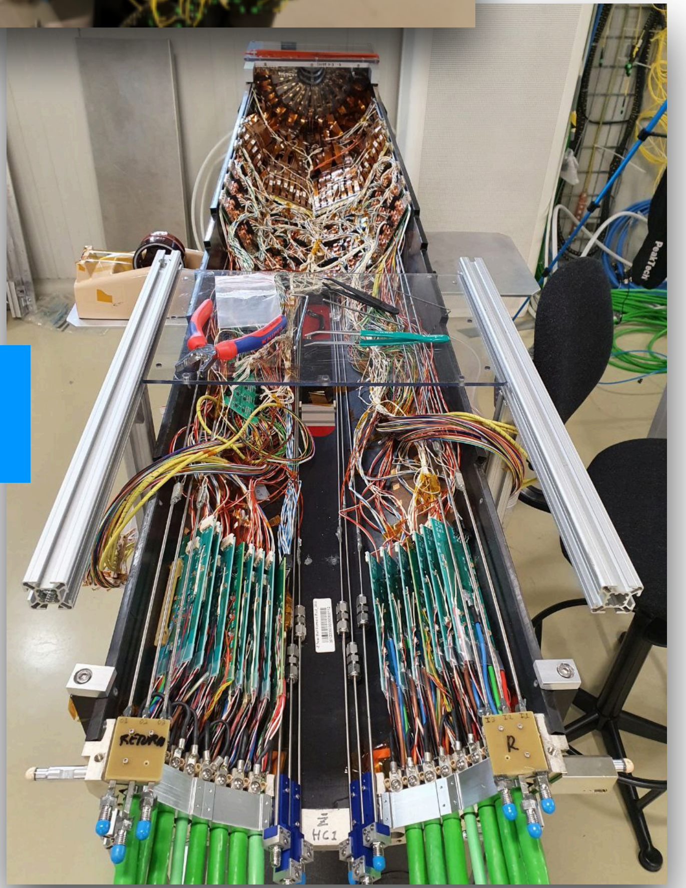
Splice fiber bundle to replace broken MTP connector

Tests before installation

- **BPix:**
  - **Hardware intervention completed** in March 2021
  - **Warm and cold tests in clean room completed** by the end of April 2021
  - Few connection related issues were taken care of
  - **No major issues, modules in good shape**

- **FPix:**
  - **Fully repaired and cold tested** in the clean room by the end of April 2021
  - No powering or cooling related issues observed after the repair work
  - One faulty filter board was replaced
  - **Modules in good condition, no new problems**

Cold box under test

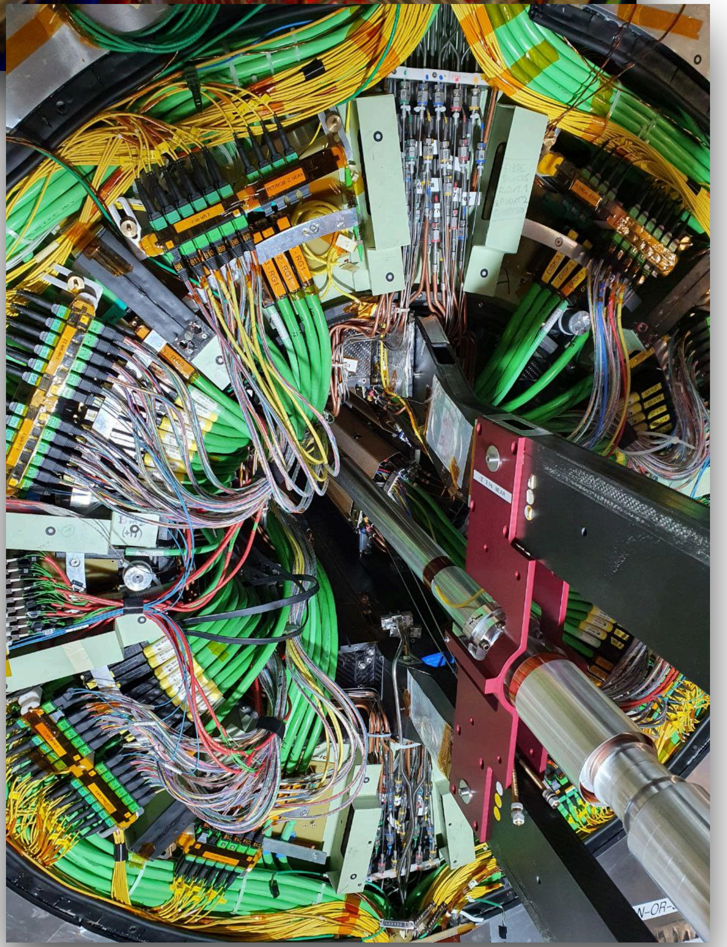


1/4 FPix completed

Installation

- **Detector installed inside the cavern at the end of June 2021**
  - cooling connection and leak test
  - pressure test for new Layer 1 lines
  - power and readout connections
  - CO_2 flow established at +17 degC

  → **very smooth installation**

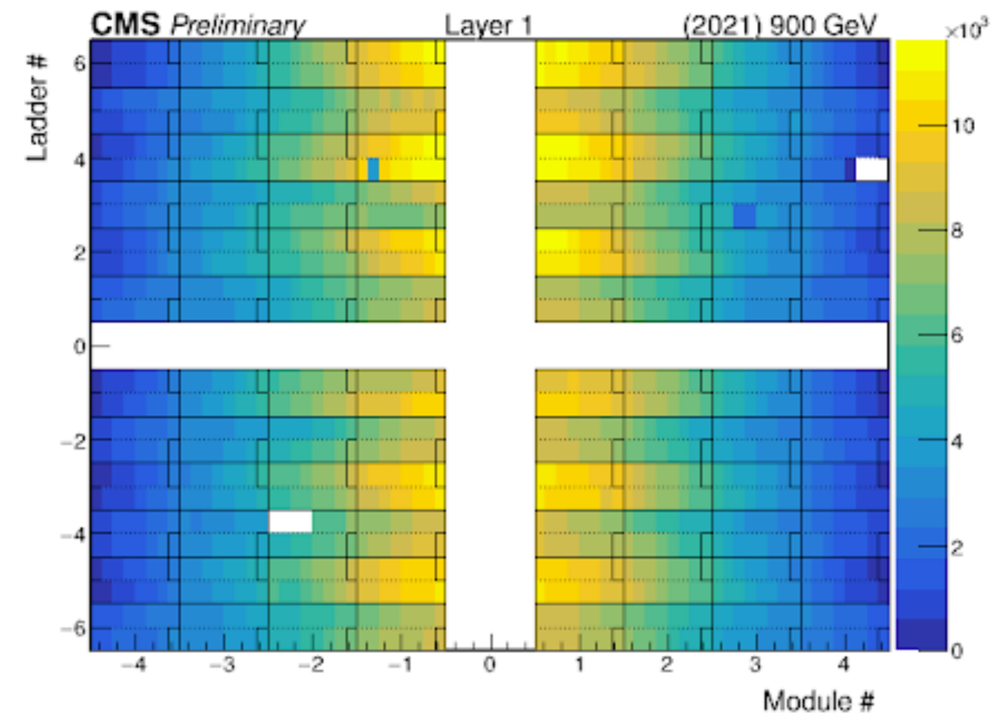


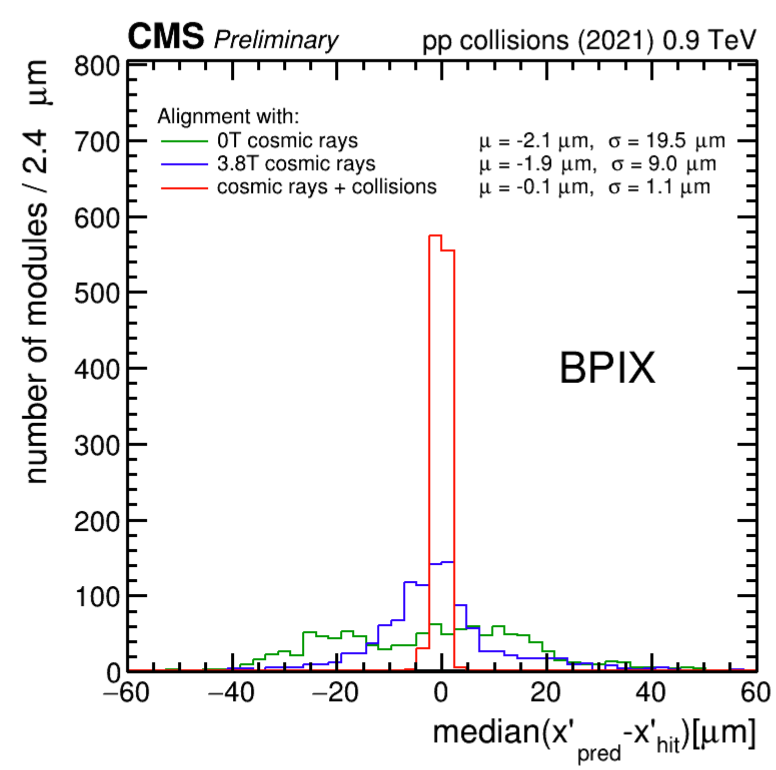
- **Detector fully commissioned after installation**
  - warm checkout at +17 degC with essential calibrations
  - cold checkout at -20 degC with full calibration cycle
  - no new problems observed after installation (compared to lab checkout)
  - only minor power supply glitches

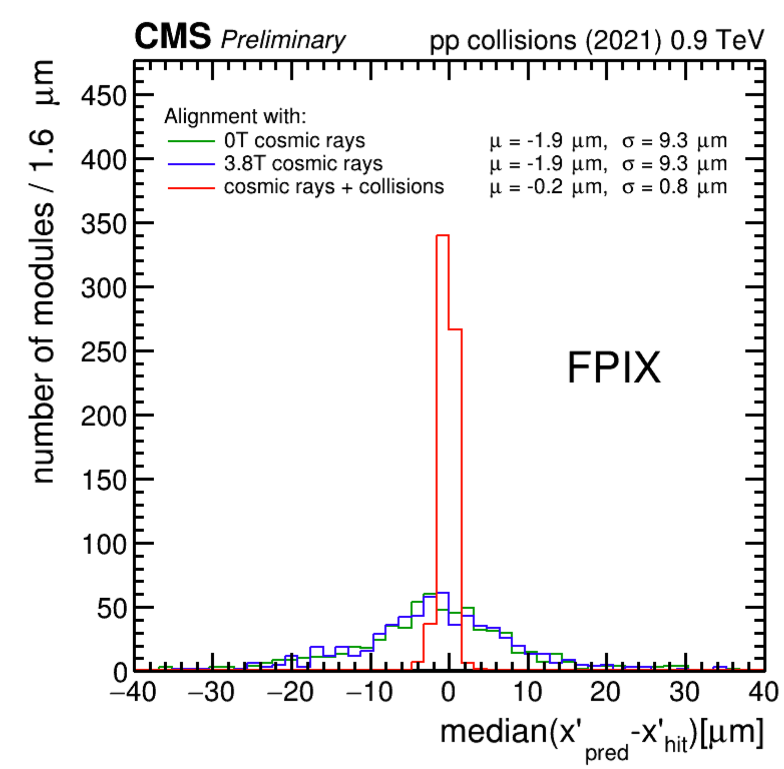
  → **detector in good state**

LHC Pilot Beam Test

- **Stable beams in October 2021.. after almost 3 years!**
- **Very stable operation from Pixel detector**
  - **collected good data quality**
- **Performed timing scan during collisions**
  - new TBM feature used to set a relative delay between Layer 1 and Layer 2
  - **optimal delay settings found** for full detector
- **Detector newly realigned after installation**
  - improved residuals with collisions data





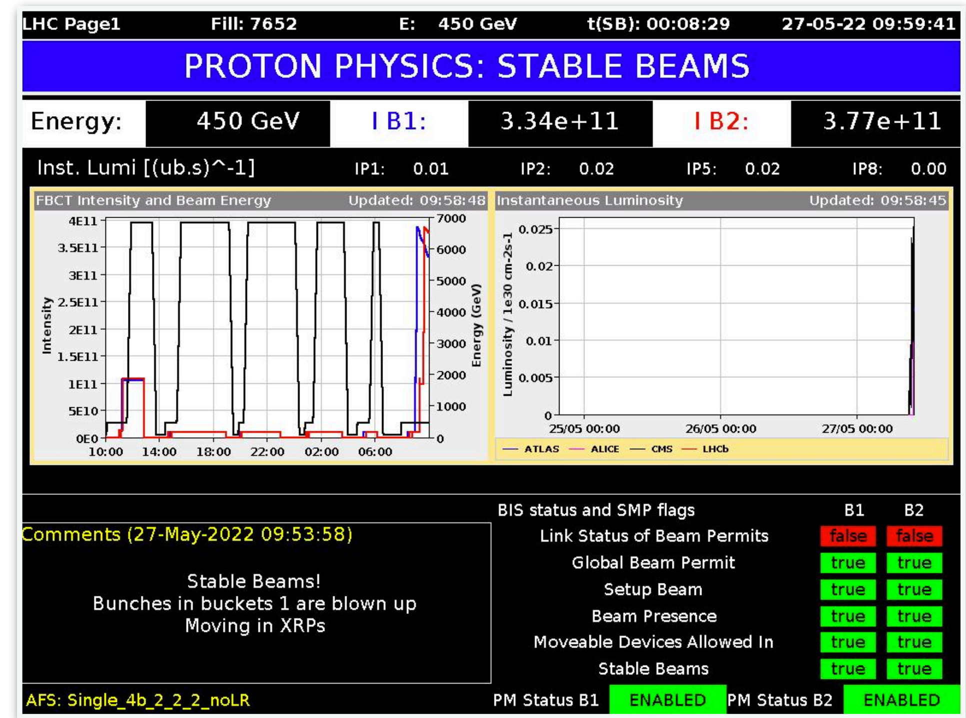


2022 re-start and first collisions

- **Detector fully ON since February 2022**
  - CO_2 cooling set at -22 degC

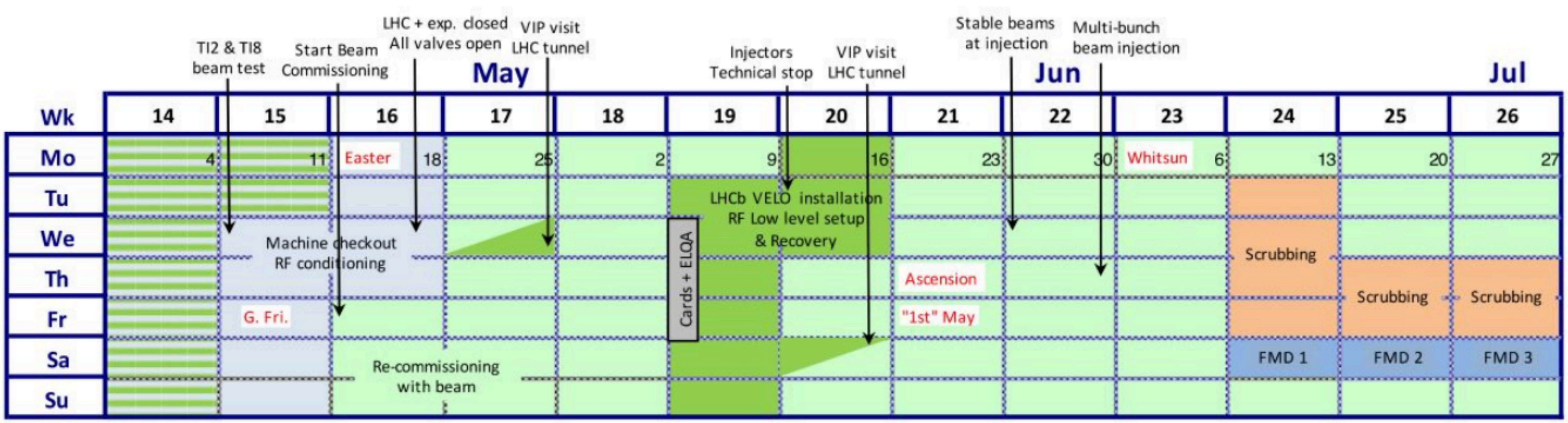
- **Standard commissioning checks and tuning performed in February-March**
  - threshold and pulse height optimization, tuning of unstable modules, masking of noisy pixels, ...

→ detector optimally calibrated and ready for Run 3



- **Pixel participated in first stable beams @900 GeV on June 3rd**

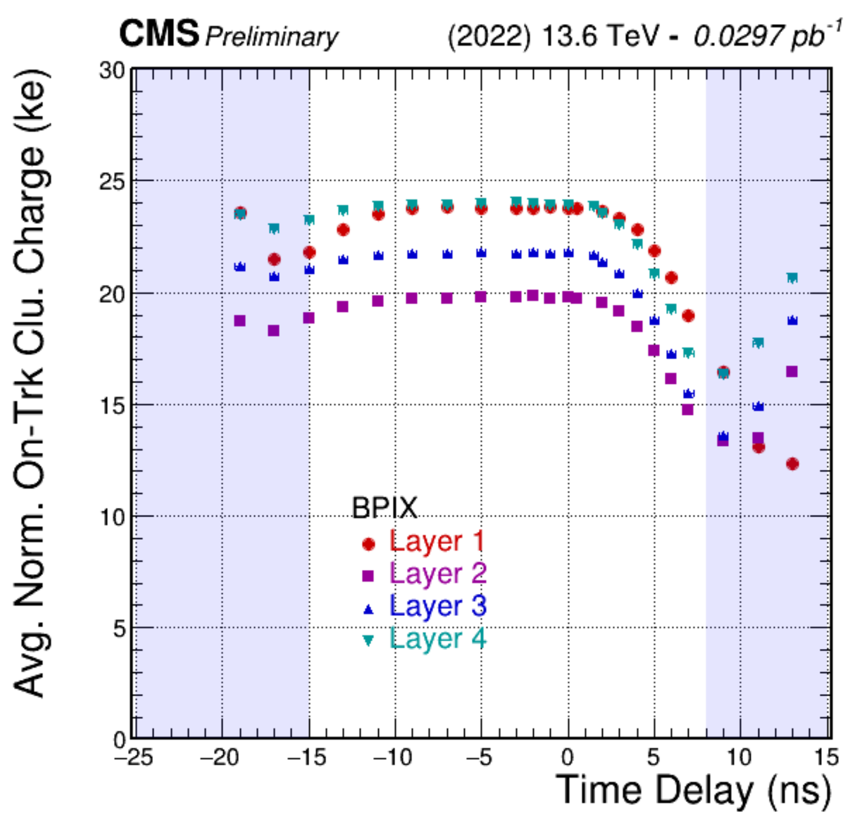
  → no particular issues, overall good data quality

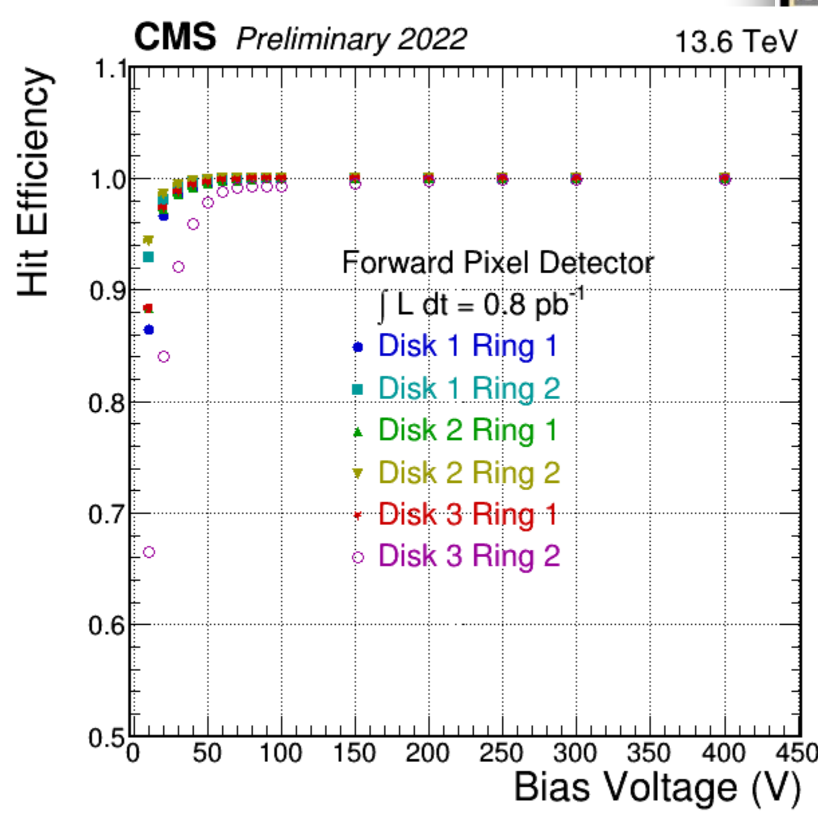


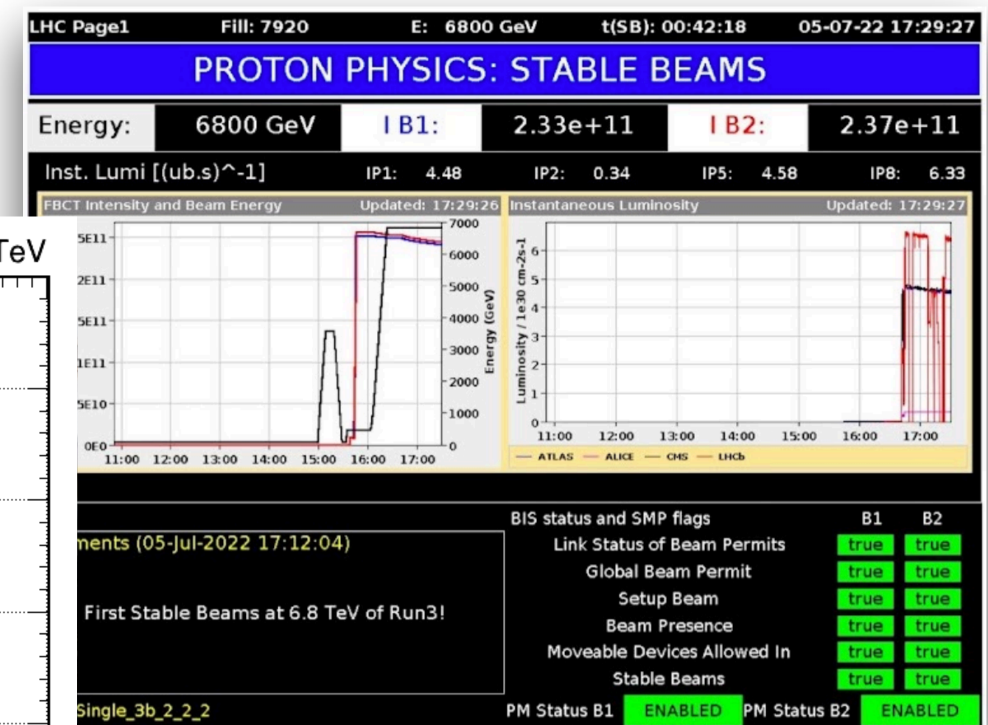
First Run 3 collisions @13.6 TeV

- **Pixel successfully participated in the first 13.6 TeV stable beams on July 5th**
  → overall good data quality !

- **Performed a full timing scan and a full HV bias scan on July 5th-6th**
  - found optimal settings for the full detector







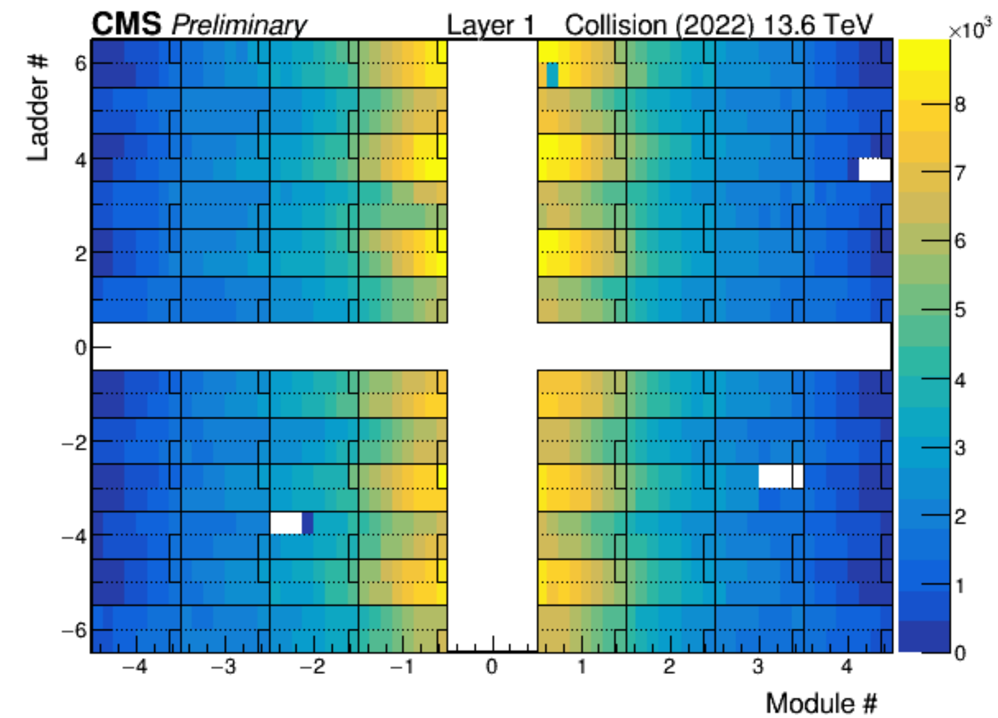
Active Detector Fraction

- Occupancy plots with bad components = non-functional readout chips (ROCs) masked at detector level
  - **BPix: 244 (1.46%)**
    - after installation: 168 (0.9%)
    - end of Run2: 1068 (5.6%)
  - **FPix: 154 (1.43%)**
    - after installation: 162 (1.5%)
    - end of Run2: 184 (1.7%)

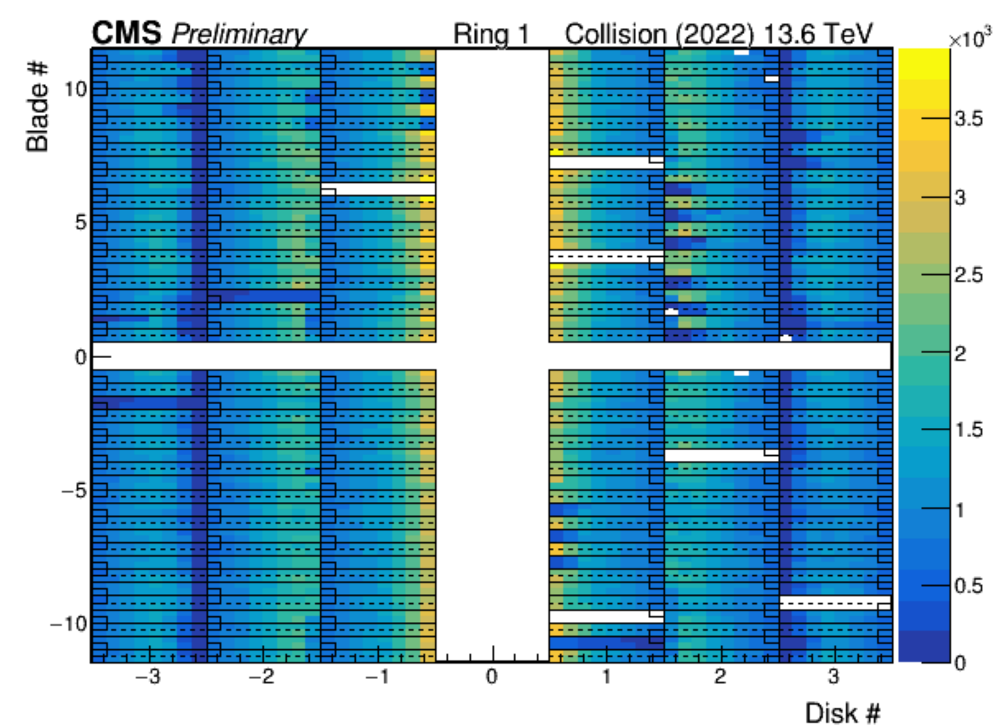
- Temporarily bad components are also visible, as well as fractionally damaged ROCs (components with partially lower occupancy)

Fraction of alive channels almost unchanged w.r.t. 2021 (after installation), improved w.r.t. end of Run 2

BPix ~ 98%



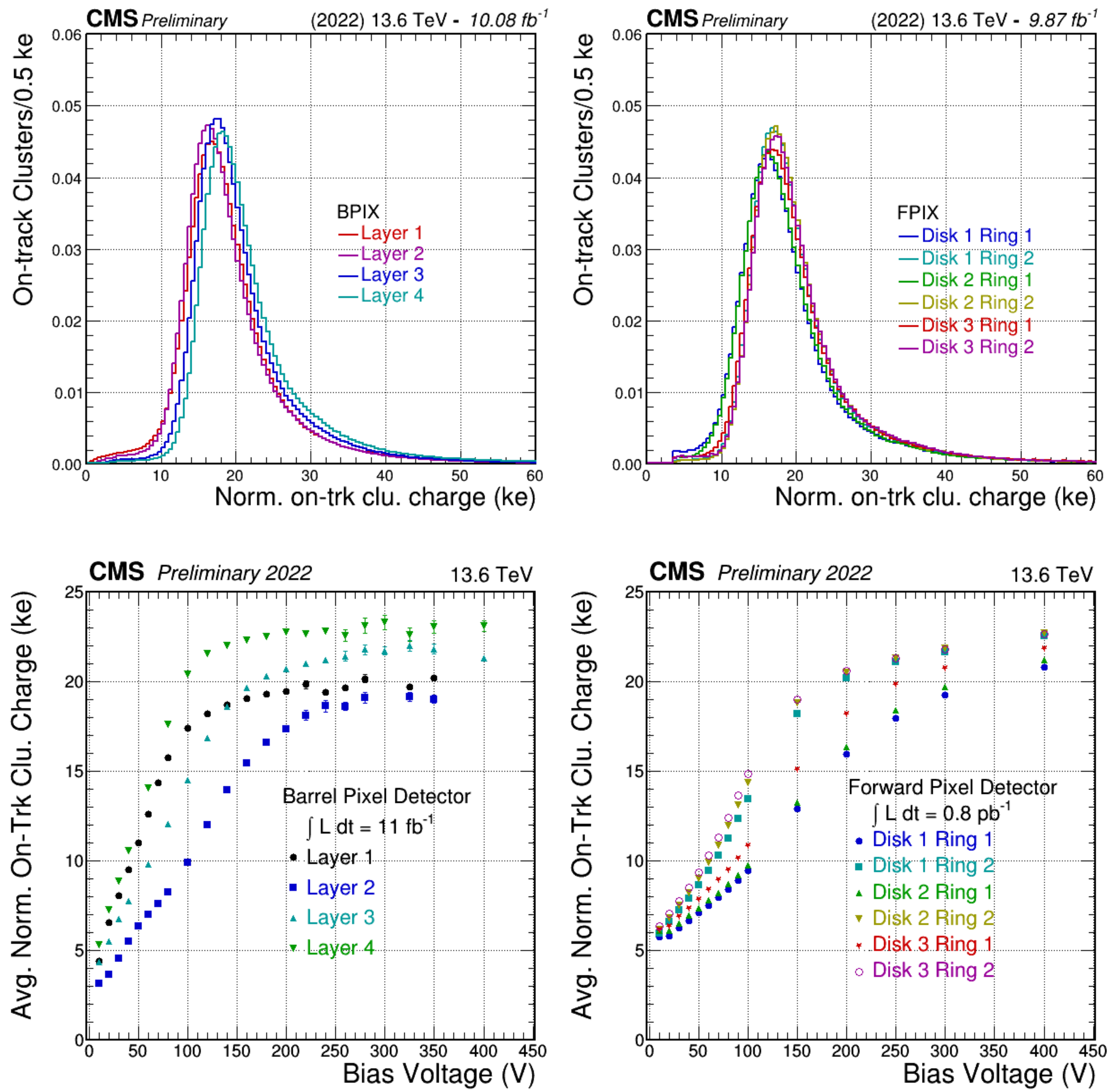
FPix ~ 99%



Cluster charge and bias scan

- **Cluster properties are good** and comparable to Run 2 performance
- Bias voltage scans are performed regularly to monitor the evolution of the silicon bulk due to radiation

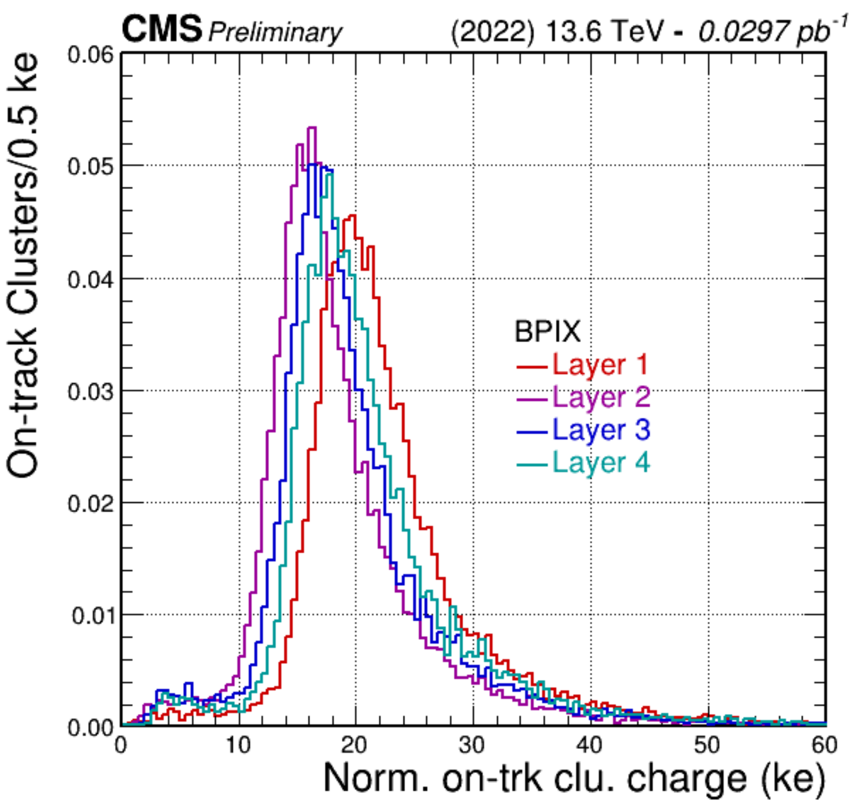
Operational voltages
Layer 1 & 2: 300 V
Layer 3 & 4: 250 V
Ring 1: 350 V
Ring 2: 300 V



Radiation damage in Layer 1

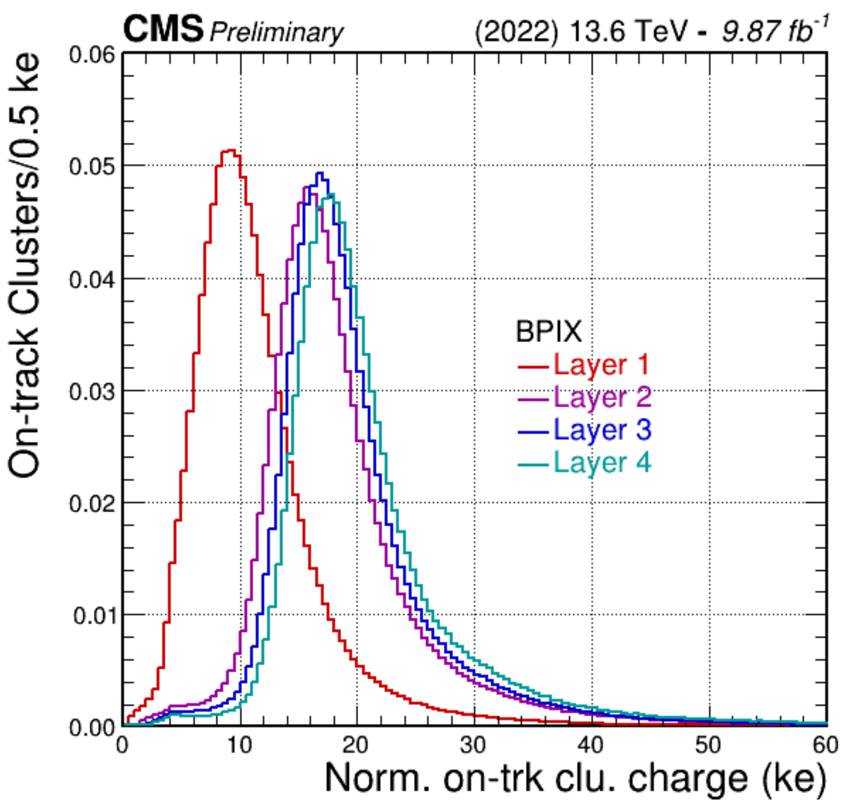
- **Strong effect of radiation damage observed in cluster properties**

Layer 1 @ 150 V



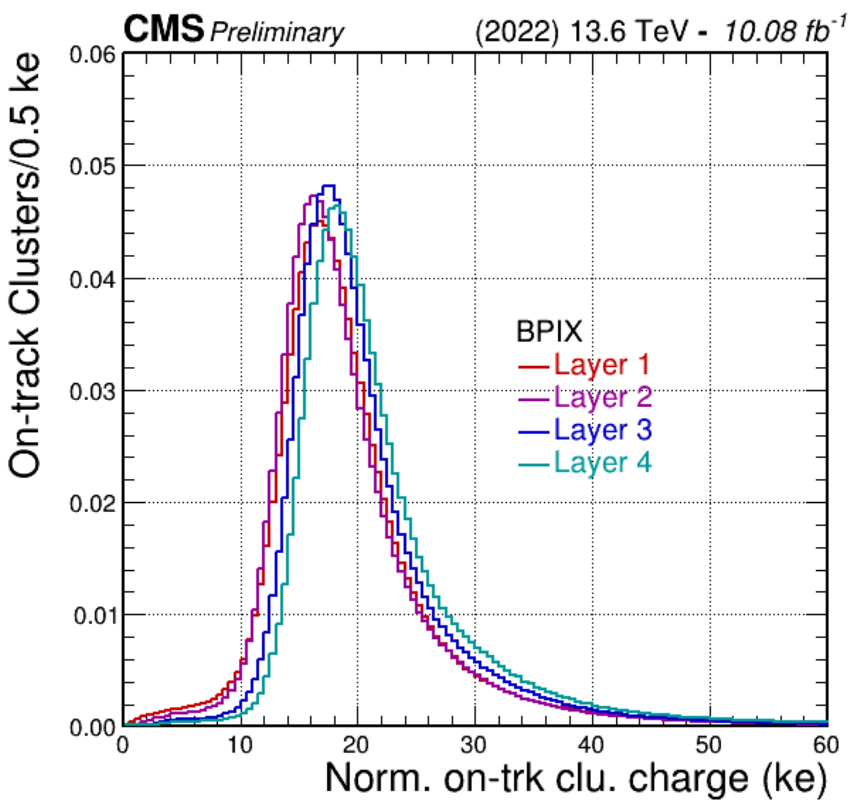
Layer 1 fully replaced during LS2 → started with no radiation damage, i.e. higher cluster charges

Layer 1 @ 150 V



large charge efficiency loss due to radiation damage observed within first 10 fb^{-1}

Layer 1 @ 300 V

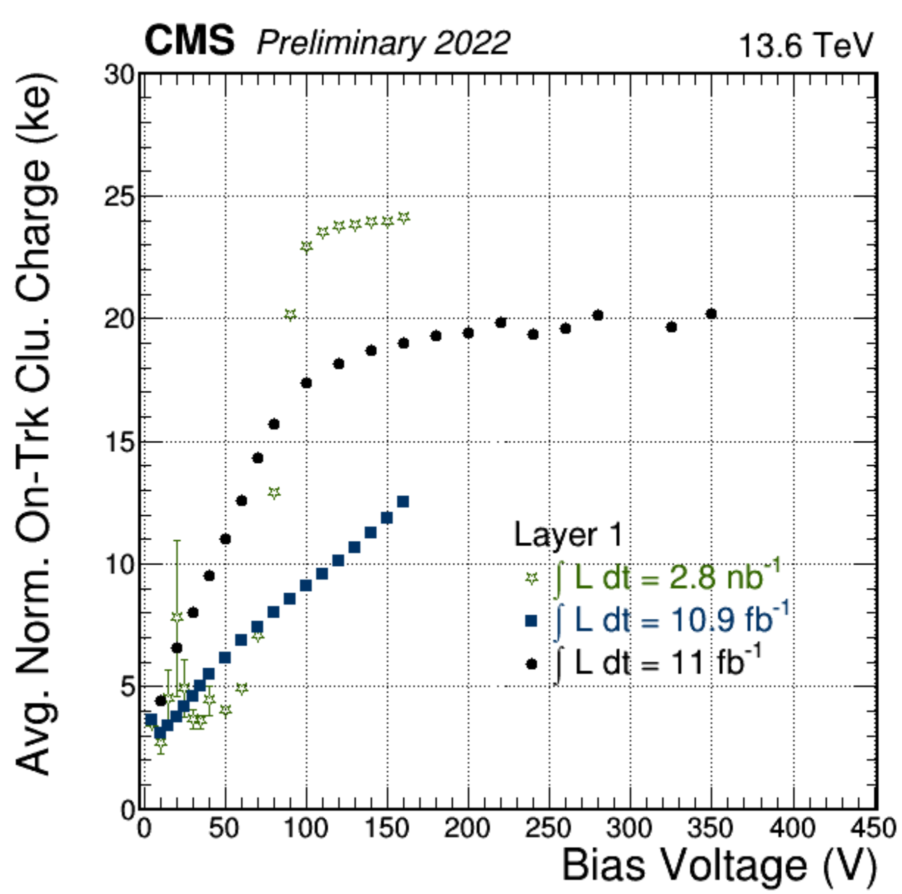


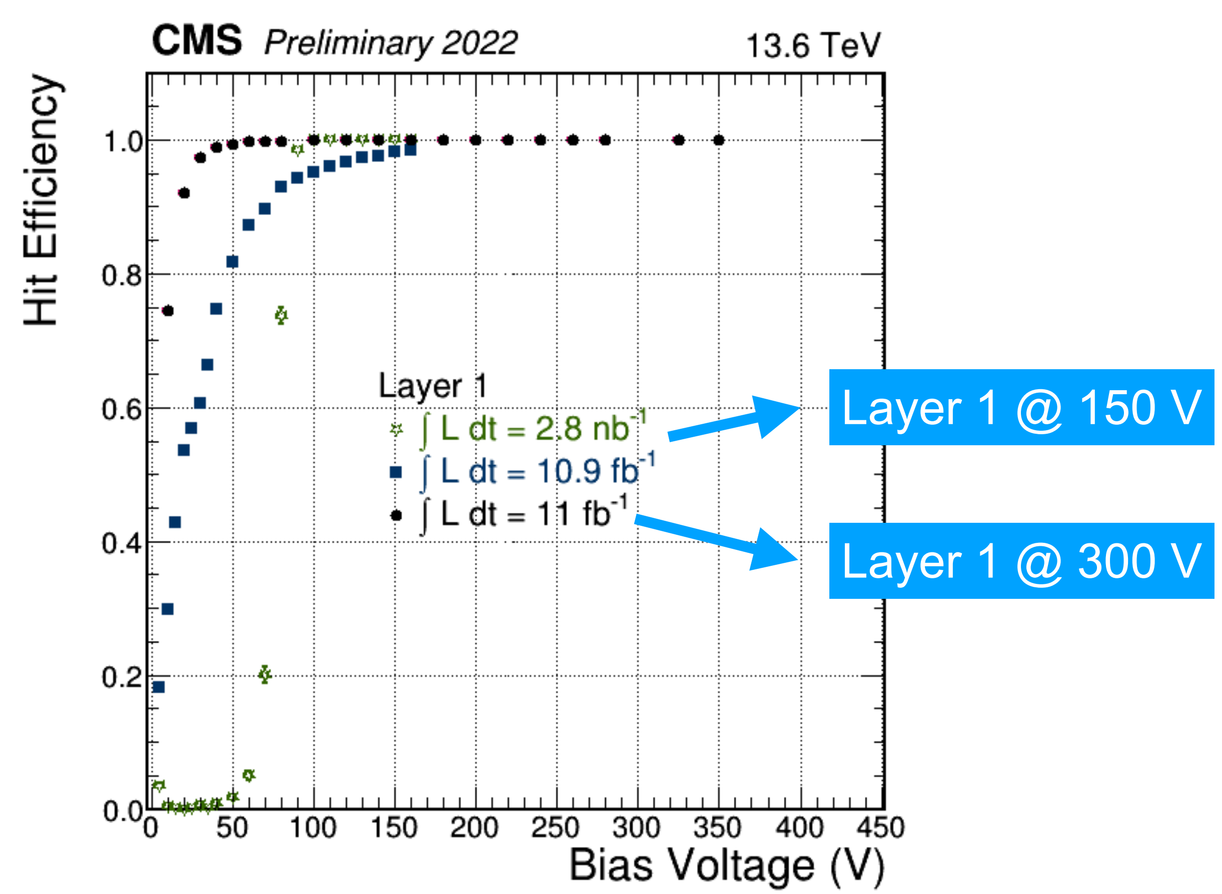
recovered by raising bias voltage from 150V to 300V

Radiation damage in Layer 1

- **Effect of irradiation in Layer 1 also visible in different bias scans:**
  - ~3 nb^{-1}: not much radiation damage accumulated yet
  - ~10 fb^{-1}: radiation damage higher than expected due to quick luminosity ramp up at beginning of Run 3
  - ~11 fb^{-1}: **charge collection efficiency improved thanks to positive annealing** during the period without data-taking (no beam for ~4 weeks due to LHC cooling incident)

→ need to monitor closely the evolution of the situation with scans once a week



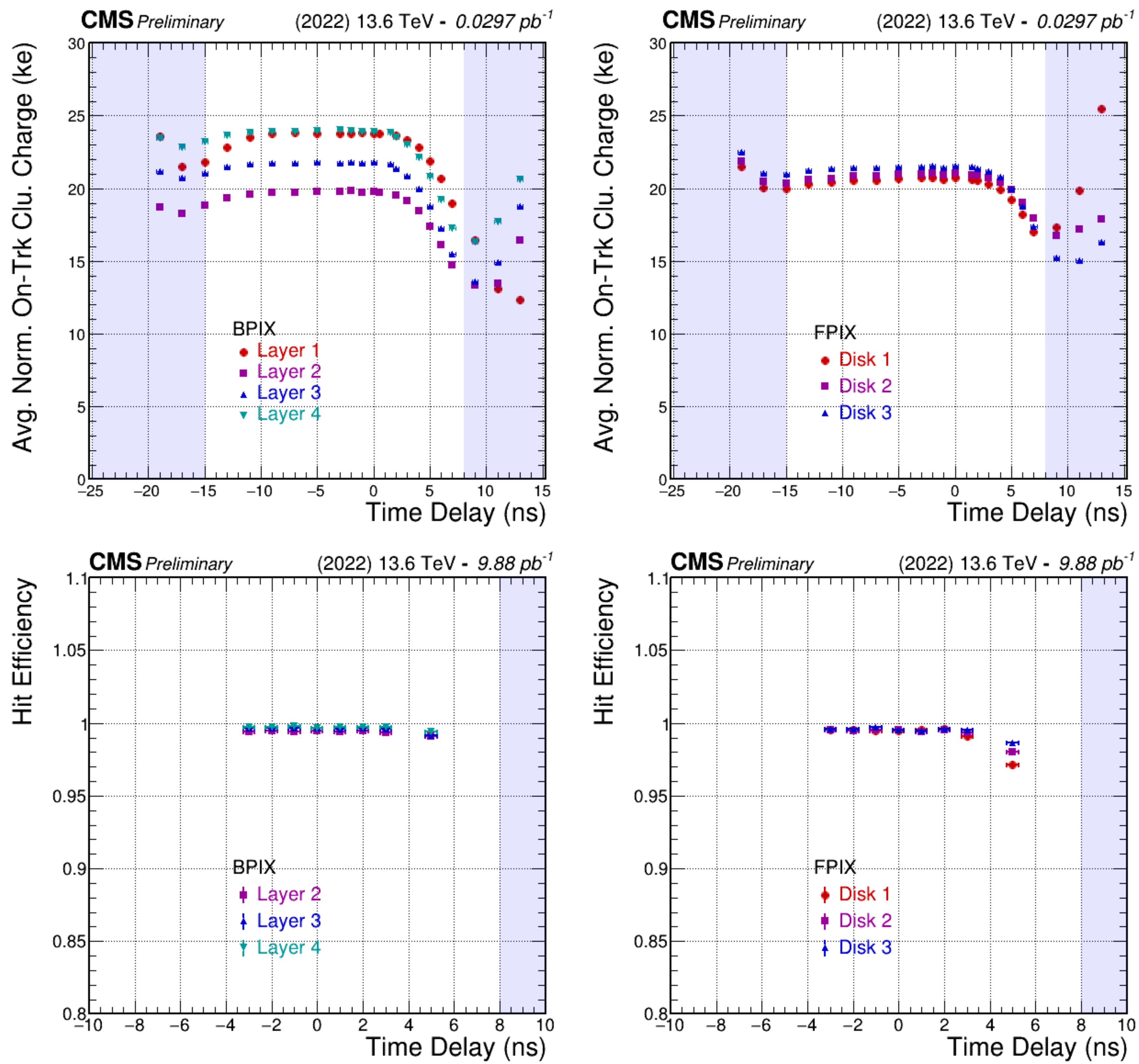


Timing scan

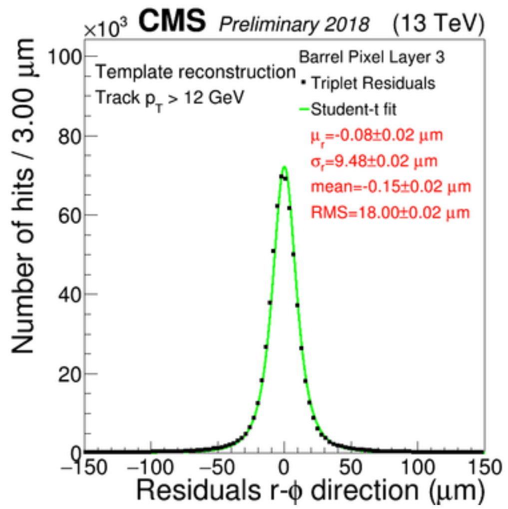
- **Timing scan done to ensure that the correct hits are read out and to find the best delays such that we have a uniform response from the detector**
  - the pixel detector is read out on receipt of a Level-1 Accept (L1A) signal
  - not accounting the delays properly could result in mismatch between L1A and bunch crossing!

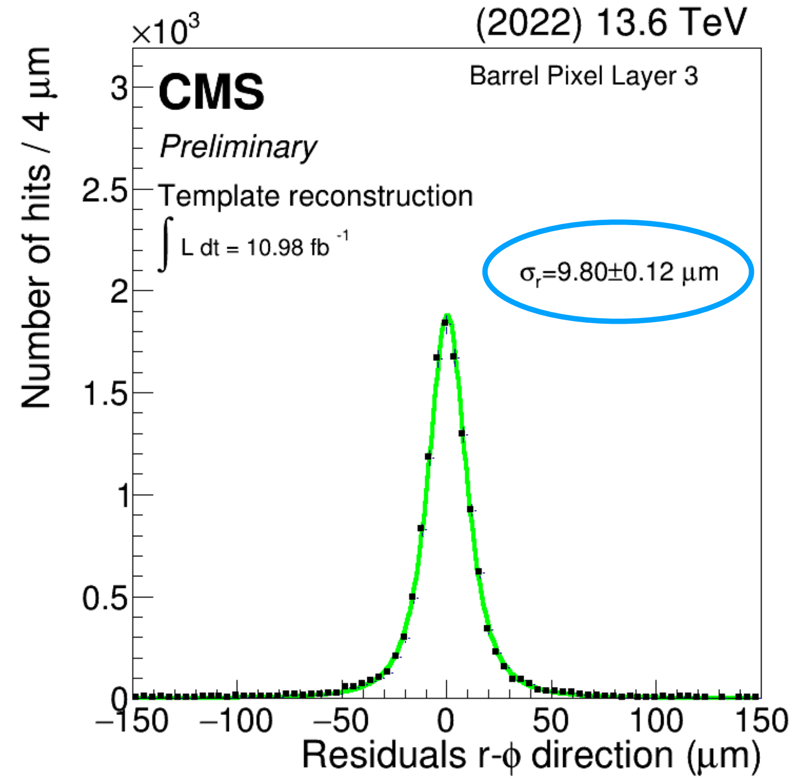
- Mini-timing scan performed to verify that **applied timing settings are correct**

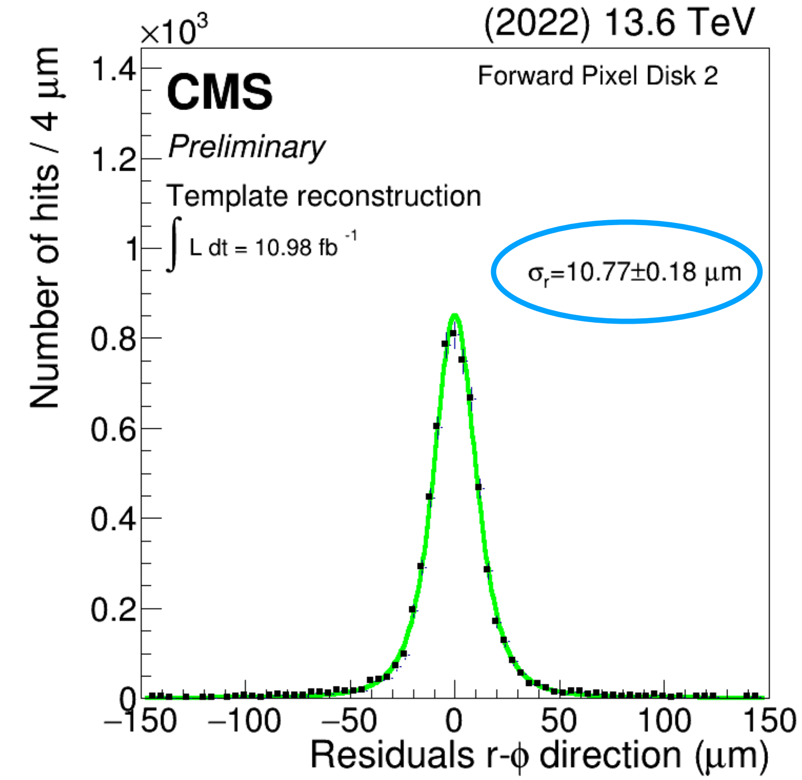
trigger delay = delay between the bunch-crossings and when the L1A arrives to the pixel ROCs



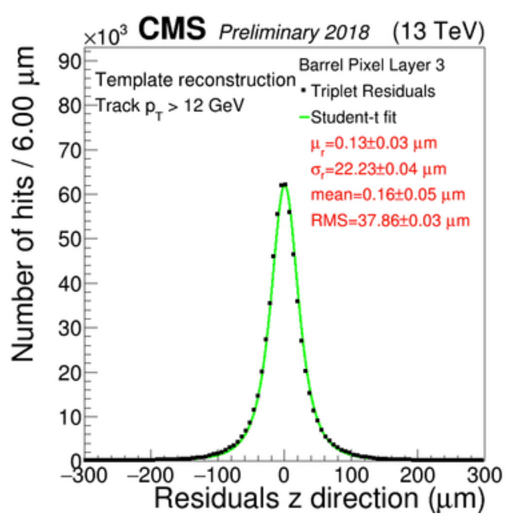
Resolution

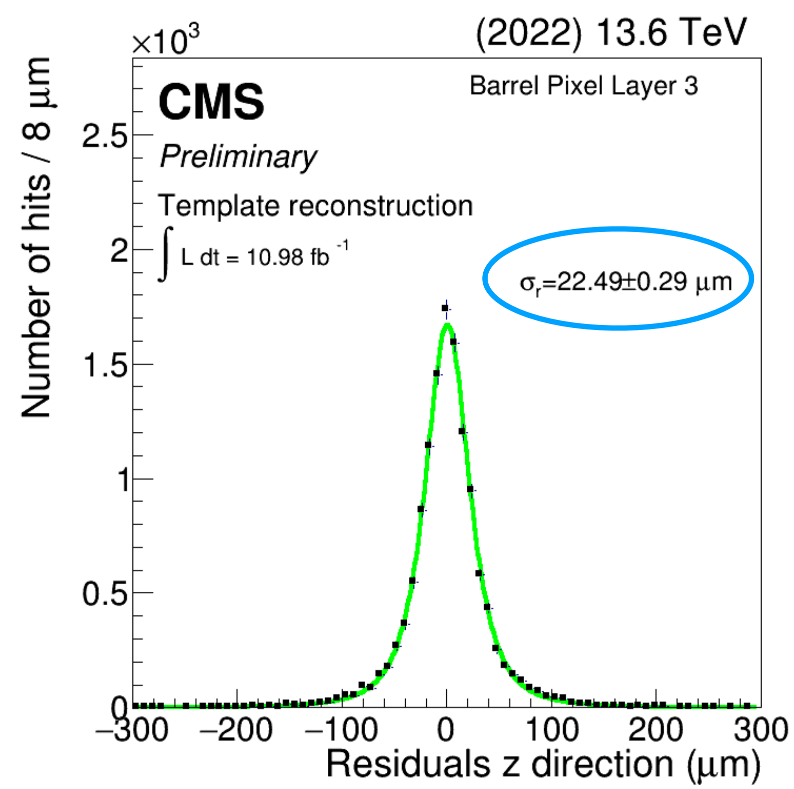


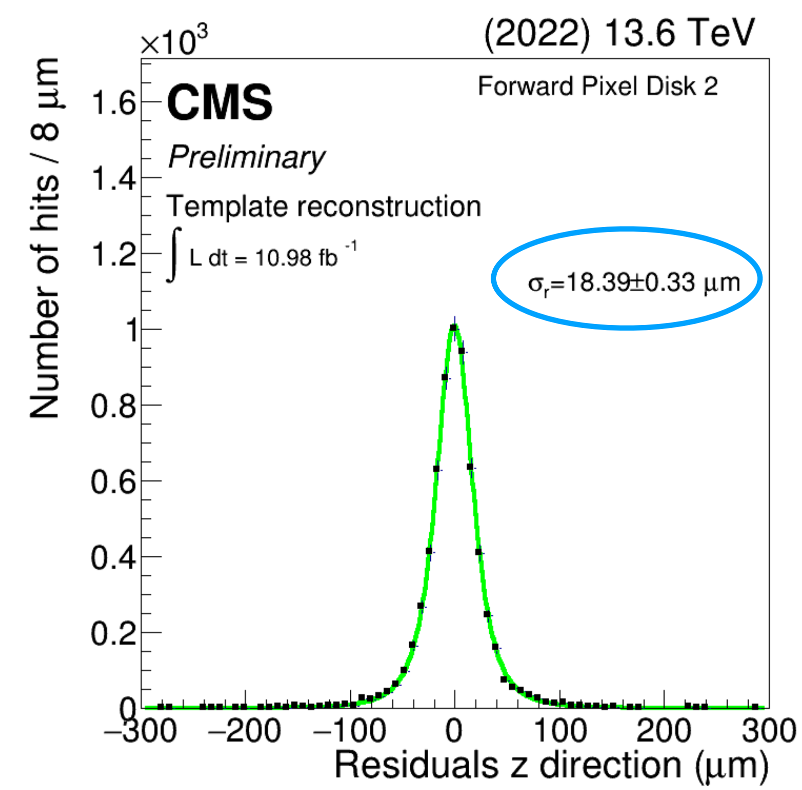




Comparable to Run 2 performance



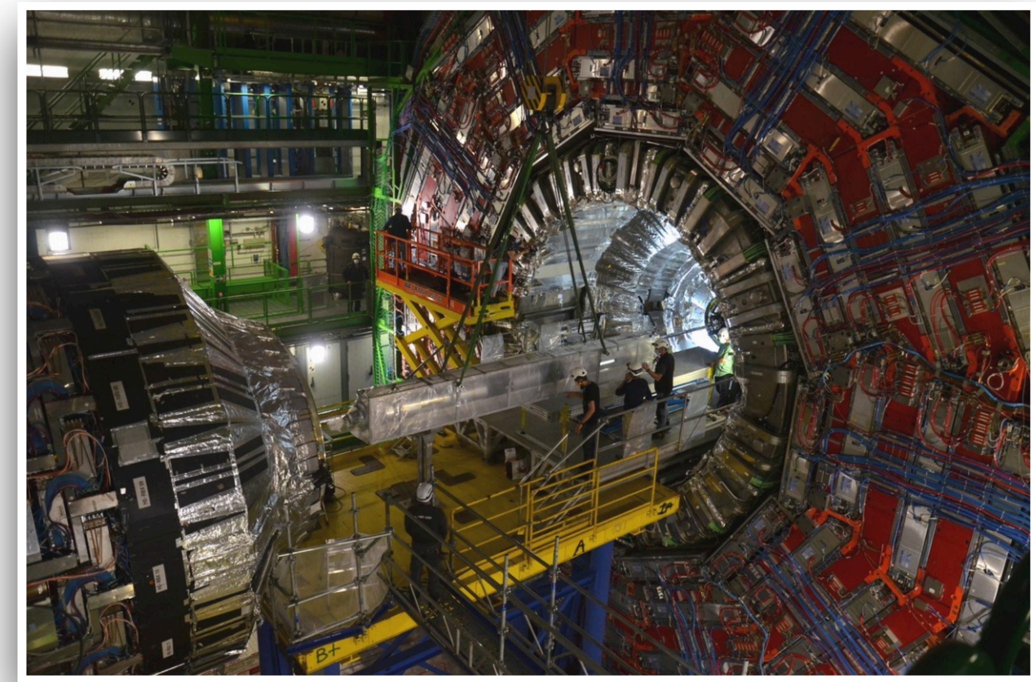


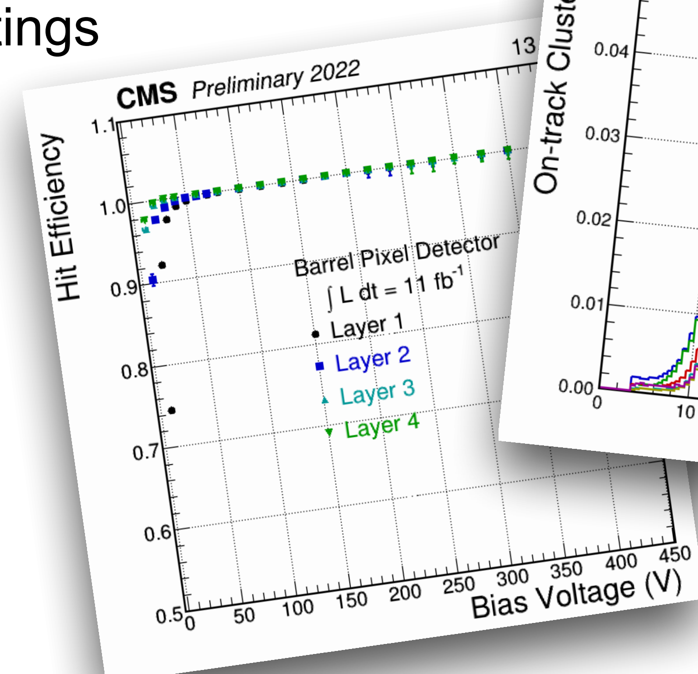


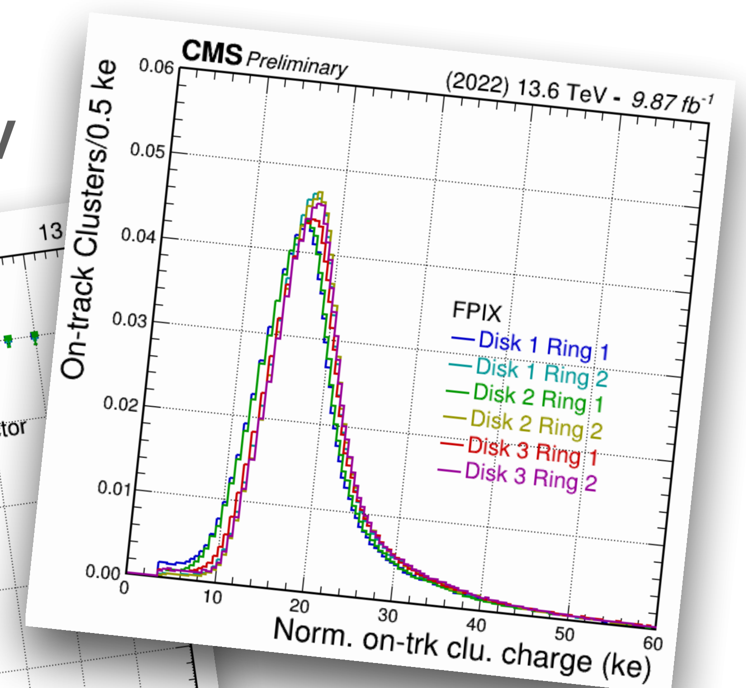
Excellent position resolution in both BPix and FPix

Summary

- **Detector refurbishment during the Long Shutdown 2**
  - full work completed on both BPix and FPix
- **Smooth installation in Summer 2021**
- **Detector commissioned in 2021**
  - no new problems observed after installation
- **Successfully participated in LHC pilot beam test in October 2021**
  - detector in good shape and ready for Run 3
- **Successfully participated in first stable beams at 900 GeV and 13.6 TeV**
  - performed bias and timing scans to find optimal settings
- **First performance during Run 3 are good!**
  - need to monitor closely irradiation of Layer 1



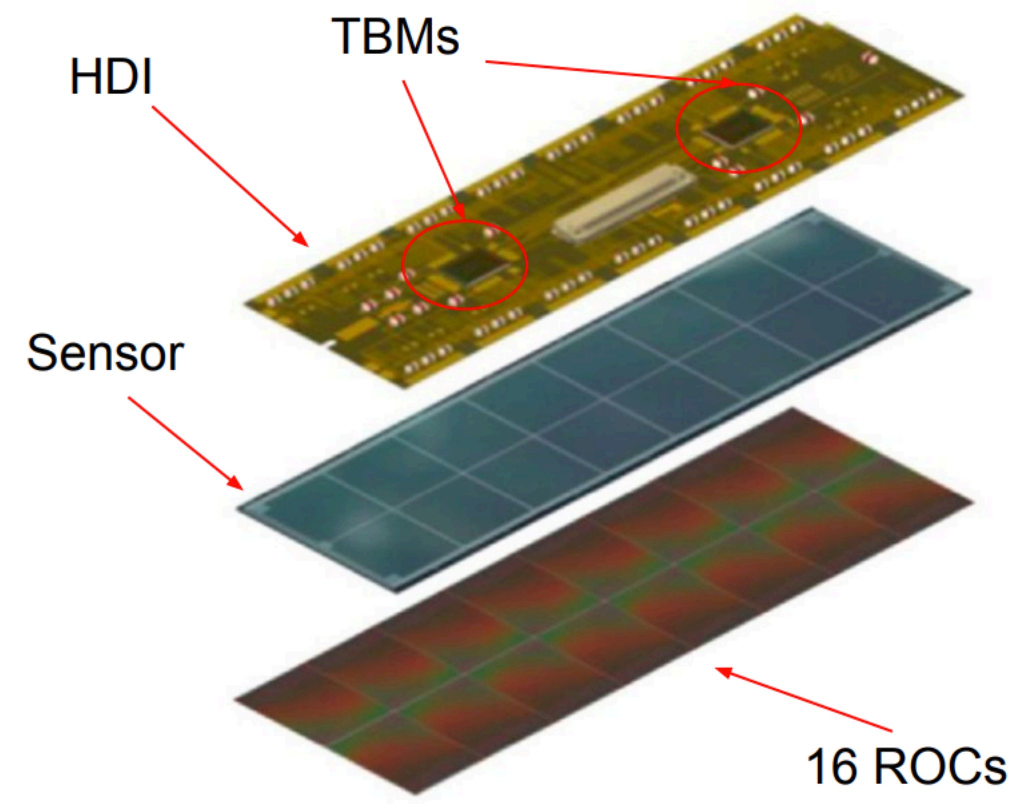


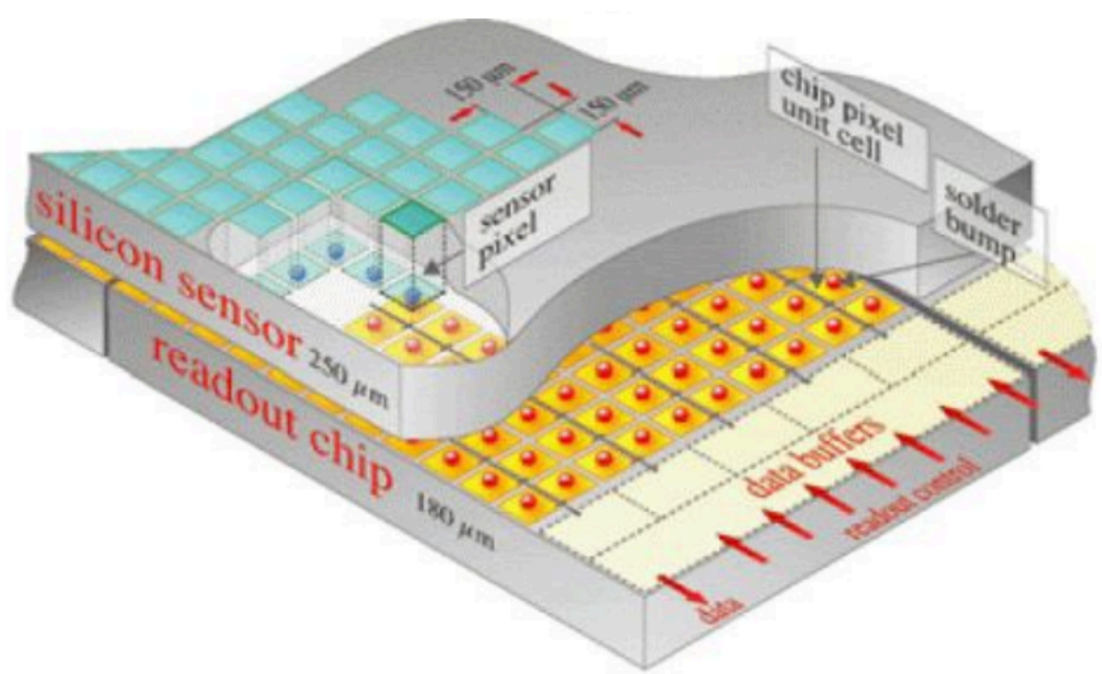


BACKUP

Layer 1 module overview

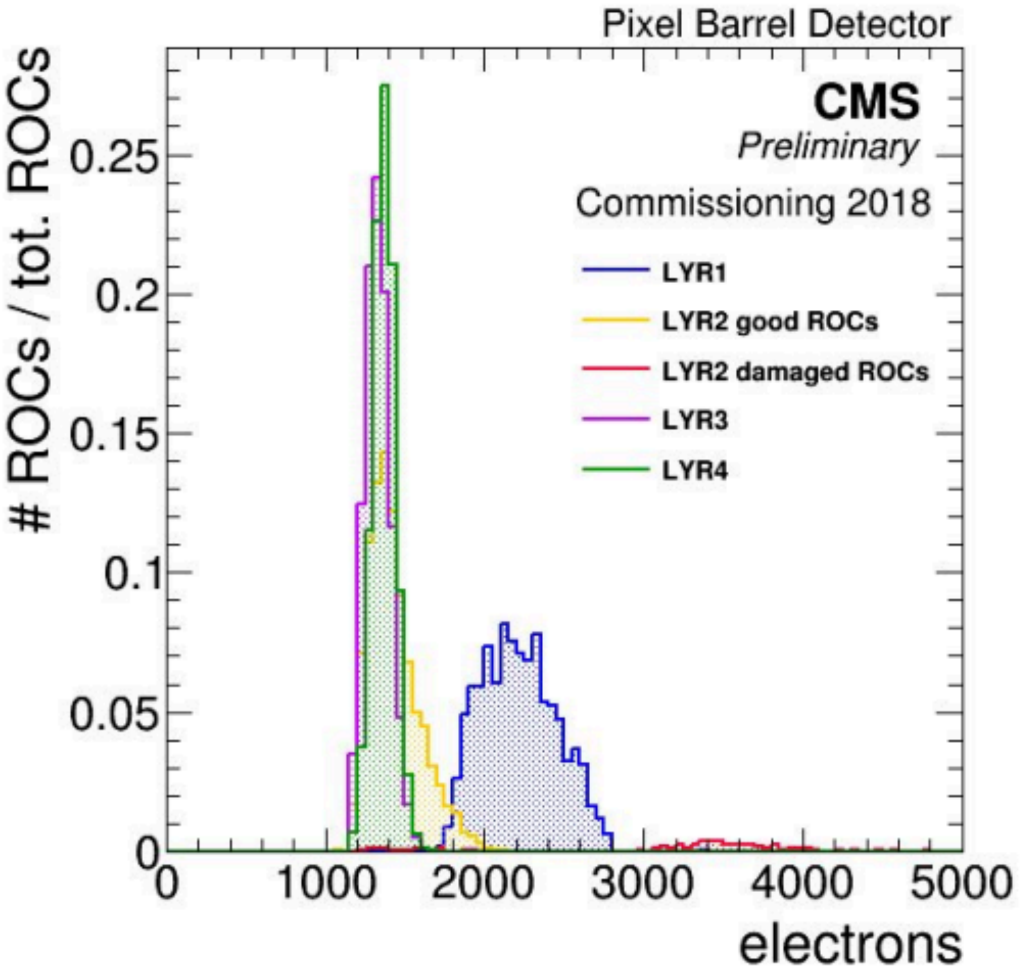
- **High-density interconnect (HDI10d)**
  - glued on top of the sensor and wire-bonded to readout chips (ROCs)
  - routes control and data signals between ROCs and token bit manager chips (TMBs)
  - routes high-voltage to the sensor
- **Silicon sensor**
  - “sandwiched” between HDI and ROCs
  - connected with ROCs through bump-bonds
- **Read out chips (PROC600 v4)**
  - 16 chips at the bottom of the modules
  - read signals from sensor, process them and send them to TBM
- After testing campaign, modules were ranked based on their quality and accordingly assigned to appropriate locations on Layer 1 (highest quality modules in the center)
- The entire readout of a module in Layer 1 is designed to cope with a particle hit rate of up to 600 MHz/cm^2





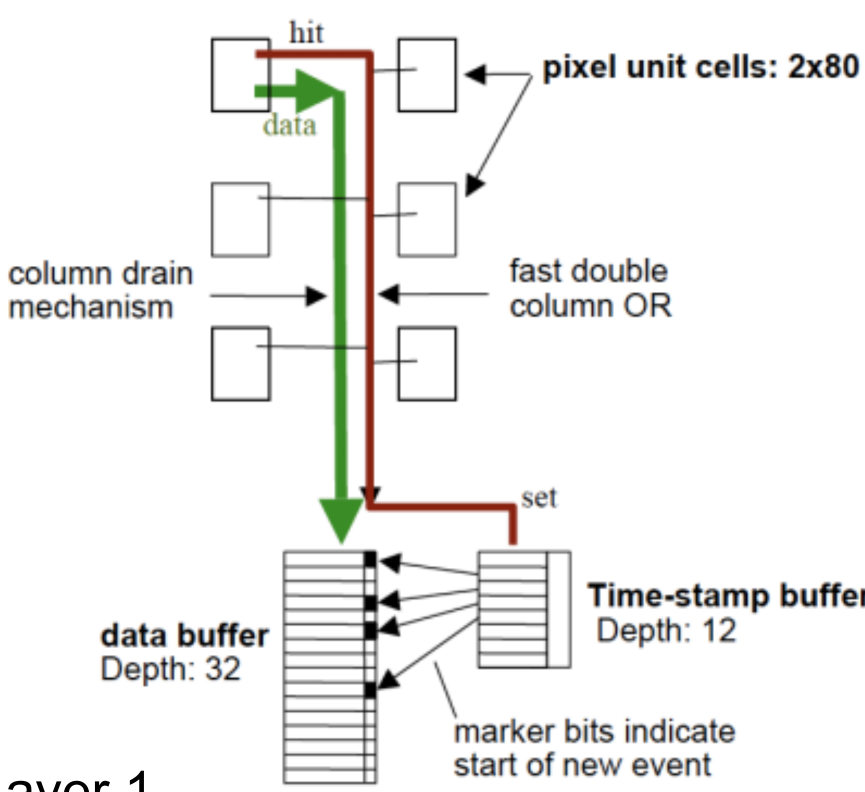
Operation challenges in Run 2

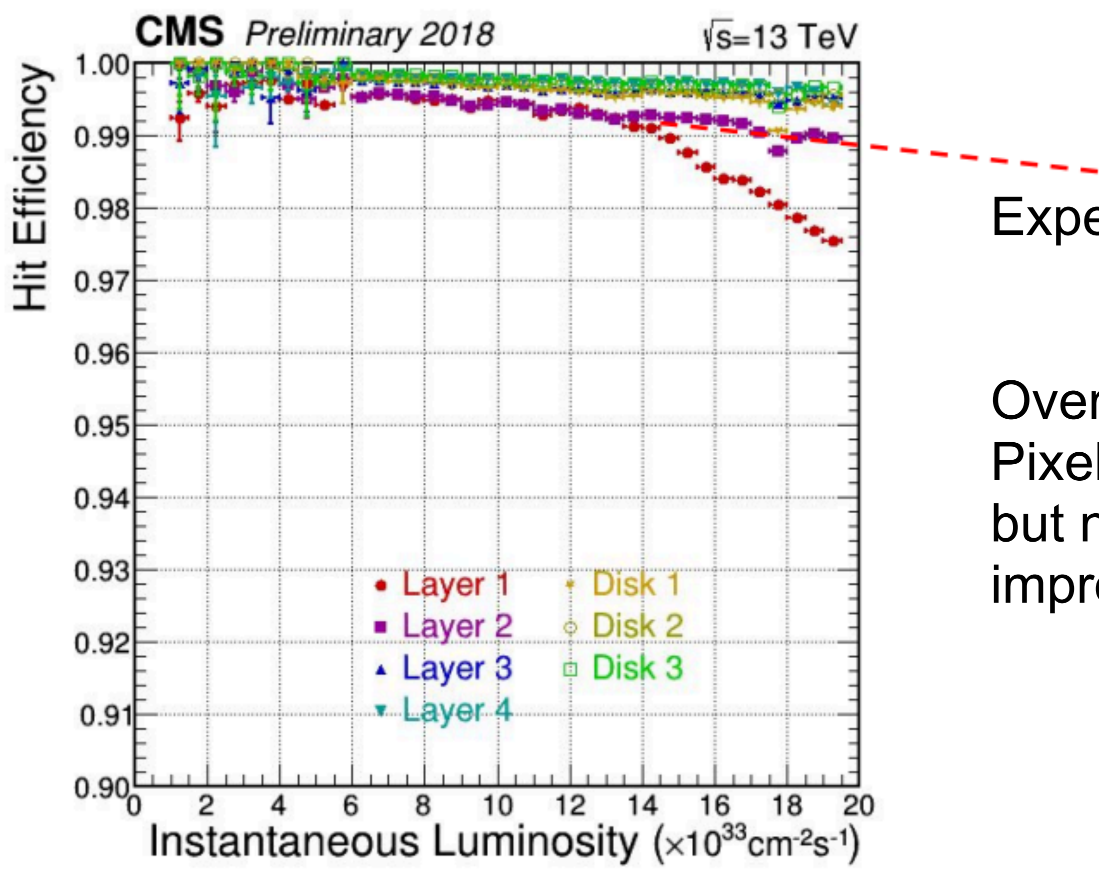
- **Crosstalk**
  - Layer 1 has higher threshold than expected, mainly due to electronics crosstalk
  - the injection capacitor was too close to the trim lines of the pixel
  - the source could be mitigated via “programming”, but a layout change solved the problem
  - **problem addressed in new version of PROC600v4**



Operation challenges in Run 2

- **Dynamic Inefficiency**
  - hits are stored in chip periphery (double column drain architecture)
    - timestamp - timestamp buffer
    - data - data buffer
  - due to a glitch we lose synchronization between data and time, leading to loss of data
  - **problem addressed in new PROC600v4**



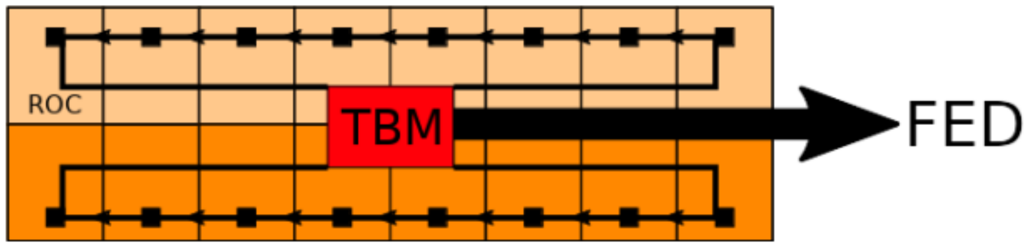


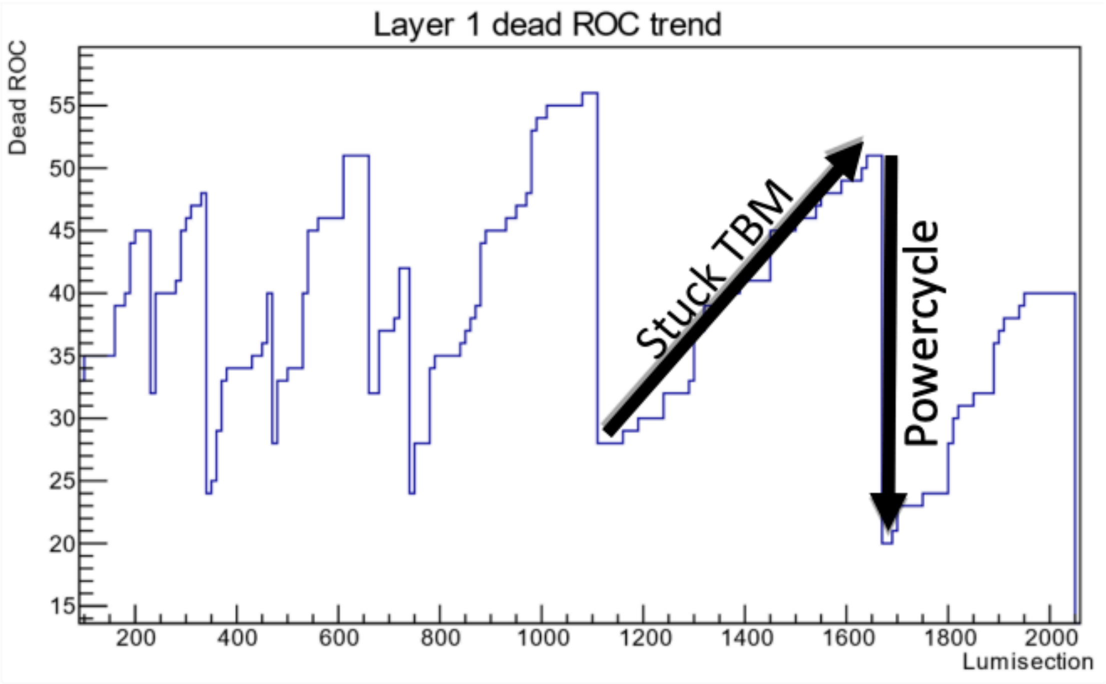
Expected for new Layer 1

Overall excellent efficiency from Phase-1 Pixel detector already in Run 2
but now we have a new Layer 1 which will improve performance substantially

Operation challenges in Run 2

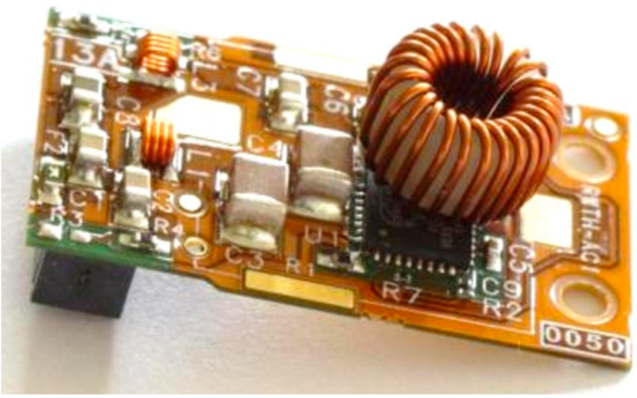
- **Stuck TBMs**
  - when a L1 trigger is received, the TBM collects data from all readout chips and sends them to a FED
  - this process is affected by Single Event Upset (SEU): TBM can get stuck in one state, leading to loss of data
  - the only way to recover is through a **power cycle**
  - new TBM for Layer 1 (TBM10d) solves this problem
    - **reset of TBM is possible in new version**





SEU rate during 2018: ~ 30/fb-1

Operation challenges in Run 2



- **DCDC converters failure**
  - resulted from a fault in the FEAST chip design
  - when a DCDC is disabled, a charge builds up on the circuit due to irradiation (>10kGy) causing the DCDC to break
  - impact on operations (2018):
    - converters not used to power cycle modules
    - power cycling needed for stuck TBMs - stuck TBMs accumulated
    - reduced supply voltage to 9V
    - power supplies (CAEN) used to power cycle modules between beams
    - high current trips in power groups with higher share of modules
    - raised trip limits, programmed to reduce start up current in power groups
    - disabled a few DCDC converters to prevent trips while power cycling/ turning on detector -> **no broken DCDCs in 2018** (active fraction ~94.5%)

Mar. 2017: Phase-1 upgrade done, Started data taking with 95.6% active detector

5th Oct. 2017: 1st DCDC Converter Broke

Dec. 2017: 5% converters not working, 11% detector not active

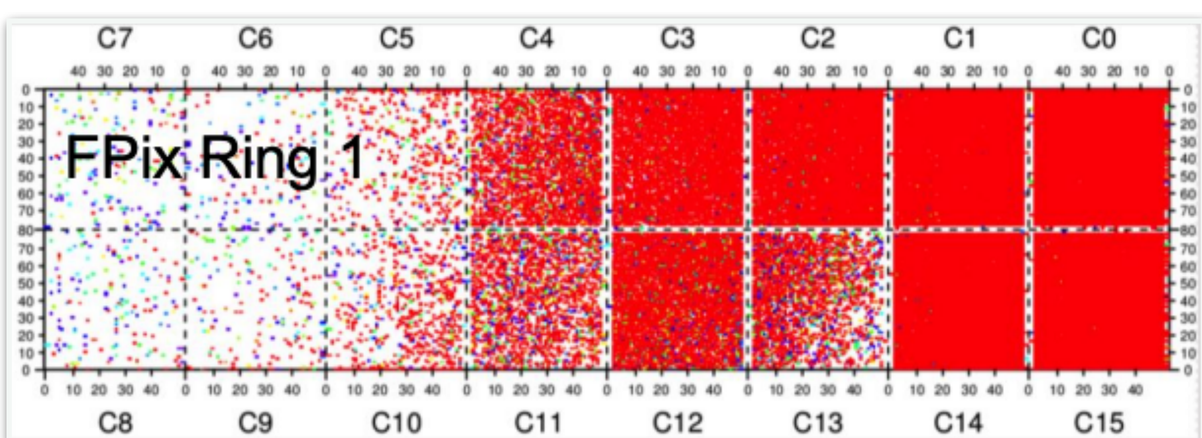
YETS 2017/2018: Detector Extracted, Replaced all DCDC with bigger fuse, problem not yet understood

May 2018: Problem reproduced in the lab (IRAD,X-ray), reason understood

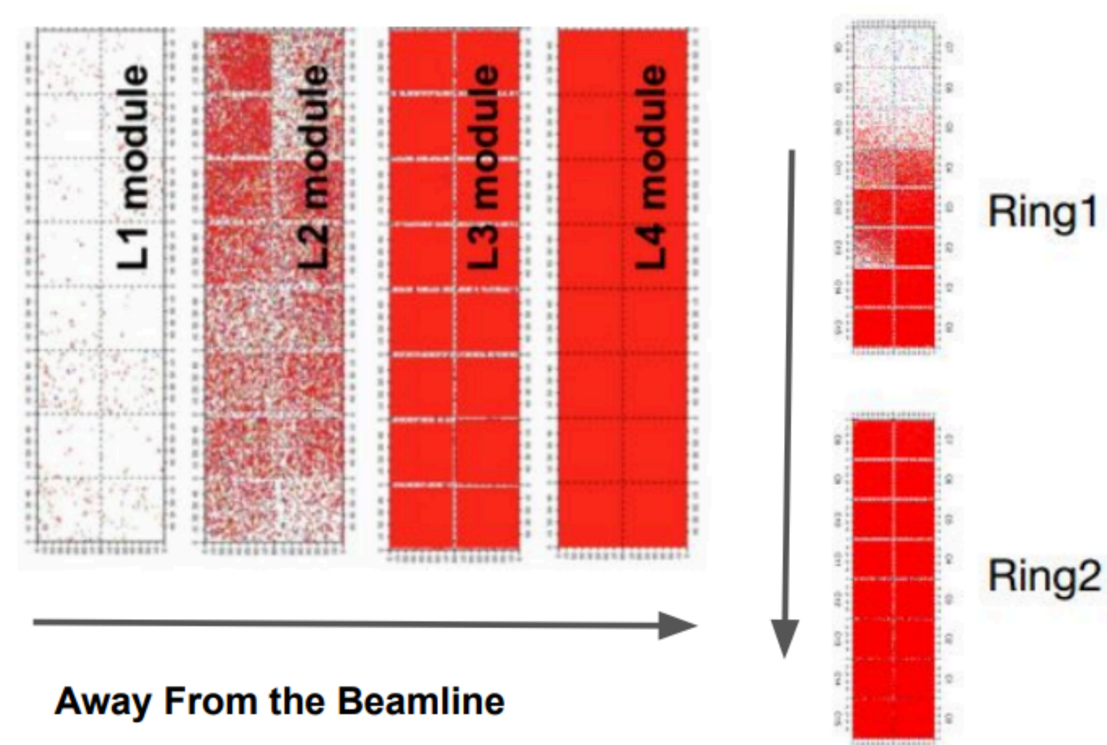
New production of DCDC converters with new version of FEAST chips for Run 3 solves the problem

Operation challenges in Run 2

- **DCDC damaged modules**
  - DCDC damaged modules were not correctly powered
  - sensor leakage current cannot be drained efficiently if the ROC is not powered
  - bias voltage (HV) ON and module power (LV) OFF leads to bad grounding
  - the leakage current is drained through the pre-amplifier, damaging the pre-amplifier and the module
  - the damage seems to accumulate with radiation and distance from beamline
  - 6 (accessible) Layer 1 modules replaced during 2017-18 YETS out of total 8 damaged modules in Layer 1
  - accessible DCDC-damaged modules in Layer 2 were replaced during LS2



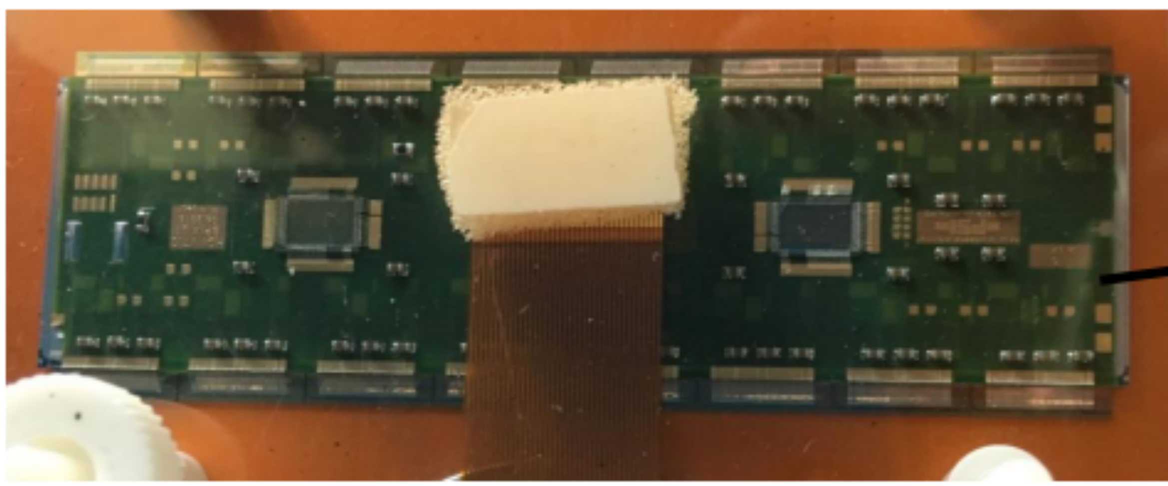
Damages due to HV on and LV off

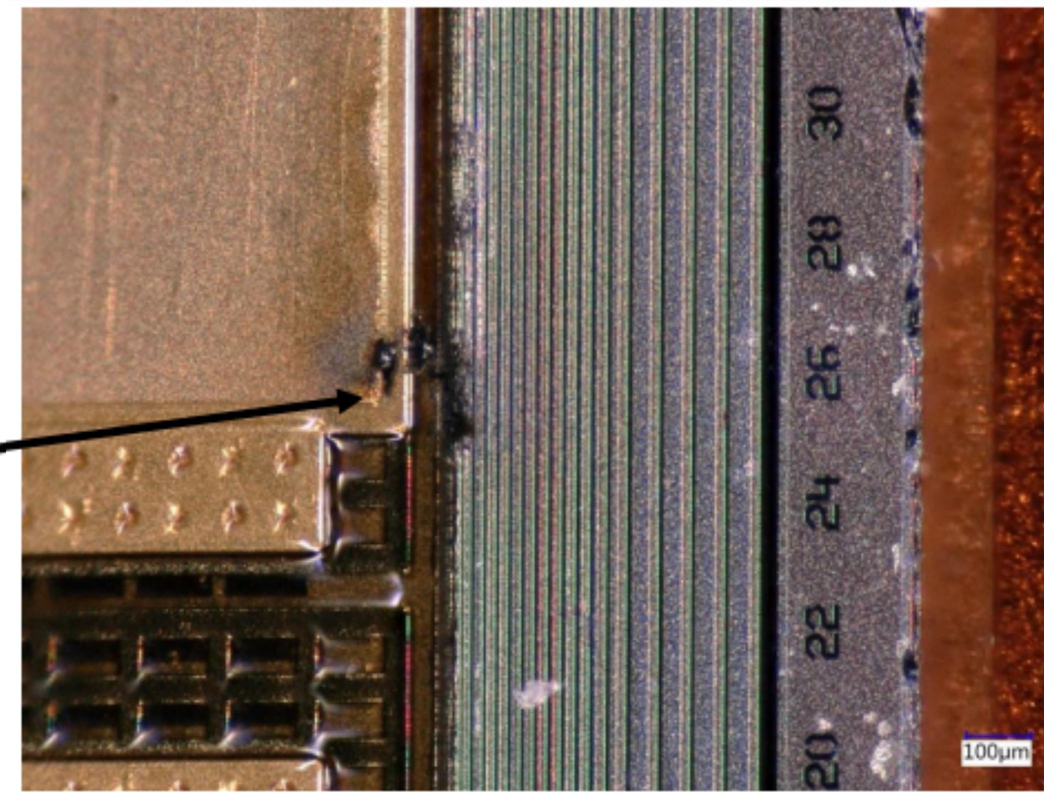


HV problems in Run 2

Problem:

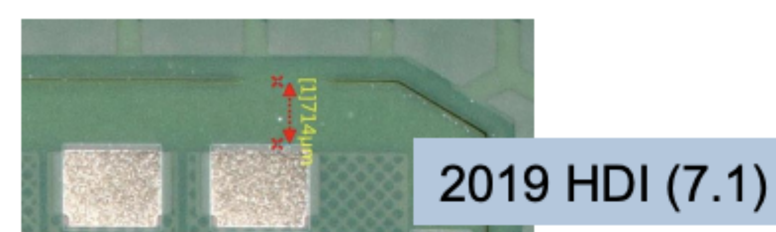
- the edge of the Layer 1 HDI was not covering the sensor enough, so a HV spark to pad ground could damage the module



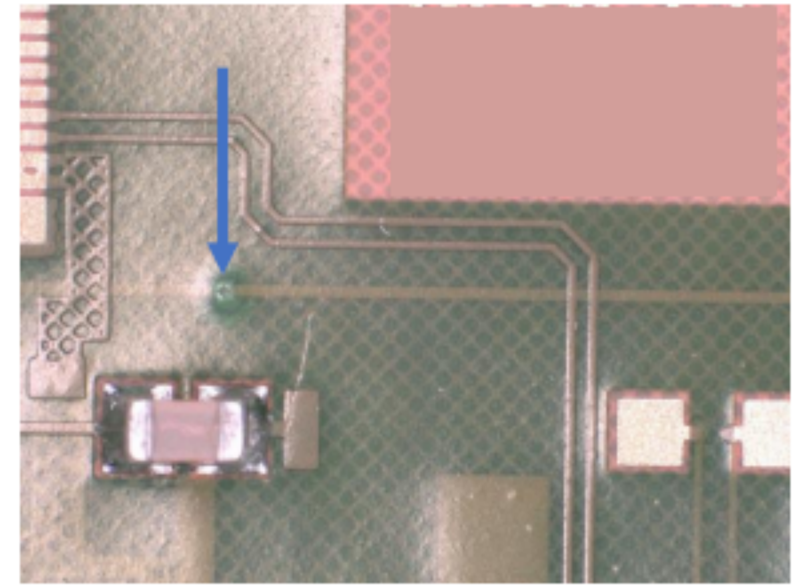


Solution:

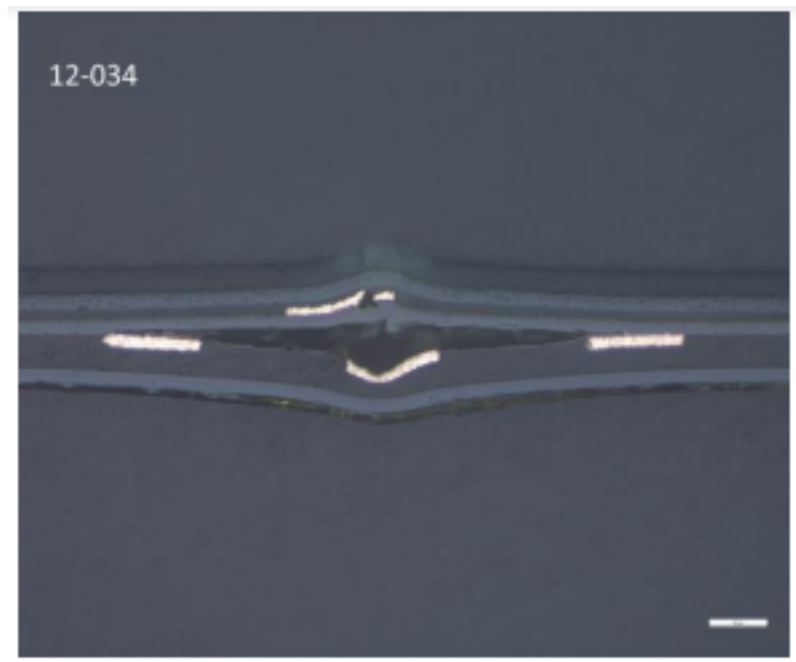
- for the new Layer 1 the HDI boarder was increased to cover the guard rings completely



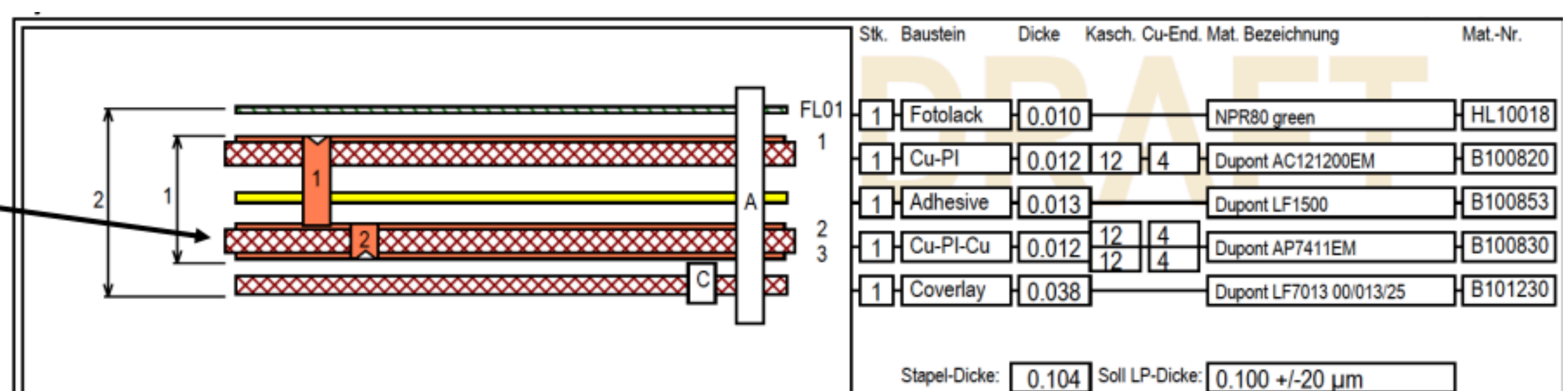
HV problems in Run 2



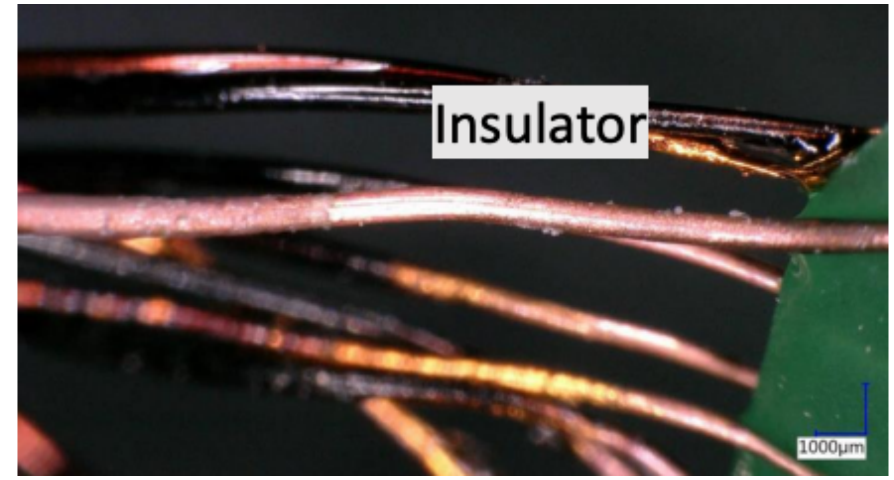
- While testing the new HDIs at 1100V (800V maximum in the detector, originally designed for 600V) a short occurred
- Further test showed that it’s not so difficult to break an HDI
  - humidity probably has an effect (or opening the test box)
- New HDI without a ground grid around the HV line
  - no problems observed for long testing at 1100V

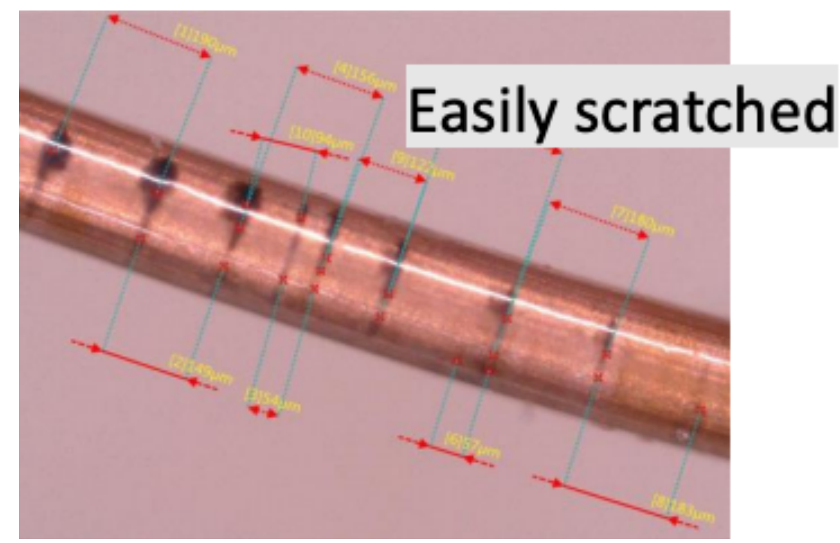


Insulator should hold 3kV

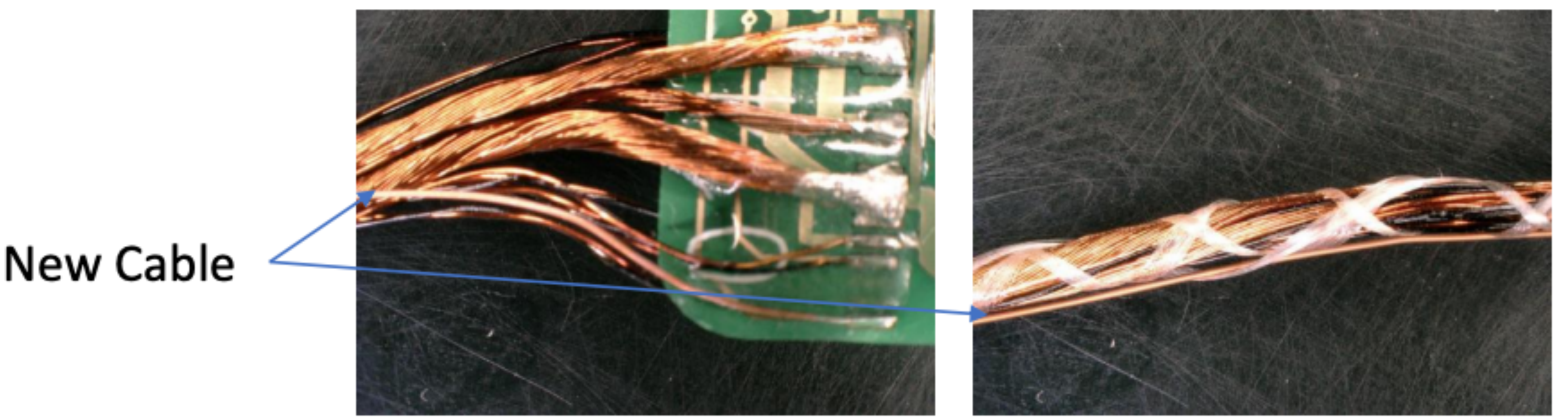


HV problems in Run 2

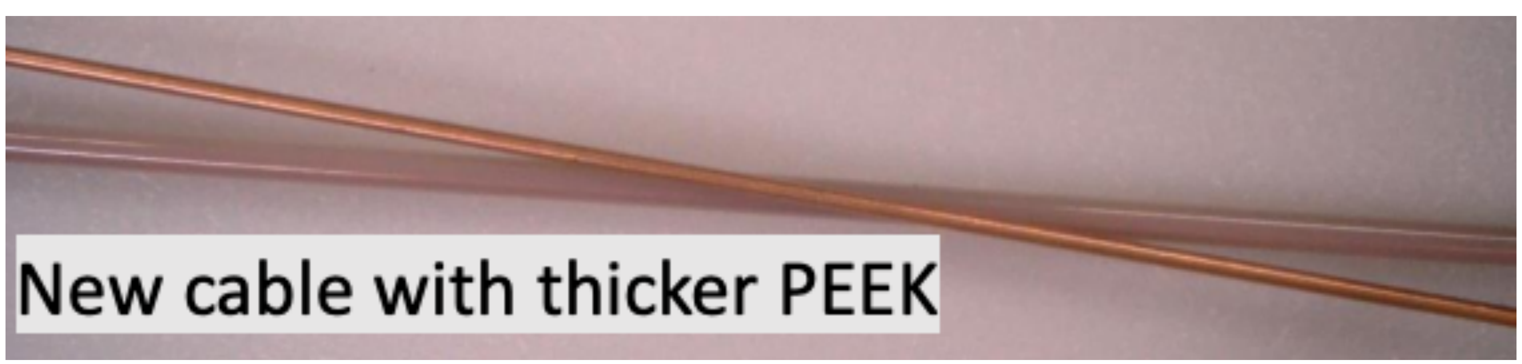




- New module cables showed HV problems:
  - insulator was stripped too far back
  - PEEK insulation was too susceptible for mechanical damage



- New thicker PEEK insulation solved both issues



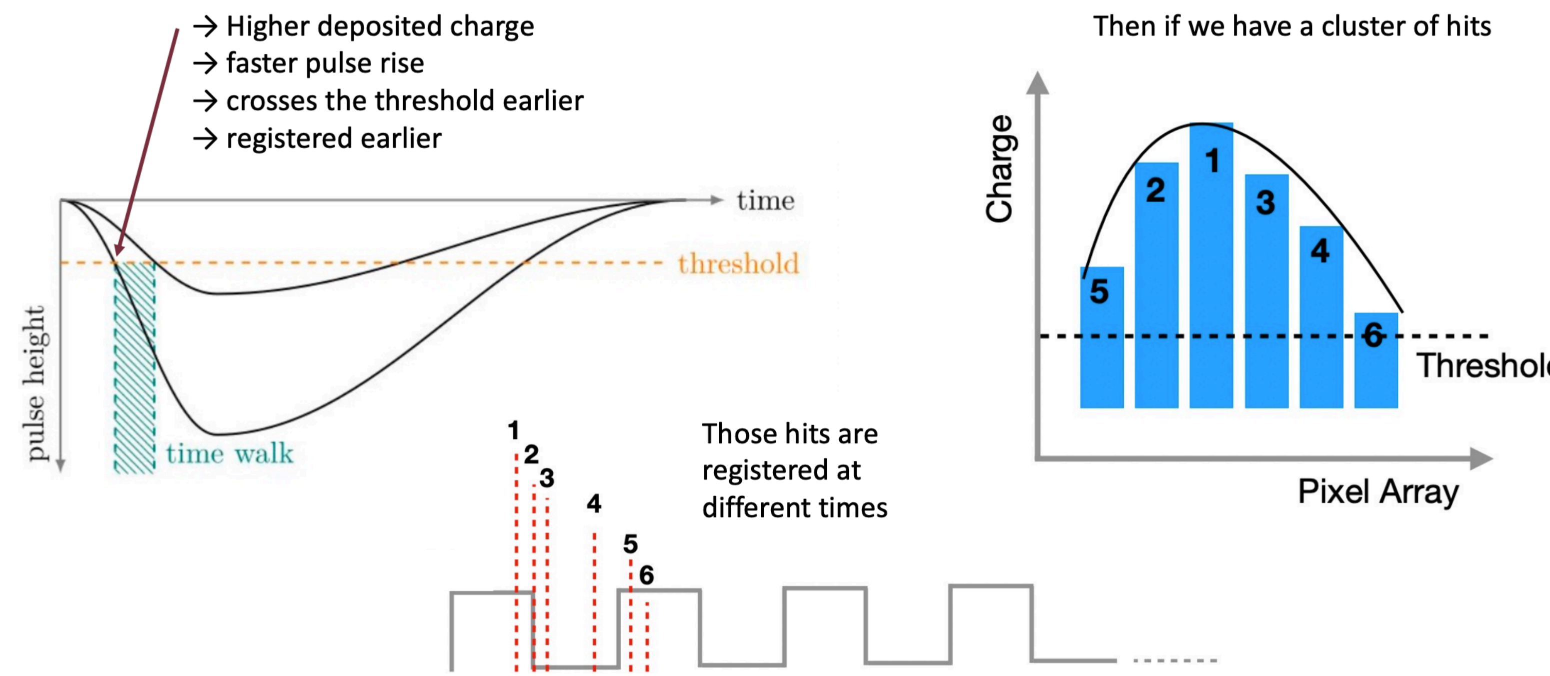
HV bias and timing scans

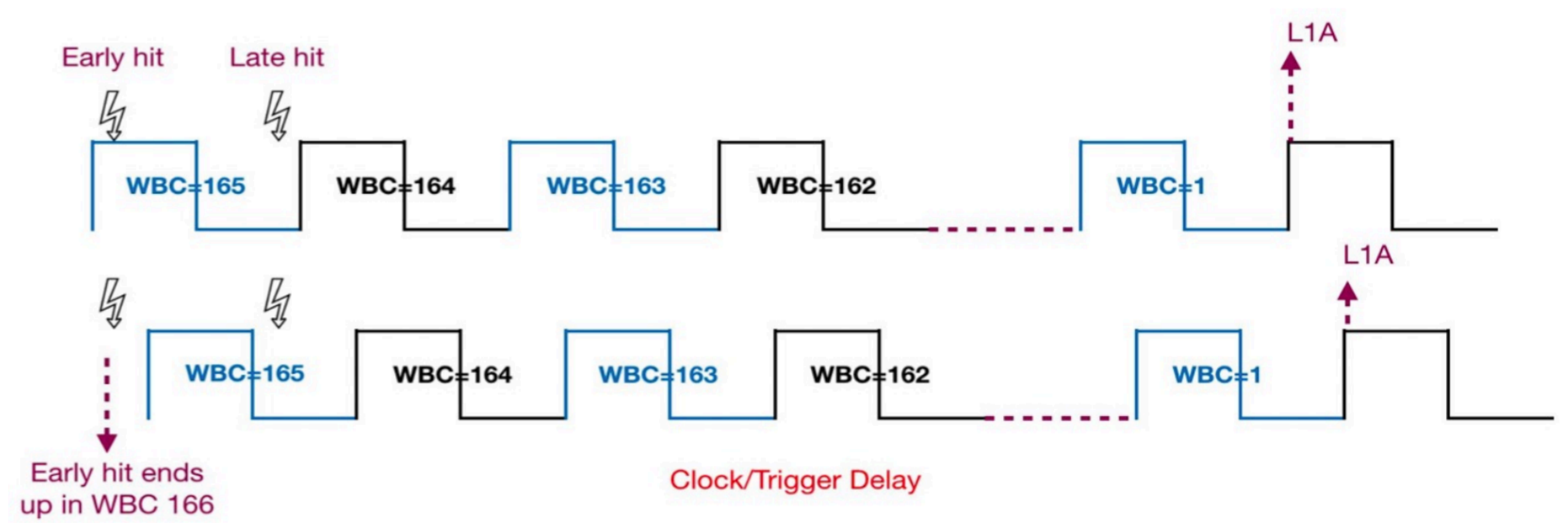
- Two types of **HV bias scan**:
  - full scan: on a full layer/disk - performed in special runs because bad data quality
  - mini scan: on a few non-overlapping modules (1 power group for each layer/ring on BPix/FPix) - performed during the data taking with negligible effect on the data quality
- The applied bias voltage is increased from zero to the operational/higher voltage and the changes in the hit efficiency and average normalized on-track cluster charge are followed
- Hit efficiency = probability to find any cluster within 1mm around an expected hit independent of the cluster quality (less affected by charge collection efficiency)
- The effect of radiation damage is visible in the shift of the plateau in different scans
- The complex evolution of the hit efficiencies with irradiation is understood to come from multiple effects some of which are the inversion of the charge carrier type in the silicon sensor and the annealing during the periods with no data-taking

- **Timing scan** over different values of (globalDelay25 and WBC) settings to find a delay that maximize cluster properties and hit efficiency
  - the timings of all layers are changed at the same time: if one layer is inefficient, the measurements of the cluster properties are affected by the missing layer and have large systematic uncertainty (intervals indicated by the shaded bands)
  - L1 is not displayed because it is needed for track seeding so the quantity proportional to hit efficiency is not well defined for L1

Timing scans

- The pixel detector is read out on receipt of a Level-1 Accept (L1A) signal
- Trigger delay = delay between the bunch-crossings and when the L1A arrives at the pixel ROCs
- Sources of delay:
  - dominant: Global trigger latency
  - other: fiber length, electronic response along the path
    - critical: not knowable exactly and vary among different readout groups
- Time-walk effect = hits that deposit low charge in the sensor are registered later than hits that deposit higher charge i.e. the registration time of hits is dependent on deposited charge





Residuals

Hit residuals measurement: Triplet method

- BPix:
  - pT > 12 GeV tracks with hits in 3 layers are selected and refitted using hits in two of three layers
  - trajectory extrapolated to remaining layer
  - triplets considered for Layer 3, propagated from hits on Layer 2 and 4
- FPix:
  - pT > 4 GeV tracks with hits in 3 disks are selected and refitted using hits in Disks 1 and 3
  - trajectory extrapolated to Disk 2
- residuals with the actual hit are calculated and residual distribution fitted with the Student-t function

Reconstruction

- Positions are reconstructed with two algorithms:
  - Generic: a simple algorithm based on track position and angle; used in our High Level Triggers (HLT) and early track iterations offline
  - Template: an algorithm based on detailed cluster shape simulations predicted by PixelAv; used in the final fit of each track in the offline reconstruction
- Observed residual distribution is the sum of the intrinsic detector resolution and a track extrapolation error (larger for lower pT tracks)
- The performance of the Template algorithm is seen to be better than the Generic algorithm