24th-28th October
VERTEX 2022
Tateyama Resort Hotel, Japan

TIME and SPace real-time Operating Tracker

Results on Sensors and Electronics and future perspectives

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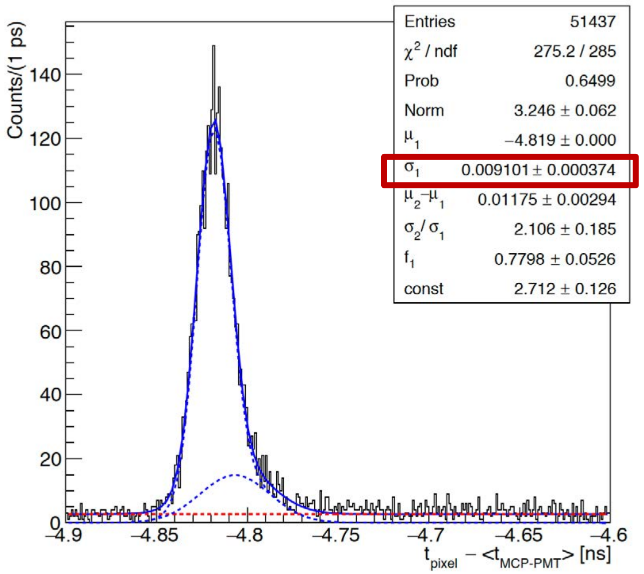
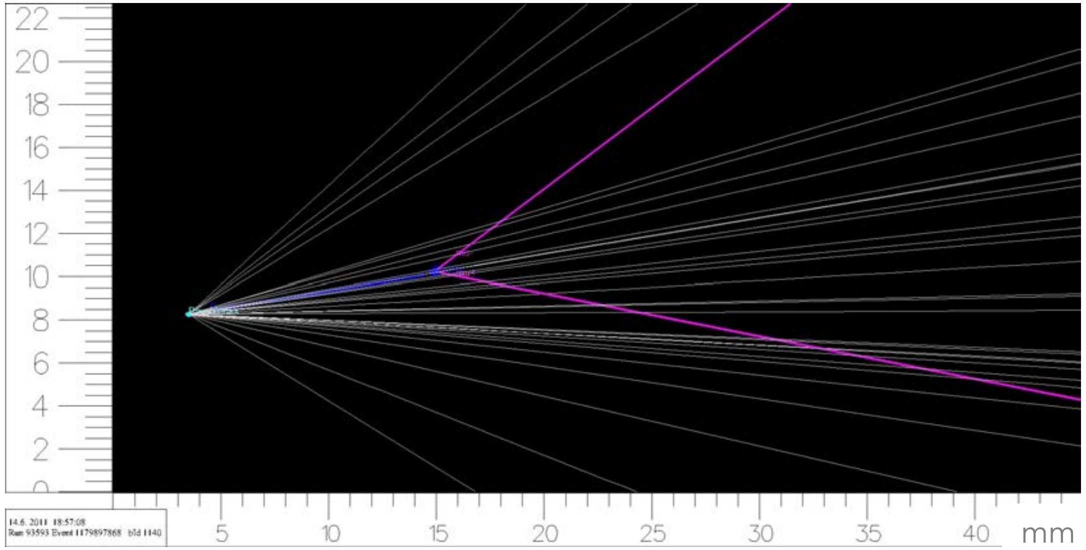


4D trackers/pixels: high density timing pixels

(beyond pile-up mitigation: when timing layers are not enough)

Plots from:
Considerations for the VELO detector at the LHCb Upgrade II – CERN-LHCb-2022-001

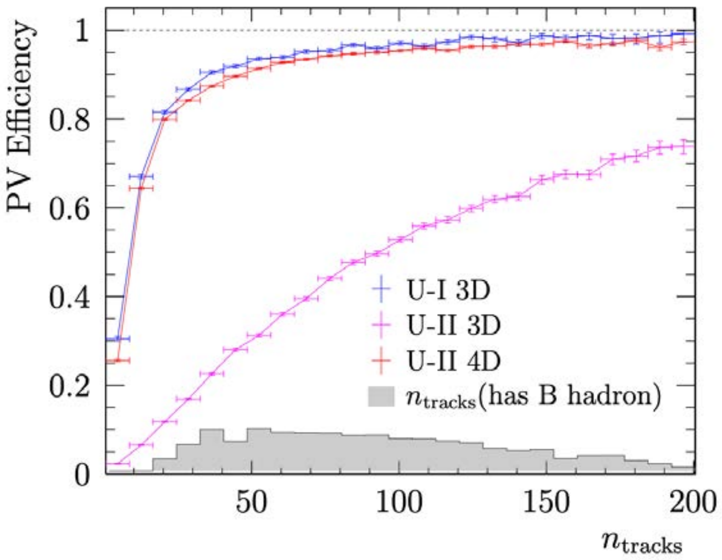
B_{0s} meson decaying into a μ^+ and μ^- pair



4D pixel:
A solid state pixel sensor (pitch ≈ 50 µm) bearing time information

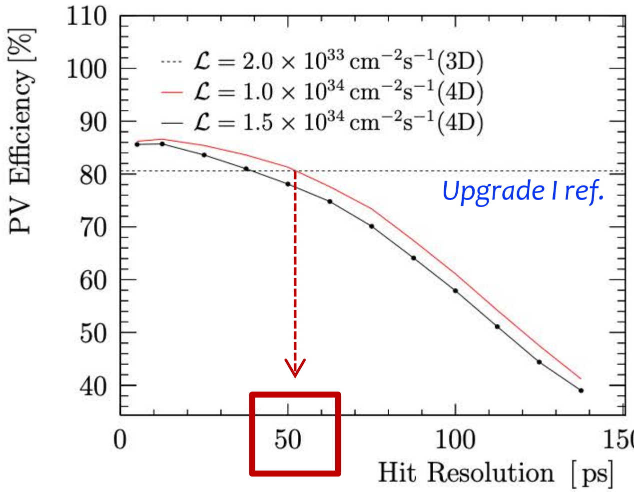
Track merging: bad Primary (and Secondary) Vertex reconstruction

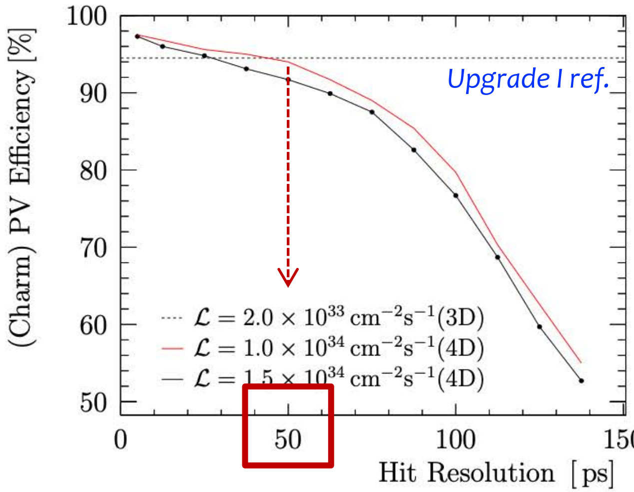
Incorrect PV assigned to tracks: poorly measured lifetime (dominant sistematic effect for time-dependent analysis)



Reconstruction efficiency vs the number of tracks per primary vertex, comparing the Upgrade I 3D reconstruction in both data conditions, and a variant using timing information to resolve the primary vertices

PV reconstruction efficiency as as function of the single hit resolution, for all vertices (left) and for vertices where at least one of the decay products is a charm hadron (right).





50 ps per hit (corresponding to 20 ps per track) are sufficient to recover the Upgrade-I efficiency

Crucial requirements for 4D-Tracking

A necessary tool for Physics at high intensity, in the **next generation of upgrades** in experiments at colliders: **LHCb Upgrade-II** (run5), **HIKE** (NA62 Upgrade), **CMS-PPS** (run4), **ATLAS AFP** (run5?), **ν–tagging**, **Pioneer** (proposal at PSI, π rare decays), **CMS endcap** (run5)… FCC-hh (far perspective)

1. **Space Resolution $\sigma_s \approx$ 10 μm**
2. **Time Resolution $\sigma_t \leq$ 50 ps per hit**
3. **Radiation hardness to high fluences $\Phi = 10^{16} \div 10^{17}$ 1 MeV n_{eq}/cm^2**
4. **Detection efficiency ε > 99% per layer tipically required (high fill factor)**
5. **Material budget must be kept below 1 ÷ 0.5 % radiation length per layer**

Fast and rad-hard sensors

Key requirements for read-out electronics:

1. **Pixel pitch ≈ 50 μm (unless amplitude information for CoG techniques is used)**
2. **Time Resolution $\sigma_t \leq$ 50 ps on the full chain ($\sigma_t = \sigma_{sensor} \oplus \sigma_{FE} \oplus \sigma_{TDC}$)**
3. **Radiation hardness TID > 1 Grad**
4. **Power budget per pixel ≈ 25 μW (referred to 55 μm pitch, 1.5 W/cm²)**
5. **Data BW ≈ 100 Gbps/cm²**

CMOS 28-nm electronics

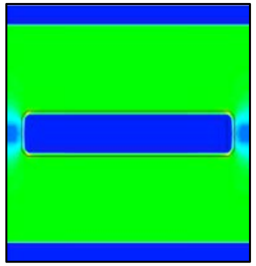
Results on 3D silicon sensors

Sensor fabrication @ FBK

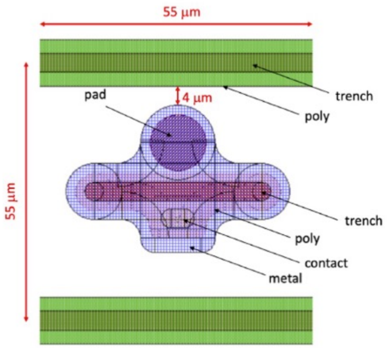
2 batches (2019 and 2020)

The optimal geometry

- 3D-trench
- 5 x 40 x 135 μm³ trench
- 150 μm pixel depth



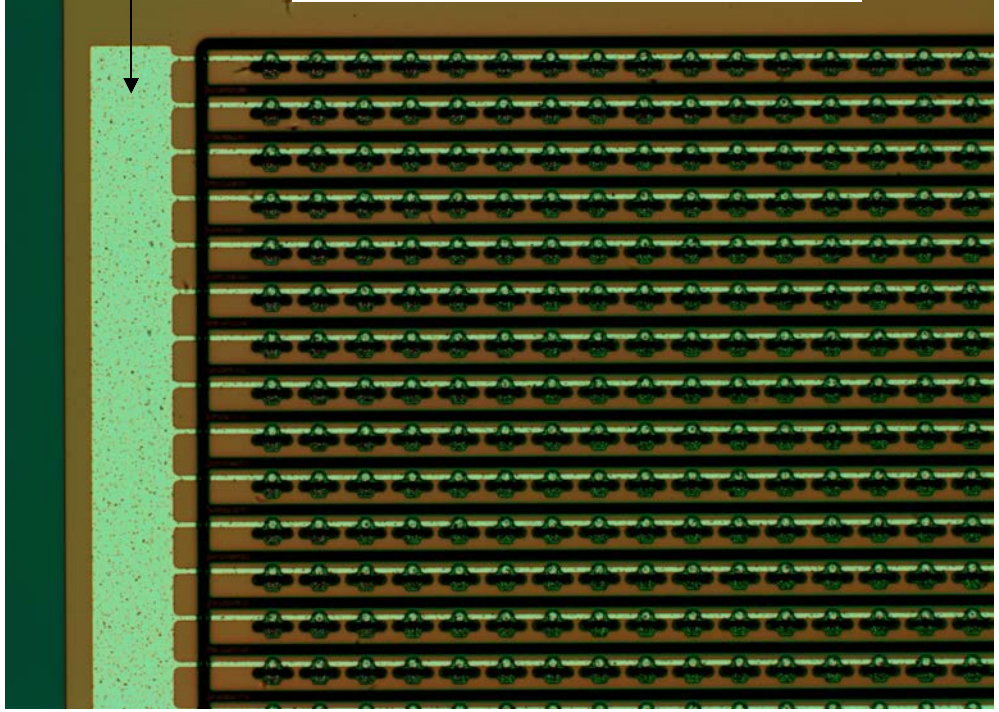
Pixel geometry



Pixel layout

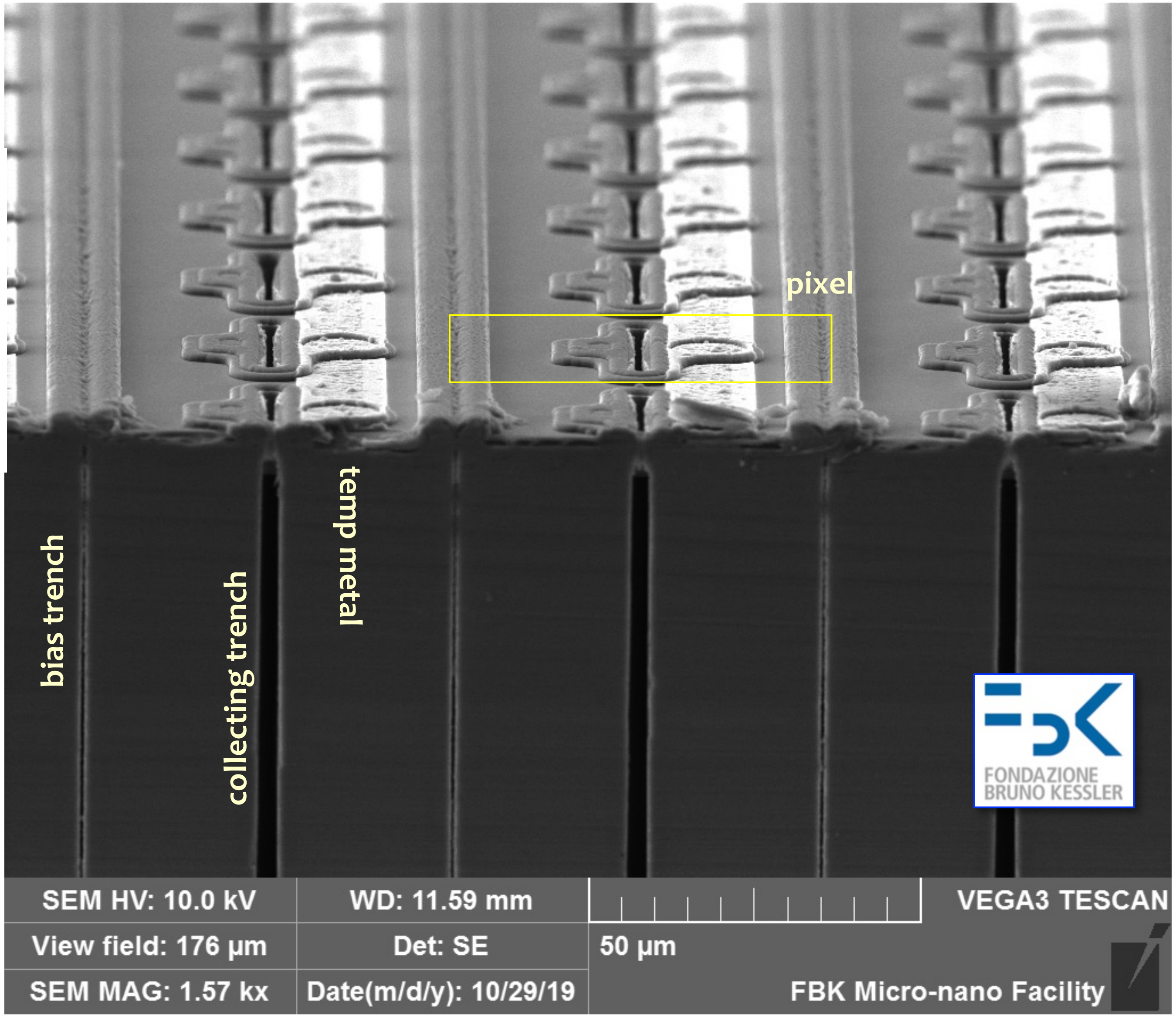
temp metal
for static tests

Matrix of 3D-trench sensors



collecting trench

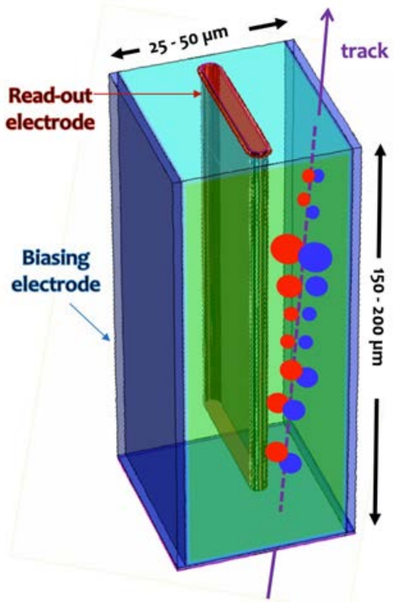
bias trench



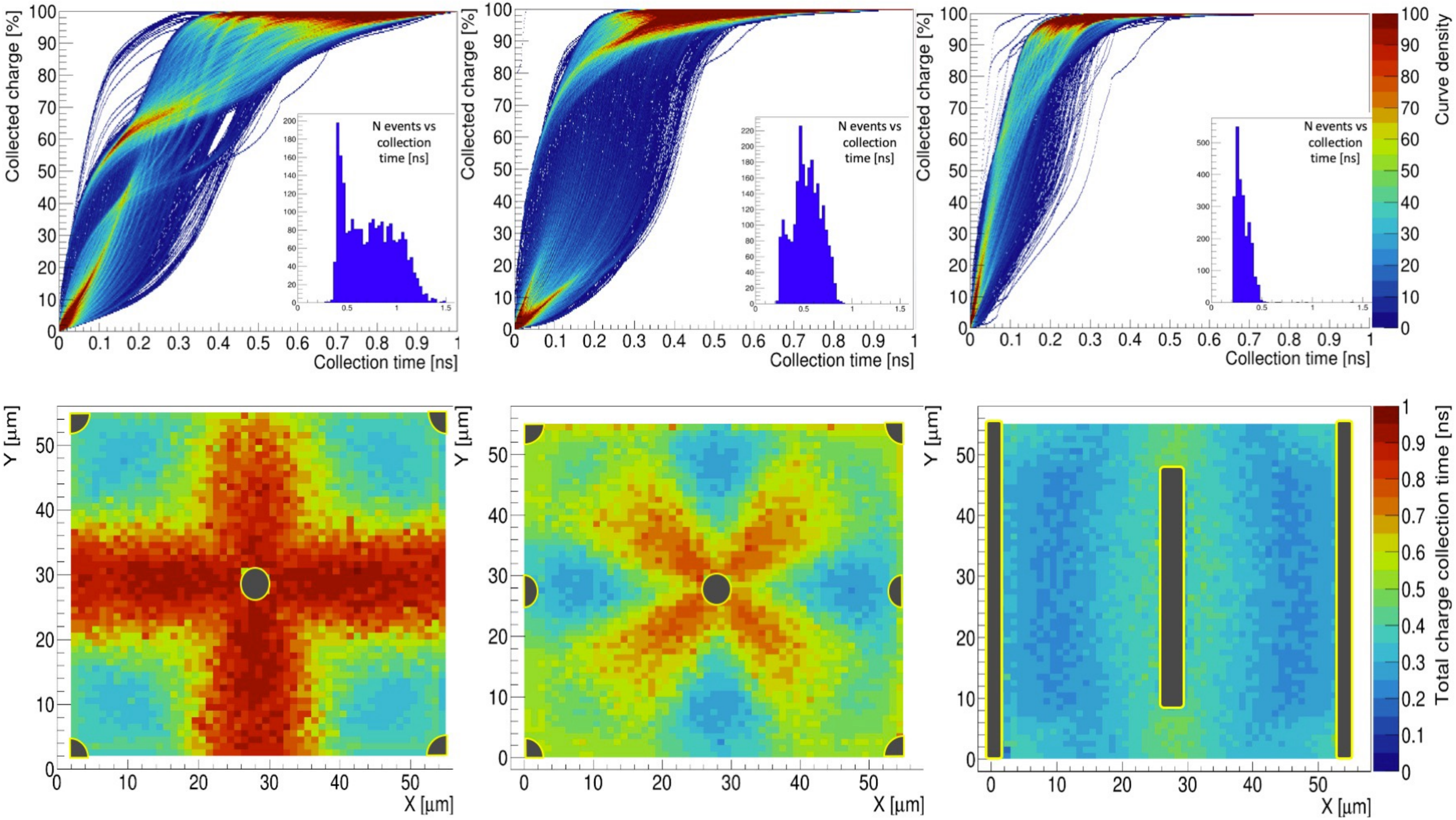
Deep Reactive Ion Etching
Bosch technology
(developed for MicroElectroMechanicalSystem technology)

Charge Collection Time in 3D sensors

Curves and maps



A "geometric sensor"



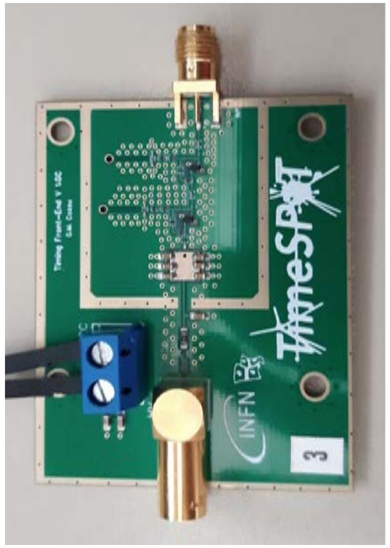
Time performance comparison among three different 3D geometries at $V_{bias} = -100V$. (Top) percentage of total charge collected on the electrodes versus time. (Top inserts) distribution of charge collection time for the three geometries. (Bottom) time for complete charge collection versus impact point for the same geometries. Each simulation is based on about 3 000 MIP tracks.

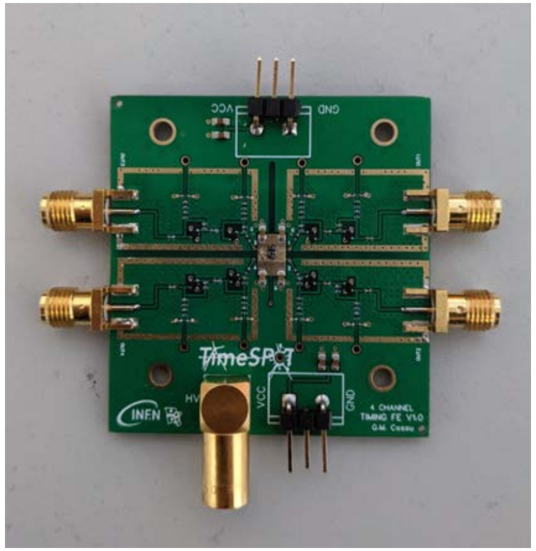
Latest results

Test-beams Nov21 & May-June 22 @SPS/H8

New faster dedicated front-end electronics

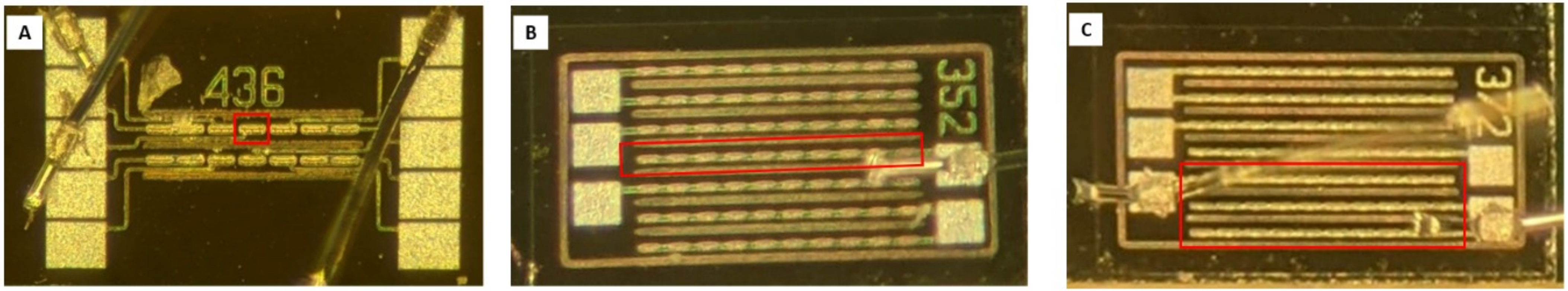
Si-Ge input stages $t_r \approx$ 100 ps. Measured *jitter* < 7 ps @ 2 fC
≈ 70 mW/channel





1. **Not-irradiated:**
   - **Landau distributions vs V_{bias}**
   - **Time resolution**
   - **Geometrical efficiency vs tilt angle**
   - **Time resolution vs tilt angle**
2. **Same with samples irradiated @ Φ = 2.5 10^{16} 1-MeV-n/cm²**
3. **First studies on charge sharing**

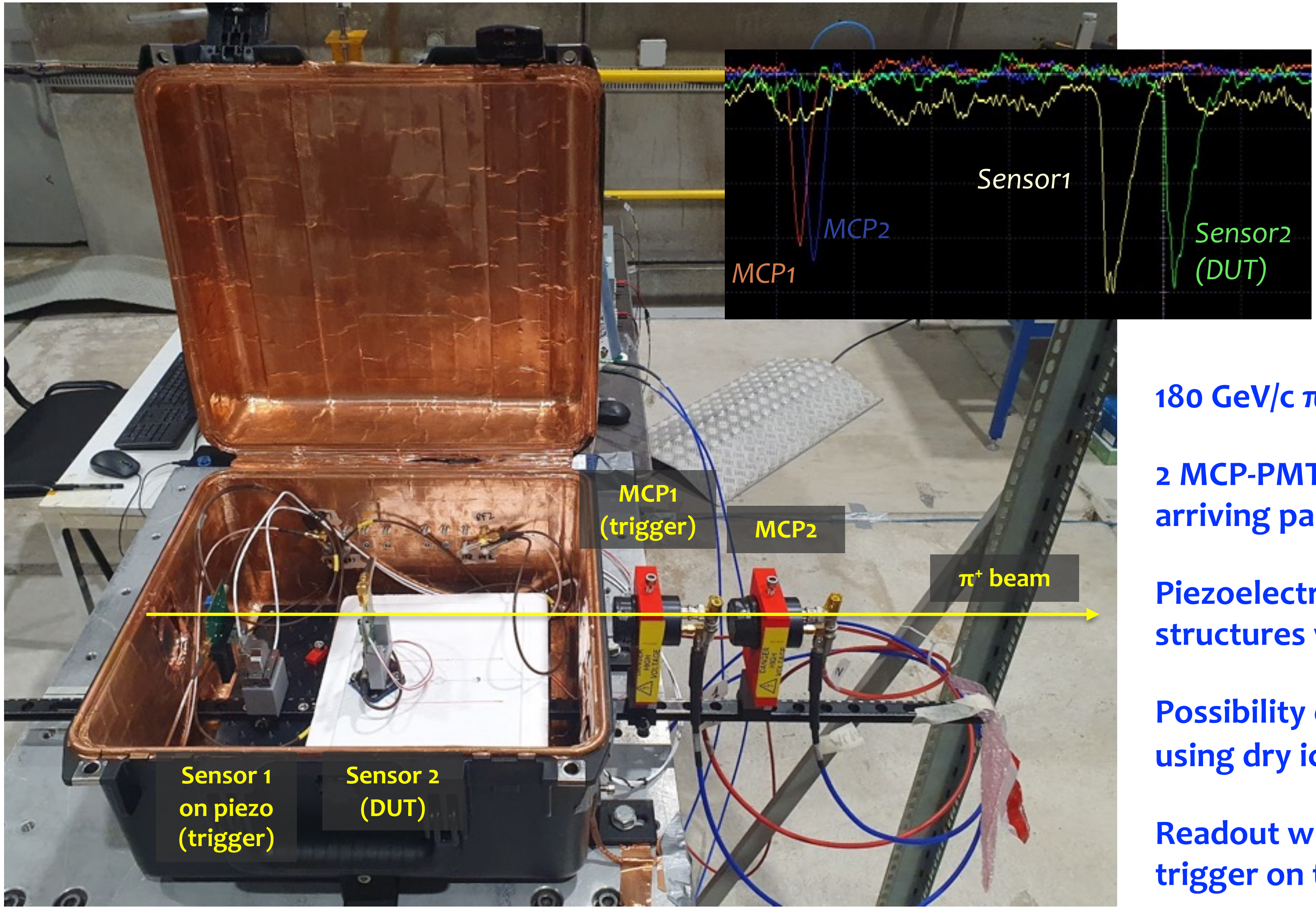
Tested structures. For each sensor the active area is shown in red.
(A) Single pixels sensor; (B) strip sensor; (C) triple strip sensor



Paper in preparation: "*New results on the TimeSPOT 3D-silicon sensors from measurements at SPS*" (Frontiers in Physics)

Experimental setup

Test-beams Nov21 & May22 @SPS/H8



180 GeV/c π^+ beam

2 MCP-PMTs on the beam line to time-stamp the arriving particle (σ_{avg} = 5 ps)

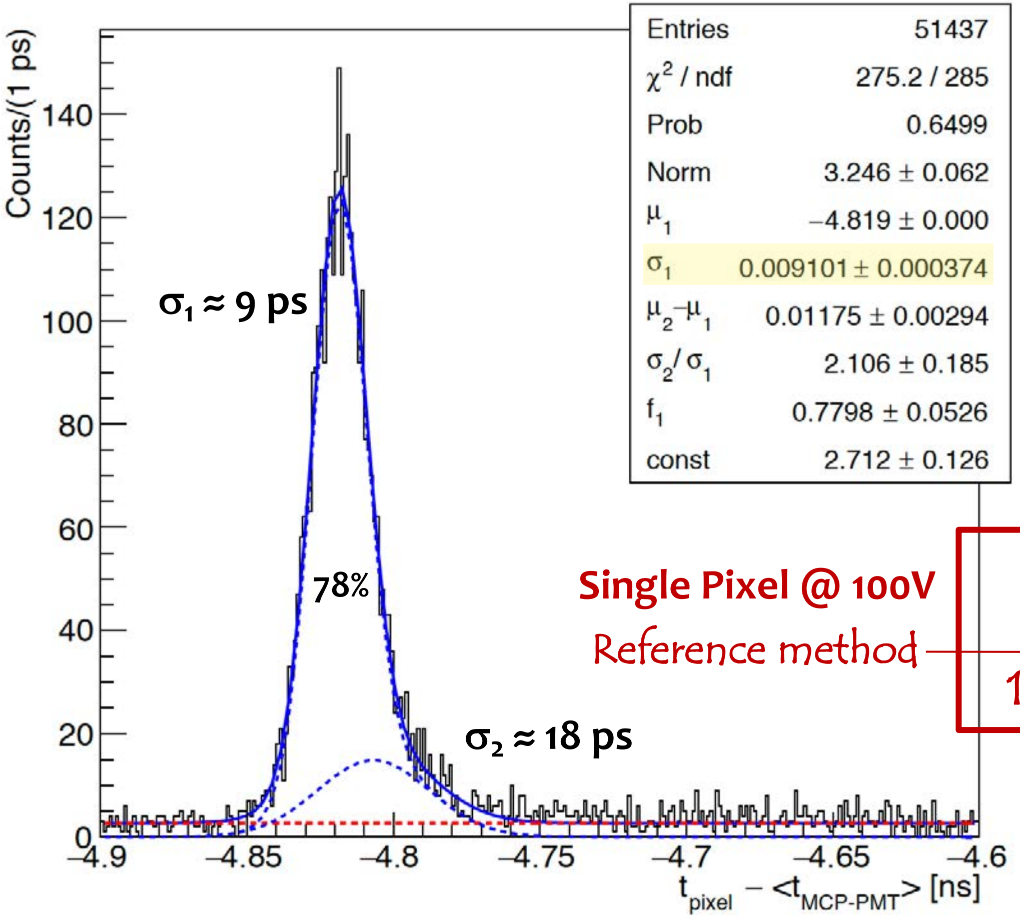
Piezoelectric stages to precisely align the two 3D structures with beam, all mounted in a RF-shielded box

Possibility of operating the fixed sensor down to -40°C using dry ice to test irradiated sensors

Readout with an 8 GHz bandwidth 20 GSa/s scope: trigger on the AND of one 3D sensor and one MCP-PMT

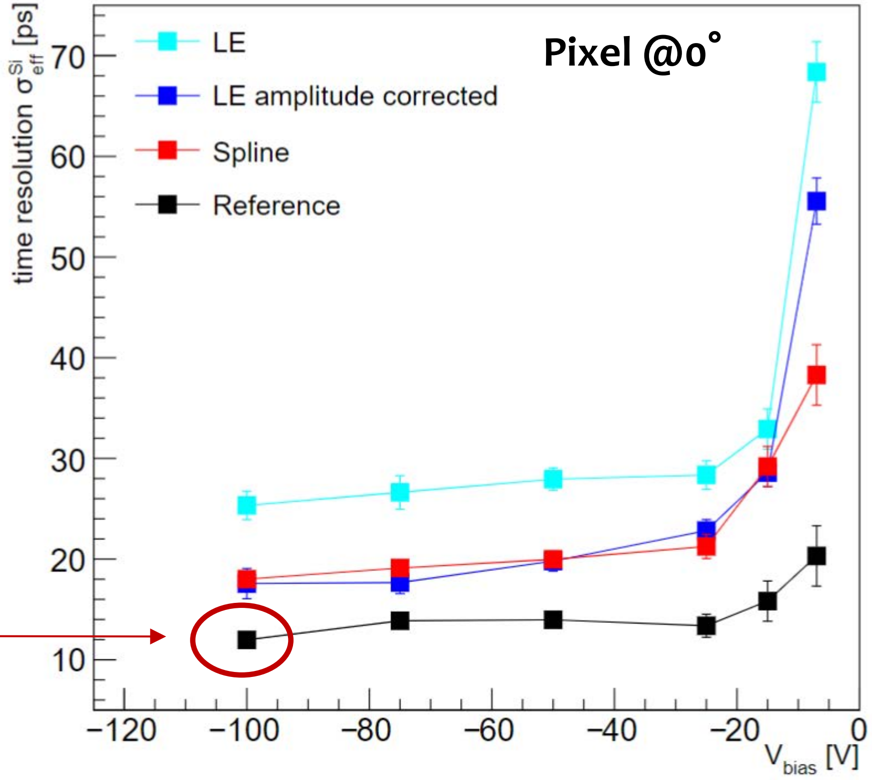
Timing measurements
(single pixel @ α_{tilt} = 0°, not irrad.)

LE: Leading edge, NO ToT correction
LE: Leading edge, ToT correction
Spline: Classic CFD
Reference: Differentiation + CFD



Single Pixel @ 100V
Reference method

σ_t^{eff}
11.5 ps



$$(\sigma_t^{eff})^2 = f_1(\sigma_1^2 + \mu_1^2) + (1 - f_1)\cdot(\sigma_2^2 + \mu_2^2) - \mu^2$$

Where f_1 is the fraction of the core Gaussian and μ is defined as

$$\mu = f_1\mu_1 + (1 - f_1)\cdot\mu_2$$

σ_t^{eff} **takes into account the two-Gaussian behaviour**

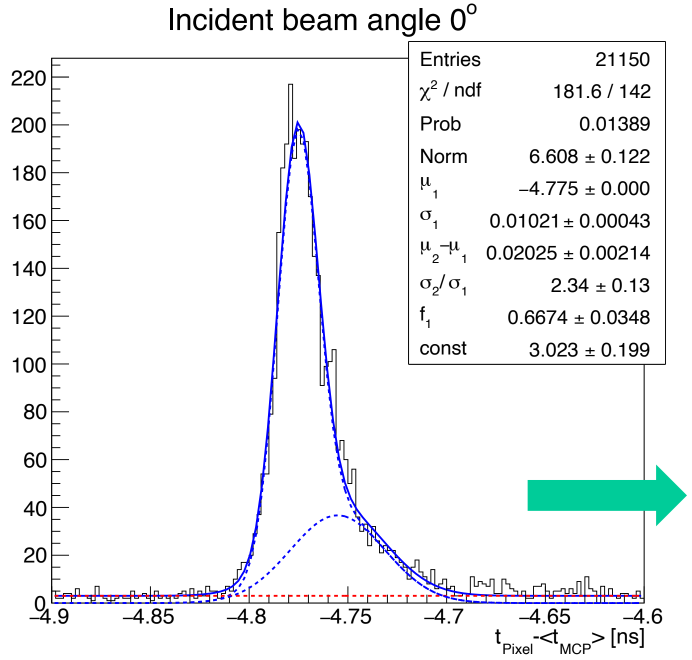
Distribution of the difference between the TOA of the single pixel and the time reference, $t_{pixel} - \langle t_{MCP-PMT}\rangle$, for the single pixel perpendicular to the beam at V_{bias} = −100 V with the reference method. The distribution is fit with the sum of two Gaussian functions (blue dashed lines) describing the signal, and a constant (red dashed line) modelling the background.

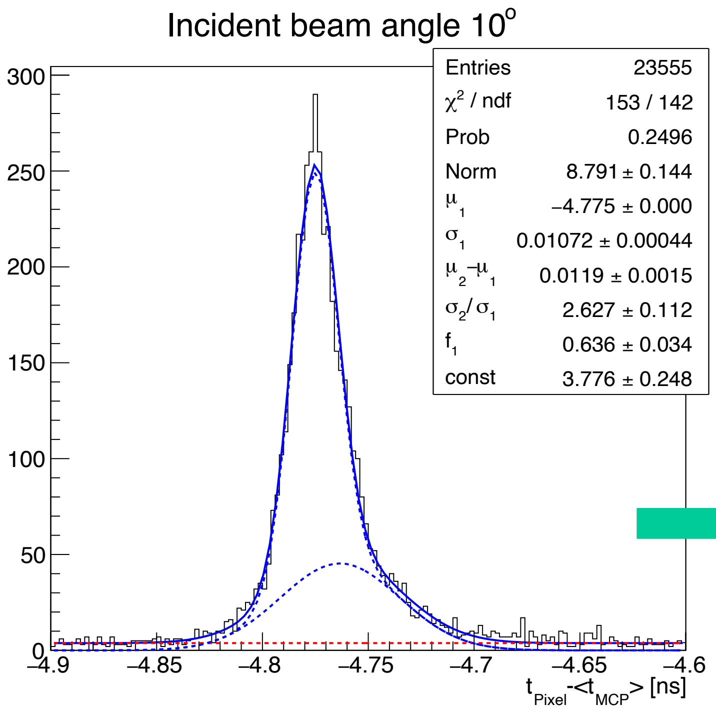
Paper to be submitted soon to Frontiers in Physics: *"New results on the TimeSPOT 3D-silicon sensors from measurements at SPS"*

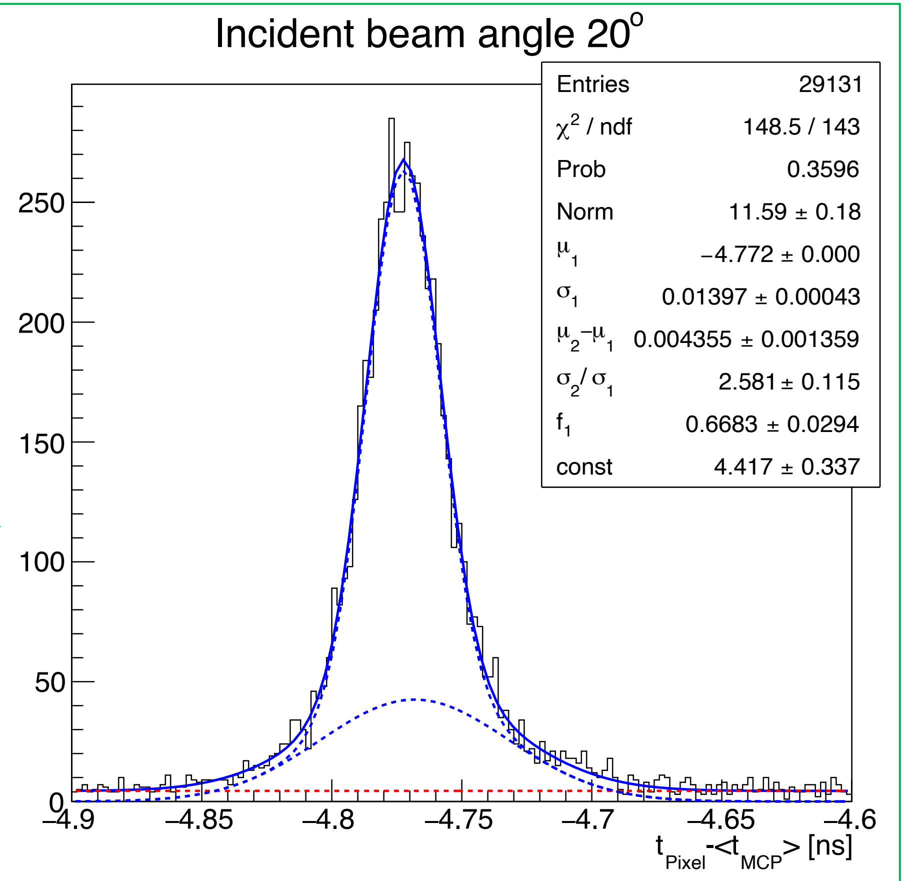
Effect of tilting on distribution shapes

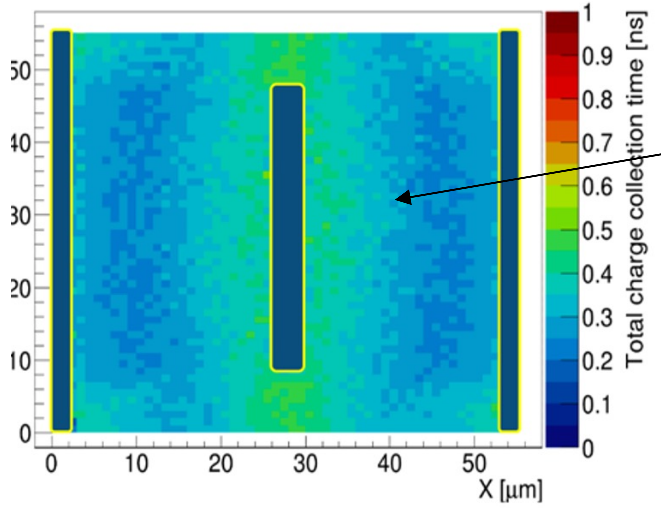
Spline method, SPS/H8 (Nov'21)

Single Pixel @ 50V





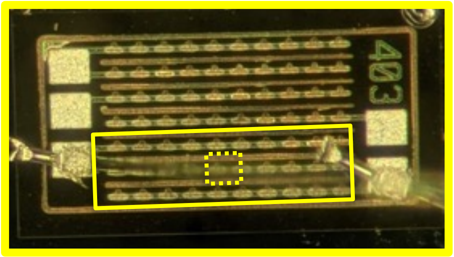


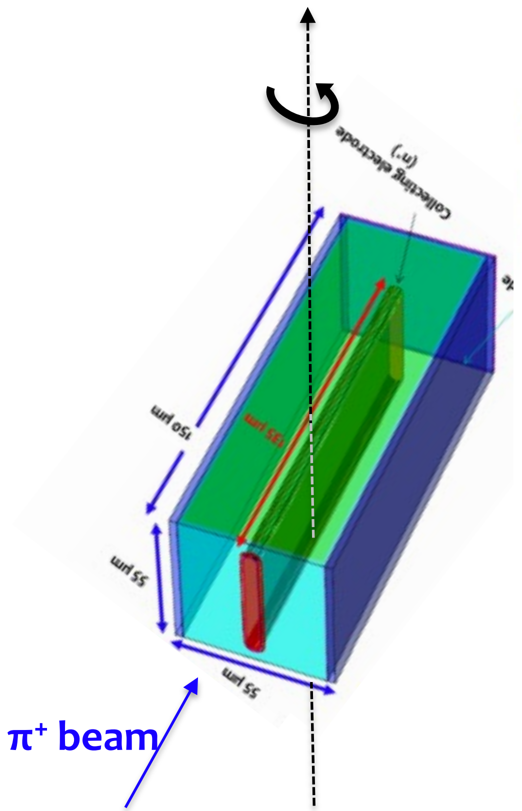


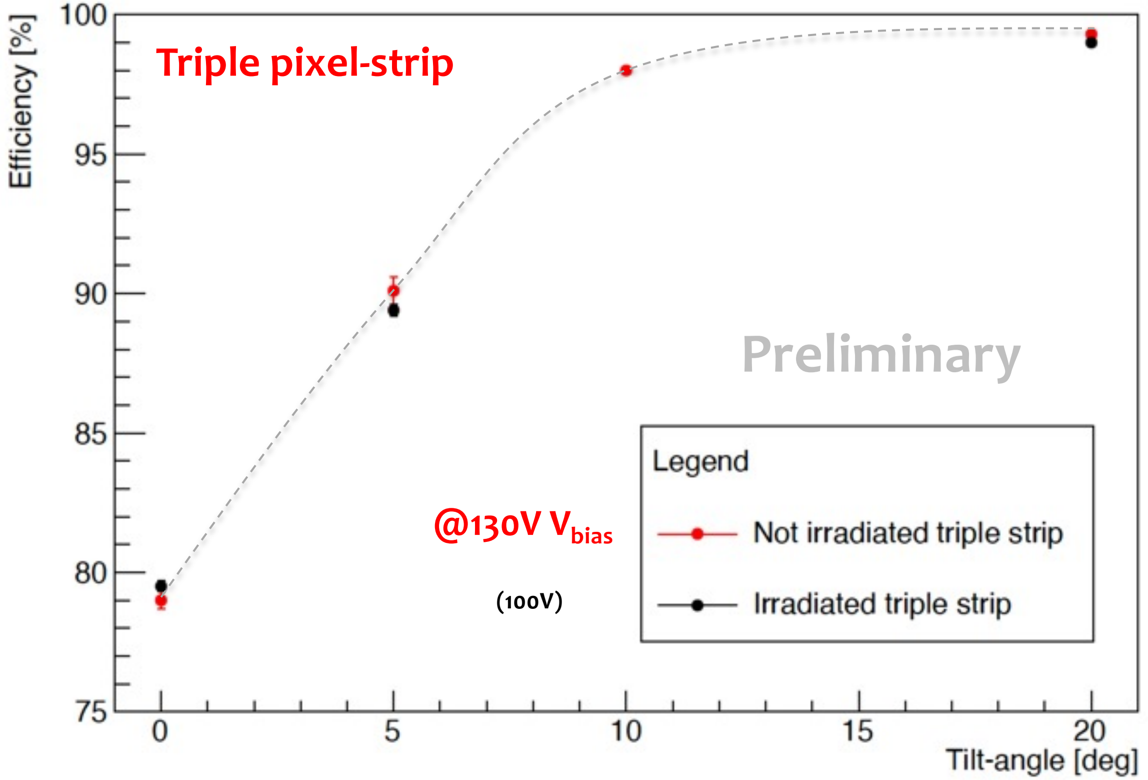
Simulated CCT map of a single 3D-trench sensor pixel scan (α_{tilt} = 0°)

Tilting has the effect of «mixing up» the fast and less-fast regions of the pixels, thus uniforming the timing response
As a result, the shapes are more Gaussian at increasing α_{tilt}
Notice that, due to detection efficiency, α_{tilt} = 20° is the normal working condition of a 3D in a detecting system

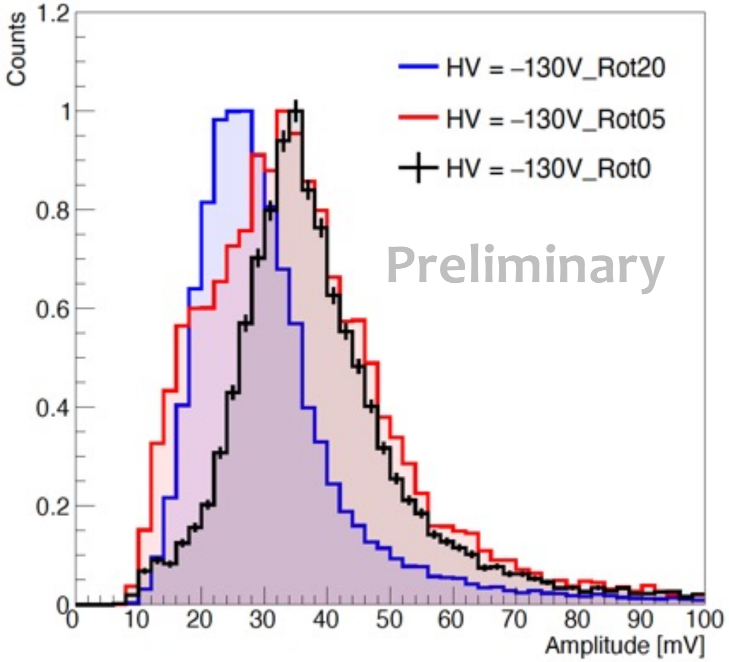
Irradiated sensors: geometrical efficiency







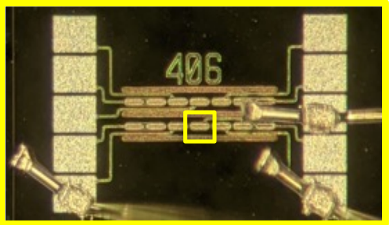
Triple strip @ 2.5 10^{16} n_{eq}/cm^2 , α_{tilt} = 0°, 5°, 20°



The inefficiency (at normal incidence) due to the dead-area of the trenches is fully recovered by tilting the sensors around the trench axis

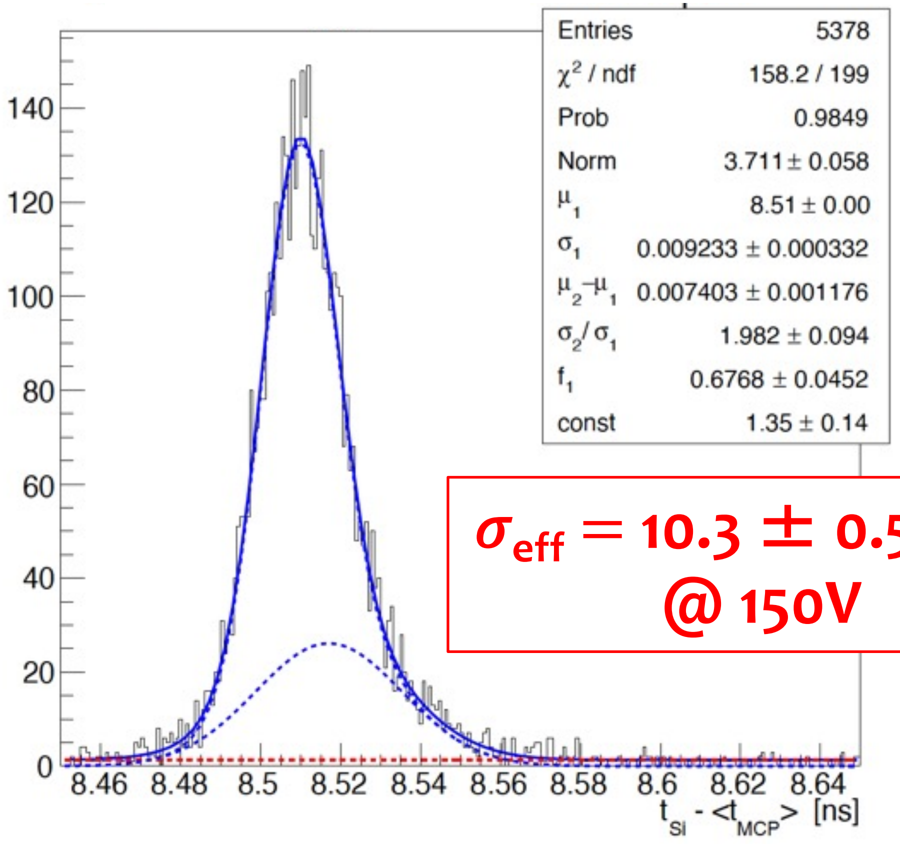
also for sensors irradiated with fluences of $2.5\cdot10^{16}$ 1-MeV neutron equivalent

Irradiated sensors: timing performance

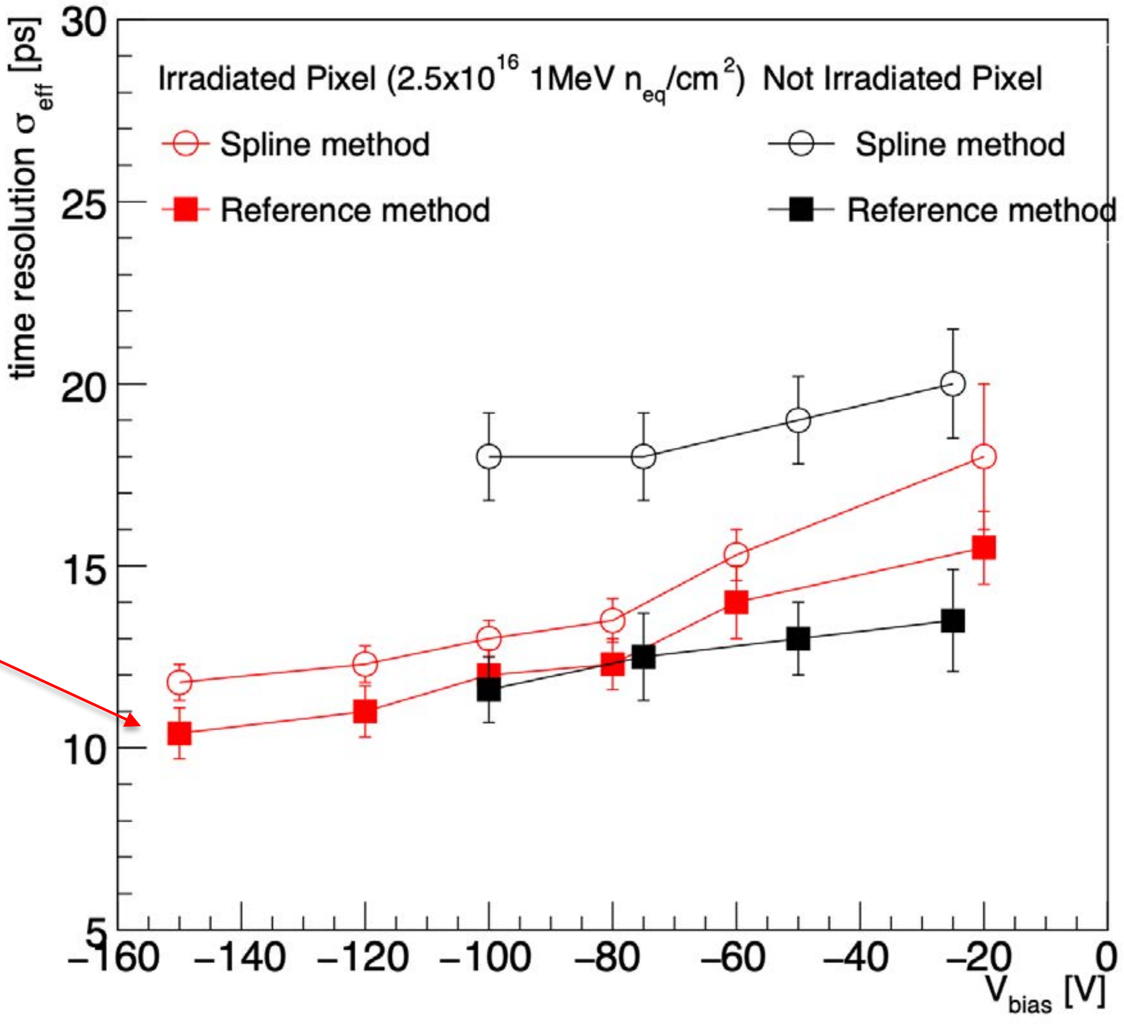


Irradiated @ 2.5 10^{16} n_{eq}/cm^2 , α_{tilt} = 0°

$\sigma_1 \approx 9$ ps
$\sigma_2 \approx 18$ ps



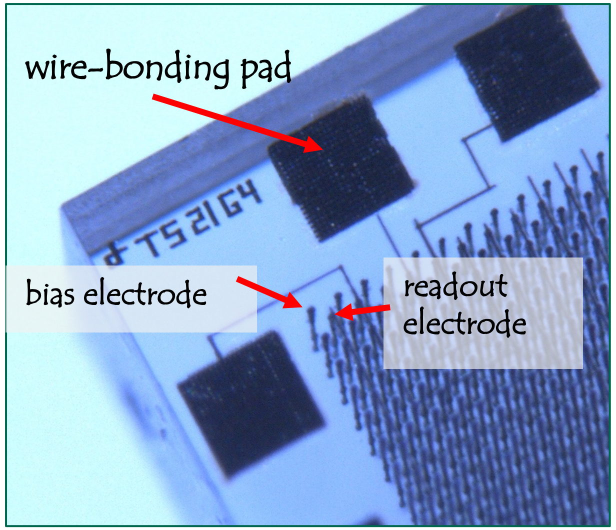
$\sigma_{eff} = 10.3 \pm 0.5$ ps
@ 150V



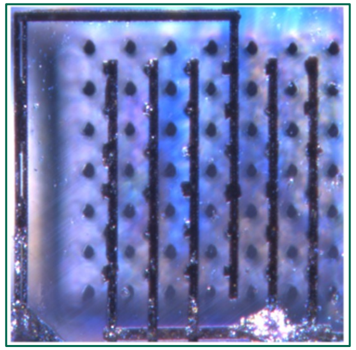
To be compared with 11 ps @ 100 V of the not-irradiated case

Time resolution of 3D-column diamond sensors

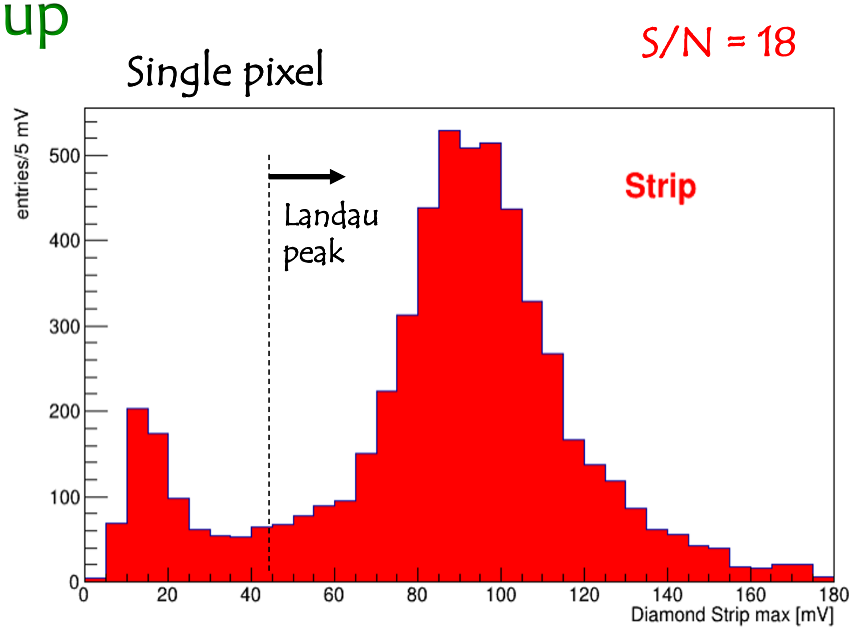
By TimeSPOT Firenze group

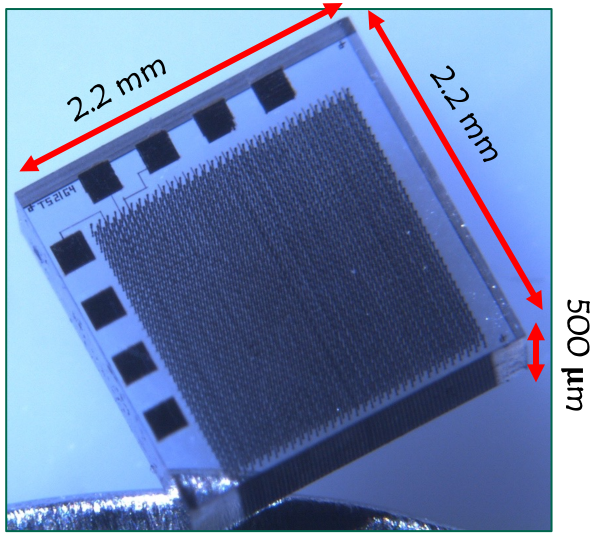


Prototype 32x32 55x55 μm^2 sensor for test-beam

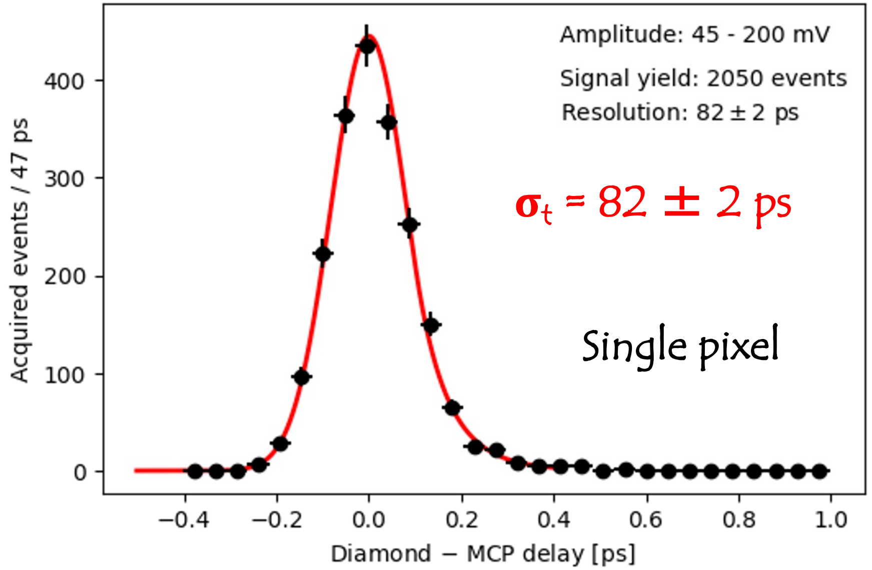


TimeSPOT Silicon pixel or strip used for trigger and scanning of the diamond sensor

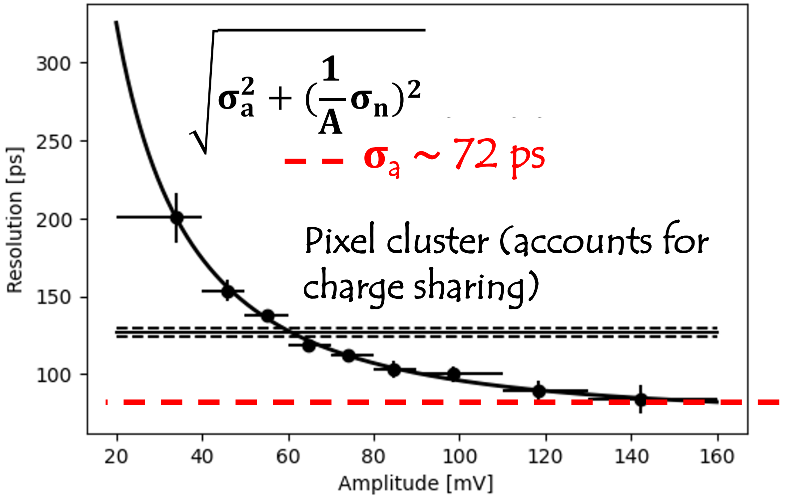




Single crystal CVD diamond by E6



Time resolution

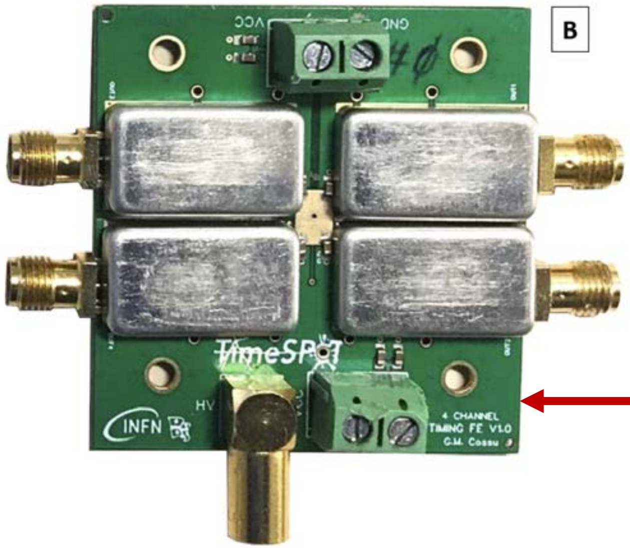


σ_a gives an estimate of the intrinsic sensor resolution

Results on CMOS 28-nm electronics

CMOS 28-nm for pixels with timing capabilities

When system constraints come into play



BUT:

Rate constraints
Area constraints
Data BW constraints
Power constraints

Intrinsic sensor performance measured by means of HBT Si-Ge input stages – discrete components
Measured $t_r \approx 100$ ps, $\sigma_{ej} \approx 7$ ps @ 2 fC (1 MIP), 900 fs @ 20 fC, 70 mW/channel

Why CMOS 28–nm? (last "bulk" CMOS node)

1. Higher integration capabilities w.r.t. 65 nm (TDC)
2. Higher speed
3. Higher radiation resistance (≥ 1 Grad)
4. It appears to be more rad-hard than subsequent (still very expensive) finFET technologies (es. 16 nm)
5. Extended availability w.r.t. 65 nm

A first complete set of «balanced HEP requirements»

Requirement	scenario S_A	scenario S_B
Pixel pitch [μm]	≤55	≤42
Lifetime fluence [1×10^{16} 1 MeV n_{eq}/cm^2]	> 6	> 1
TID lifetime [MGy]	> 28	> 5
Sensor Timestamp per hit [ps]	≲ 35	≲ 35
ASIC Timestamp per hit [ps]	≲ 35	≲ 35
Hit Efficiency [%]	≥ 99	≥ 99
Power per pixel [μW] (1.5 W/cm²)	≲ 23	≲ 14
Pixel rate hottest pixel [kHz]	> 350	> 40
Max discharge time [ns]	< 29	< 250
Bandwidth per ASIC of 2 cm^2 [Gb/s]	> 250	> 94

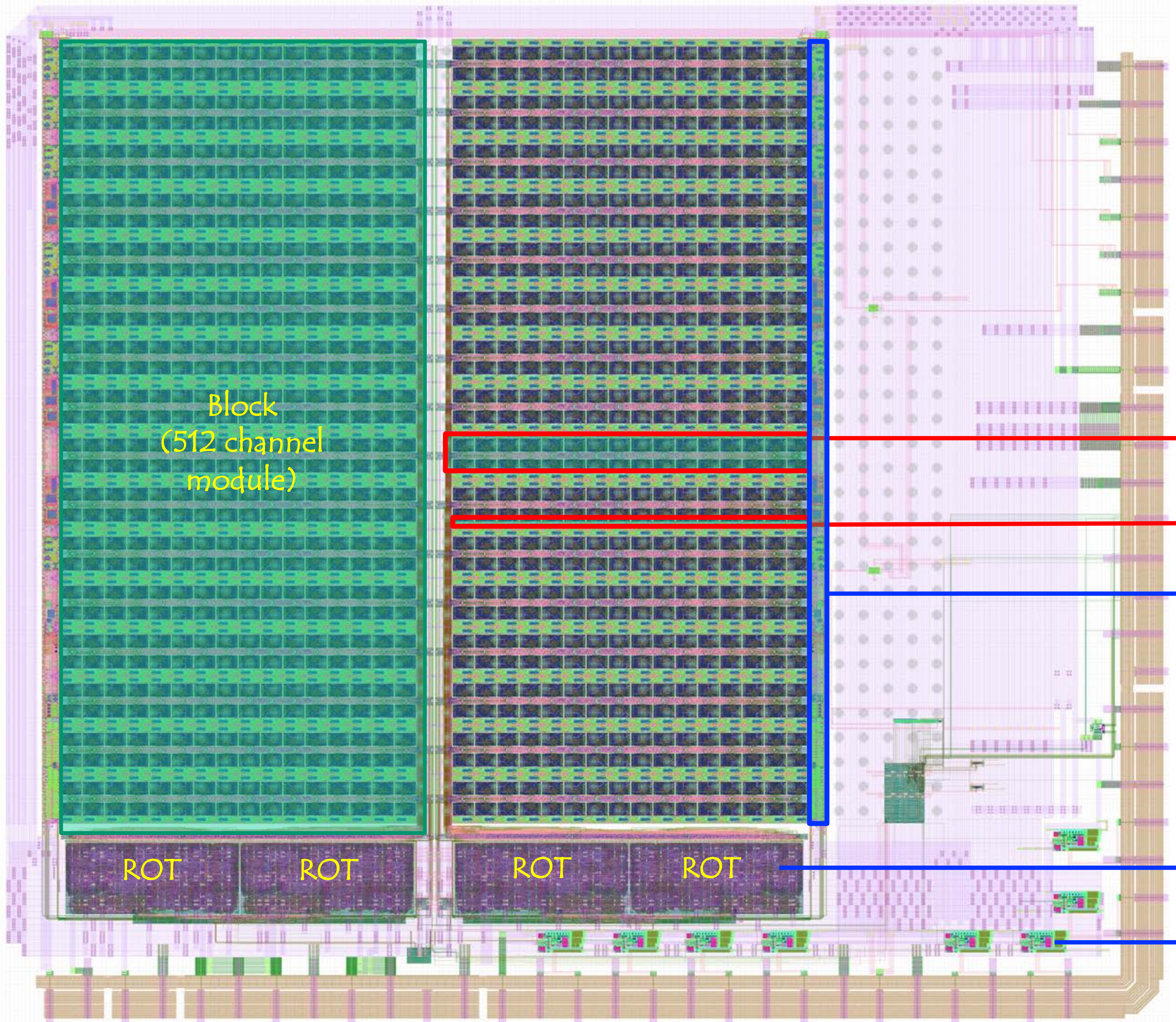
LHCb-U2 specs from physics needs. VELO support document for FTDR

The toughest constraint against speed is power budget, originating from the (un)capabilities of our best cooling system techniques at present (micro-channelling CO_2)

Timespot1 ASIC

28-nm CMOS

- Reduced size (1024 pixels, 6 mm²)
- HPC flavour
- Complete set of functionalities for pixel readout
- Slow read-out (demo-test purpose)



640 MHz master clock

Digital row: 16x2 TDC
+ Controls, Conf. registers, I²C I/F

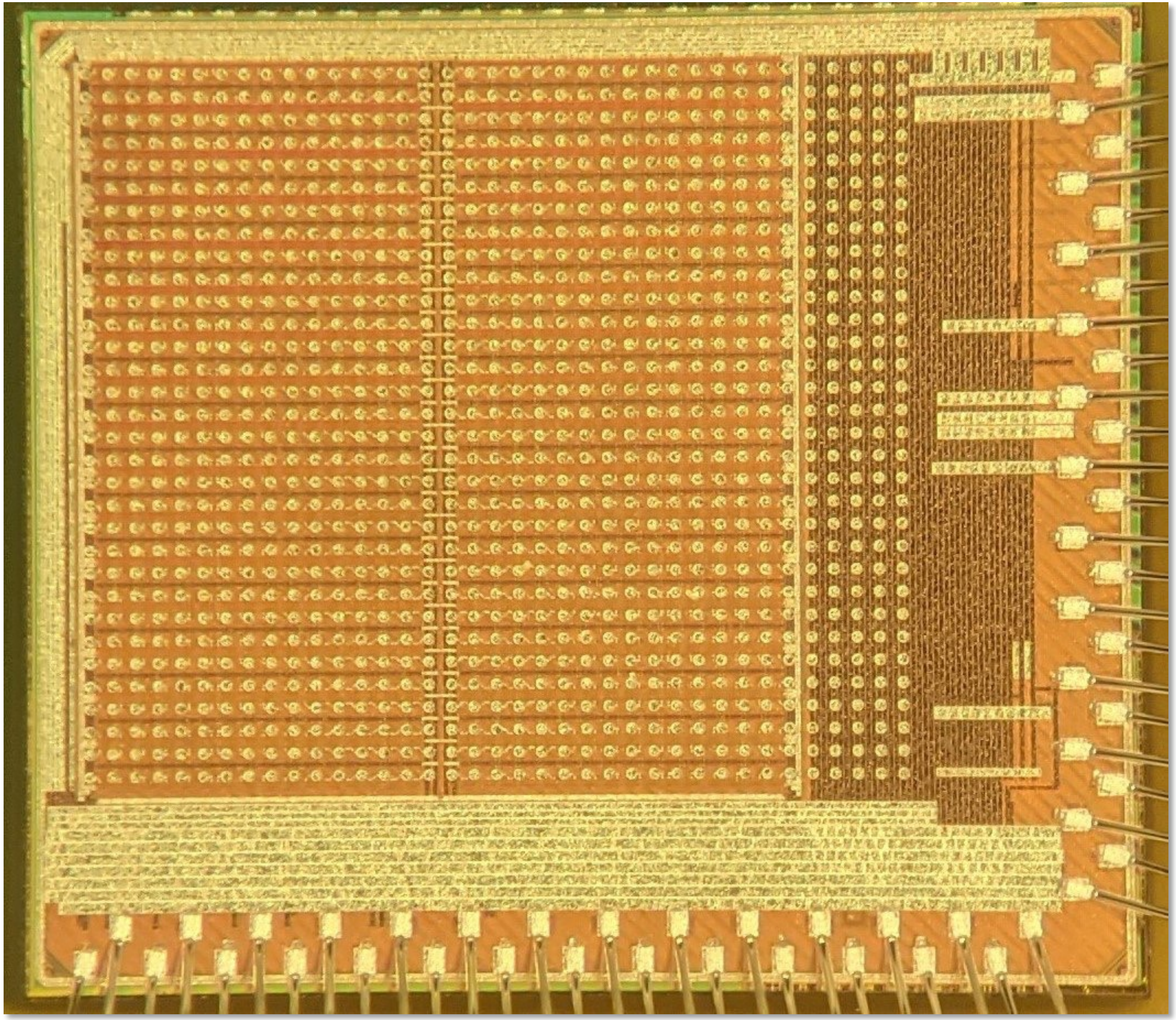
Analog row (16x2 AFE)

Analog (service) column.
Each contains:

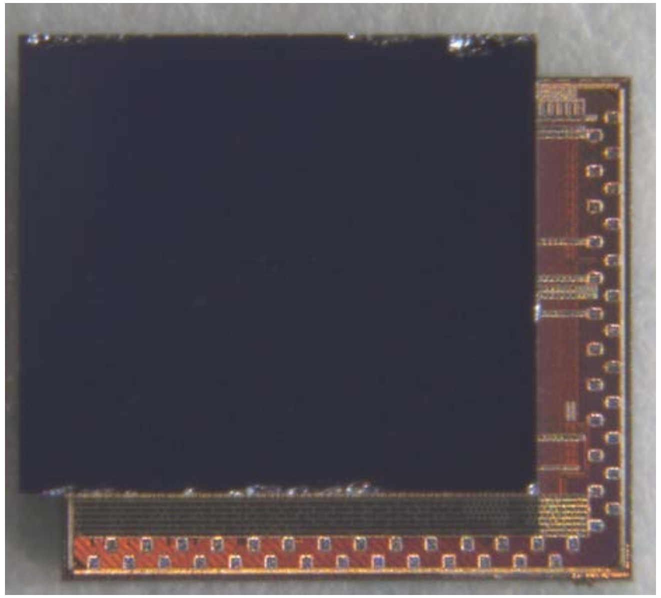
- 1 Band-Gap circuit
- 5x Σ–Δ DACs (producing analog levels used by pixels)
- Programmable bias cell (for power consumption)
- bias replicas with source followers.

4x Read Out Trees

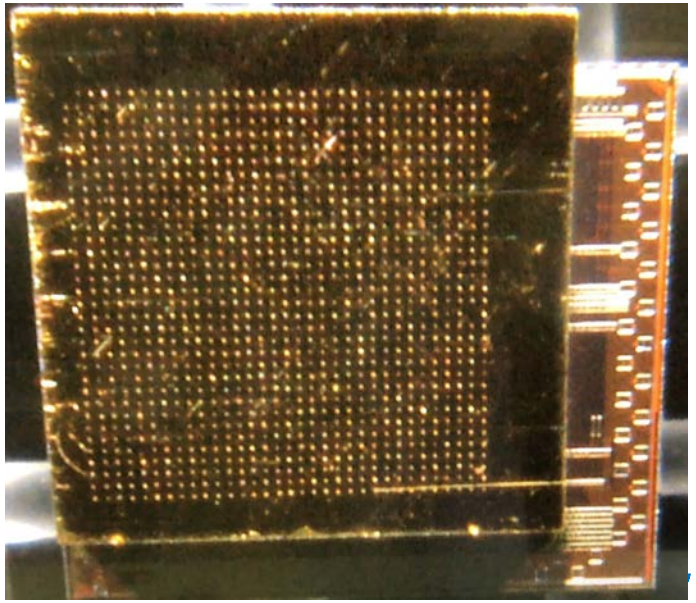
8x LVDS driver
(each @1.28 Gbps)



Timespot1 on 3D-trench silicon matrix

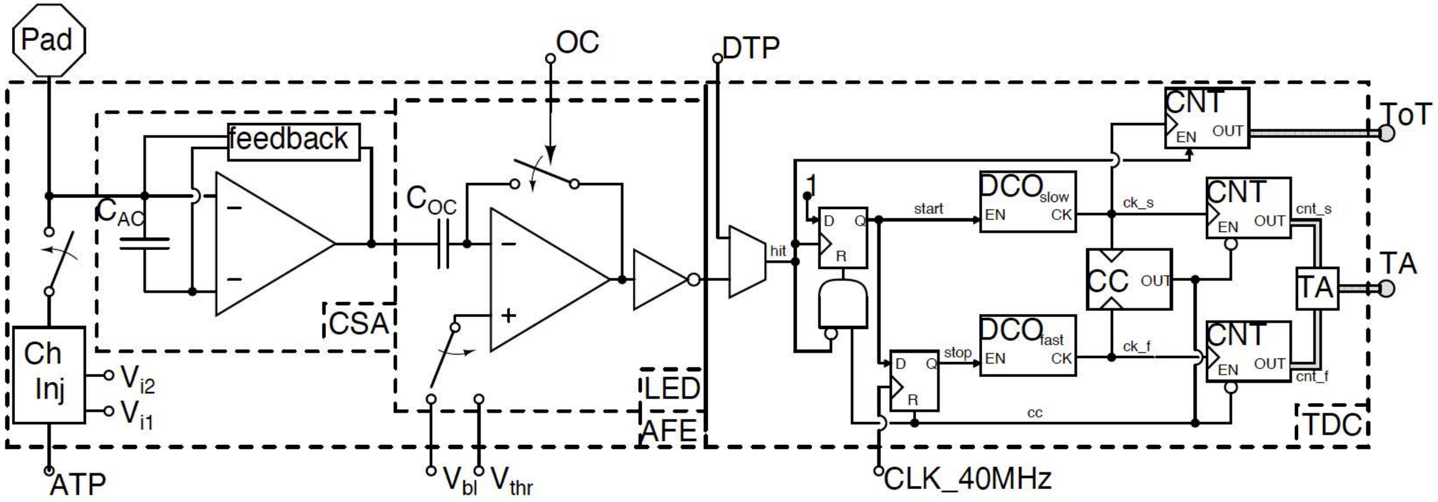


Timespot1 on 3D-column diamond matrix



Pixel architecture & characterization

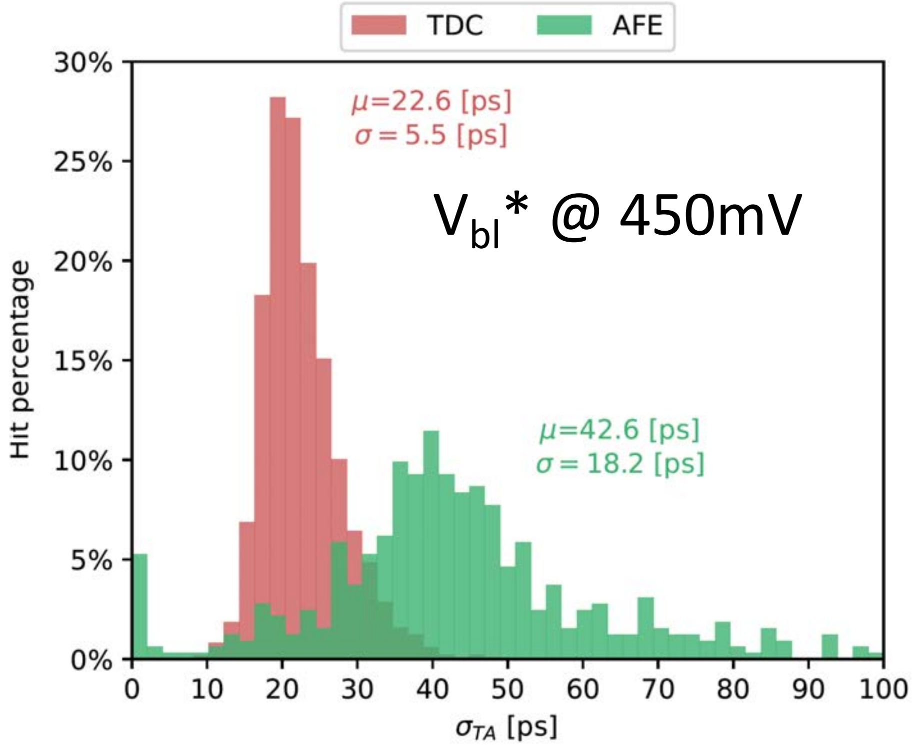
Time resolution (no sensor)



- **The TDC has a typical $\sigma_t \approx$ 20 ps, with a dispersion around 5 ps and is limited by the system clock jitter. Indeed, no improvements are visible when increasing the Vernier precision**

- **The AFE σ_t is intrinsically below 20 ps but an identified bug in the Offset Compensation of the LE discriminator spoils σ_t in most of the channels (see next slide).**

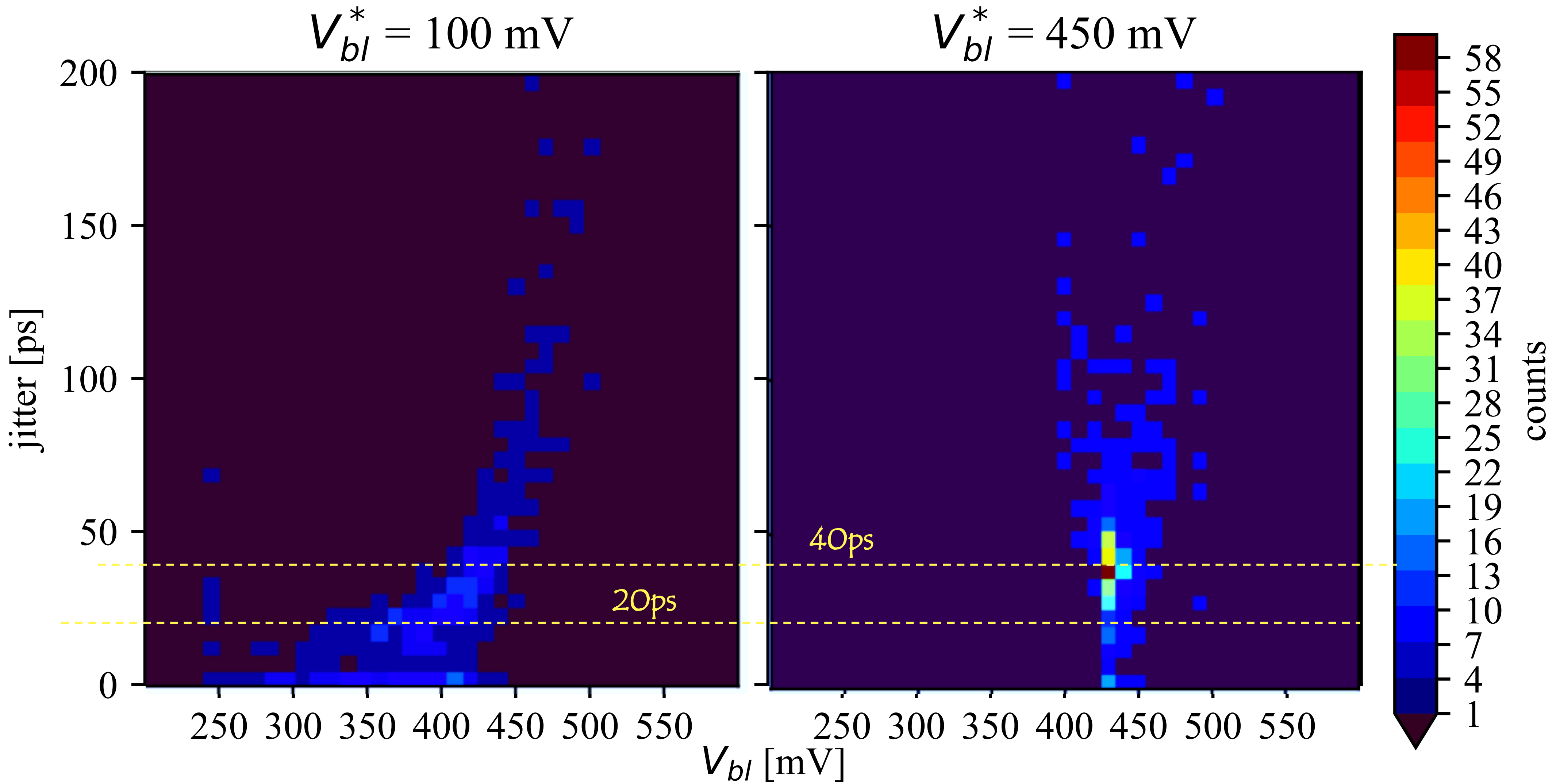
- **In general, issues which are extrinsic to circuit design limit the very good resolution at the pixel level (clock distribution, OC bug). The pixel circuit design appears adequate to system requirements.**



@ 12 µW on AFE

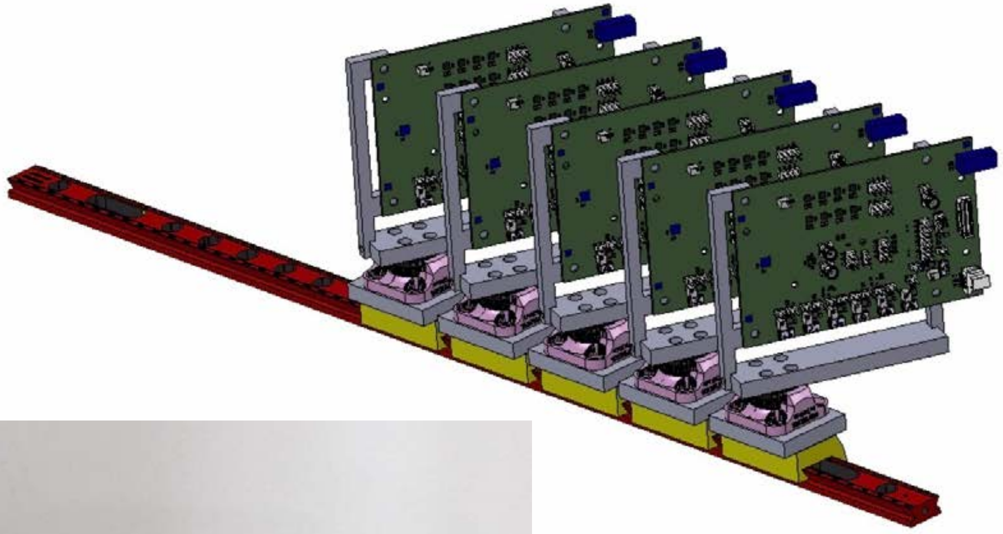
Pixel: the Analog Front End

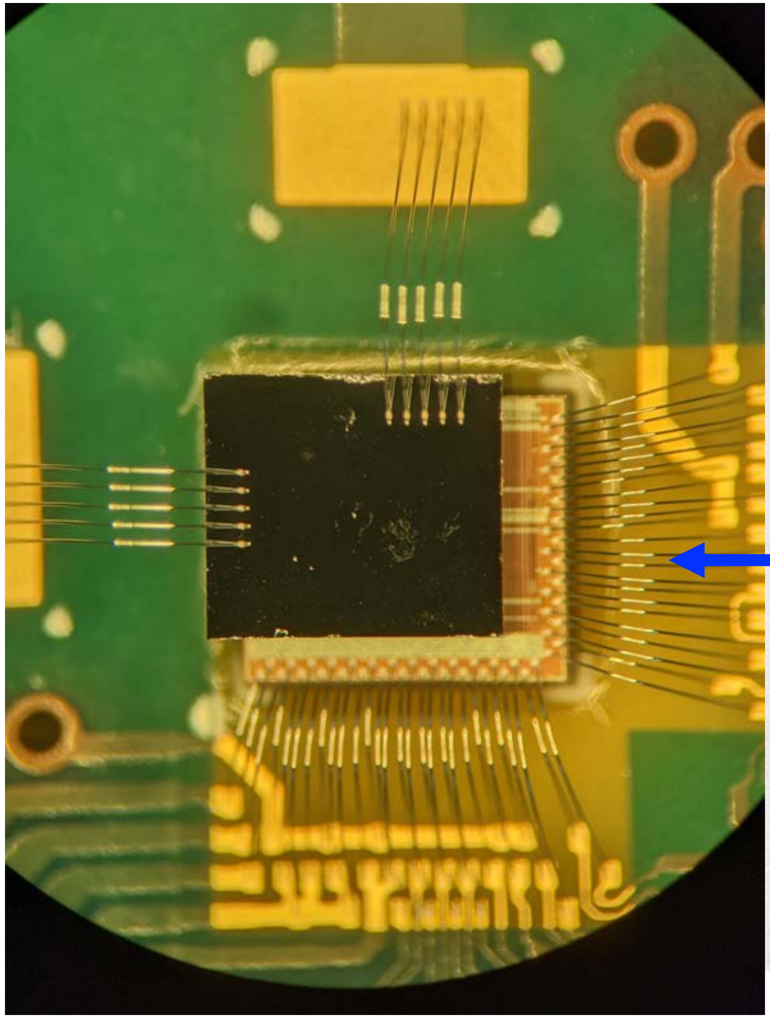
inadequate Offset Compensation

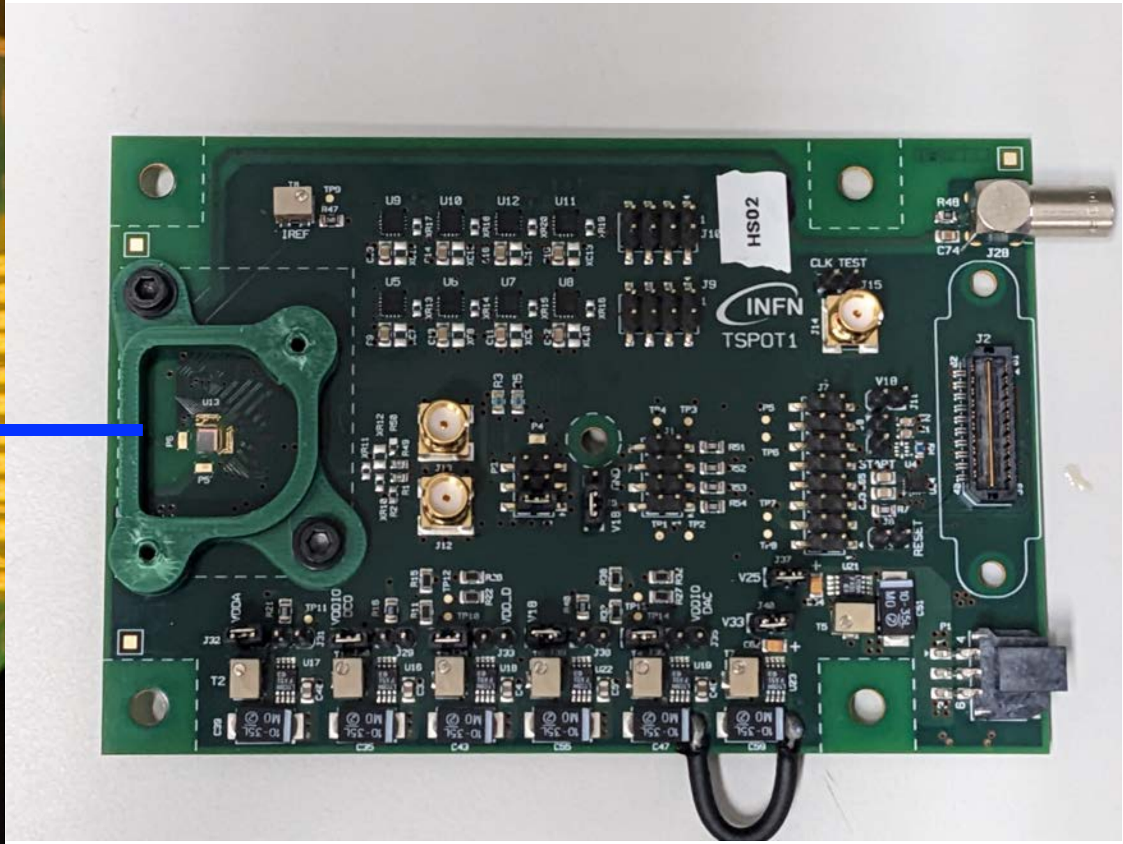


Hybridized devices

with 3D sensors





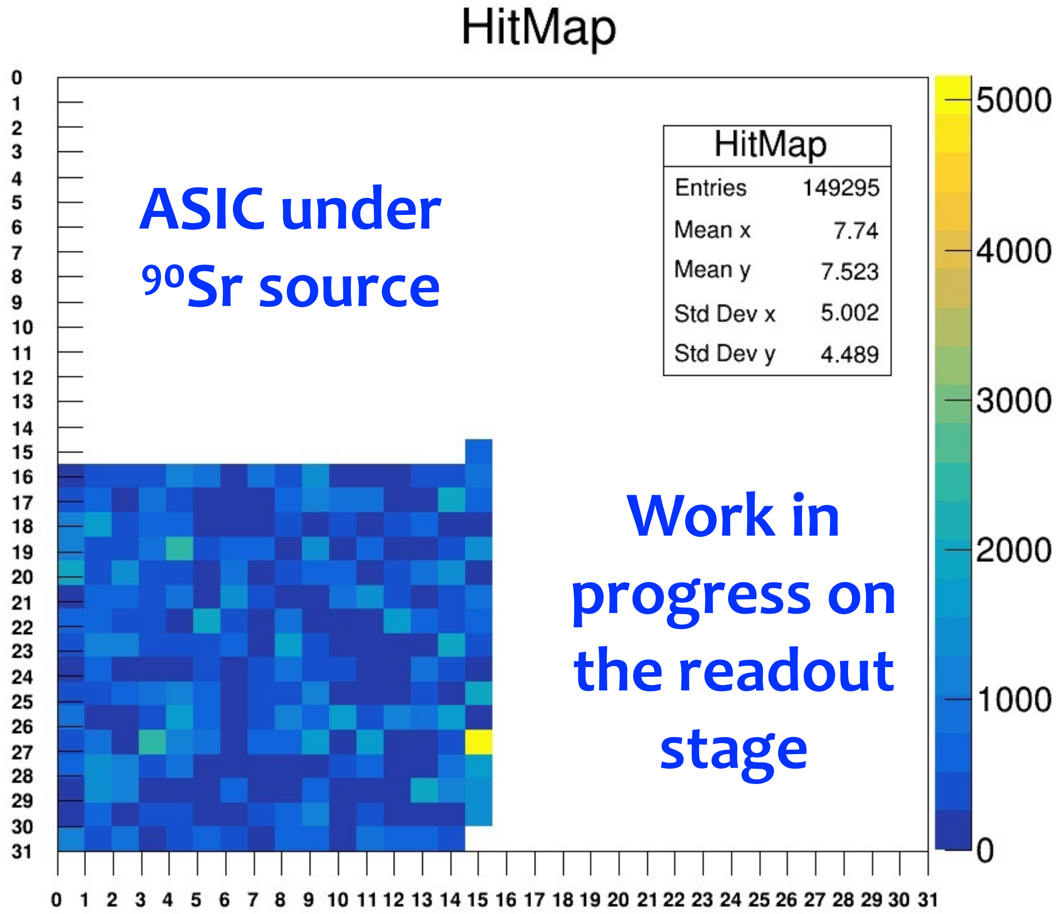


The test-bench PCB (named TSPOT1) operates also as a tracking station in the demonstrator

Hybridization @IZM. Also a version with diamond sensors, same pitch

First hybridized devices

Test bench (INFN Cagliari)



ASIC under ^{90}Sr source

Work in progress on the readout stage

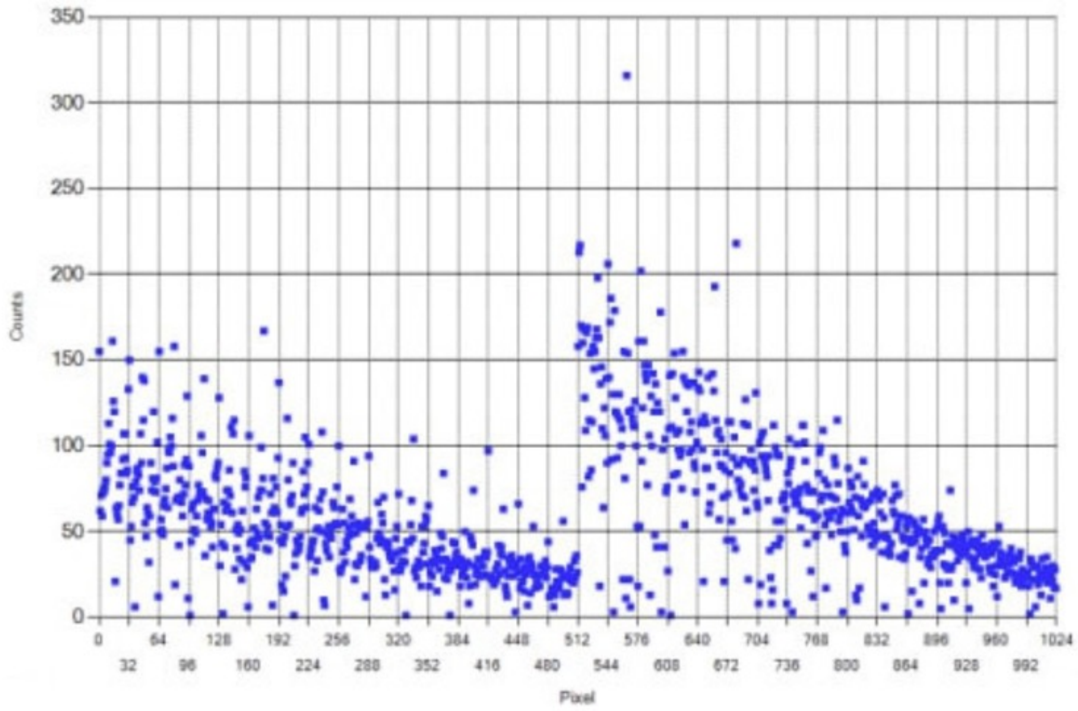
Readout on the full chain of a quarter (2 LVDS links). The DUT readout is possible also in aslow mode by I²C interface

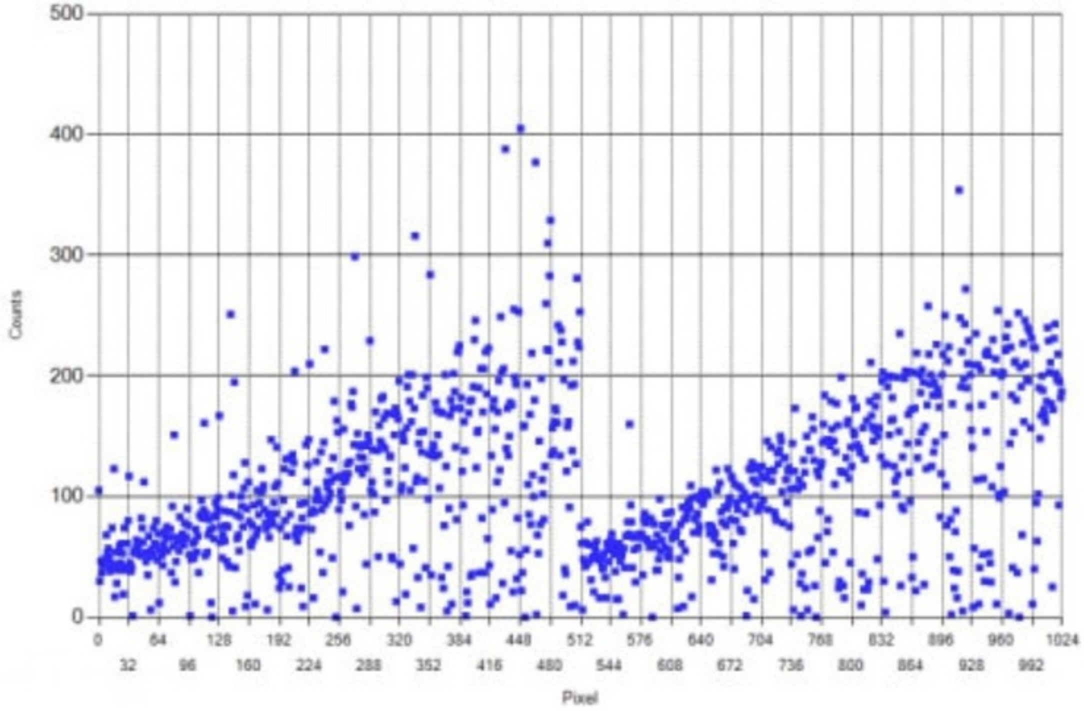
Clock distribution board Si5341

Mezzanine (max 8 tracking layers/DUT) and KC705 FPGA readout board

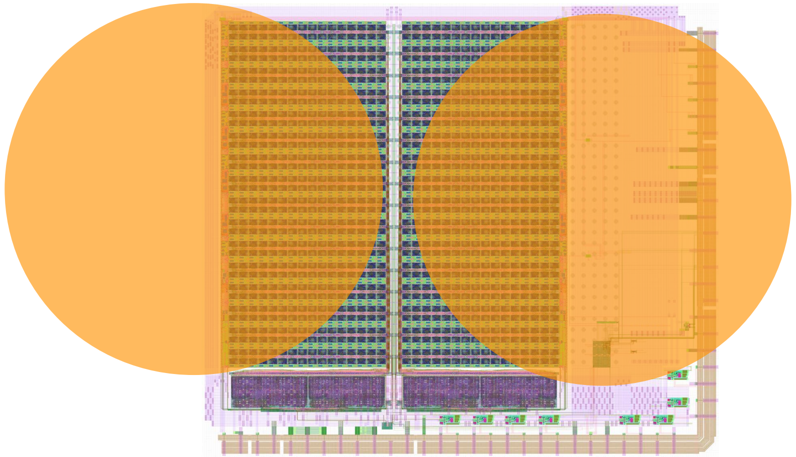
2 DUT on 2 TSPOT1 PCB

Hybridized device under ^{90}Sr source



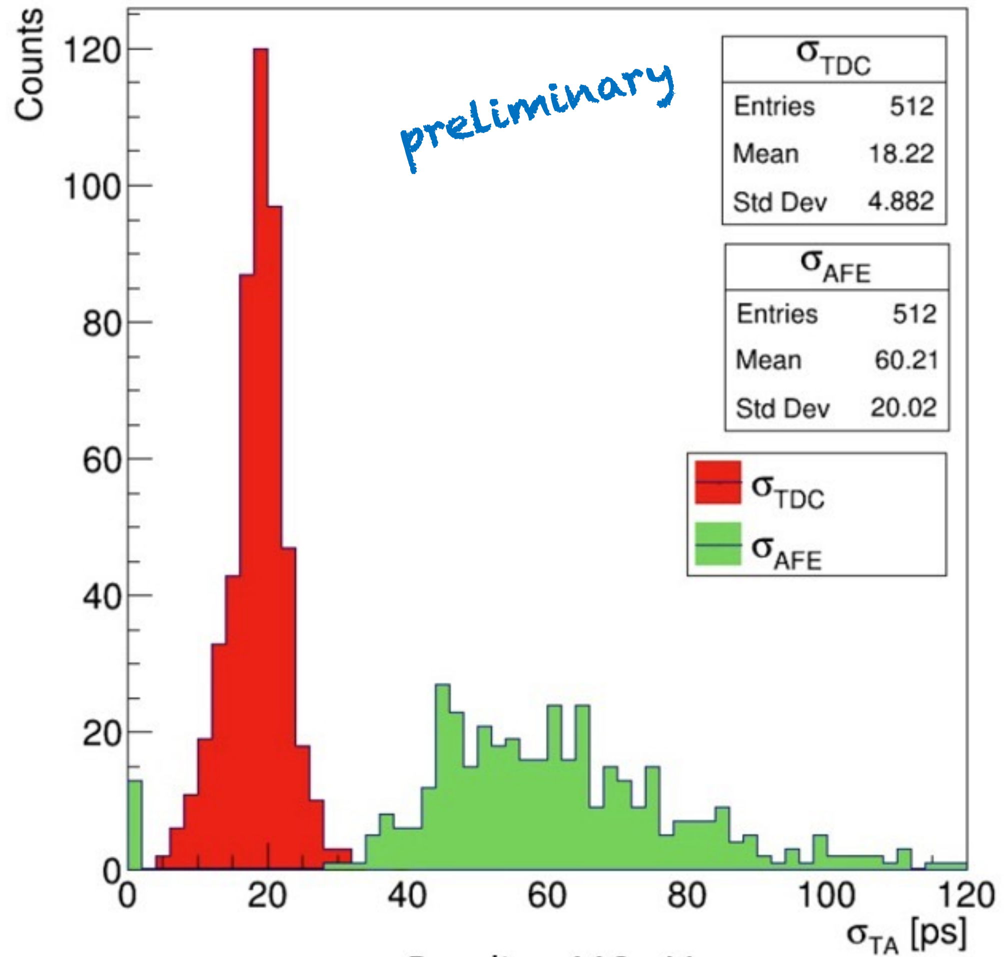


Off-centered ^{90}Sr source

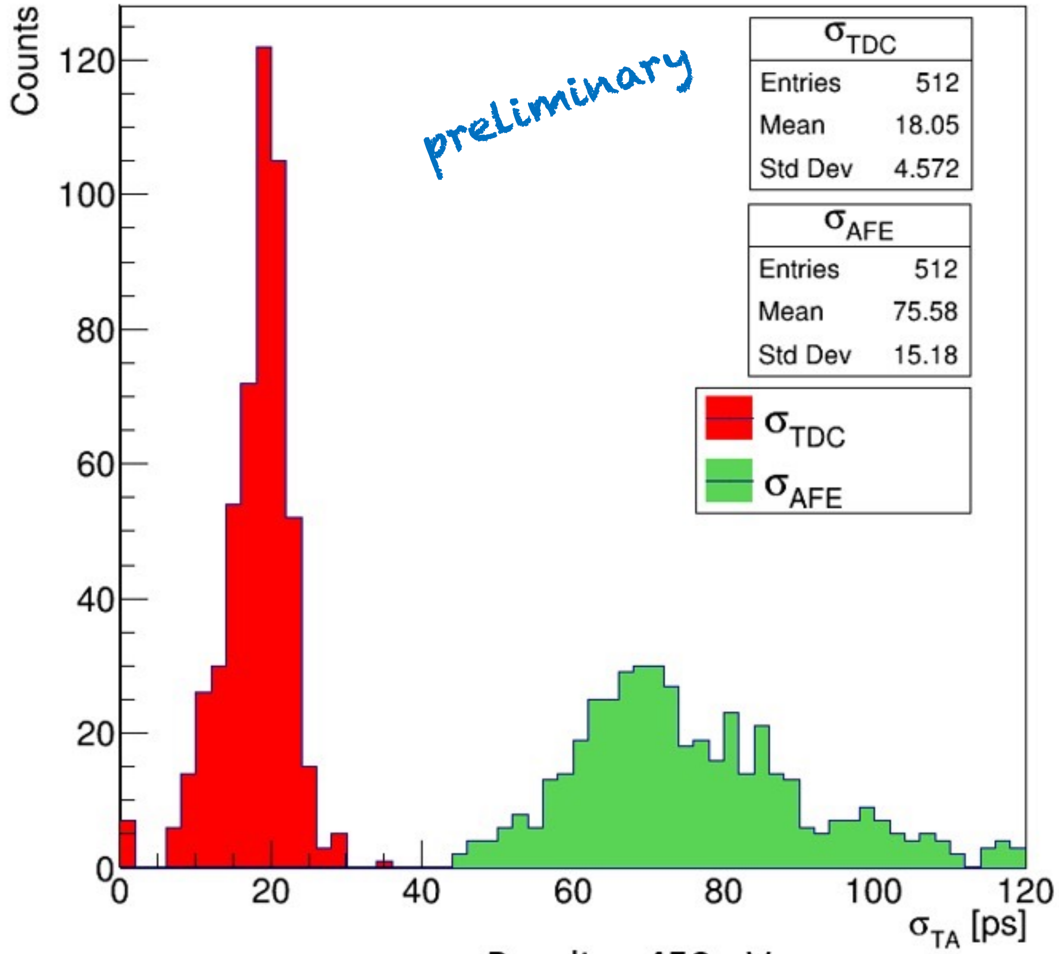


First hybridized devices

time resolution (2 fC pulses) – 2



Baseline 110mV



Baseline 450mV

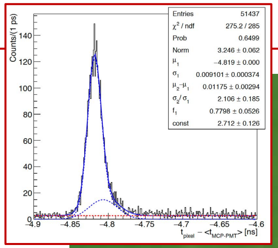
Same behaviour with slight worsening of timing performance

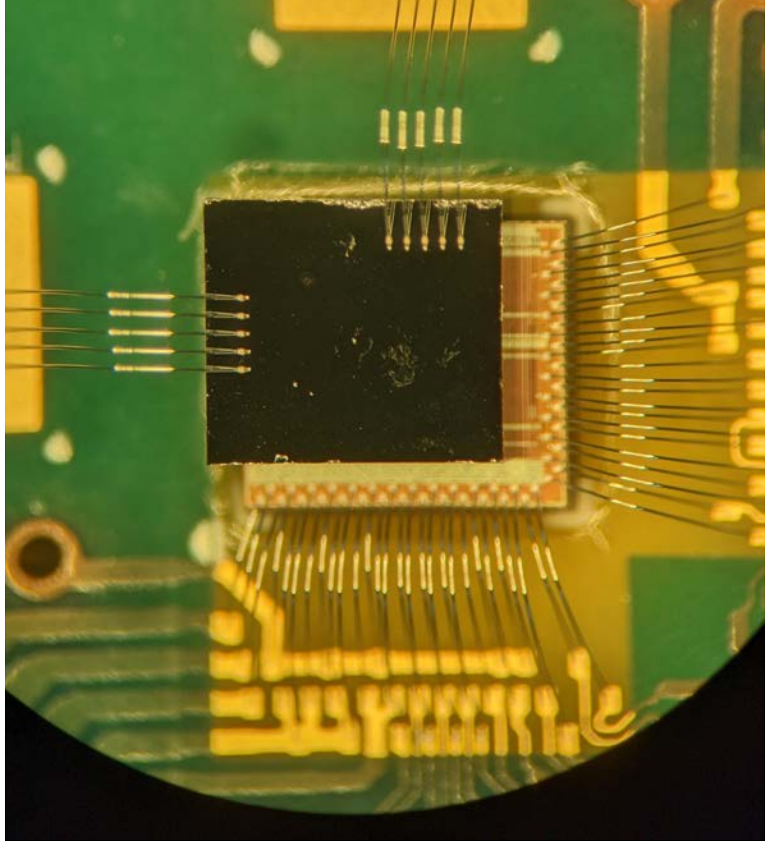
$\sigma_t \propto \sigma_n, C_{in}, \sqrt{t_r}, 1/Q_{in}$

Summary on TimeSPOT results

TIME and SPace real-time Operating Tracker

1. Space Resolution $\sigma_s \approx 10\ \mu m$
2. Time Resolution $\sigma_t \leq 50$ ps per hit
3. Radiation hardness to high fluences $\Phi = 10^{16} \div 10^{17}$ 1 MeV n_{eq}/cm^2
4. Detection efficiency ε > 99% per layer tipically required (high fill factor)
5. Material budget must be kept below 1 ÷ 0.5 % radiation length per layer

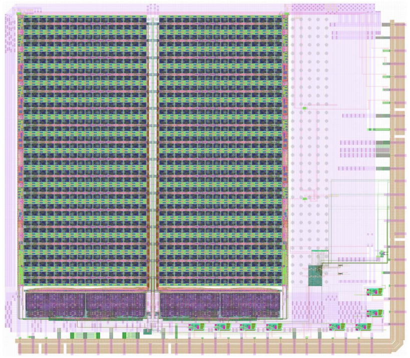


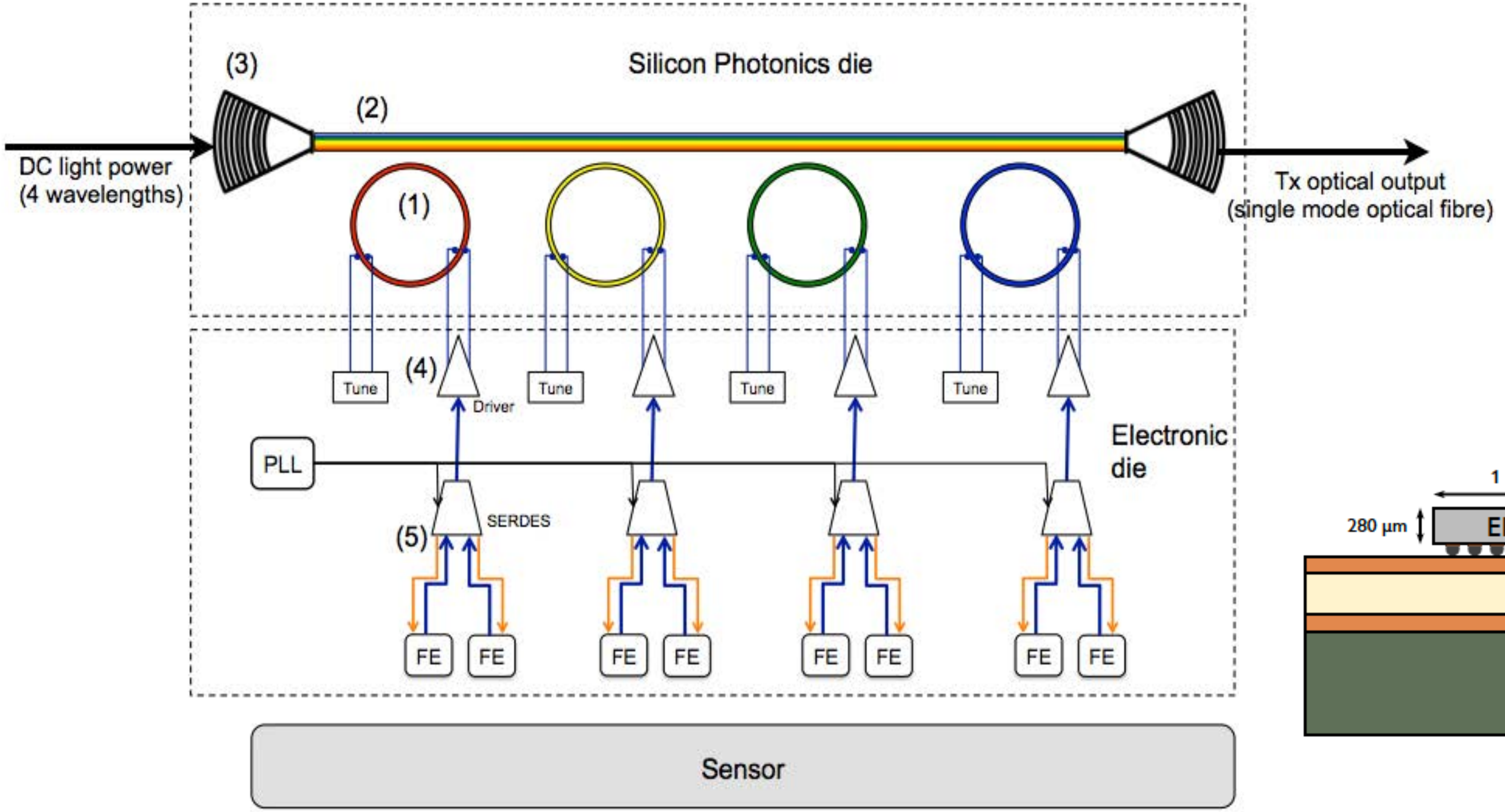


- Most of the very challenging requirements, which appeared almost an absurdity when we started this RnD, have been matched at the prototype level:
  - ≈ 10 ps at the sensor level at 99% efficiency and >> 10^{16} n_{eq}/cm^2
  - 55 µm pitch on sensor and electronics
  - < 30 ps on full chain at the ASIC level within power budget
  - high hit rate ≈ O(1) MHz per pixel

- The next step is to reproduce comparable results on a larger system:
  - ✓ Better production yield on larger area sensors
  - ✓ Better uniformity in time resolution on larger area ASIC
  - ✓ Better clock and power distribution is critical
  - ✓ Increase the readout BW capability
  - ✓ Design protection against radiation hardness
  - ✓ …

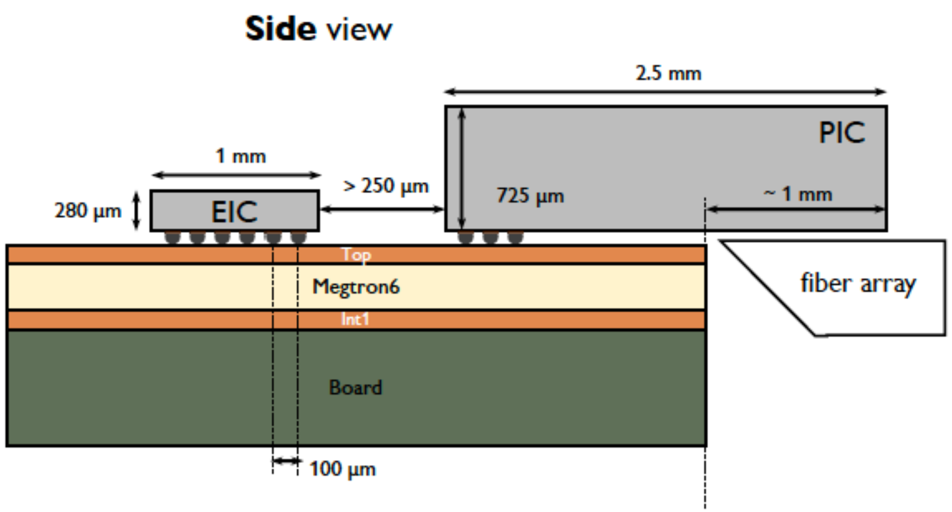
The future: TimeSPOT meets Photonics
(Falaphel *project and* **IGNITE**)





Schematics of the PIC and EIC assembly (FALAPHEL demonstrator). Ring resonators (1) with different and tunable resonator wavelengths are located along horizontally drawn bus waveguides (2) which are connected to optical glass fibers by efficient and robust focusing grating.

Falaphel



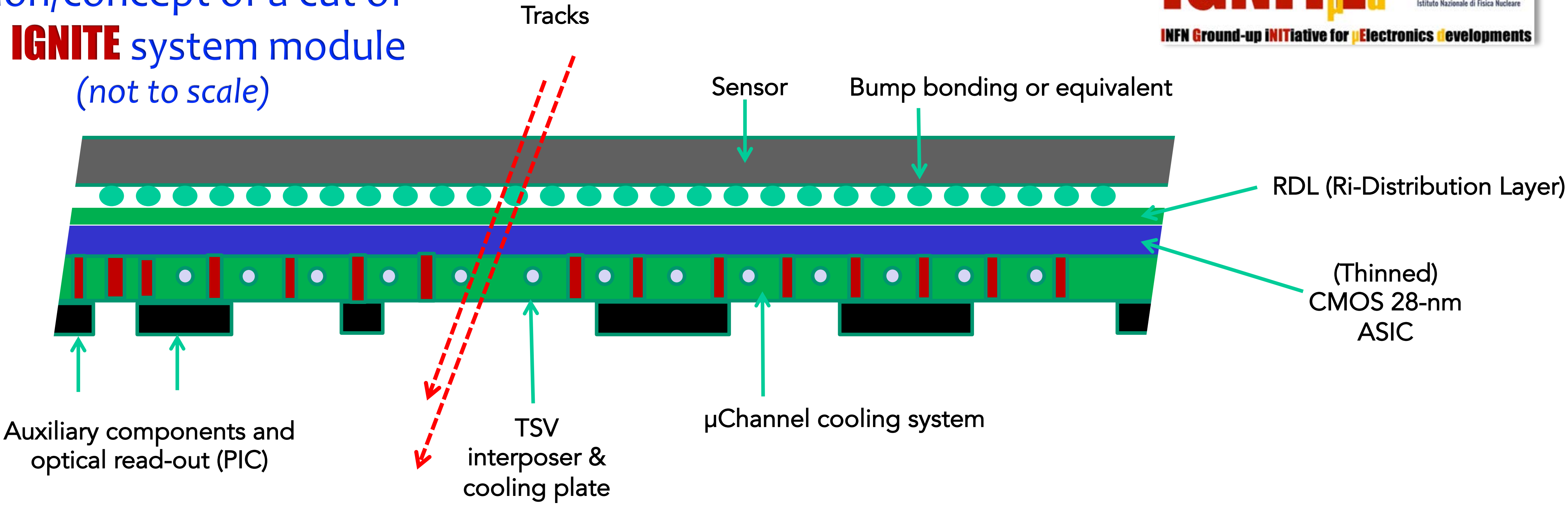
Interposer-free flip-chip integration using a high-speed PCB

Electronics and Technologies for fast (high density) timing

(in the «hybrid approach»)

Vision/concept of a cut of the **IGNITE** system module

(not to scale)



Target deliverable of the IGNITE project:

- **A complete module (sensor, read-out ASIC, vertical IC, photonic circuit for data links, cooling system)**
- **The module development as a route to optimize material budget issues and High Density Interconnectivity between the device stages**
- **The whole thing below 0.8 (LHCb) ÷ 0.5 (NA62) % X_0**

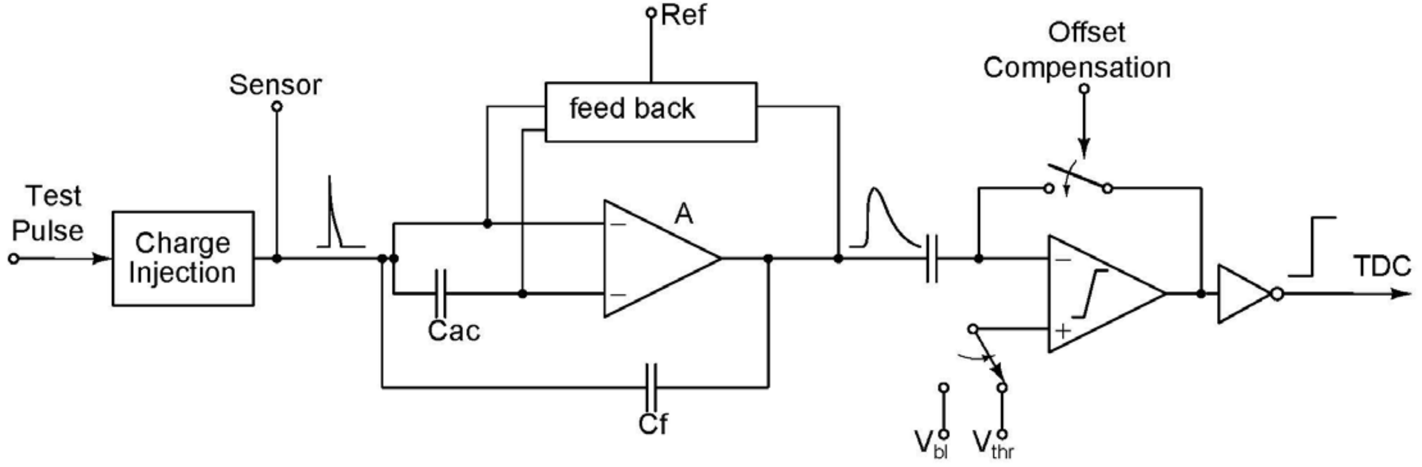
INSIGHTS

Timespot1: Analog Front End

Inverter core amplifier with double Krummenacher FB

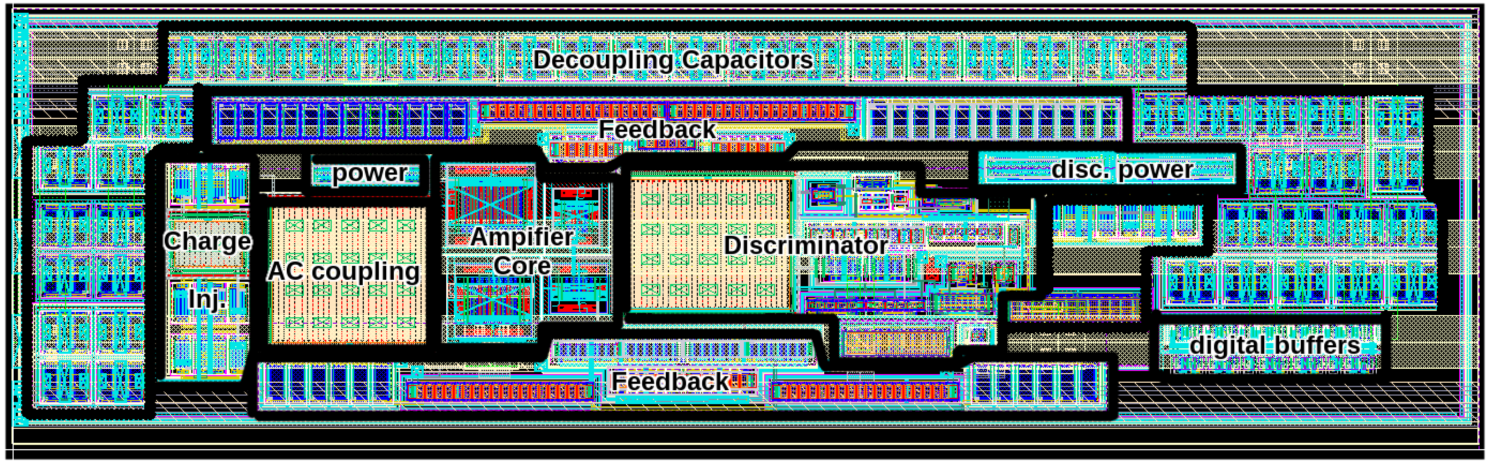
Inverter-based Charge Sensitive Amplifier (CSA) with DC current compensation.

Leading Edge Discriminator with Discrete-time Offset-Compensation for threshold uniformity
OC procedure: 250 ns every ≤800 μs



Pwr regime	nominal	high
Pwr/channel [μW]	18.6	32.9
Slew rate [mV/ns]	250	360
Z_{in} [Ω] in BW	23k	23k
Gain [dB]	93	93
RMS noise [mV]	3.9	3.8
BW [MHz]	311	455
Jitter [ps]	15.6	10.5

Expected performance @ 2 fC (post-layout simulation)



50x15 μm²

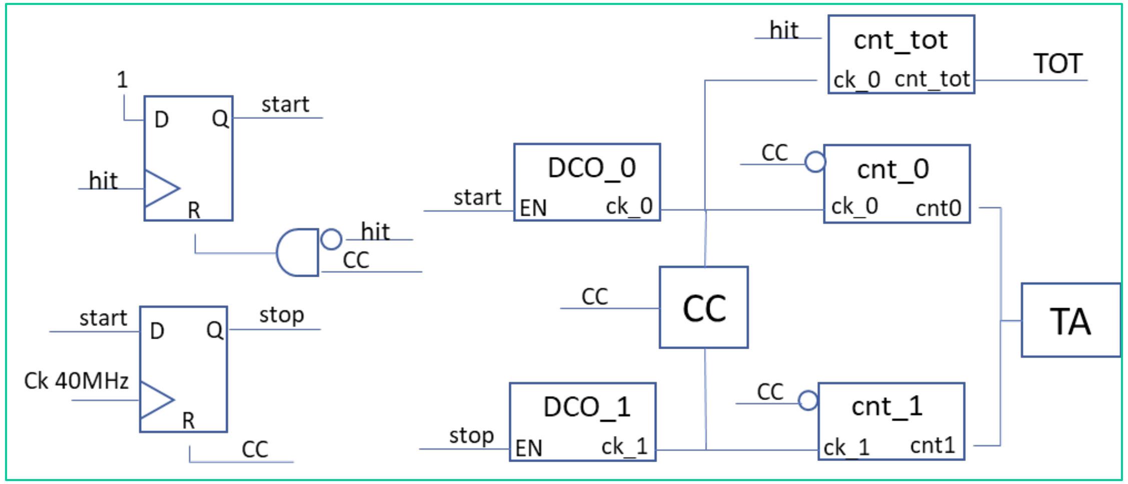
Timespot1: TDC

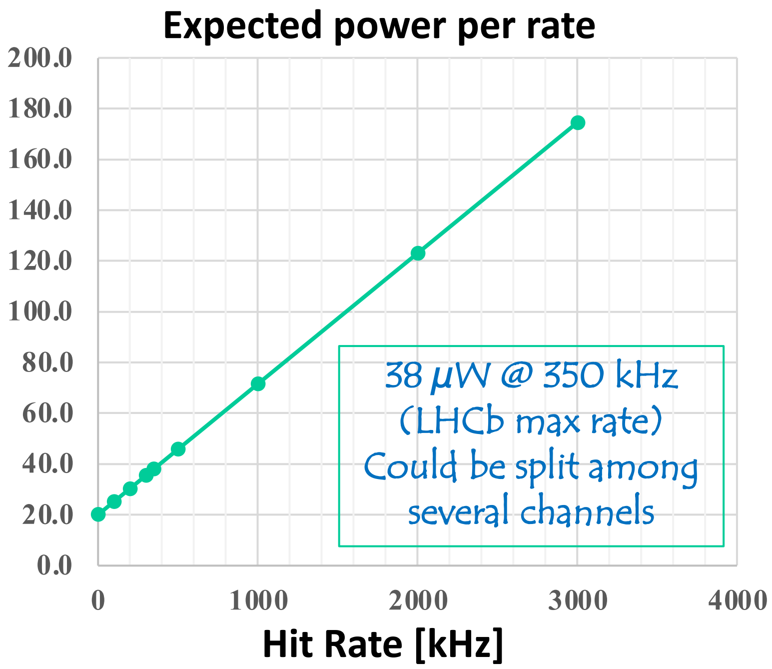
Fully digital design, standard-cell based

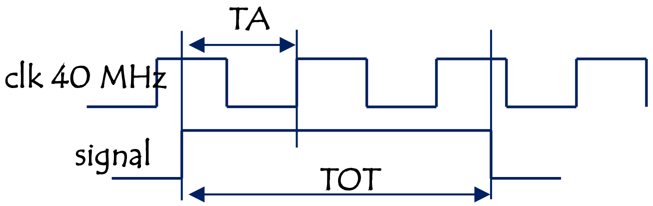
To maximize sustainable rate, 1 TDC per pixel channel has been integrated

Max input rate = 3 MHz
23 bits output word (ToA + ToT)
ToT resolution ≈ 1 ns

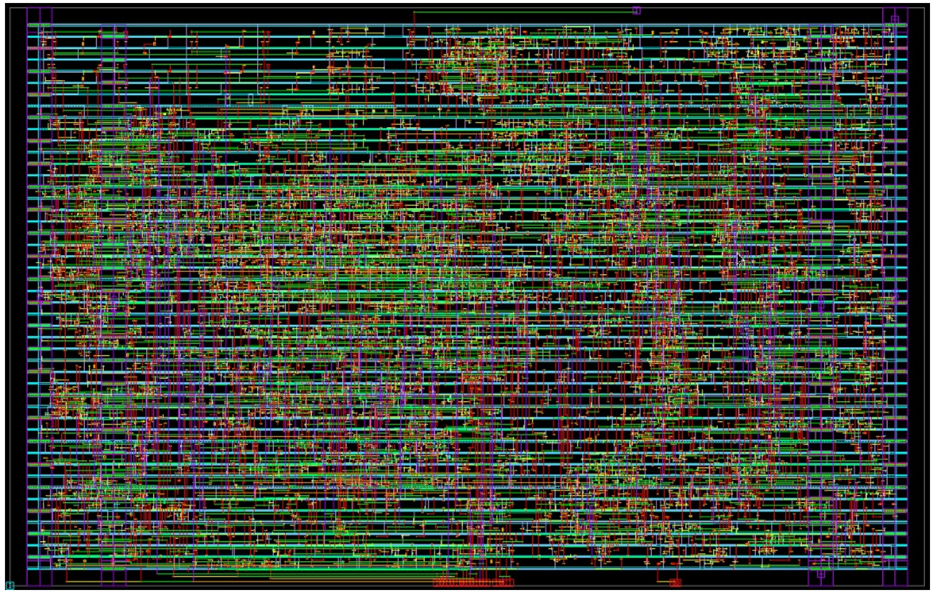
High resolution, "low" consumption TDC based on 2 DCOs and a Vernier architecture







The TDC gives the phase of the signal wrt the 40MHz BX clock
The TDC and the counter use the same DCO-generated Clk (~1 GHz)
4 levels of Vernier precision (Δ*f* in DCOs) can be programmed.
Typical LSB 12 ps

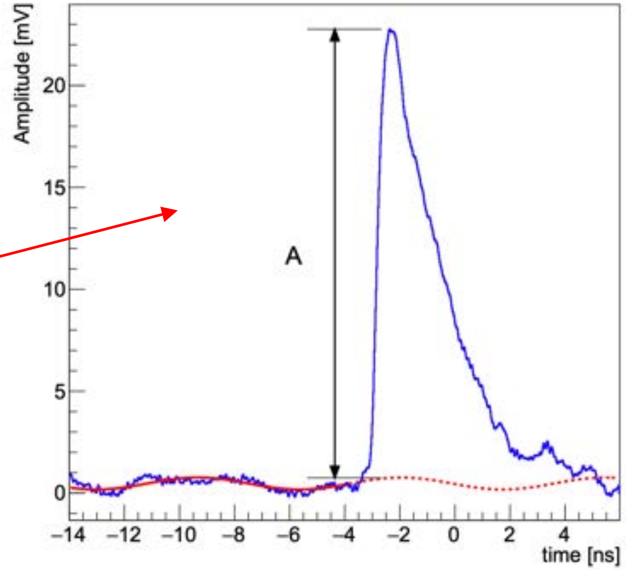


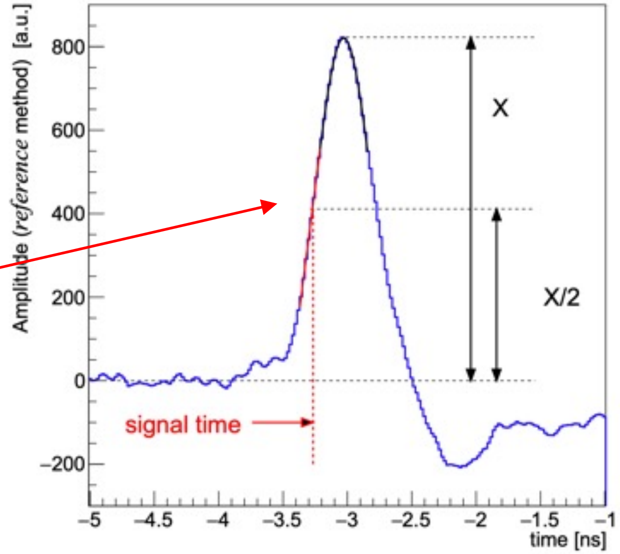
50x32 μm²

Waveform processing

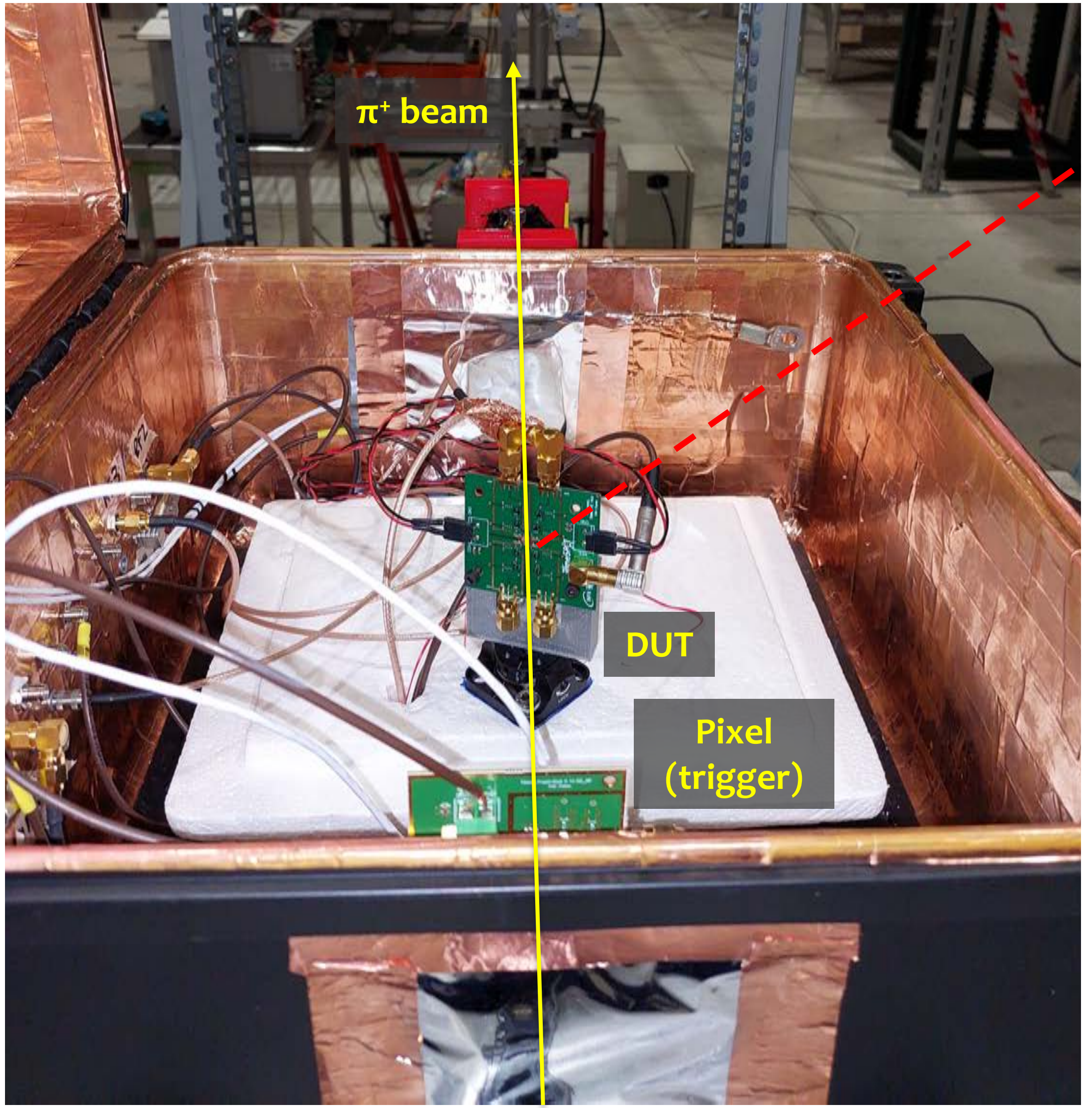
For each sensor's waveform:

- Signal baseline (red-dashed line) is evaluated on an event-by-event basis
- The signal amplitude A is measured (w.r.t. to the event baseline)
- Signal time of arrival evaluated with various methods:
  - Leading-edge: time at 15 mV signal amplitude, linear interpolation around threshold (time-walk effect is present)
  - LE corrected for the amplitude to suppress the time-walk effect
  - Spline: a classic CFD at 20% with rising edge interpolated with a spline
  - *Reference*: subtract each waveform from a delayed (by about half of the signal rise time) copy of itself, then on the resulting signal we trigger at X/2 height

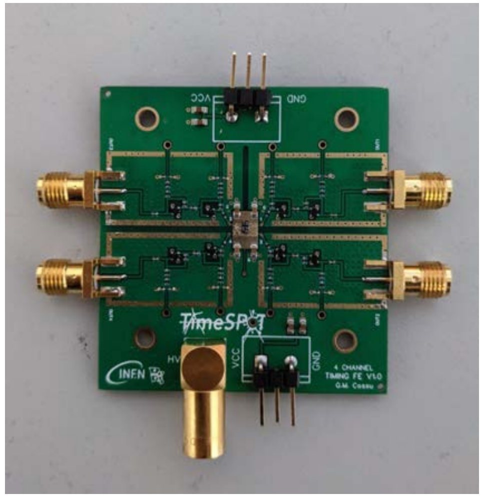




Charge sharing studies: setup



4-channel FEE board

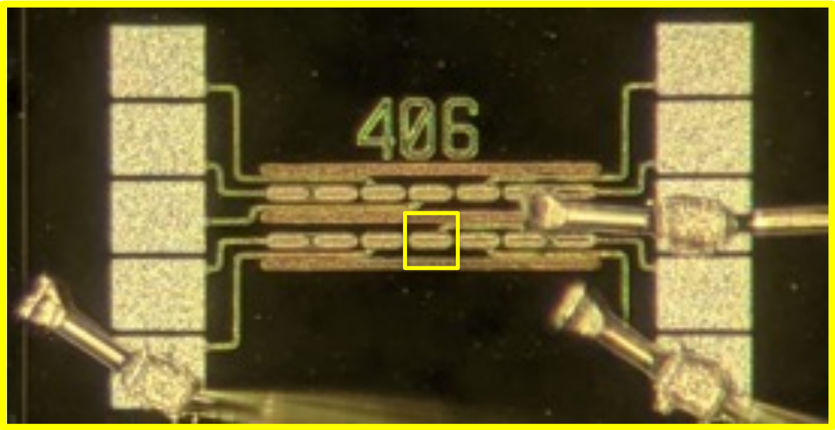


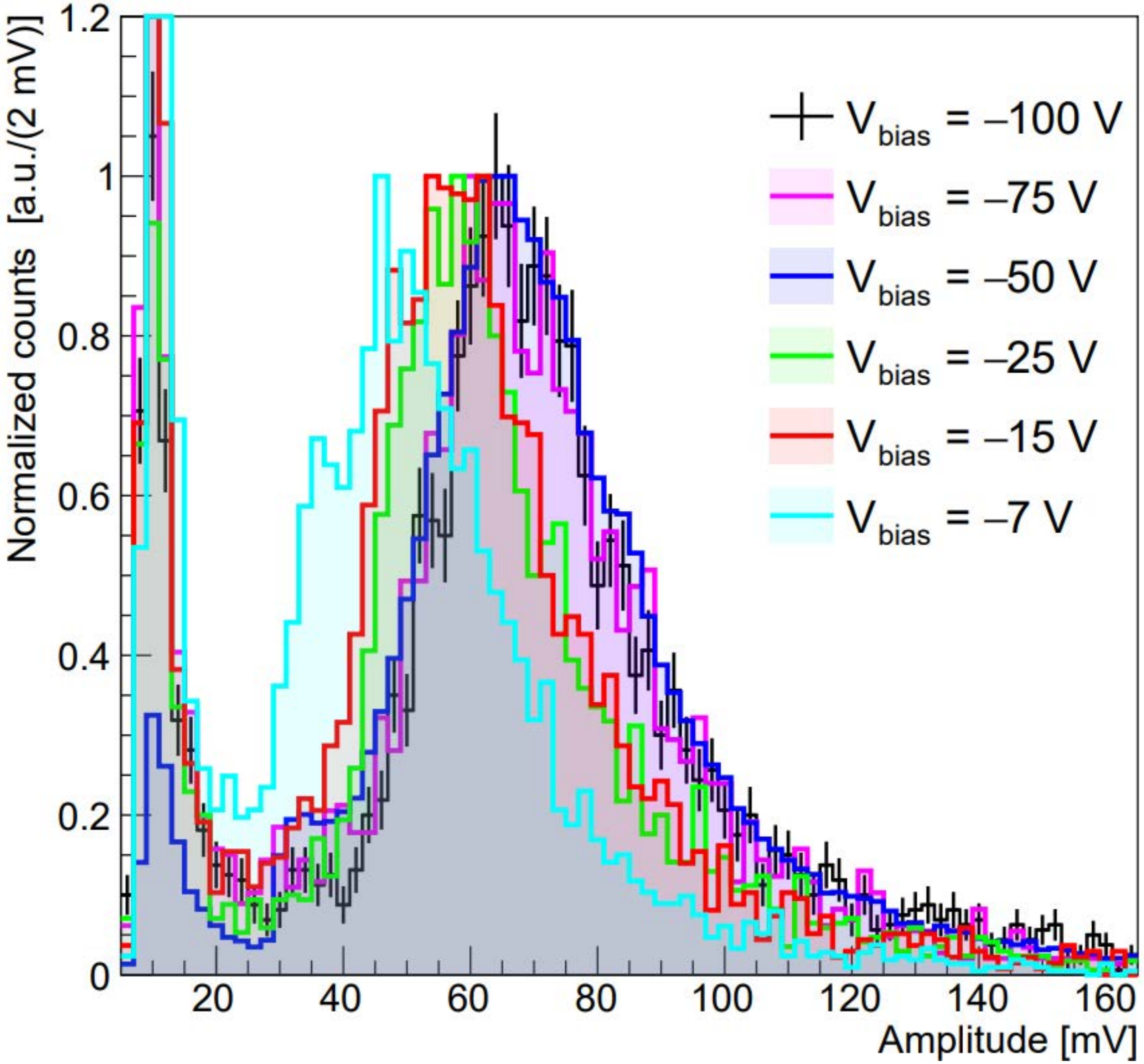
2 adjacent pixels – each one read-out by one FEE channel

Tilting the sensor it is possible to study the behaviour of two pixels when a charged particle crosses both of them

Amplitude distributions vs bias

Single pixel, not irradiated





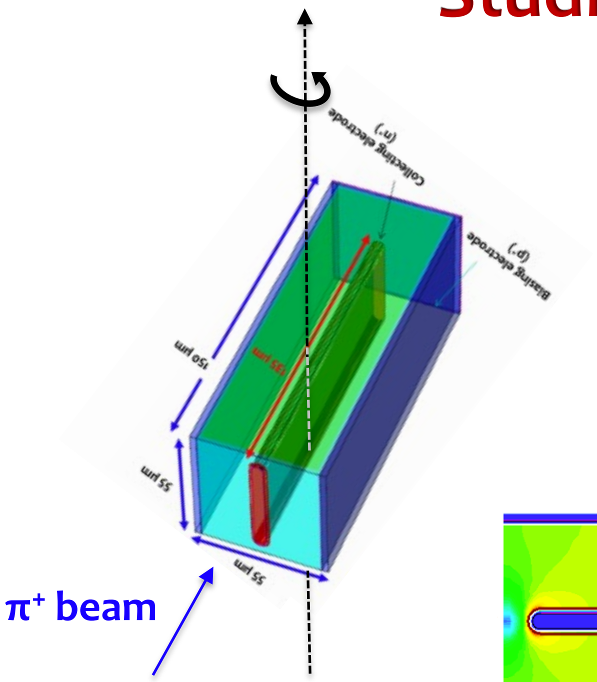
Normal pion incidence (α_{tilt} = 0°)

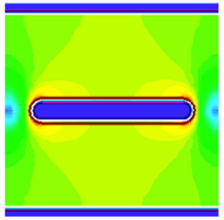
DUT not on the trigger

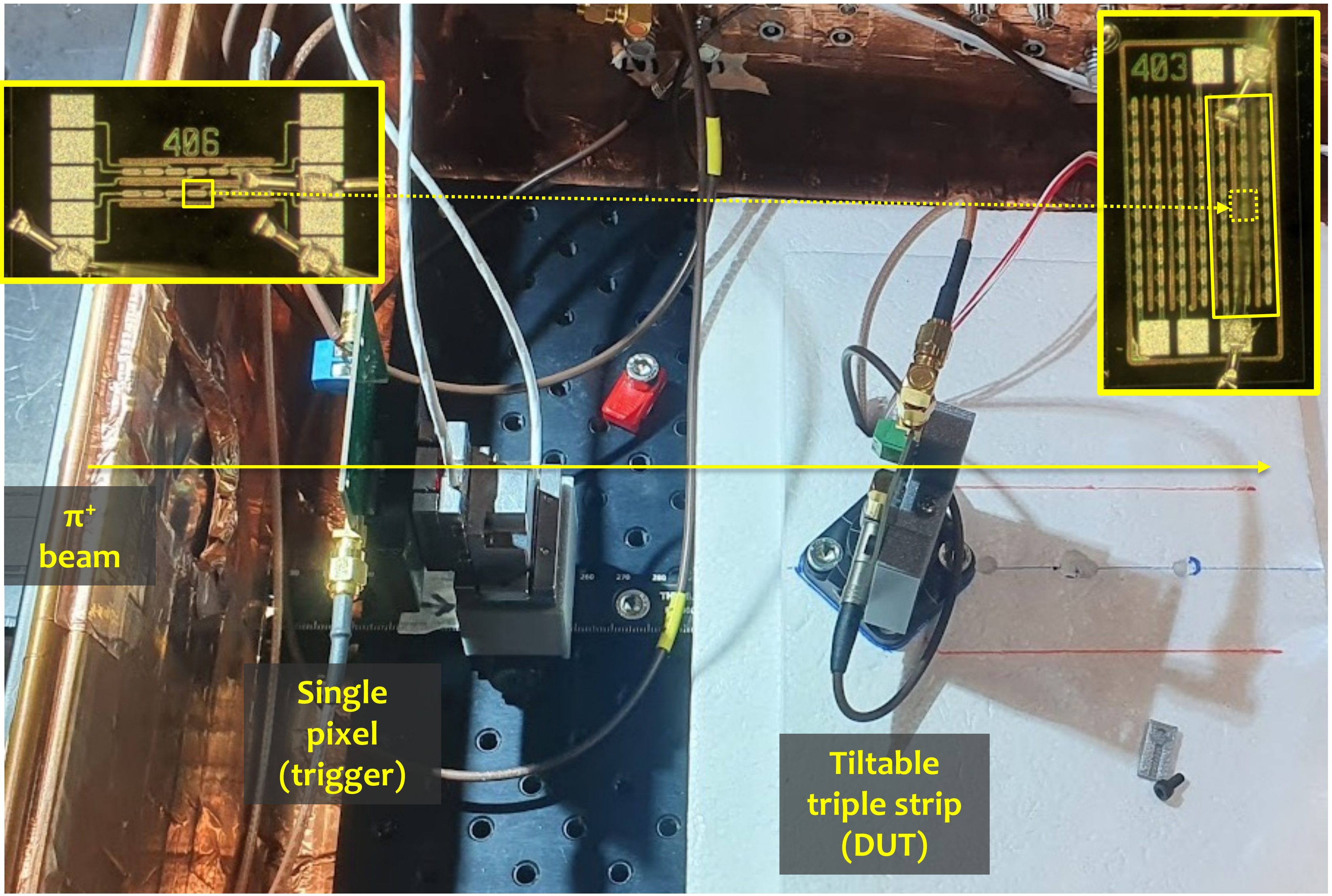
Very good sensor performance even at **low V_{bias}** (prompt full depletion)

Studies of Geometric Efficiency: setup

Single pixel, not irradiated





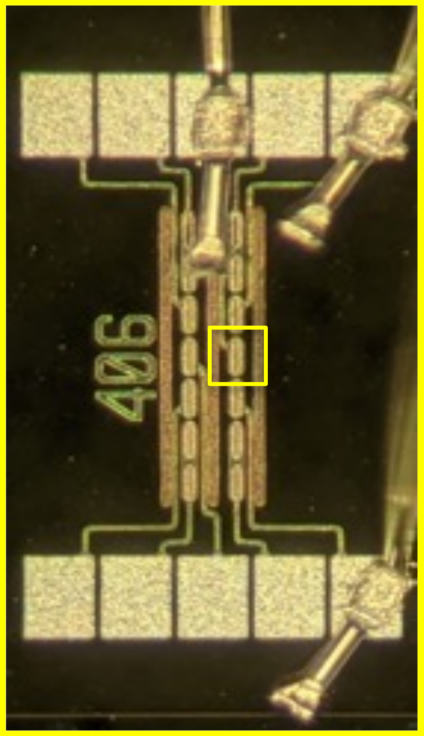


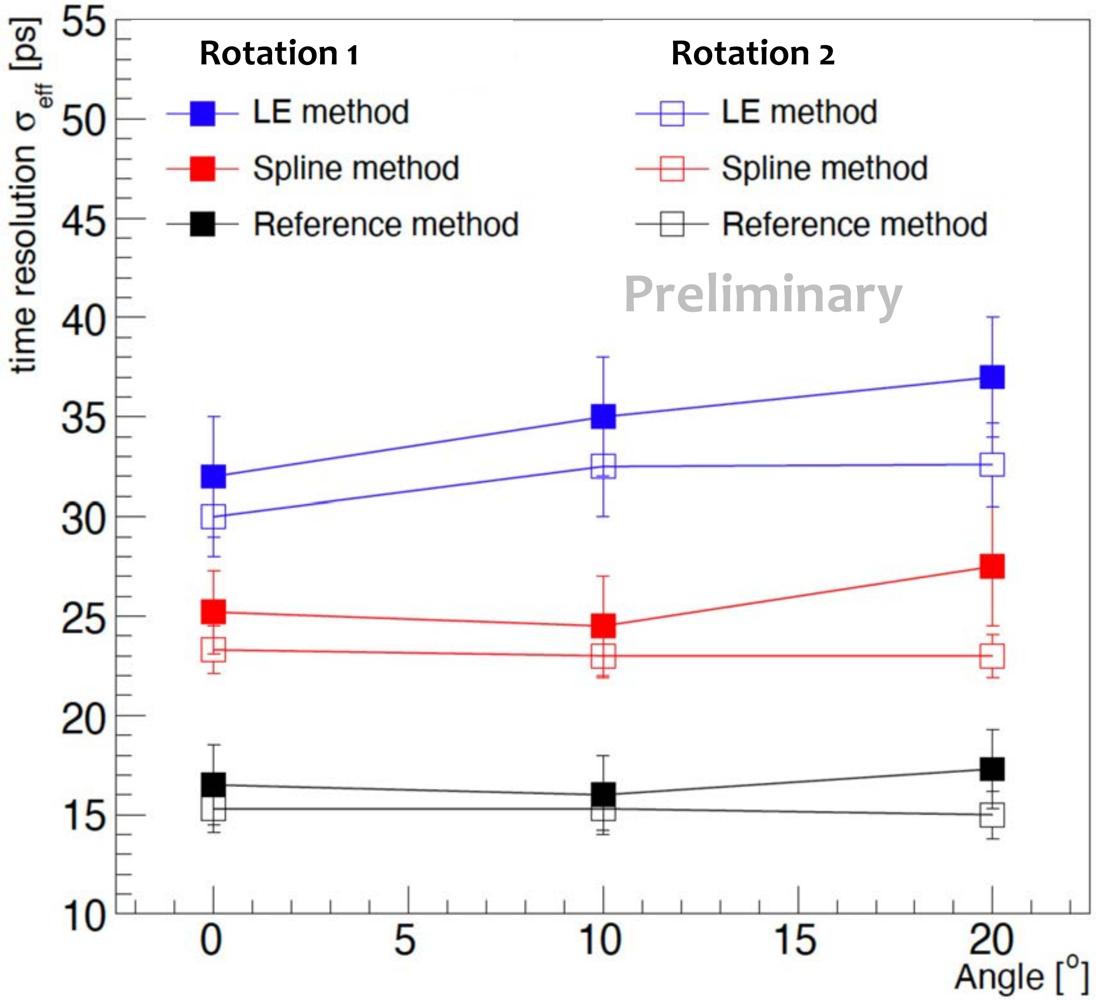
Tilting the sensors with respect to normal incidence should allow **to recover geometric efficiency**

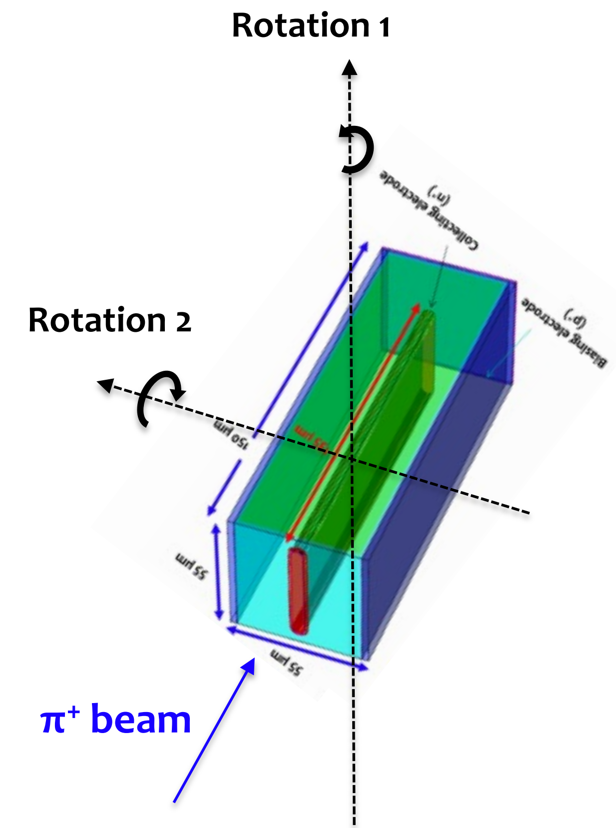
Trigger on one pixel (55 μm x 55 μm, on piezos) centered on a triple strip (165 μm x 550 μm, DUT) and **counting the fraction of signals seen in the triple strip** (on a single FE channel)

The DUT is rotated around the trench direction

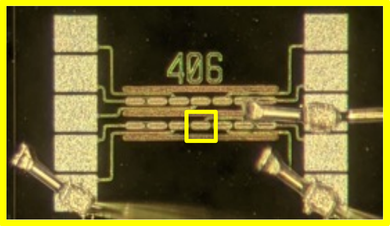
Tilted sensors: timing performance



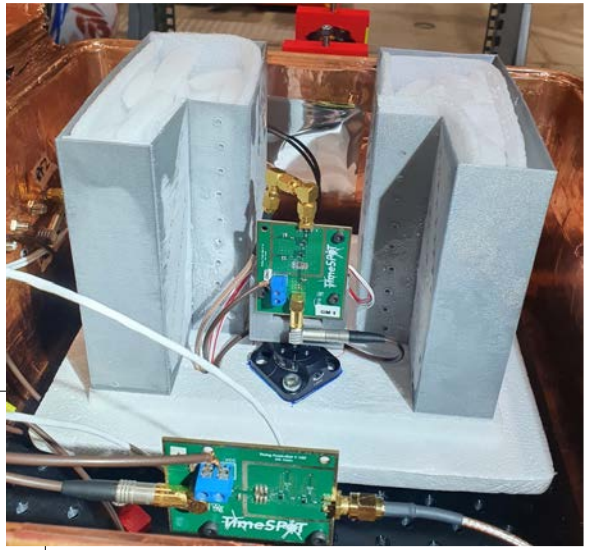




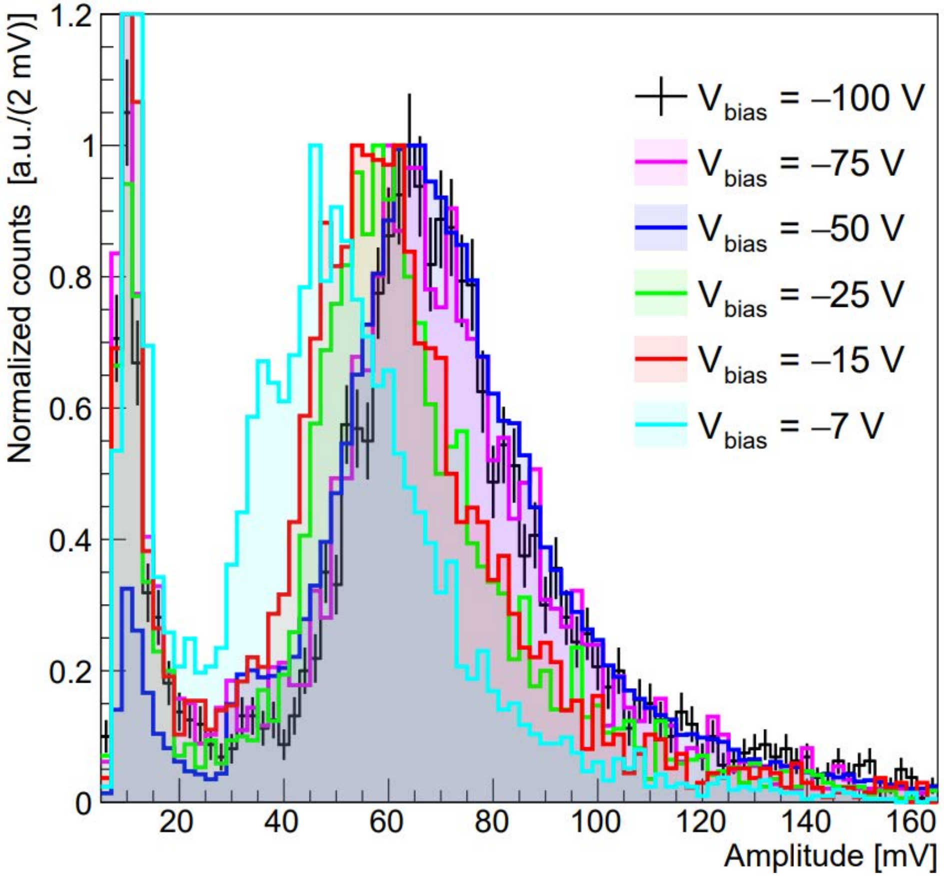
Single Pixel @ 50V



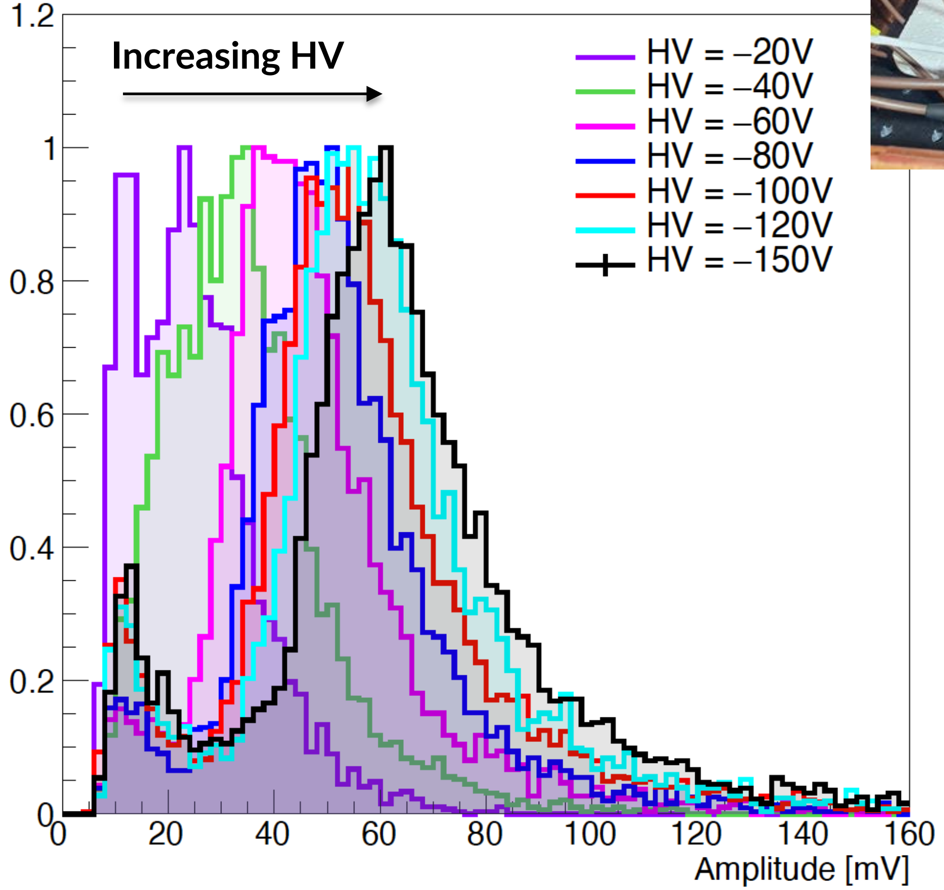
Amplitude distributions vs bias
*Single pixel, **irradiated***



Not IRRADIATED, α_{tilt} = 0°

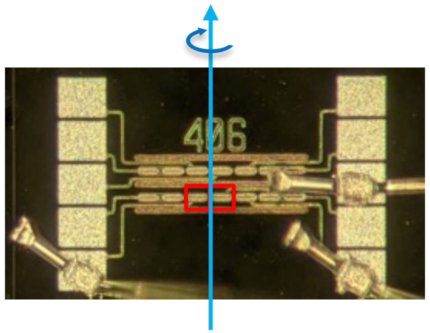


Irradiated @ 2.5 10^{16} n_{eq}/cm^2 , α_{tilt} = 0°



The effect of fluence is evident from the ΔV_{bias} needed to reach the same Amplitude

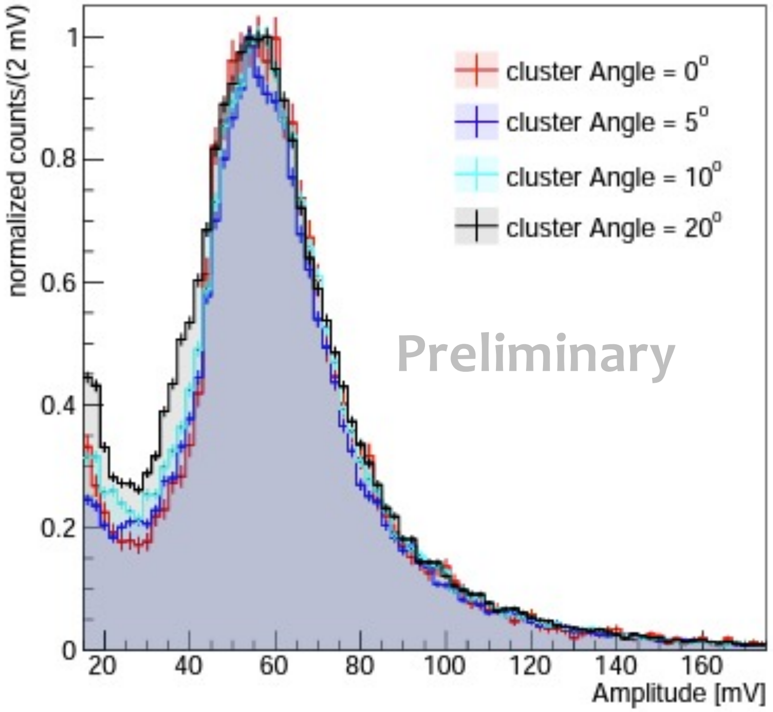
Charge sharing studies: results



When a particle crosses two pixels:

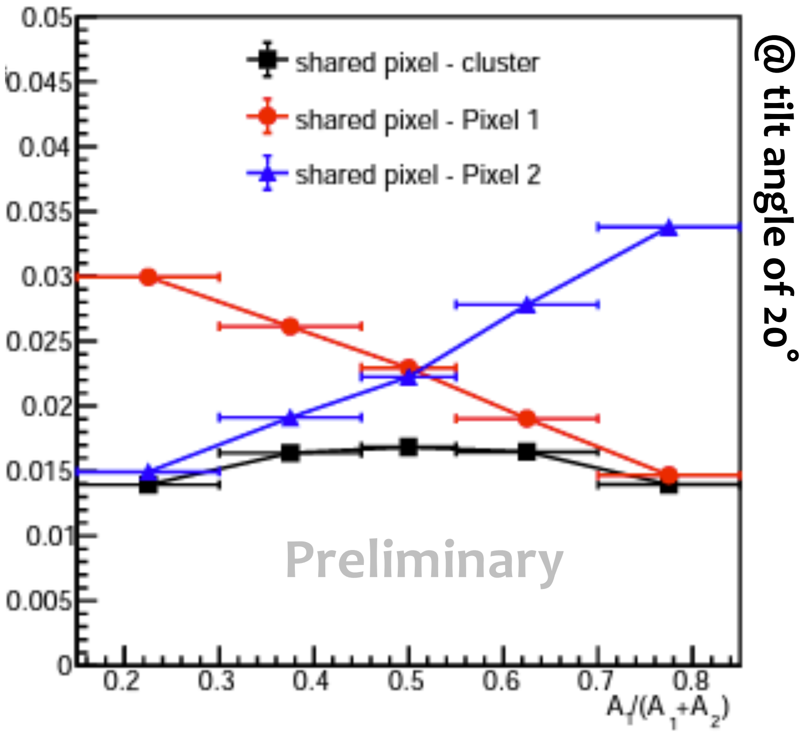
1. Amplitude = sum of the amplitudes of the two signals
2. Time of Arrival = weighted sum on amplitudes of the ToA in the two pixels

Amplitude distributions at different angles



Combining the two pixels information, it is possible to recover the amplitude distribution expected at normal incidence angle

Time resolution as a function of the fraction of sharing

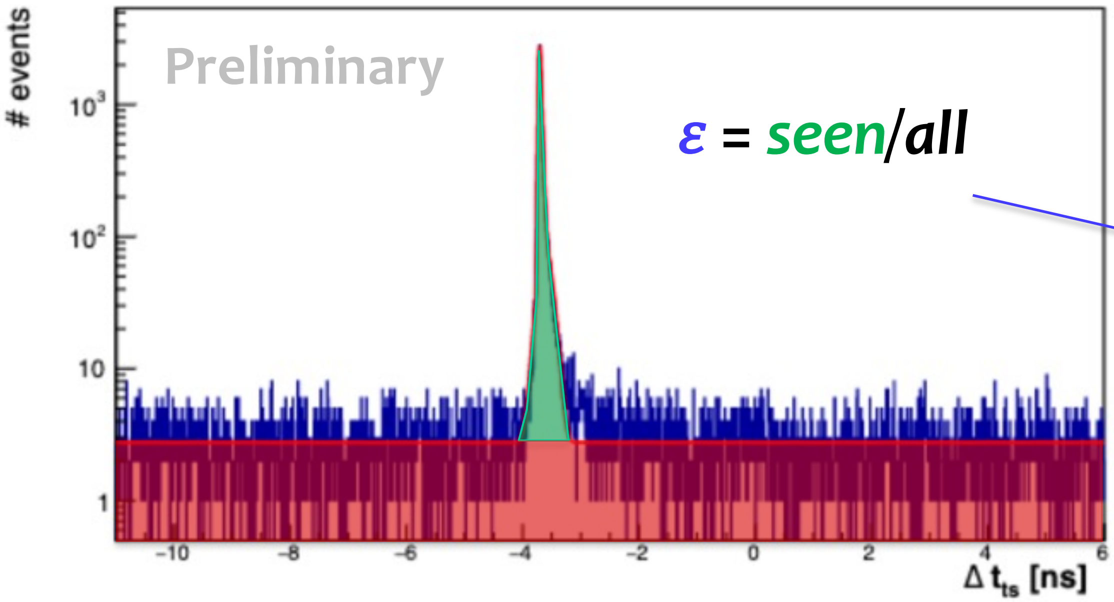


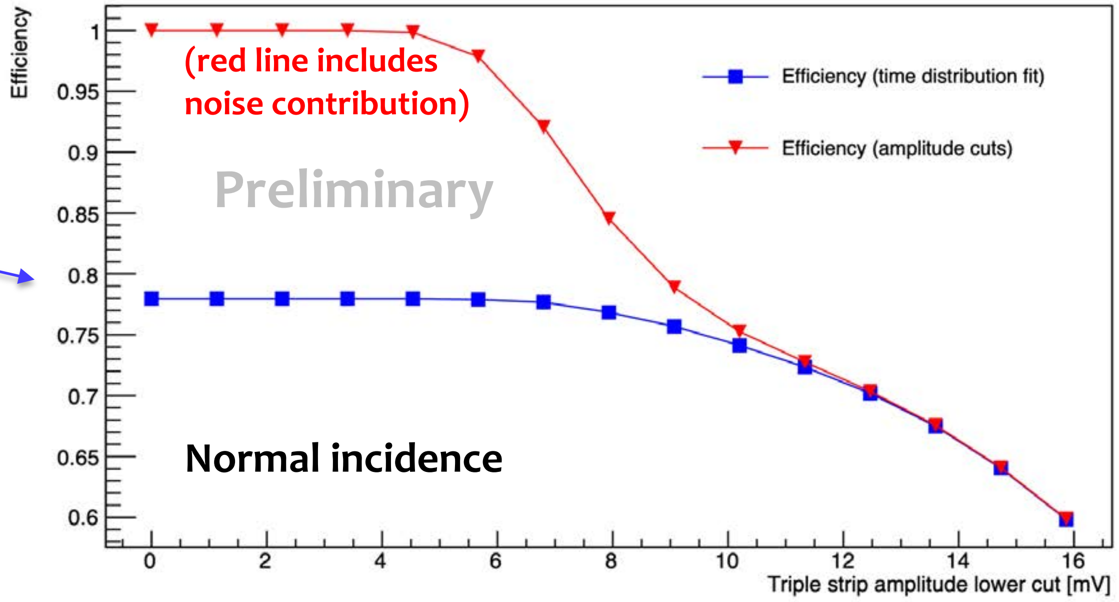
*time resolution from histogram RMS

Using the information of both pixels, timing performance improves

Efficiency: method

Time distribution t_{strip}- $t_{MCP\text{-}PMTs}$





- Time distribution of **all triple-strip signals** w.r.t. MCP-PMTs and count as ‘seen’ the ones under the peak (the flat background corresponds to undetected hits)
- 3D pixel detection (geometrical) efficiency at normal incidence is in agreement with calculated fraction of active area (~80%)