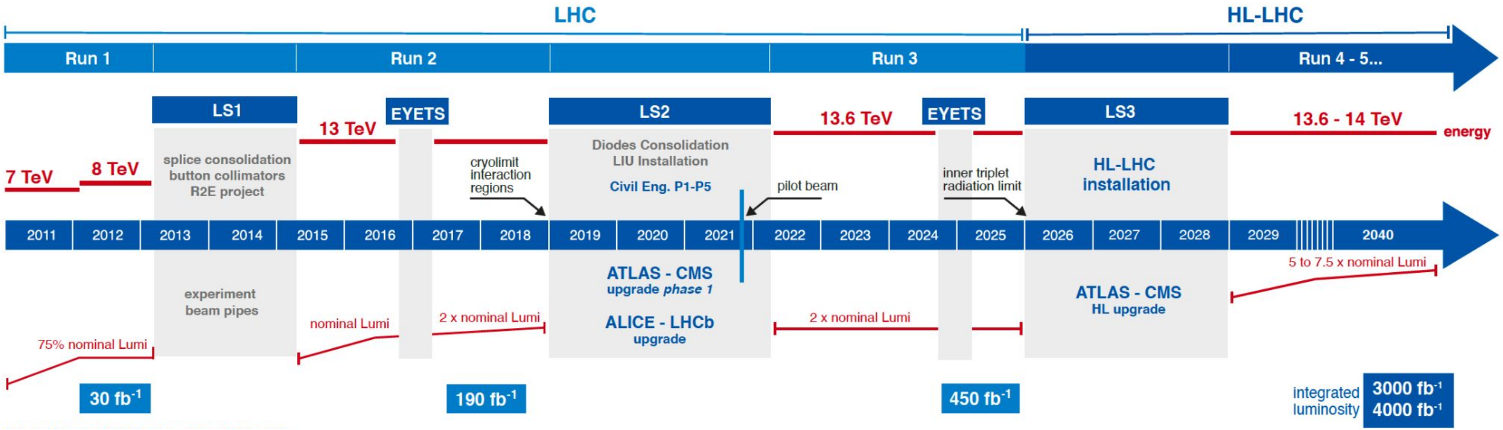
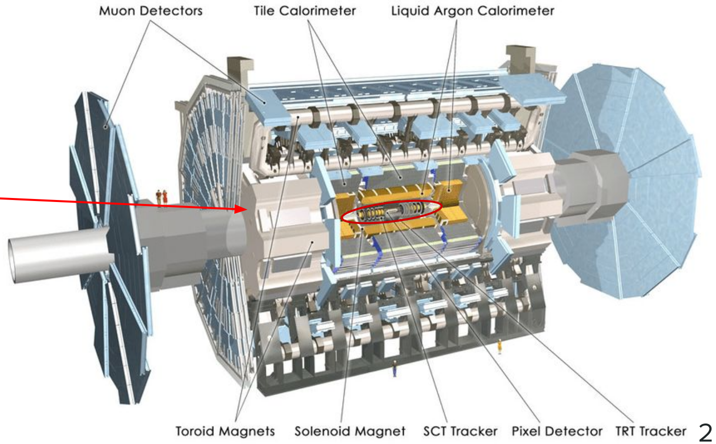
ITk Pixel Detector



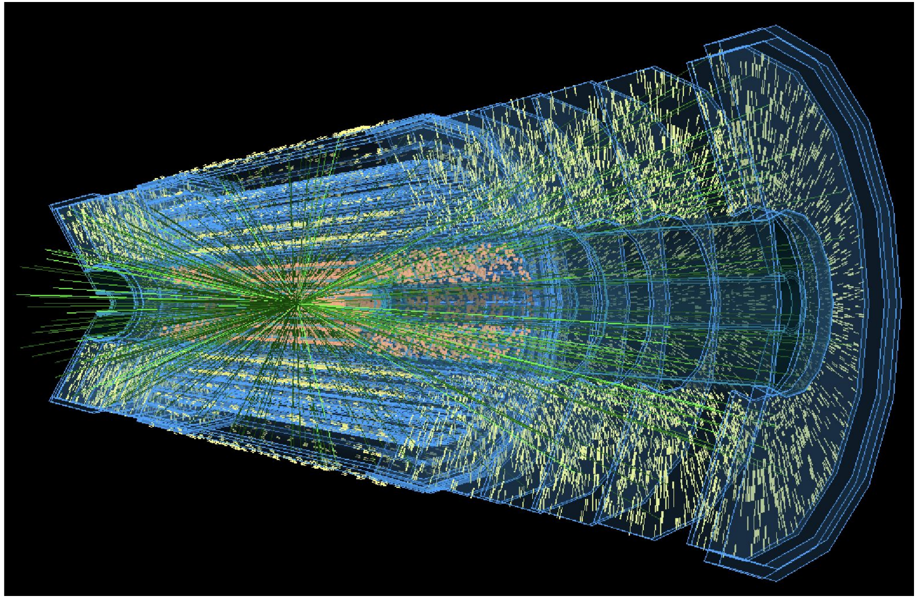
The LHC will upgrade to the HL-LHC in 2027

The ATLAS inner detector will be replaced by a new all-silicon Inner TracKer for the ATLAS detector (ITk)



The ITk is designed for :

- Increase by factor 7 on the instant luminosity
  - Higher granularity of sensors
- Increase in data rate:
  - Average multiple pp collisions (pile-up) increases from <μ> = 50 to <μ> = 200
- Improved radiation tolerence:
  - Radiation levels will increase by a factor 20,
- Integrated luminosity of up $4000fb^{-1}$
- Increased acceptance upto eta 4



(A simulated event at the HL-LHC, with a future inner tracker. Credit: ATLAS)

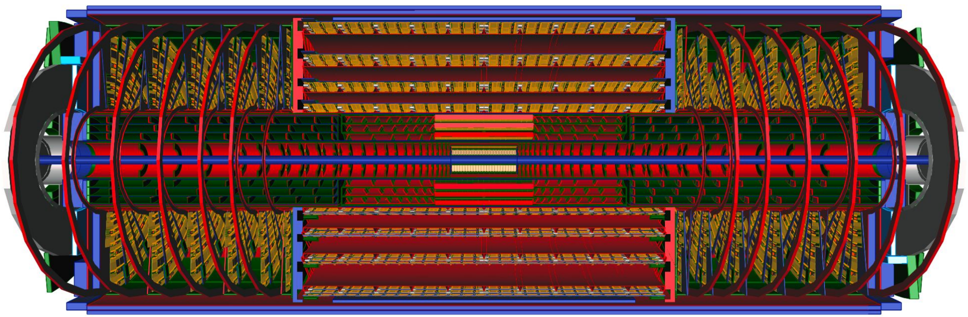
ITk Design

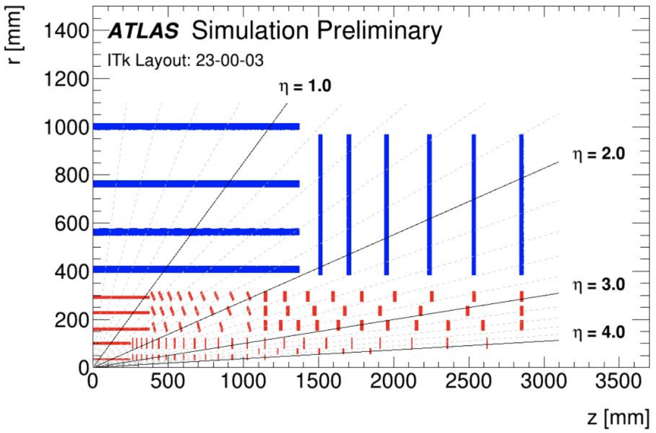
Strips: 4 barrel layers, 12 disks

Pixels: 5 pixel layers

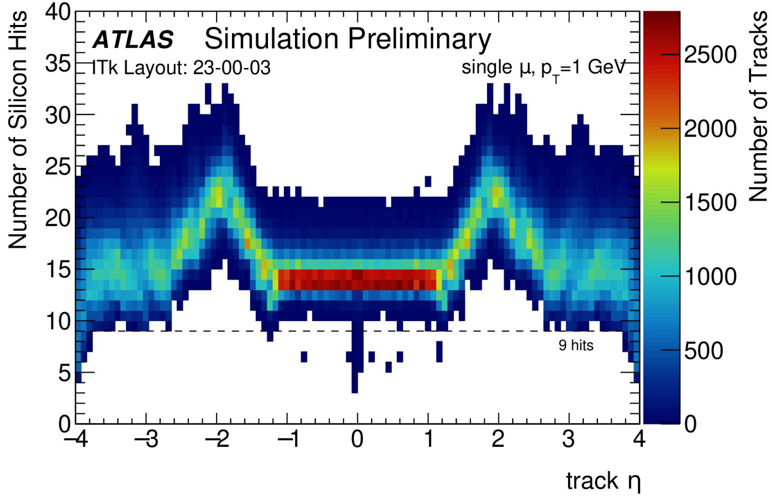
Together: ≥ 9 Si Hits per track

All supported on low mass CF supports.

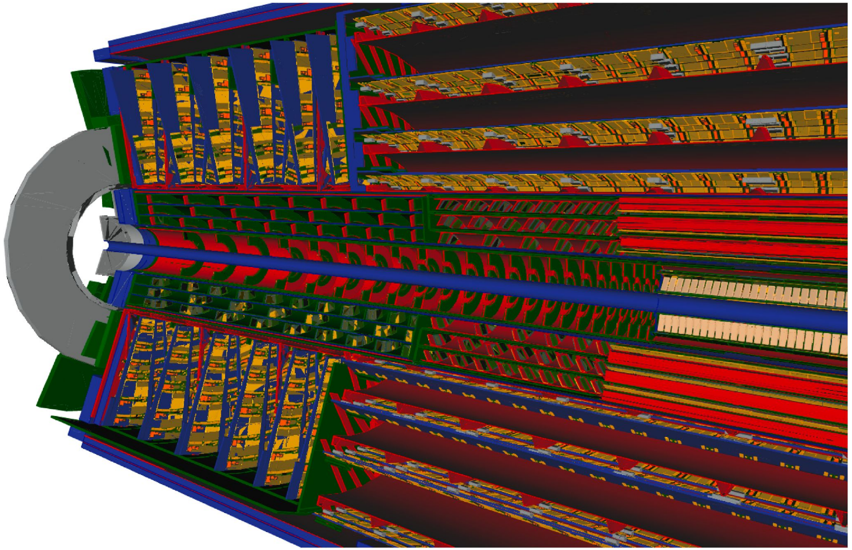




(ATL-PHYS-PUB-2021-024)



Pixel Detector

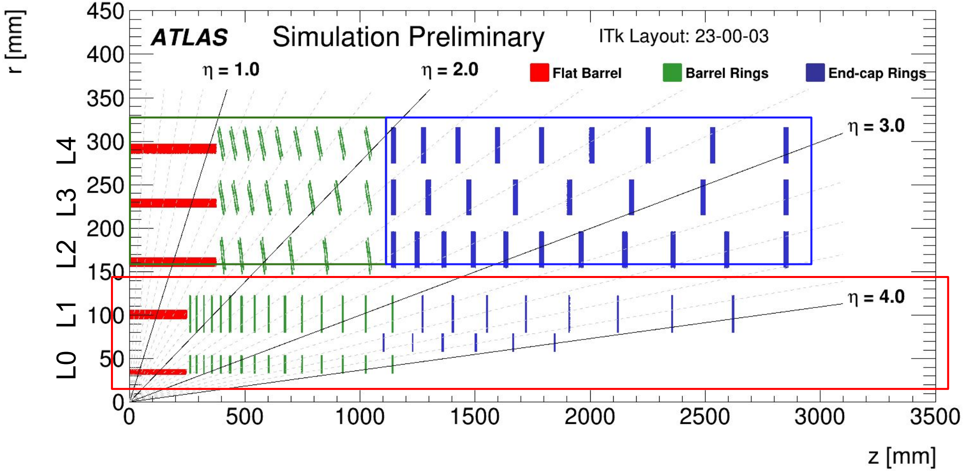


Outer System (L2, L3, L4)

- Outer Barrel: flat staves and inclined rings
- Outer EndCap: Rings

Designed to perform for HL-LHC@4000fb^{-1}

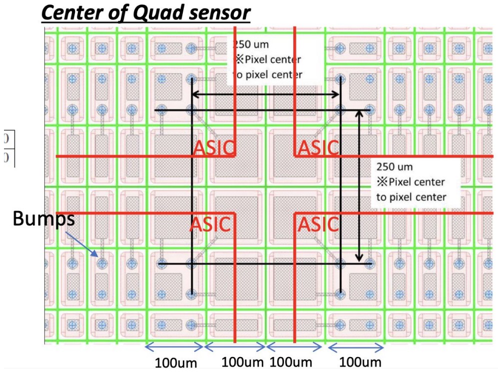
- Fluence upto ~ $5\times10^{15} n_{eq}/cm^2$ (2.5 safety factor)



Inner system (L0, L1)

- Inner System: Flat staves and rings.
- Designed to be replaced
- HL-LHC@2000fb^{-1} (2.5 safety factor)
  - Fluence upto $1.9\times10^{16} n_{eq}/cm^2$
  - TID up to 1 Grad

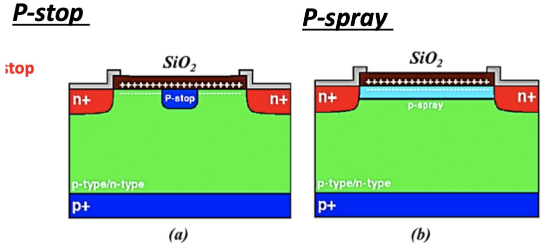
Pixel Sensors

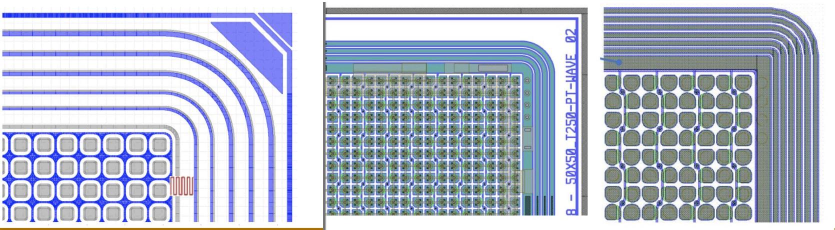


Planar:

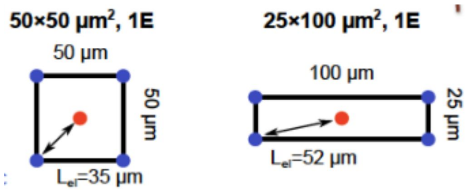
Various design left up to vendor:

- P-stop or p-spray insulation
- Polysilicon bias or punch through
- Guard ring geometry
- Requirements defined on performance

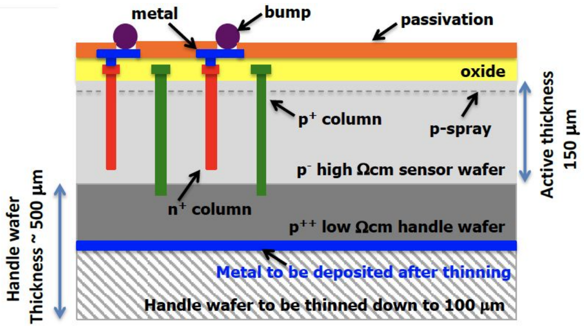




3D



- Higher radiation tolerance
- Lower bias voltage

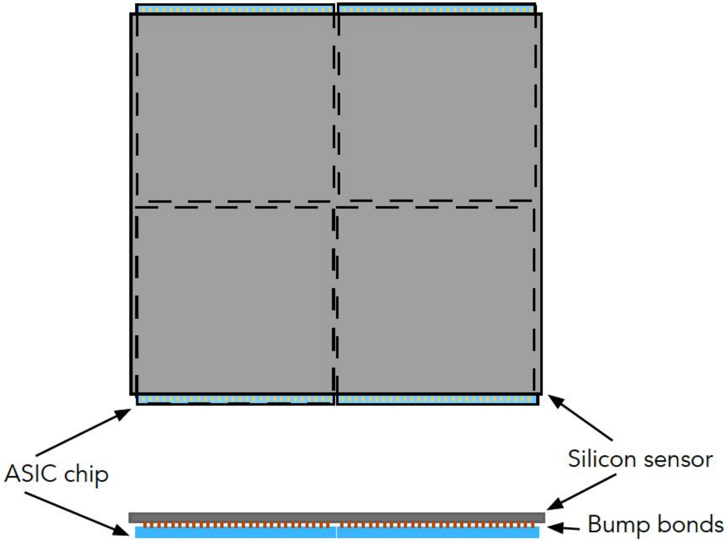


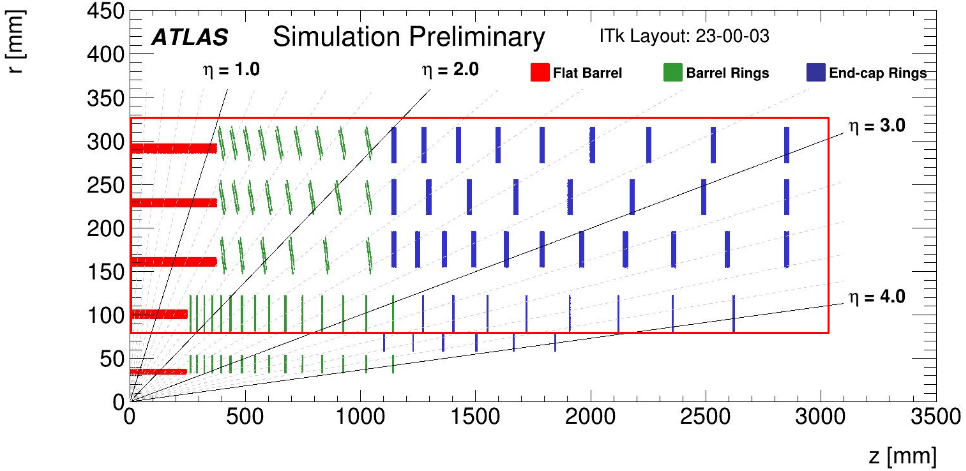
The pixel modules

Total 5x 10^9 pixels, 8372 modules (7976 quads, 396 3D)

Flip-chip assembly of Silicon sensor with ASIC

Printed board flexible circuit glued on sensor, wire bonded to ASICs





Planar Quad modules:

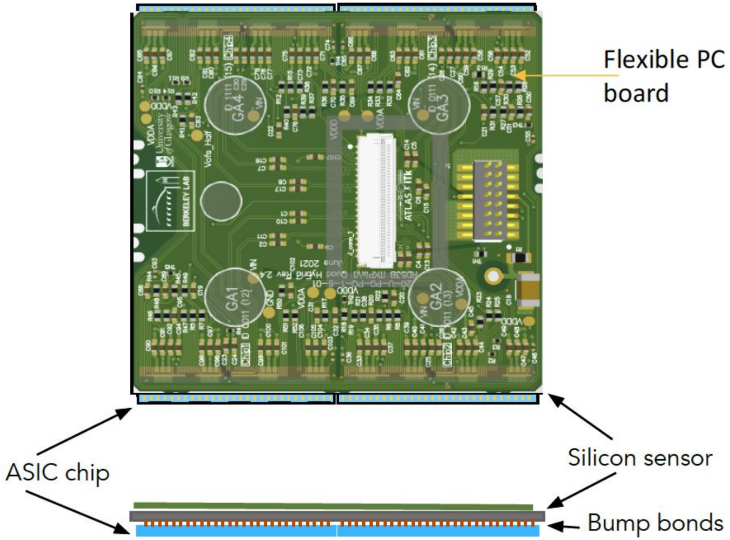
- 50x50 µm
- Planar sensor
  - L1 - 100 µm thick sensor
  - L2,L3,L4 - 150 µm thick sensor
- ASIC - 150 µm thick

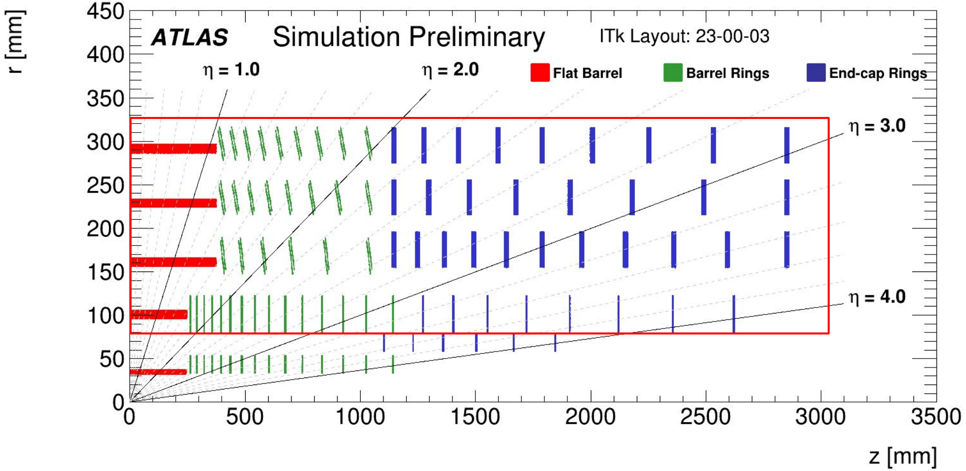
The pixel modules

Total 5x 10^9 pixels, 8372 modules (7976 quads, 396 3D)

Flip-chip assembly of Silicon sensor with ASIC

Printed board flexible circuit glued on sensor, wire bonded to ASICs





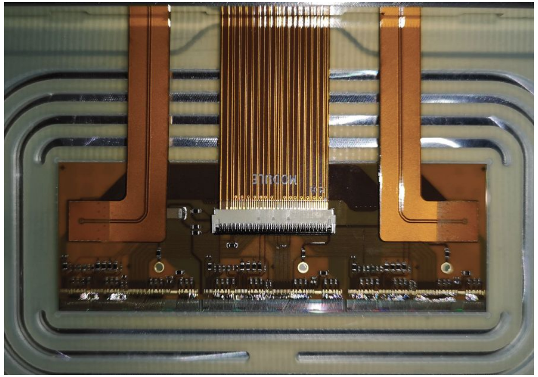
Planar Quad modules:

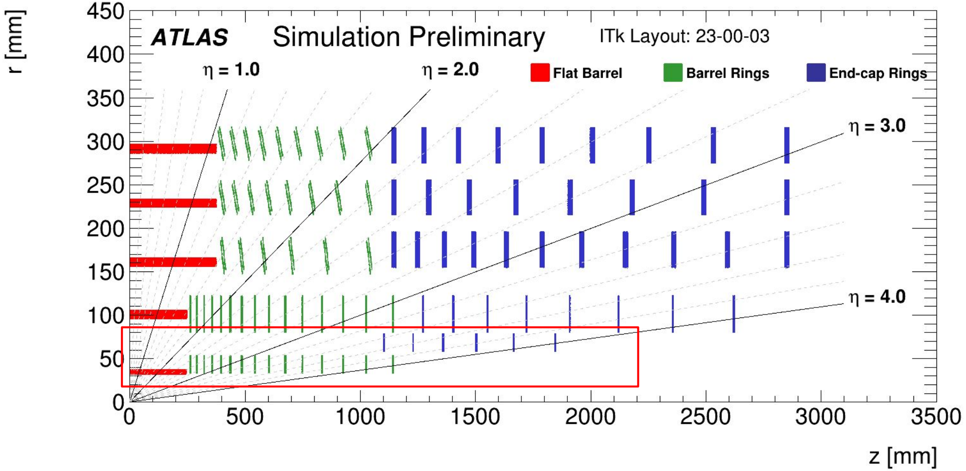
- 50x50 μm
- Planar sensor
  - L1 - 100 μm thick sensor
  - L2,L3,L4 - 150 μm thick sensor
- ASIC - 150 μm thick

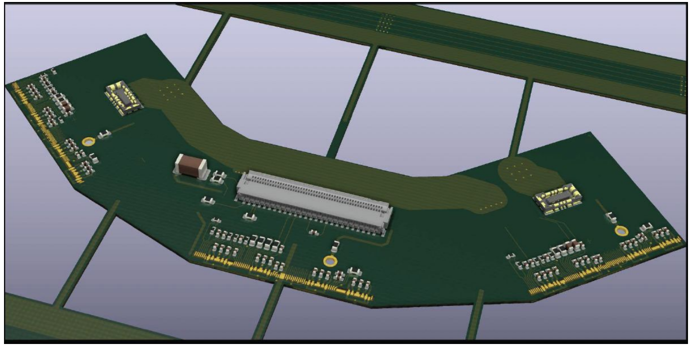
3D pixel modules

L0: 3D 150um, triplets

- L0 is 34mm from the beam axis, EC rings down to 33.2 mm
  - (Current pixel detector is 33mm)
- 25x100μm^2 in the stave, 50x50μm^2 in the rings
  - Choice is to optimize impact parameter resolutions





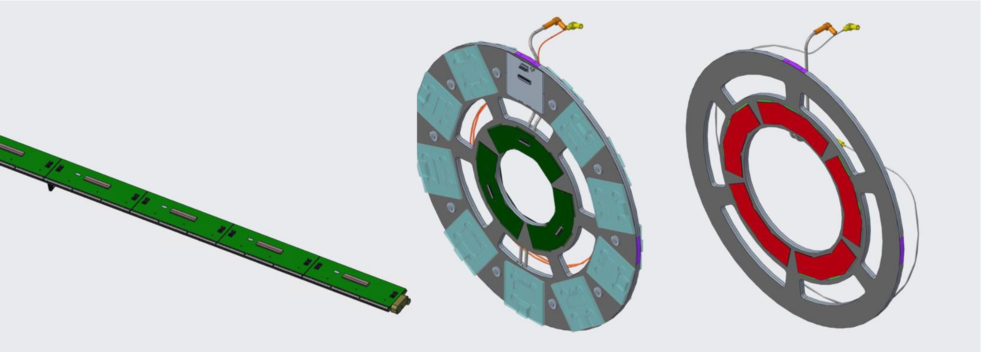


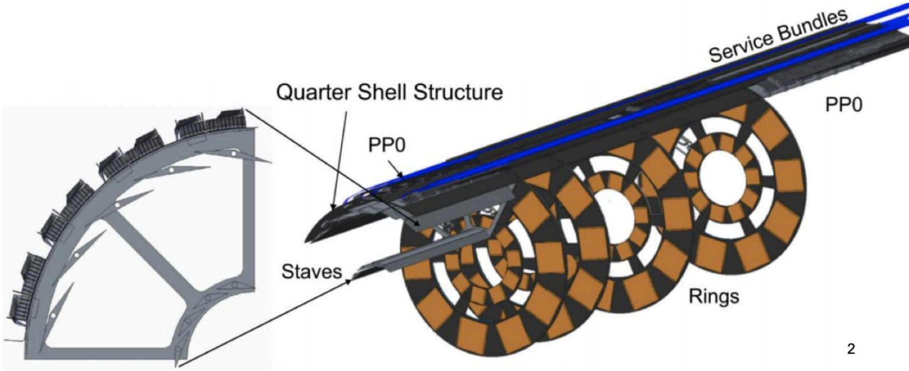
Inner Pixel System Layout

Barrel (stave)
L0: 96 triplets
12 staves x 8 triplets

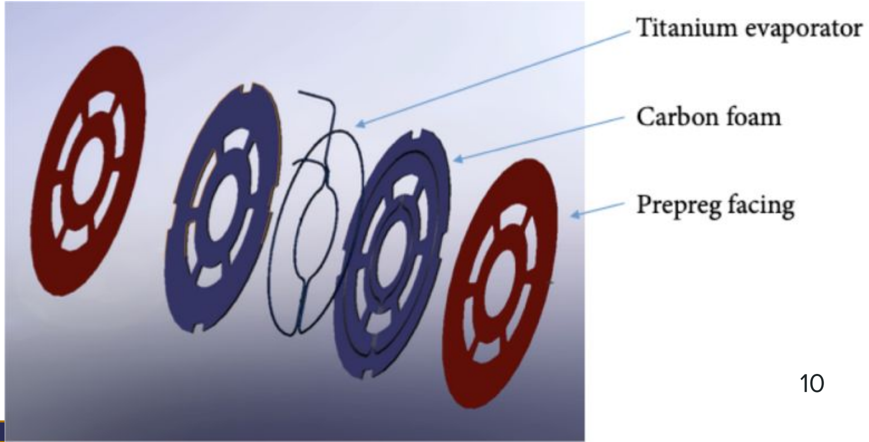
R0: 180 triplets
30 rings x 6 triplets

R0.5: 120 triplets
12 rings x 10 triplets

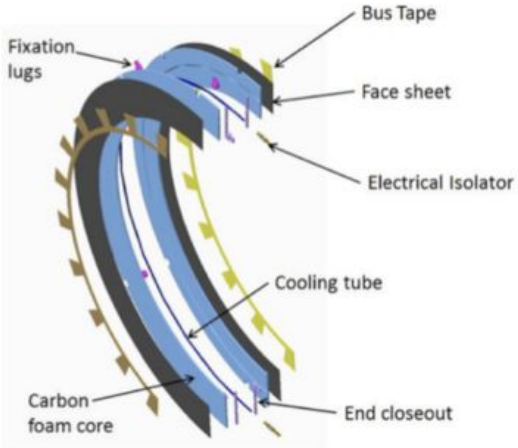


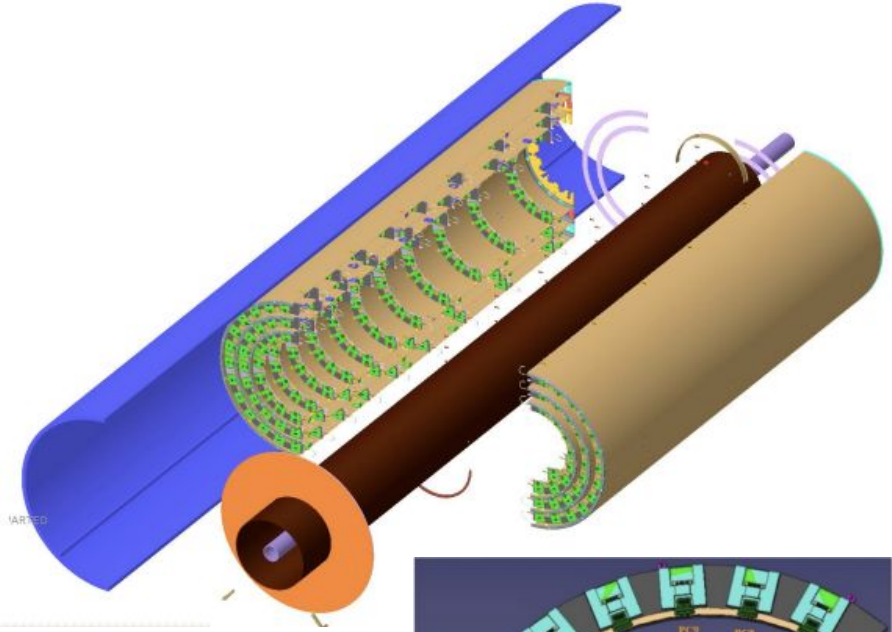


- Cooling integrated into local support
- Services integrated in shell structure
  - Patch panel (PP0) for data and power transmission
  - Other services in the quarter shell

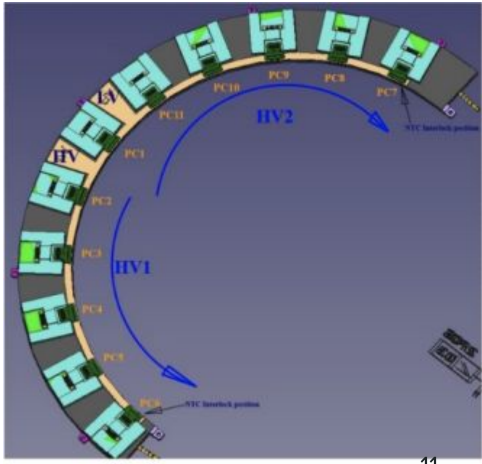


Outer Endcap Layout





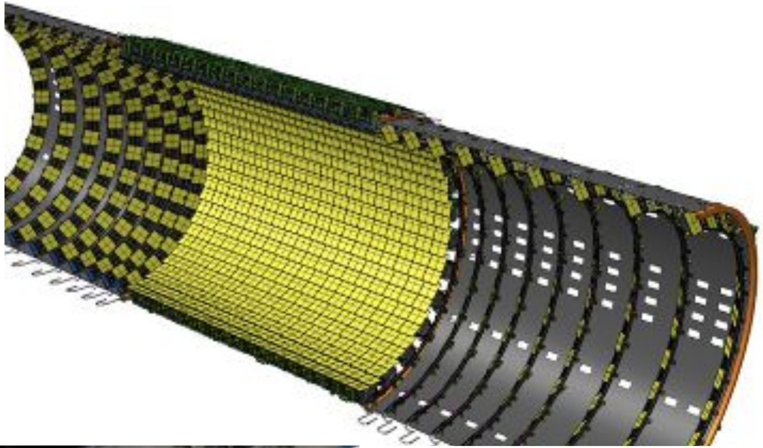
- Each outer EC has 6 carbon fibre half-cylinders
- 3 sizes (L2, L3, L4) of local support
  - 16, 22, 26 modules on each local support
- One serial powering chain per side
  - Upto 13 modules per SP chain
- Cooling pipes integrated into local support

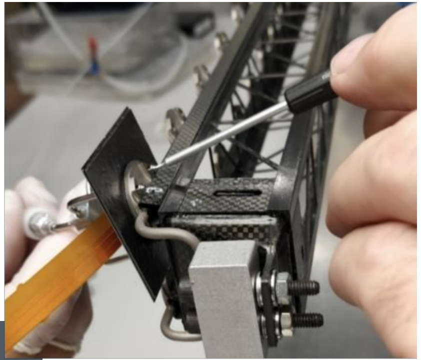


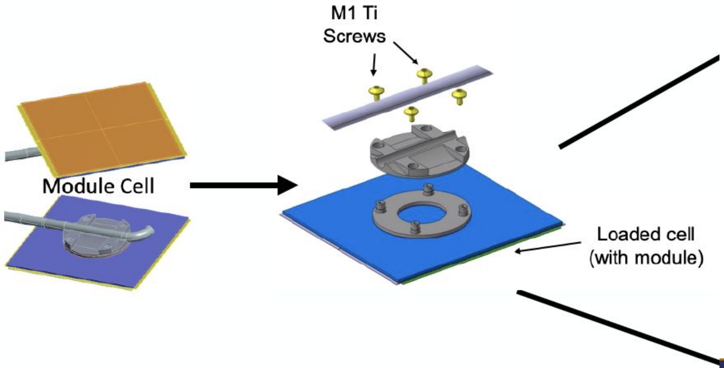
L3

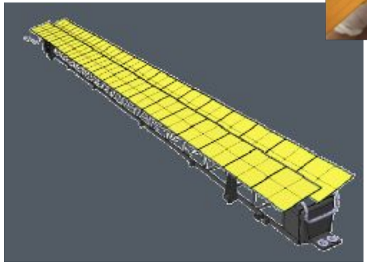
Outer Barrel Layout

- The outer barrel consists 3 half shells of staves and inclined rings
    - 4SP per stave, 2SP per half ring
- cooling to the OB modules provided by cooling-cells which interface the module to the cooling pipe mounted on the CF support









Mechanical prototypes

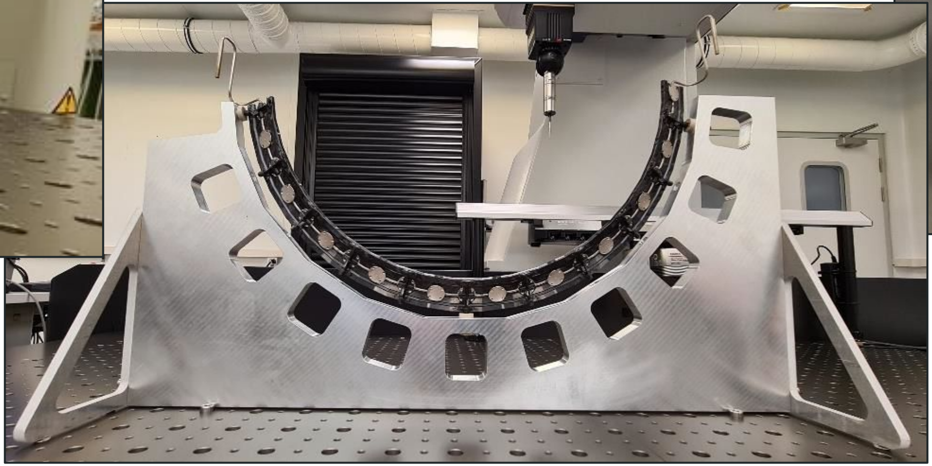
Prototypes of different mechanical supports produced and evaluated.

Metrology, evaluation of thermal properties, thermal cycling, vibration analysis

EC half-ring

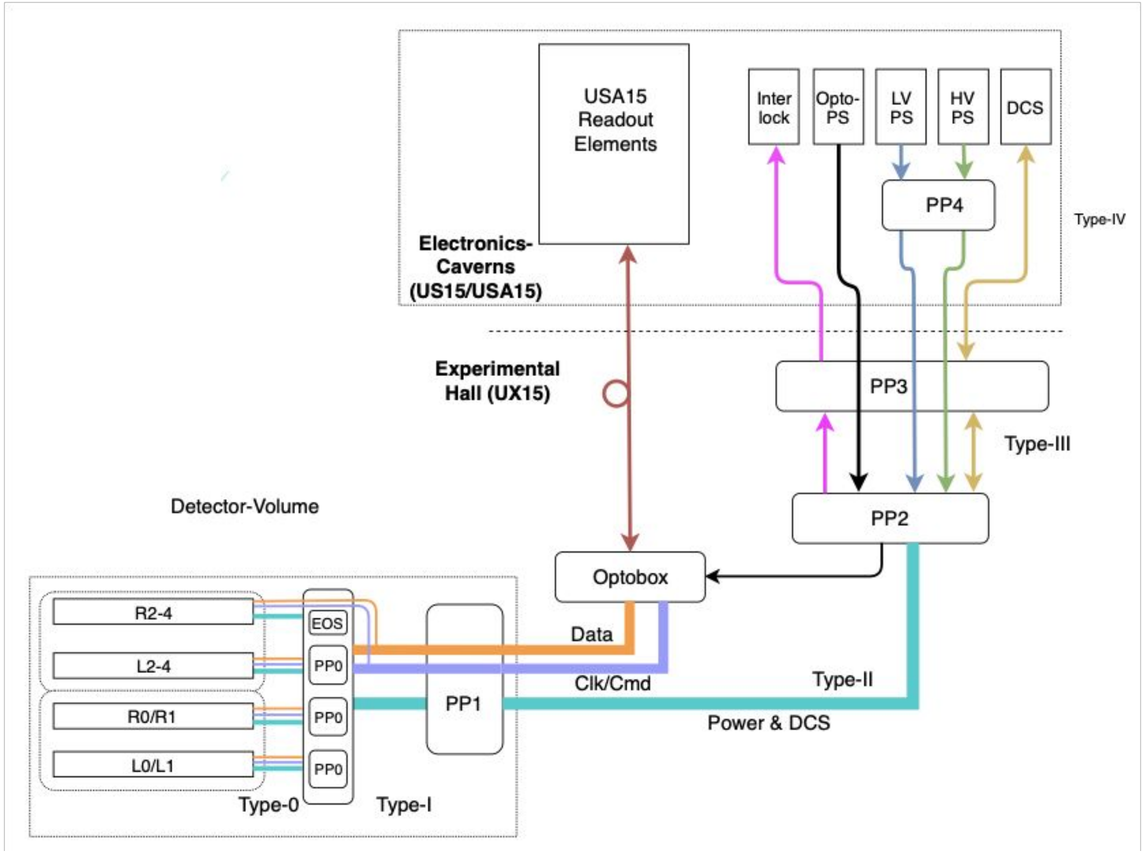
OB longeron

OB inclined half-ring



ATLAS ITk pixel services

- SP chain of upto 13 modules
- Quad modules connected to PP0 via pigtails and type0 services. Voltage and temperature are monitored by one MOPs chip per SP chain



- Data is driven to optobox (outside detector volume) by twinax cables at 1.28 Gbps, and by optical fibre from optobox to readout.

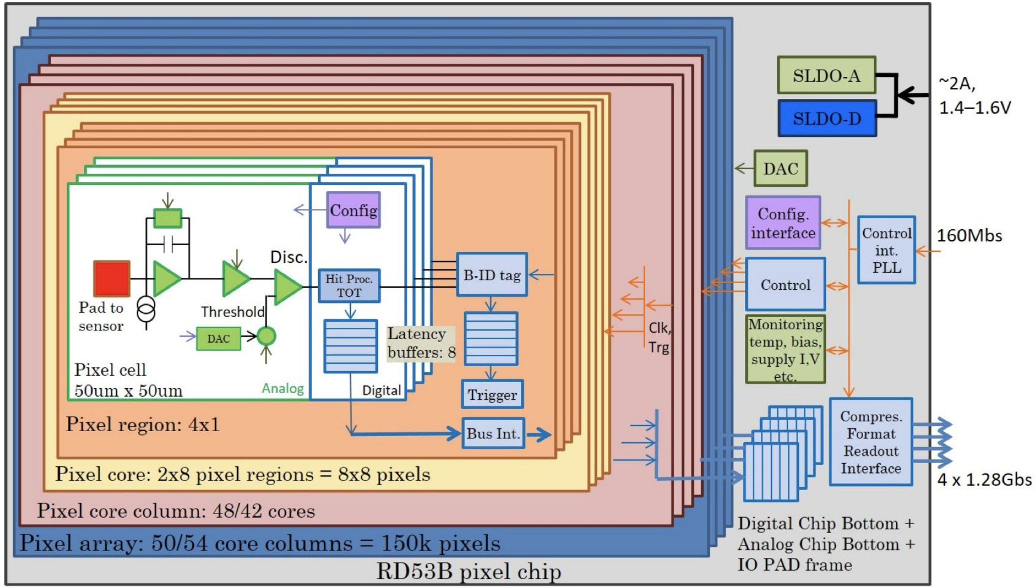
Readout chip

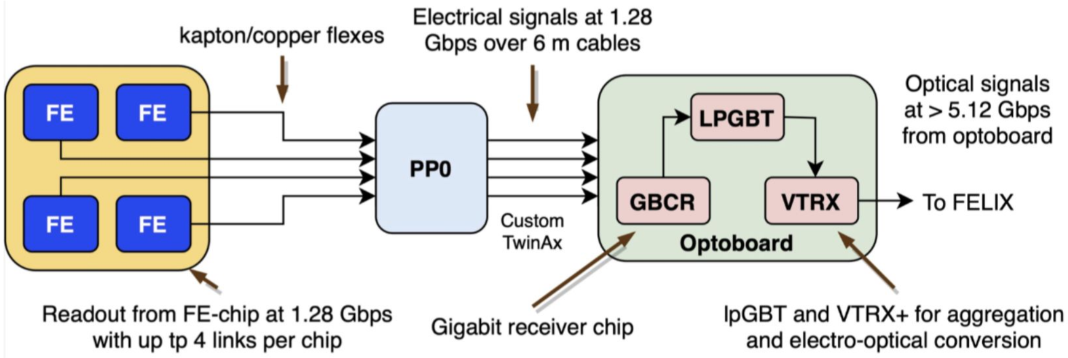
All modules readout with the same “ITkPix” ASIC

- ATLAS flavour of RD53 common ASIC

Main features:

- 152800 pixels per chip (384 rows per 400 columns)
- 65nm technology, 50x50 μm2, total area 2x2 cm2
- 4 data links per chip at 1.28 Gb/s,
- **“Differential” analog input**
- Digital readout with Time over Threshold
- Column readout, data encoding
- 40 MHz clock with 780ps phase adj.
- Data merging: FE readout via another FE
  - Used in lower occupancy layers





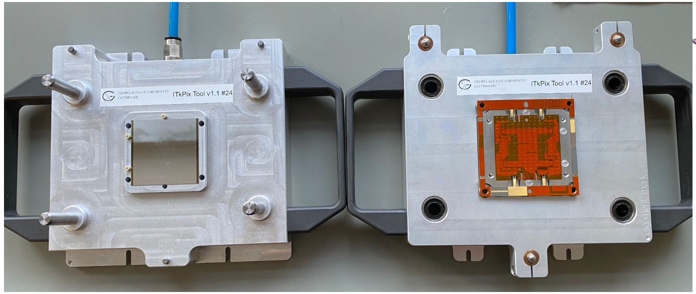
RD53A program

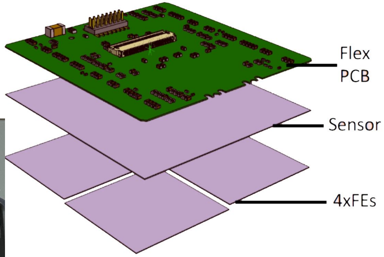
FEI4 (R&D)-> **RD53A** (prototyping)-> ITkPixV1.1 (pre-production)-> ITkPixV2 (production)

Program of module building, QC, and serial powering tests on realistic prototype supports based on RD53A modules[CERN-RD53-PUB-17-001, https://rd53.web.cern.ch/]

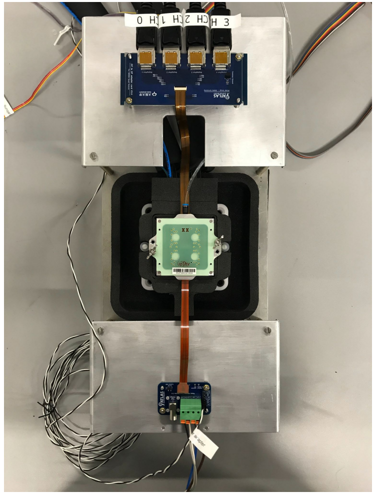
- A total of 163 RD53A Quads have been assembled in all assembly sites.
- Prototypes to mimic the real detector ⇒ study system aspects:
  - services,
  - PSU,
  - DCS,
  - cables, . . .
  - validate the loading concept
- What can we learn before moving to ITkPixV1.1 and pre-production loaded local supports and systems?
  - Includes processes, tests, equipment, time-taken……

Module assembly and QC





- In total 20 module building institutes
- Assembly based on tool with jigs incl. vacuum suction and dowel pin alignment
  - => 50µm alignment precision
- Glue height (40 ± 15 µm) adjusted with spacers and precision adjustment screws
- Glue dispensing on flex with stencil sheet
  - =>improvement of glue pattern
- After gluing -> Wirebonding
- **Currently development of new tooling for ITkpix chip ongoing**
  - =>**HV-protection with Parylene**



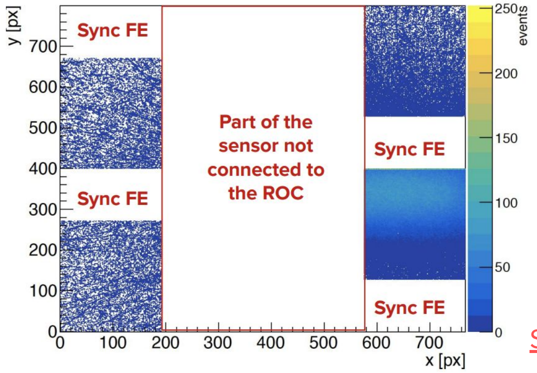
QC

- Visual Inspection
- Pull Testing
- Tuning and scans of front ends (FE)
- Monitoring of environmental parameters, voltages and currents
- Thermal cycling (to -55°C)
- test behaviour expected from CO_2 cooling
- Source scans to validate the functionality of the sensor pixels

RD53A module irradiation

Quad

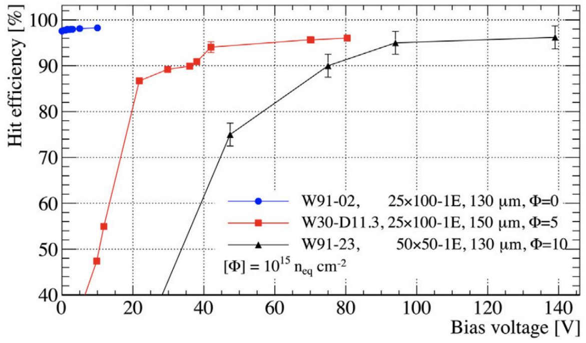
- 1 RD53a planar quad module (50x50) irradiated to $5 \times 10^{15} n_{eq} cm^{-2}$;ested in testbeam
- Due to RD53A's smaller size only half the sensor is connected. Sync. FE disabled
- Observed > 99% hit efficiency at 600 V



S.Hadzic et al.

3D

- 3D sensors have been irradiated and tested in testbeams at CERN and DESY
- Modules from 3 vendors, Italy, Spain and Norway
  - Irradiation tests of single chip modules from 3 vendors irradiated to $\Phi \geq 1 \times 10^{16}$neqcm^{-2} all show a hit efficiency > 96% at 100 V bias voltage



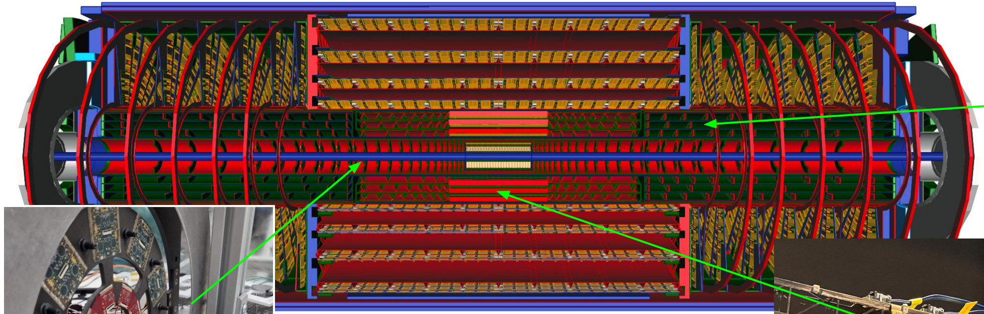
https://doi.org/10.3389/fphy.2021.624668

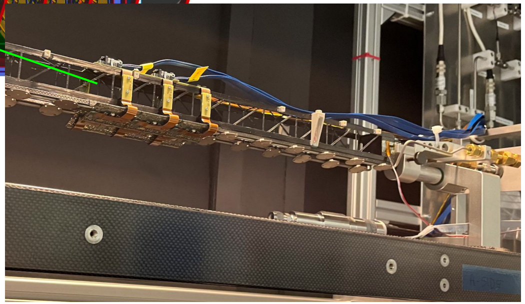
RD53a system test program

(More details in next talk)

How do we go from operating single modules to realistic serial power chains of modules fixed on their support structures?

- Program of 3 prototype loaded-local supports
- Testing of loading, electrical and mechanical functionality and robustness



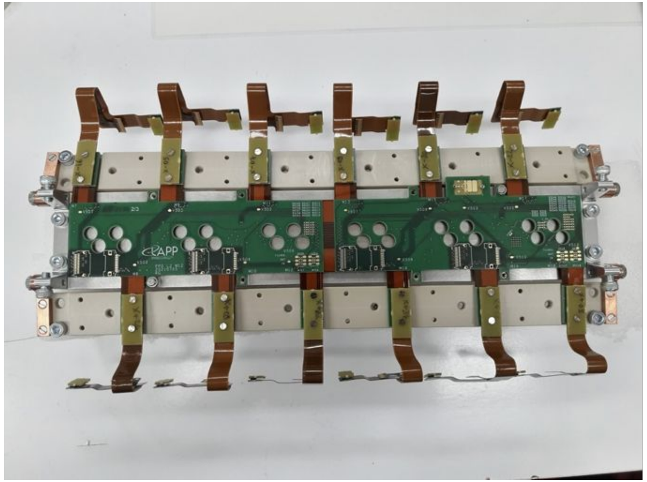


Inner System Prototype

Electric / DAQ prototypes:

- First loaded R0 ring with RD53A prototypes
- Tested with modules powered at room temperature
- No significant difference in digital scans / disconnected bump bond scans before and after loading -> no significant damage during loading
- One RD53A module read out with Type-0 ring + Ring flex + PP0

OB system prototype

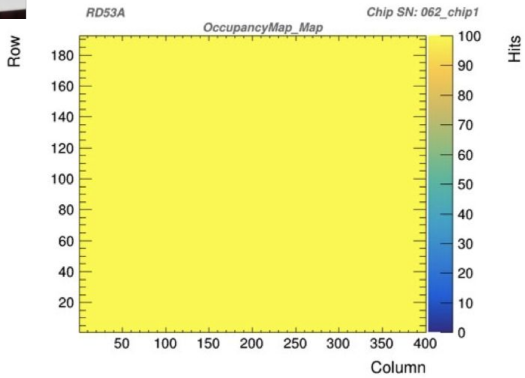


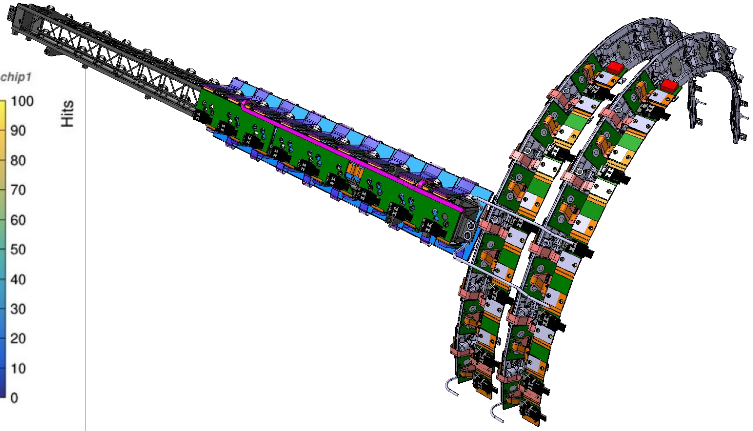
Multi-layer flex-rigid PCBs (Patch-Panel 0, PP0s) for the on-detector services of the Outer Barrel.

SP chains of upto 12(14) quad pixel modules in the OB flat (inclined) regions

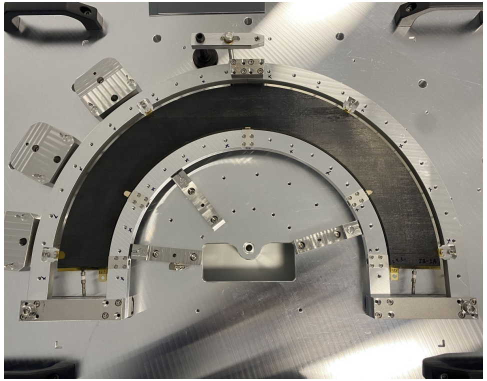
Readout tests performed using PP0, MOPs ASIC, module pigtail and RD53A digital module

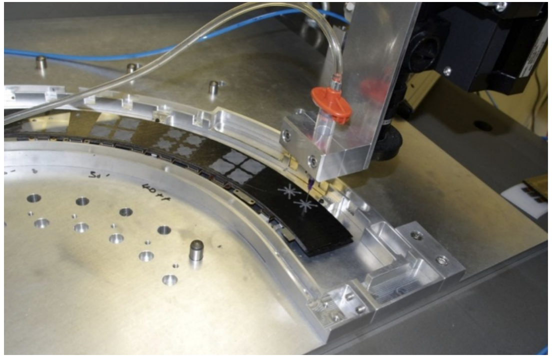
See next talk (B. Vormwald) for details





Pixel loading (e.g EC)

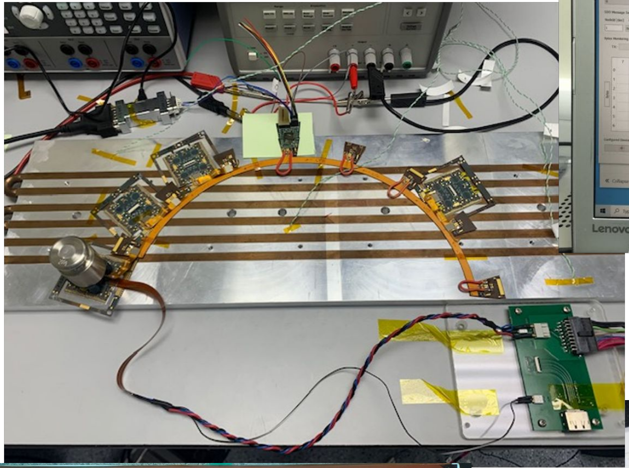


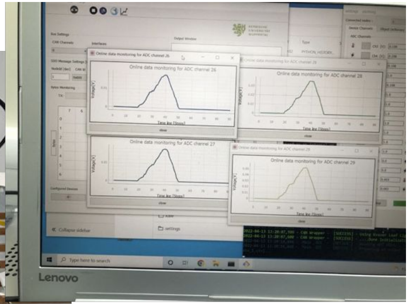


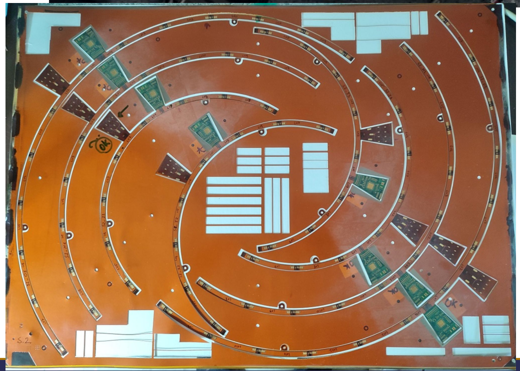
Ring 1 being prepared for System Test - 11 modules each side

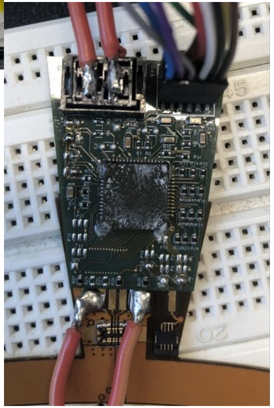
- Demonstrate different techniques of glue deposition and loading,
- Glass beads ensure very well control of glue layer (105+/- 13)µm
  - Used for EC and IS
- Placement accuracy in x and y better than 30µm

EC system prototype





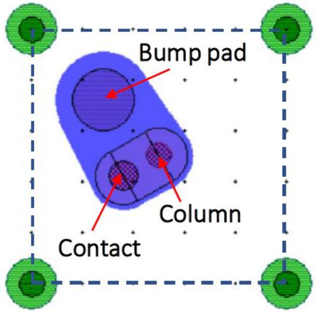


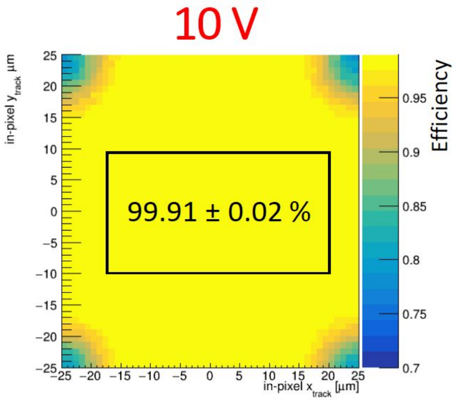


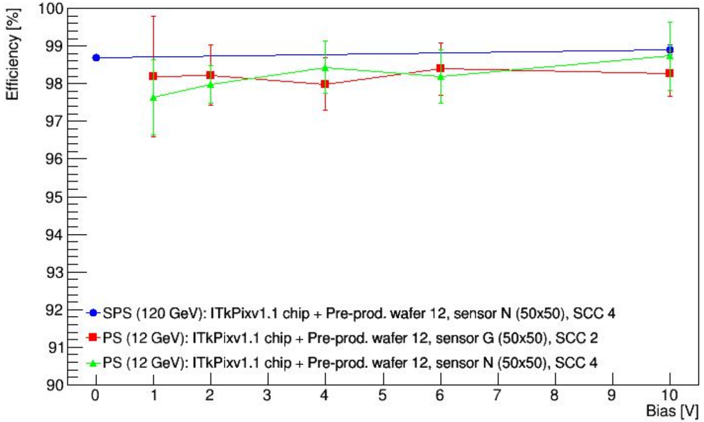
- Bus tape routes LV serial power, temperature and voltage monitoring lines to each module on a serial powering chain.
- EOS cards are the interface between the routing lines on the local supports and the cable bundles:
  - LV, includes the MOPs (Monitor of Pixel System) Chip, passive components and connectors.
  - HV, includes only connectors.
- Prototypes of bus tape and EOS cards have been tested with RD53 modules and used in first full prototype:
  - local support+bus tapes, EOS cards + modules.
- Serial current for both bus tapes is up to 4.5 A.
- Data rate is up to 5.12 Gb/s per front end chip.
- Event readout rate - 1 MHz.
- **Moving on to full analysis of ring 1**

ITkPix1.1 Testbeam results

- 8 Single Chip Card assembled in Genova: 2 bare chip (ITkPixV1.1) + 6 modules (ITkPixV1.1 + FBK 3D)
- Chips are responding properly, tuned to 1000 e threshold:
  - 70 +/- 10 e mean noise @ 10 V bias
- Sensors IV are compatible with wafer level measurements: leakage current <0.05 µA/cm 2 @ 25 V bias
- Testbeam data with proton beam perpendicular to SCC, unirradiated devices:
  - PS (1, 2, 4, 6, 10 V bias): efficiency > 97.5 %
  - SPS (0, 10 V bias): efficiency = 98.9 +/-0.1 % @ 10 V bias
    - Central area: efficiency = 99.91 +/- 0.02 % @ 10 V bias
    - Lower efficiency zones visible in corners (75% +/- 99%)
- SPS testbeam of irradiated SCC
  - 2 SCC to 1e16 n eq /cm 2 (Bonn, 14 MeV protons)
    - Preliminary >98% with less than 40 volts
  - 2 SCC to 1.7e16 n eq /cm 2 (IRRAD , 24 GeV protons)







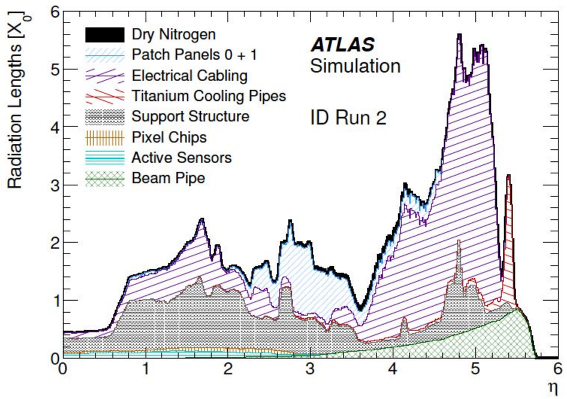
Lapertosa et al.

Overall Pixel Material

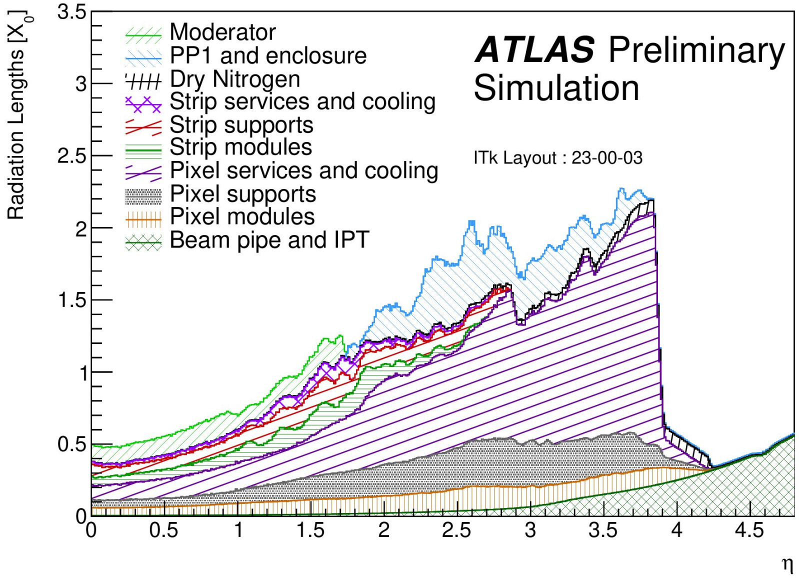
Reduced material budget w.r.t. Run-2:

- Evaporative CO_2 cooling with titanium pipes
- Carbon fibre supports
- Serial powering
- Optimised number of readout cables using link sharing

CERN-LHCC-2017-021



Result: Approximately half the X0 of the current atlas Inner detector

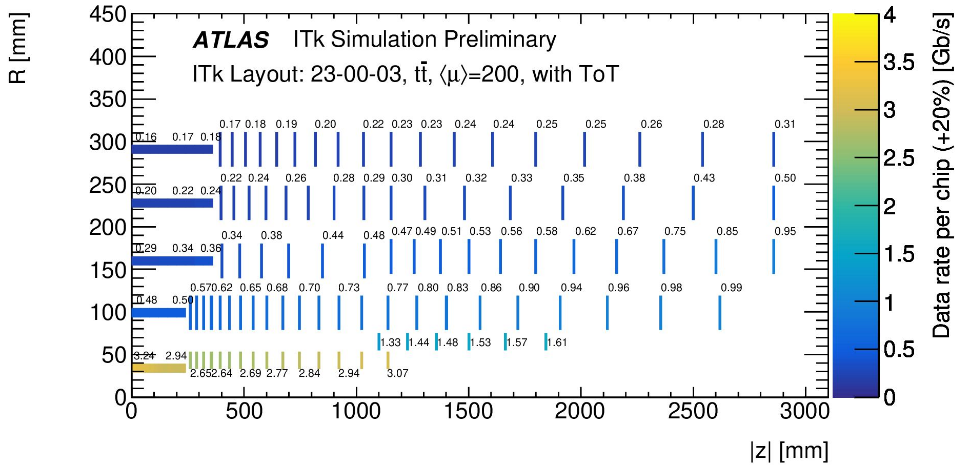


ATL-PHYS-PUB-2021-024

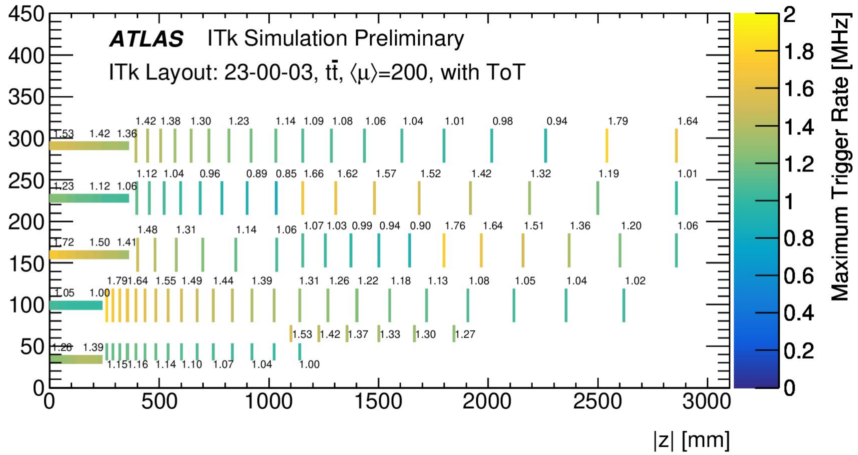
data rates

- With accurate material estimates of the detector we can predict the data and trigger rates of the pixel modules
  - The data format of the ITkPix read-out chip allows for 25% reduction to the average event size with respect to what obtained extrapolating from Run 2 data to the Phase-II conditions
  - Can optimise pixel chip discriminator thresholds or drop ToT information if needed

Data rate



Trigger rate limits



ATL-ITK-PUB-2022-001

Status

- Pre-production of pixel sensors is almost complete.
  - All planar sensors delivered, awaiting final 3D sensors - due by December
- RD53a module production exercise complete
  - Production procedures established, sites qualified
- Have demonstrated we can build the CF support structures
- Demonstrate we can load modules with required specifications, connect and electrically test
- **Now: evaluation of realistic loaded local supports with RD53a modules readout in serial power chains.**
- ITkPixV1.1 modules being built
- Finalize the electrical test procedure
- Proving sites are ready for production - procedures, infrastructure ready
- Final production tooling being prepared.

Summary

The pixel project is entering pre-production phase

RD53A program a vital milestone in the validation of the pixel detector design

Next step - full evaluation on pre-production ITkPixv1.1 modules, systems and structures

=> Production!