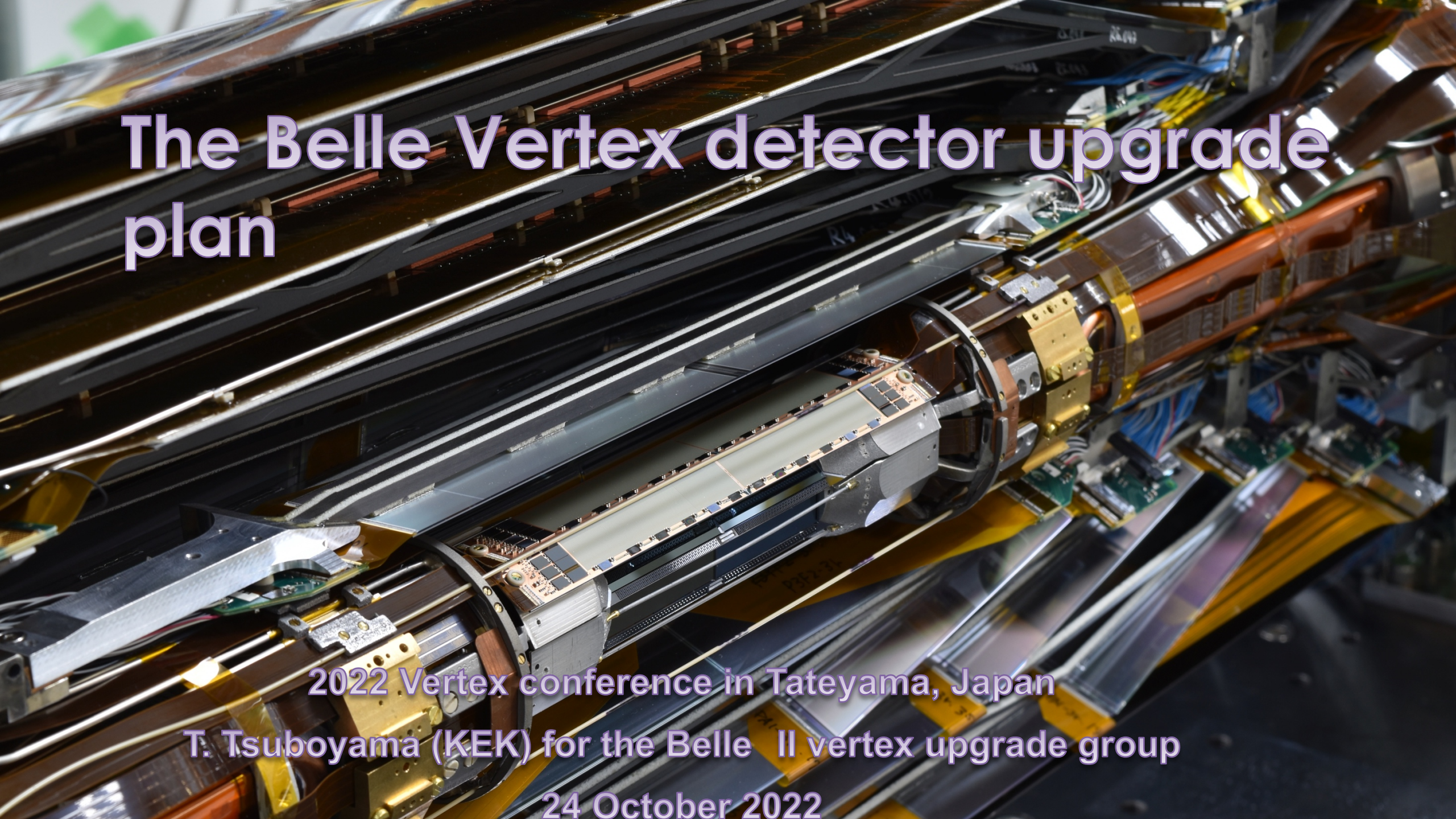
The Belle Vertex detector upgrade plan



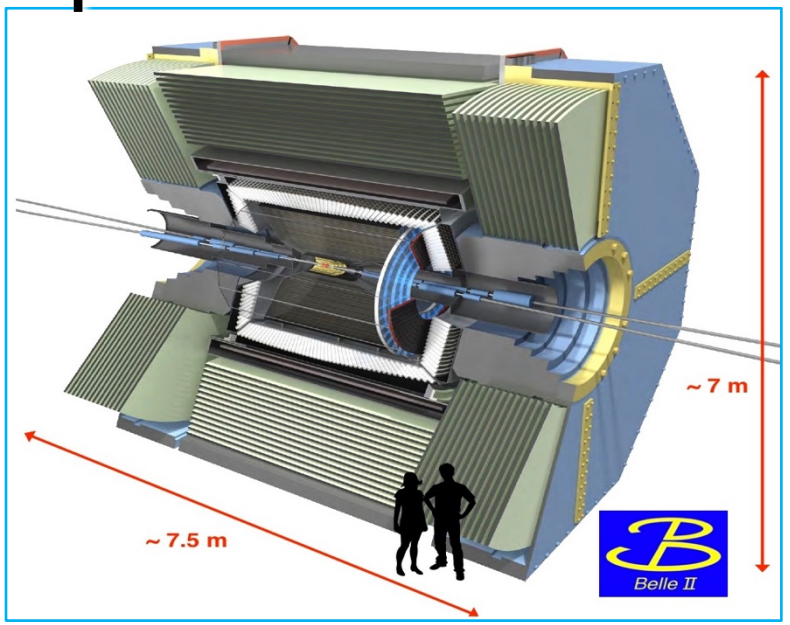
2022 Vertex conference in Tateyama, Japan

T. Tsuboyama (KEK) for the Belle II vertex upgrade group

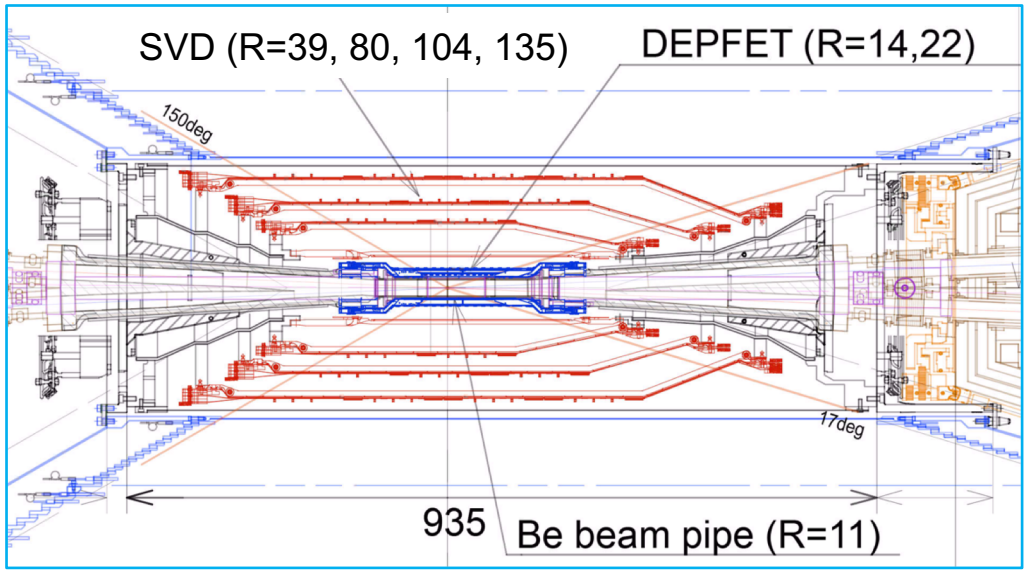
24 October 2022

Belle II experiment at Super KEKB

- Super KEKB is an asymmetric energy e^+e^-collider at the $\Upsilon(4S)$.
- Belle II aims to study, primarily, the B decays with high statistics.
  - The B mesons moves along the beam direction(z).
  - The position resolution in z is equally important to that in $r-\varphi$.



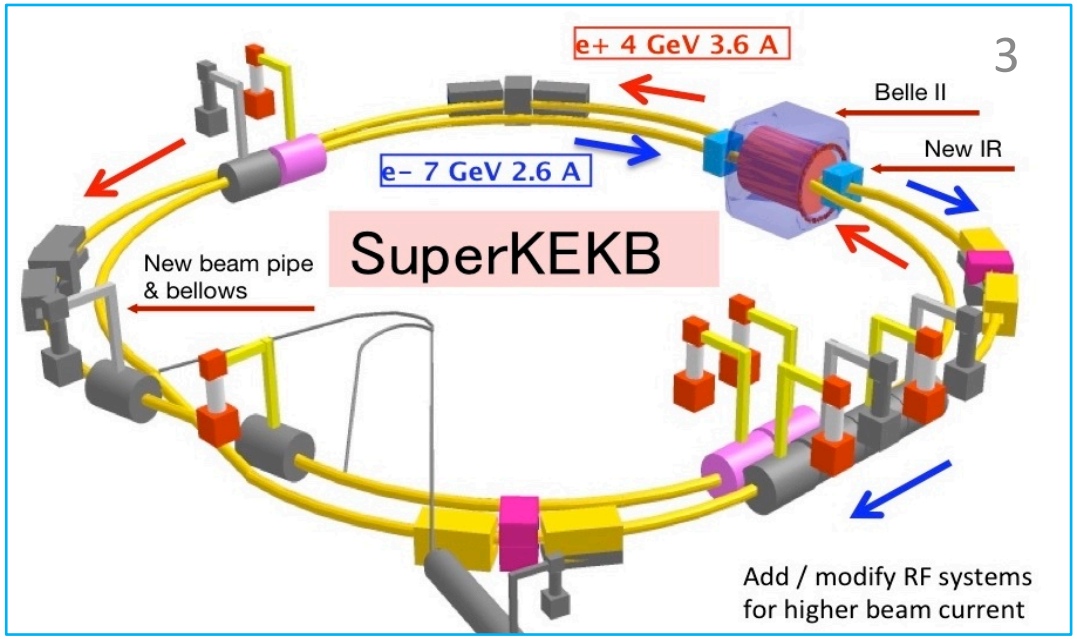
- The current Belle-II vertex detector (VXD) consists of
  - Two Layers DEPFET pixel detector (PXD)
  - Four Layers double sided strip sensors (SVD)
- The angular acceptance $17° < \theta < 150°$ covers 99% of the CMS solid angle.
- The VXD has been working successfully since 2018.
- The performance of the current system is reported in this conference.



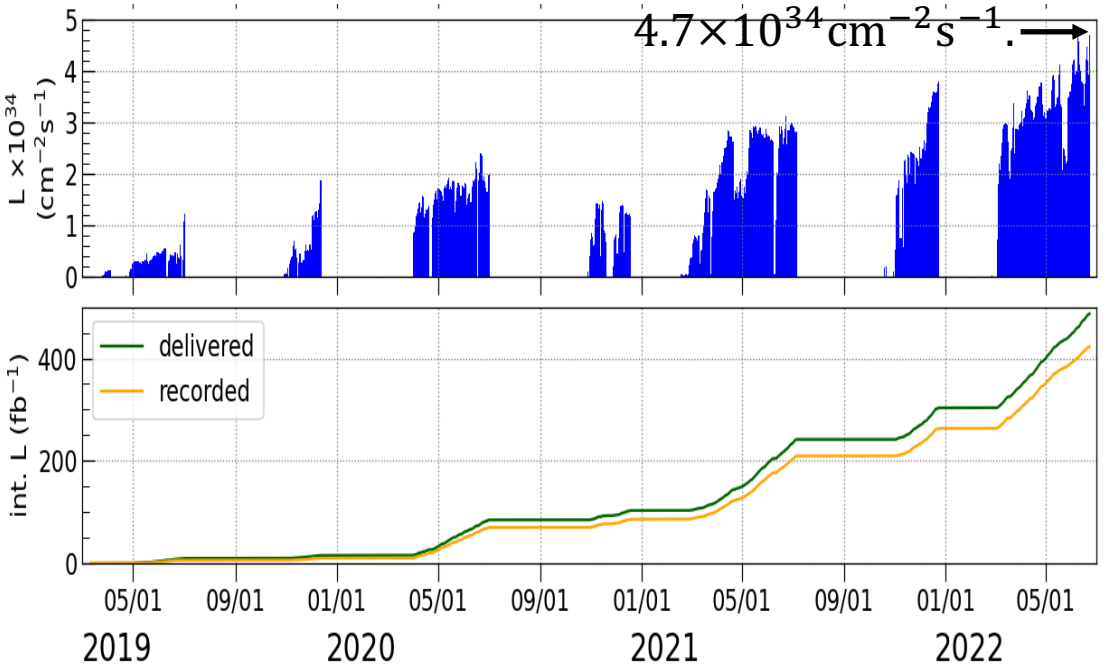
Talks in this morning *Arthur Bolz (PXD)*
Kookhyun Kang (SVD)

The Super KEKB

- The nano-beam scheme is adopted.
  - The beam bunches are shrunk to $0.05\ \mu\mathrm{m} \times 10\ \mu\mathrm{m}$.
  - The accelerating RF is 509 MHz and minimum collision spacing is ~2 ns.
  - The beam life is 10-15 minutes.
  - The radiation background level at the collision point is high.

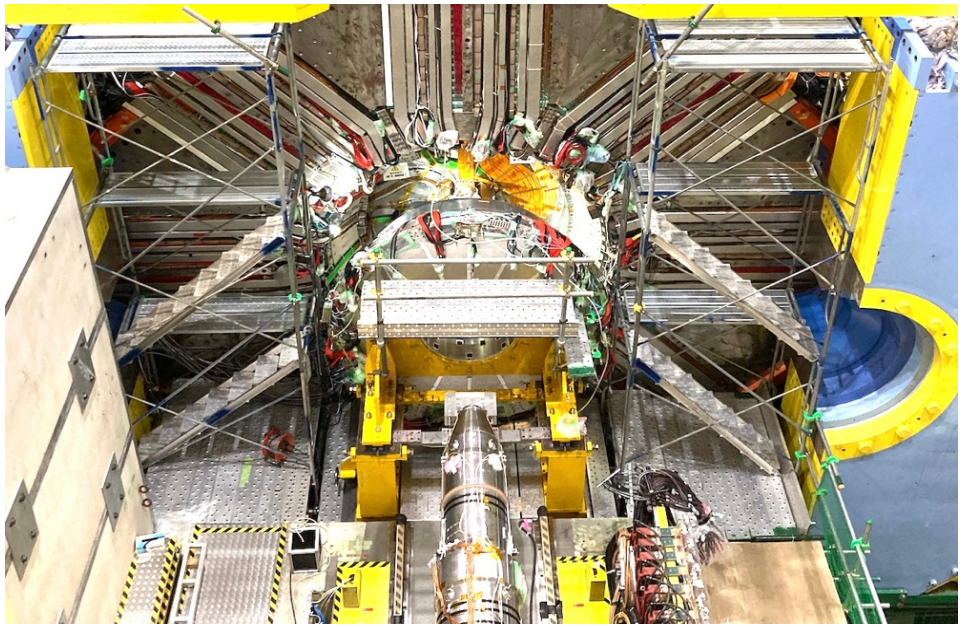


- July 2022
  - The peak luminosity reached to $4.7\times10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$.
  - Beam current LER/HER = 1A
  - Accumulated data corresponding to $428\ \mathrm{fb}^{-1}$.

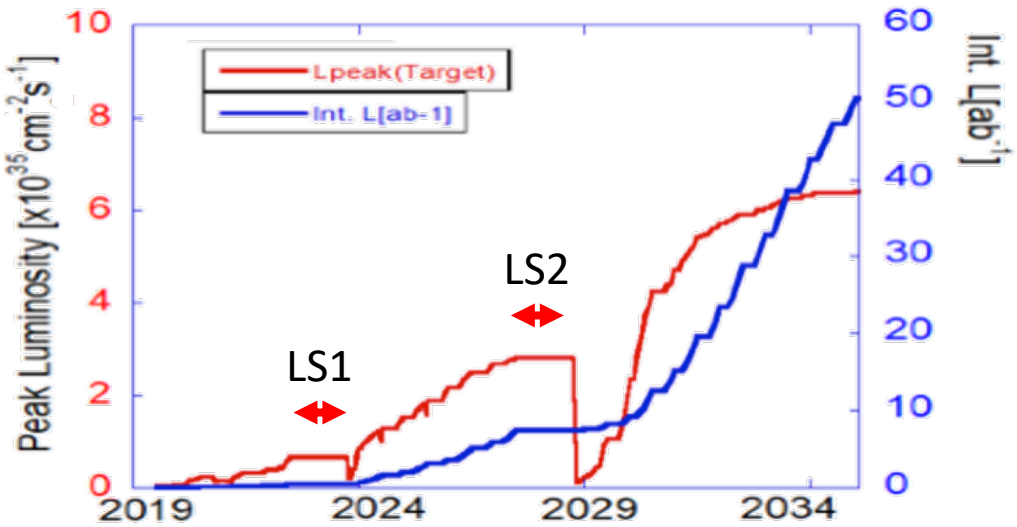


Belle II upgrade plan

- Belle II is under Long Shutdown 1 (LS1)
  - Completion of the DEPFET pixel detector.
  - Reinforcement of the outer detectors against the beam backgrounds.
  - Improving the accelerator for the stable operation and higher luminosity.



- The Belle II vertex detector upgrade takes place in LS2.
  - Luminosity goal is $\mathcal{L} = 6.5\times10^{35}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ and $\int \mathcal{L}\,dt = 50\ \mathrm{ab}^{-1}$.
  - LS2 is tentatively scheduled at 2027-2028.



Key issues of the vertex detector upgrade

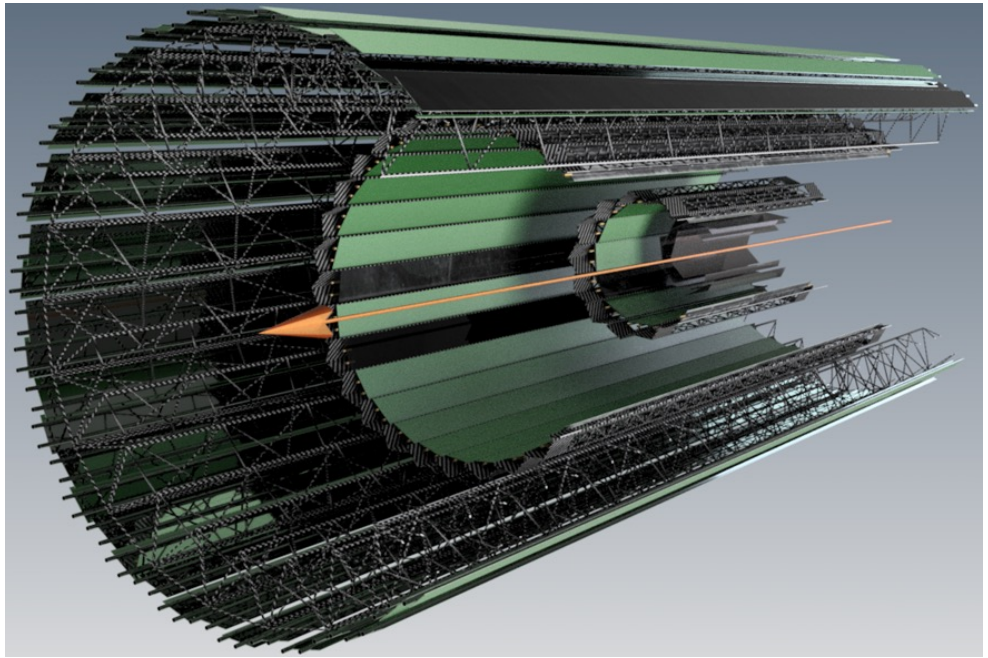
- The vertex detector should be designed assuming 5 x luminosity goal: $\mathcal{L} = 4\times10^{36}\mathrm{cm}^{-2}\mathrm{s}^{-1}$
- Background hit rate
  - The background hit rate at the innermost layer is estimated to be 113 M hits/cm^2/s.
- Radiation hardness
  - Backgrounds are estimated to be: TID: 10 Mrad/year and NIEL flux 5x10^{13} /cm^2 /year
- Trigger latency
  - The Belle II trigger system takes >5 μs for the trigger decision.
- Low material
  - Thinned sensor is beneficial to keep low material in the tracking volume.
  - With thinned sensors, the resolution degradation for angled tracks is mitigated.
  - The slant layers (in the current SVD) will not be necessary ➔ Simpler detector geometry

Upgrade proposals

- Pixel detector
  - DMAPS
  - SOI
- Silicon Strip
  - TFP (Thin fine-pitch DSSD)

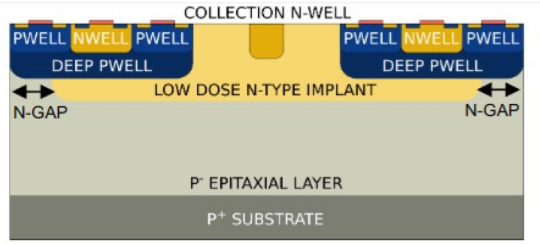
DMAPS

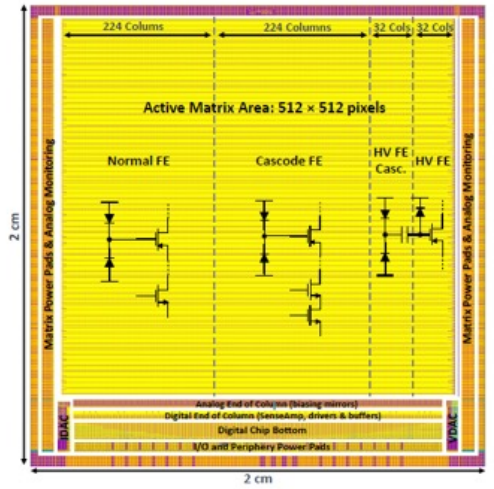
- Preparation is actively done by the collaboration of European institutes
- Baseline concepts are
  - High position and time granularity
  - 5 layers (R=14.1 – 140 mm)
  - Low material: 2.4% X_0 in total
  - Covering the Belle II acceptance by using same chip

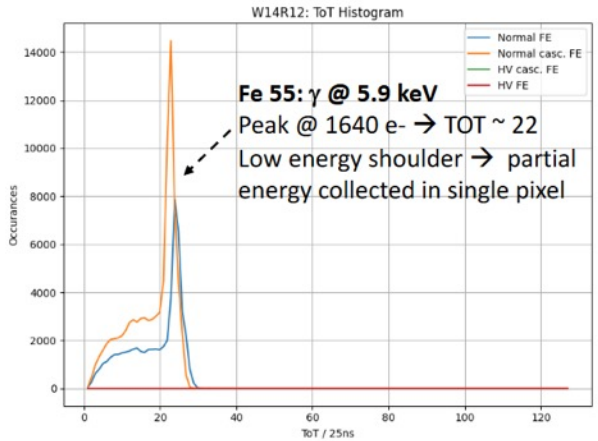


DMAPS

- Tower Jazz 180 nm modified process (full Depletion) is adopted. With small diode as sensing node for the better charge collection.
- The test chip (Monopix2: 33 µm pitch, 25 ns integration, 17x17 mm^2 matrix) were fabricated and tested.
  - Four types front end circuit are implemented.
  - In-pixel detection threshold + Time-Over-Threshold (ToT)
  - Various sensing volume thickness CZ-bulk, epi-30 µm



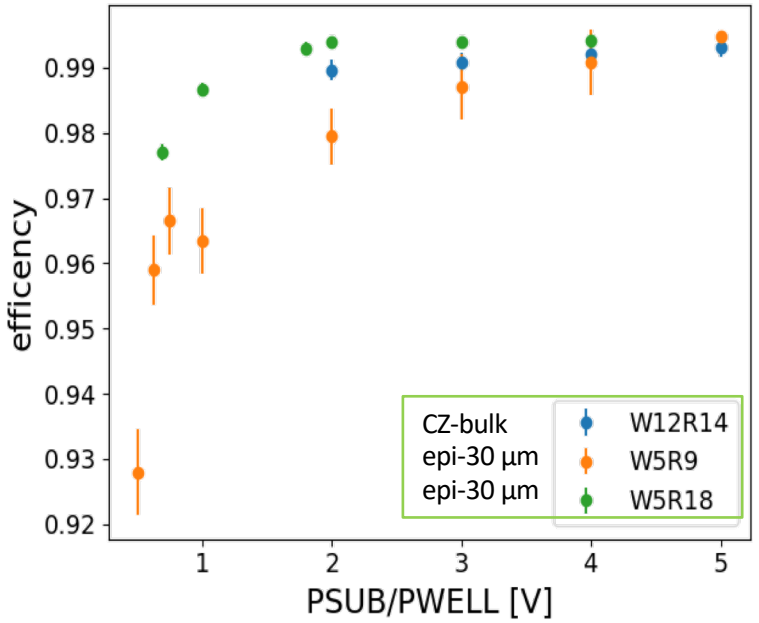


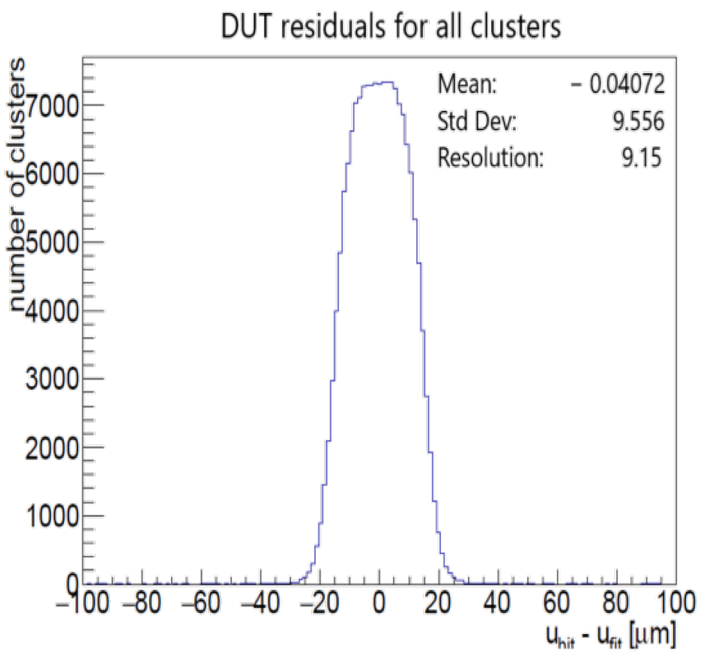


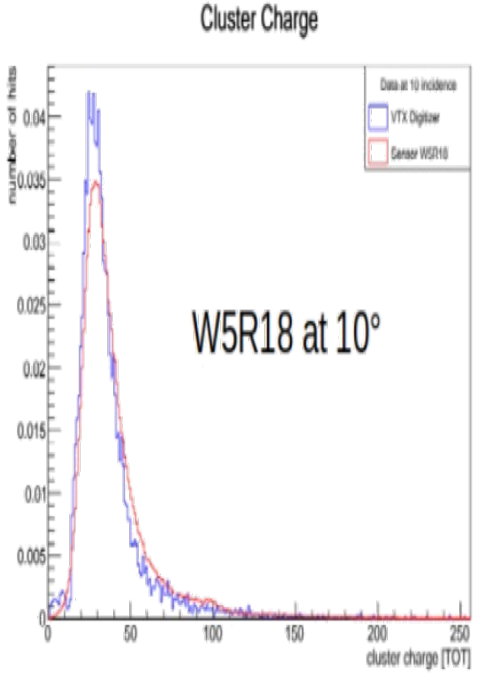
Talk by Ivan Dario Caicedo Sierra 9:45, 25 Oct.

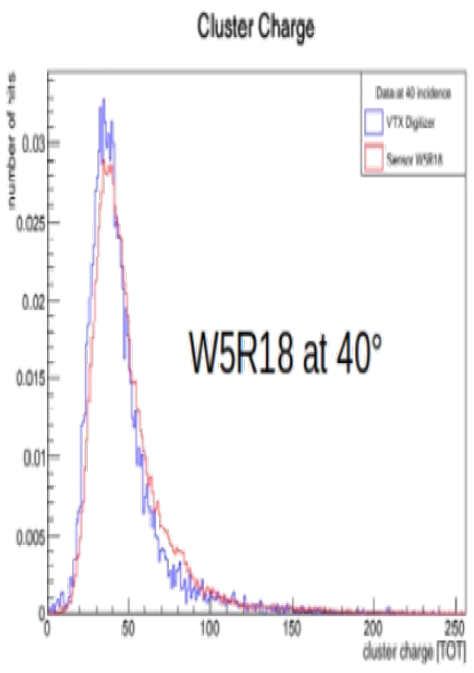
DMAPS

- A beam performed in DESY 5 GeV electron beam
- Detection efficiency: 99.020 ± 0.040 %.
- Position resolution ~9 μm
- The charge distribution was taken and implemented to the simulation code for the tracking performance study.



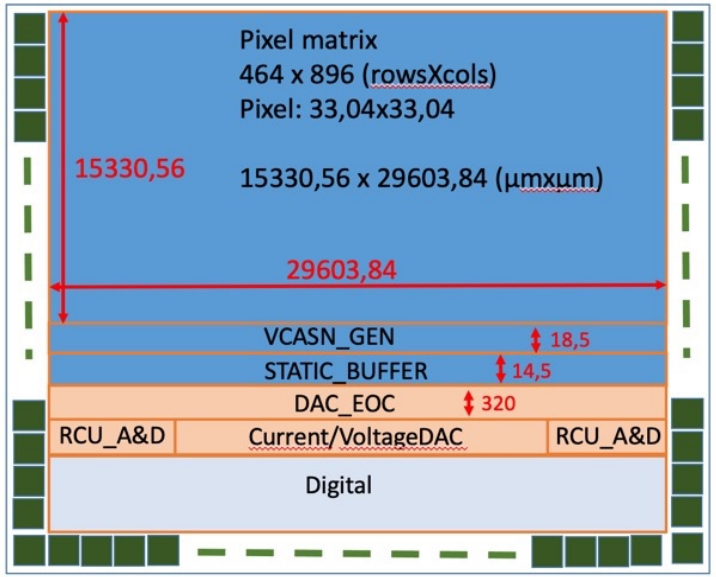


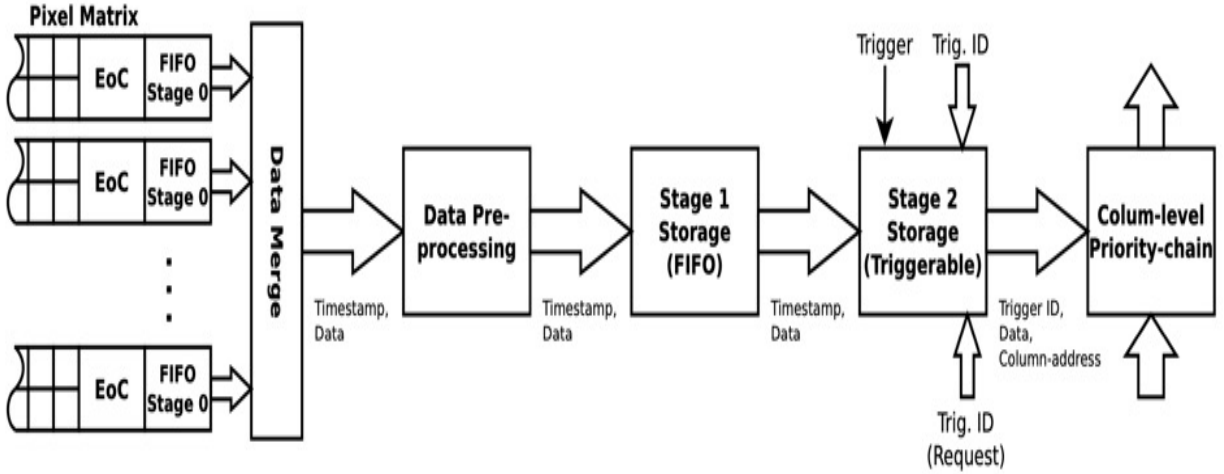




DMAPS OBELIX: Optimized BELle II pIXel sensor

- Readout scheme
  - Architecture is set
  - Checking functionality with hit rate/ToT
  - Power dissipation to be estimated (200mW/cm^2) → Necessary for the determination of the cooling scheme (next page)
  - Investigating hitOR and BCID behavior => integration time, power saving mode
- Status
  - Main layouts (matrix, logic, regulators) ready soon
  - Power optimisation of Front-End on-going
  - Still some parts to complete
  - Submission < Jan 2023

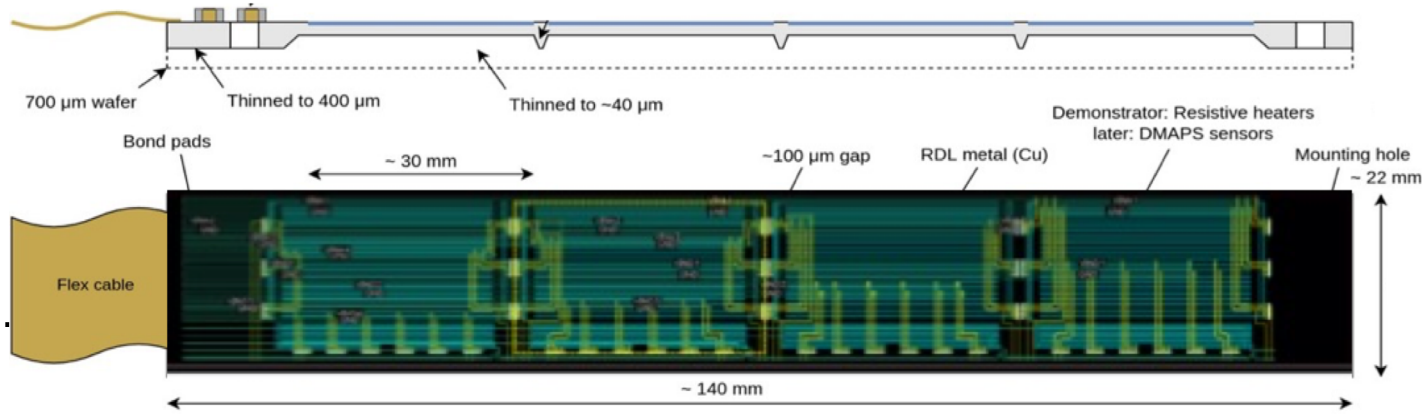


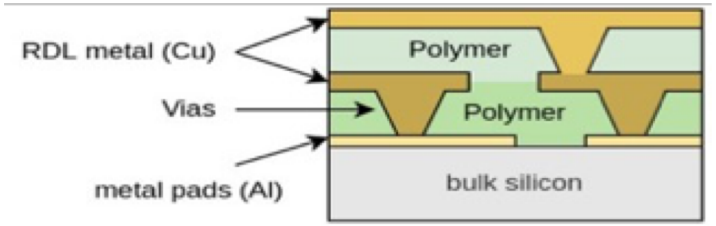


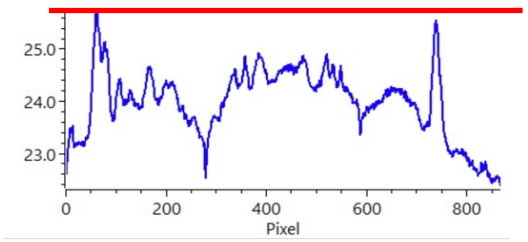
DMAPS OBELIX: Optimized BELle II pIXel sensor

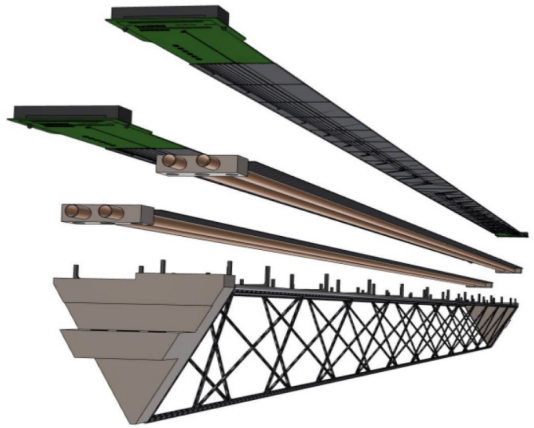
- Inner 2 layers:
  - 0.15% X_0 /layer
  - Cooling simulation with 15°C air (200mW/cm^2). Max temp. < 20°C
  - Re distribution layer (polyimide + cupper lines) is developed on the wafer.
- Outer 3 layers:
  - Light and stiff structure 1.2/1.5/1.8 % X_0 /layer
  - Cooled with negative pressure water: CF plate with polyimide water tube
    - T(water): 10°C, T(ambient): 24°C
    - Heat load 20-200mW/cm^2.
    - The result satisfies the cooling requirement

T<45°C



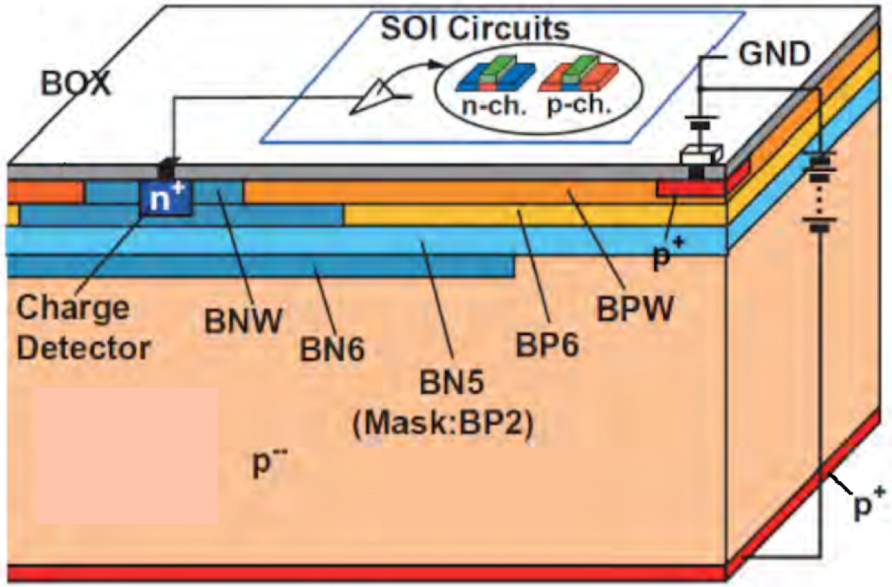


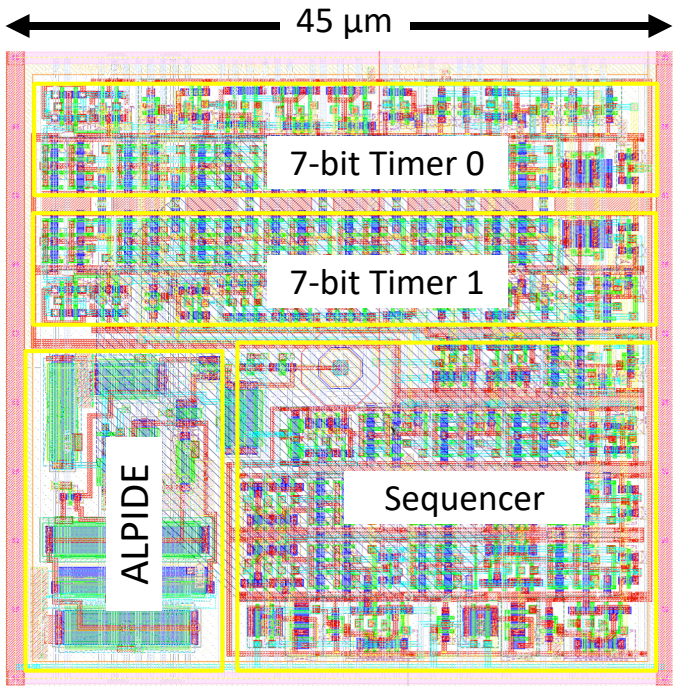




SOI

- Lapis 0.2 μm FD-SOI technology
  - Wafer: High-resistivity FZ silicon
  - CMOS circuit is separated from the wafer with BOX.
    - (Almost) no limitation in the circuit design
  - Pinned well structure (PDD), similar to that of DMAP, is used for the efficient and fast charge collection.
    - Small sensor capacitance: C_{det} = 3 fF.
- DuTiP pixel sensor designed for the Belle II upgrade
  - ALPIDE type frontend (modified for faster response) is adopted for the low power consumption
  - The hit signal is delayed with two timers and coincidence with the Belle II global trigger is taken: Background reduction
  - The hit occupancy can be reduced < 0.1% under the 113 MHz/cm2 background hit condition.
  - Smooth data transfer with the two stage FIFO.

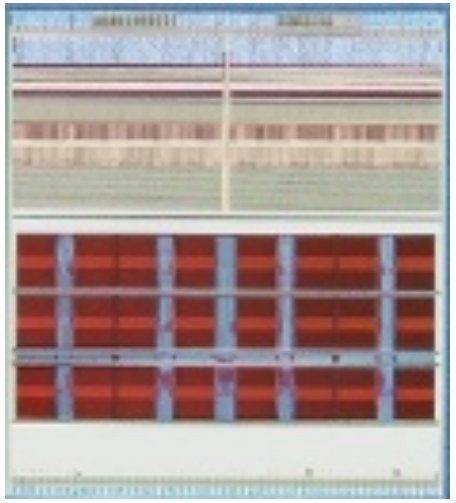




Talk by Akimasa Ishikawa (25 Oct 16:00)

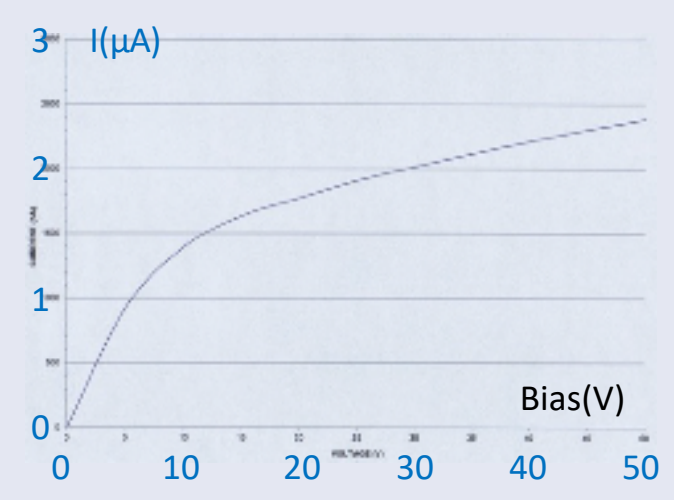
TFP Thin fine-pitch DSSD

- TFP aims the replacement of the current silicon strip layers.
- Lower material thickness using thin (150 μm thick) DSSD sensors
- A new binary readout chip SNAP128A
  - Front end optimized for 150μm double sided sensor
    - Fast shaping time
    - p/n signal flip
  - Fast strip “OR” signal for trigger generation
  - Digital pipeline: Level-1 trigger latency > 8 μs

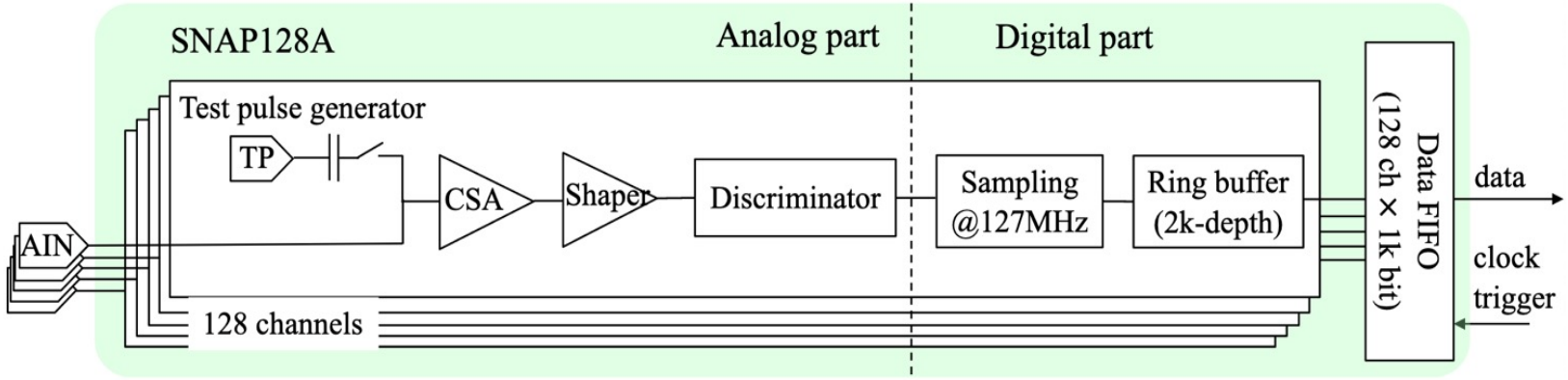


5.945 mm x 6.12 mm

Prototype 59mmx52.6mm
0.15mm (Micron (UK))

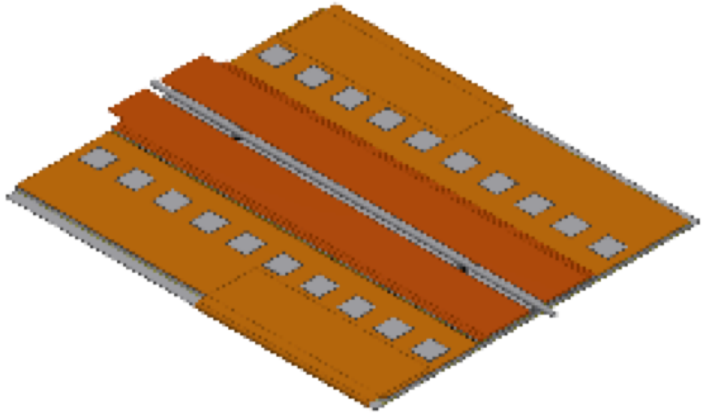


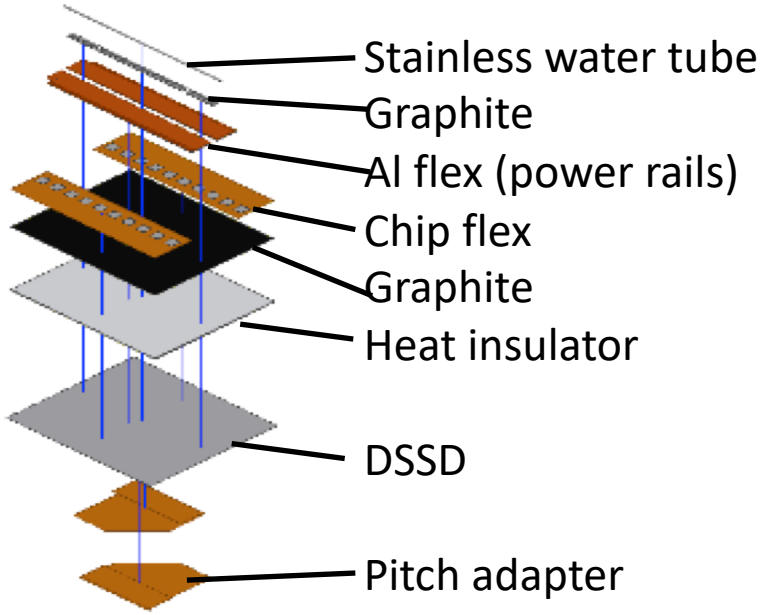
The performance is presented by Zihan Wang (Next Talk)



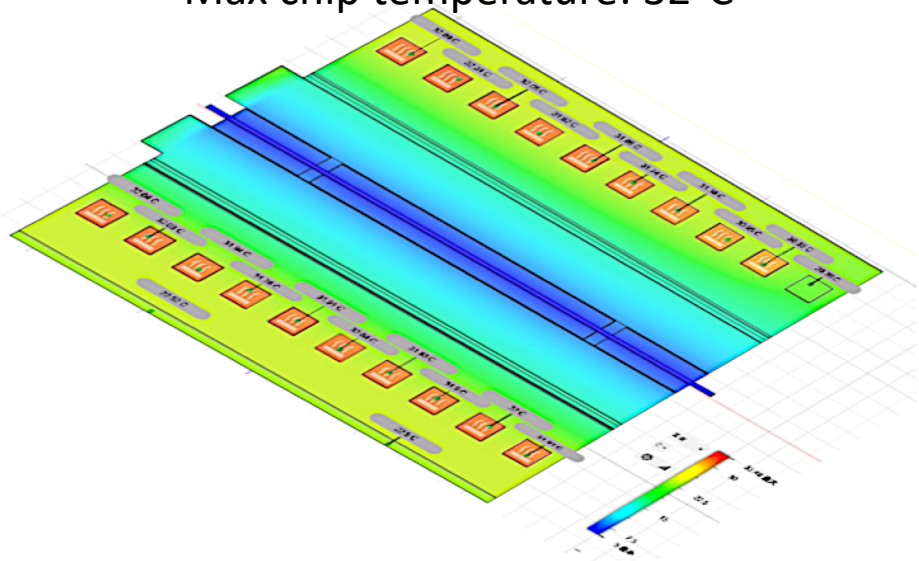
TFP

- Concept of the ladder structure is shown here.
- Consisting of DSSD/Pitch Adapter/Heat spreader/Water cooling tube
- Aluminum flex R&D for power distribution
- Heat simulation: Cooling with 5°C water satisfies the cooling requirement
-





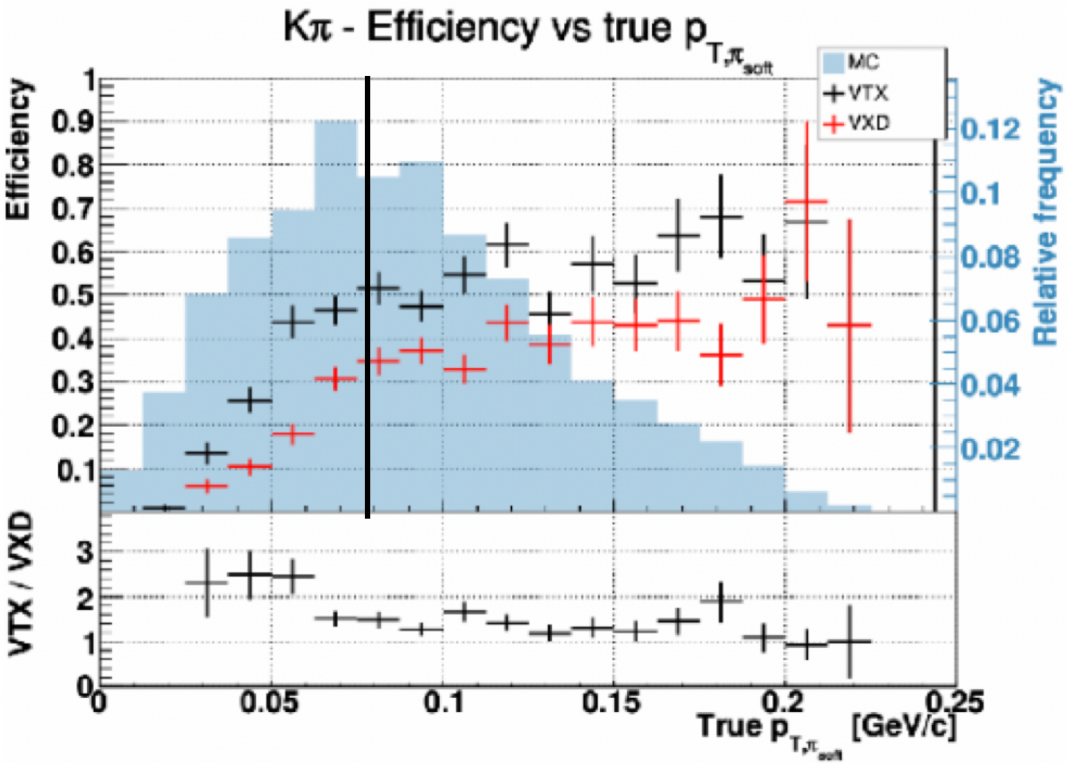
Water temperature 5°C
Power dissipation 0.4W/chip
Max chip temperature: 32°C

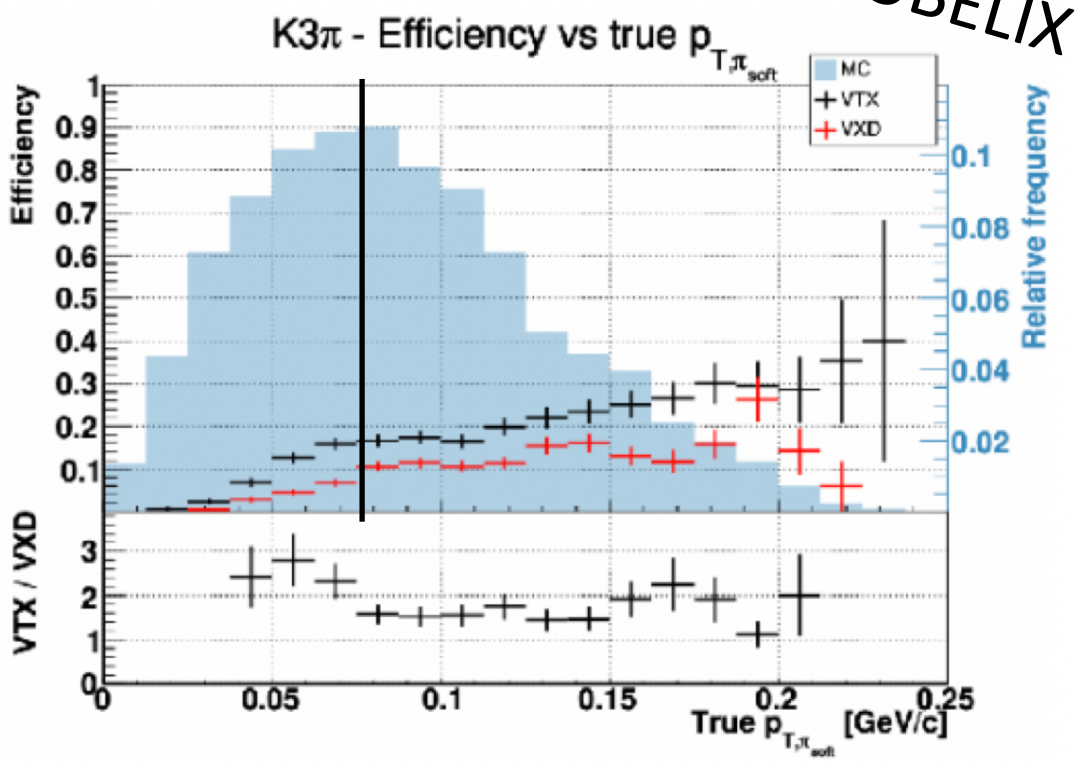


Expected physics performance

- MC benchmark: Reconstruction of soft π decaying from $D^* \to D^0\pi$.
  - The reconstruction of soft π determines the physics sensitivity.
- Thanks to the low material thickness, the reconstruction efficiency improves 50-80 %.
- Especially, at $p_t < 0.075\ \mathrm{GeV/c}$, the efficiency is improved twice.

OBELIX

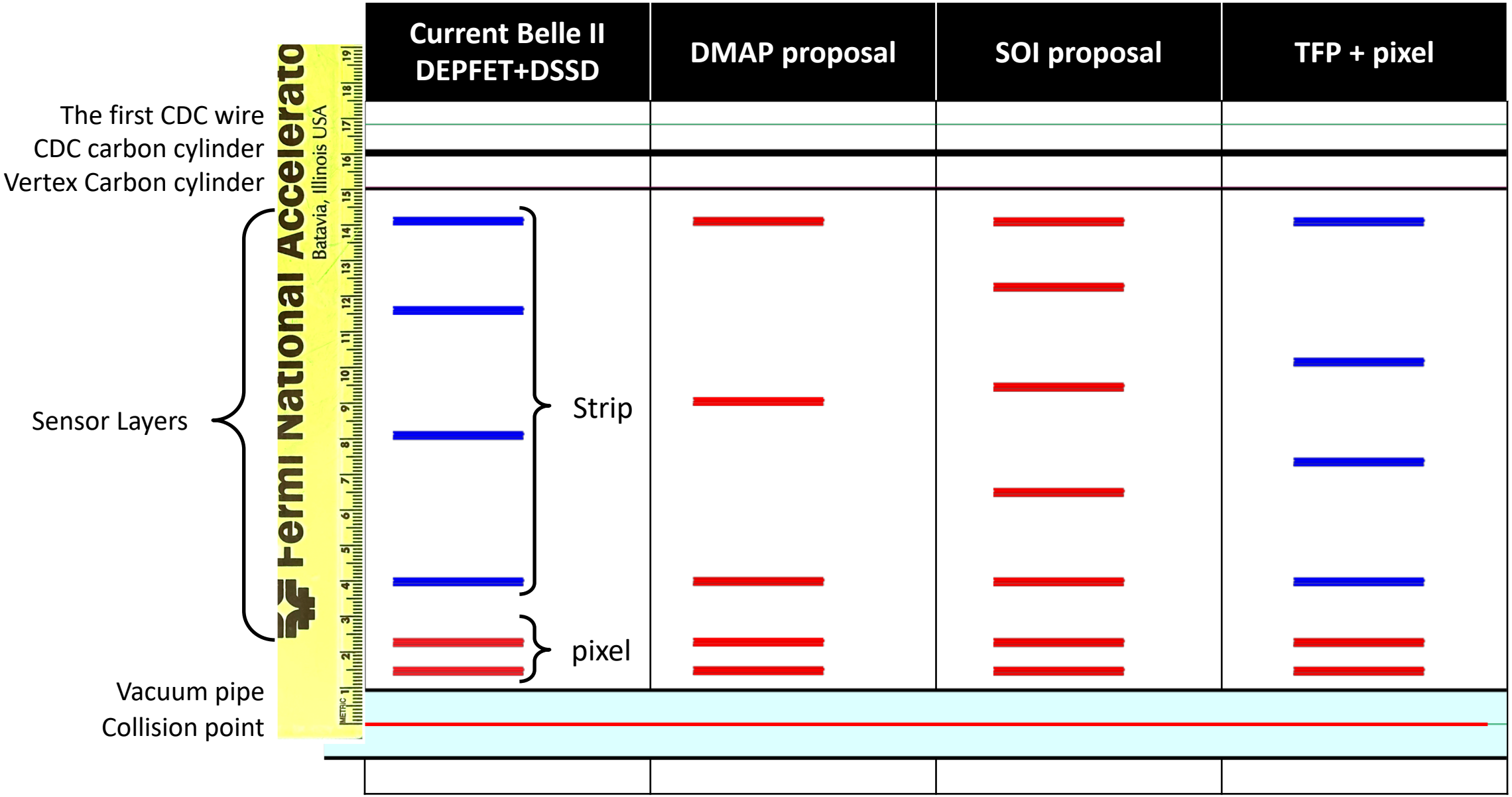




Radiation tolerance

- Our goal of the radiation tolerance for the inner most pixel layer is
  - 10 Mrad/year and NIEL fluence of 5×10^{13} /cm^2 /year.
- DMAPS
  - Monopix2 has been tested and proved up to 1000 kGy (100 Mrad) and 1×10^{15} /cm^2 /year.
- TFP
  - At the DSSD position, the radiation level is 2kGy/year.
  - Test sensors were irradiated to electron beam up to 70kGy.
  - The dose corresponds to NIEL 2×10^{13} /cm^2 .
  - Analysis in progress.
- SOI:
  - Double-SOI structure proved to be functional up to 100 Mrad.
  - The newly introduced PDD structure needs radiation tolerance tests.
  - Several Chips were irradiated in the above exposure.
  - Analysis yet to start.

Proposed Layer Structure



Summary: Toward the construction

- R & D activities of the Belle II vertex upgrade have been shown.
- The outcomes of the R&D are summarized in the Conceptual Design Report, assuming 2027 installation, will be submitted to the PAC committee in the next Spring.
- Then the preparation of Technical Design Report starts.
- We welcome new contributions.