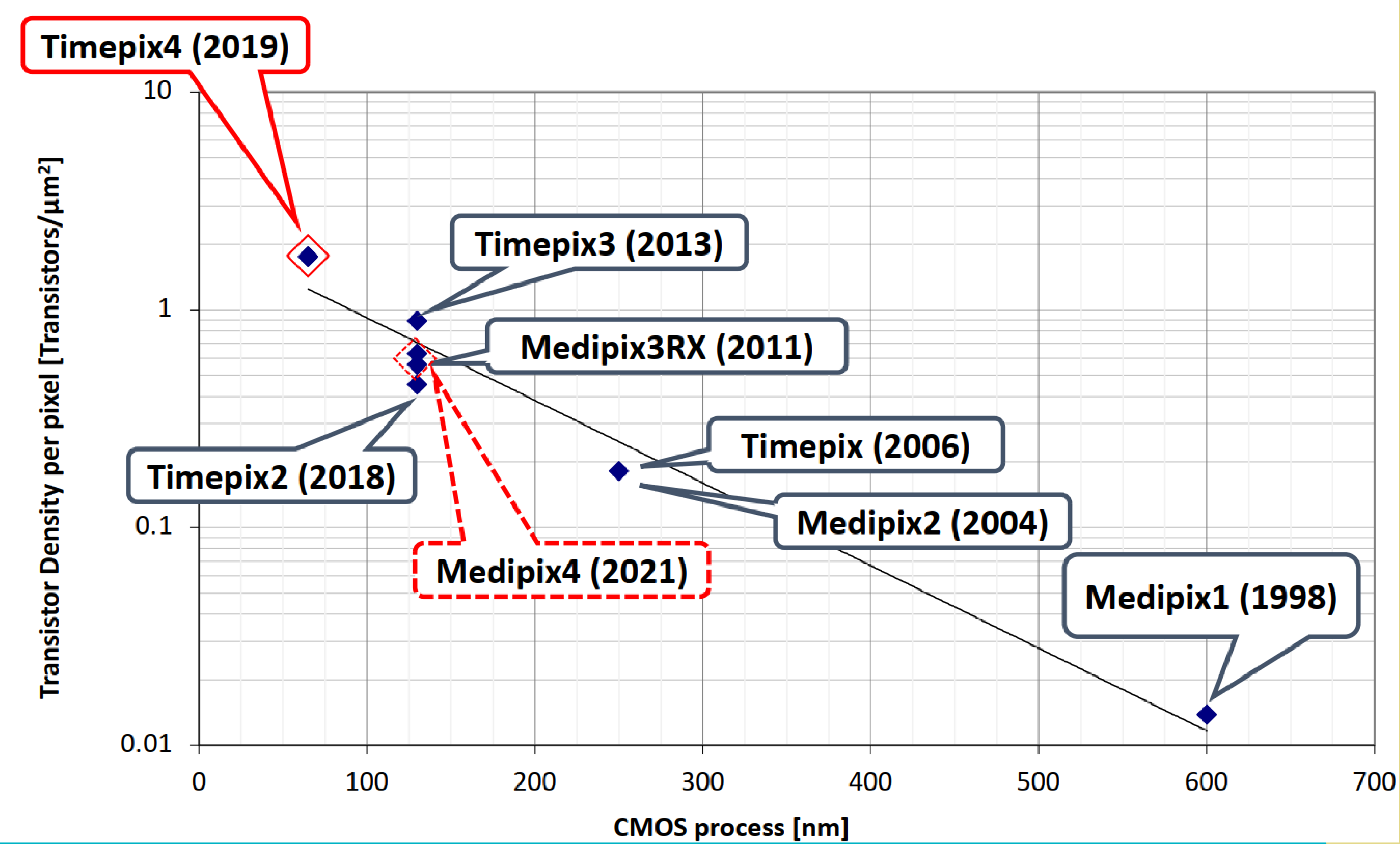


Timepix4 Timing Performance and First Beam Test Results

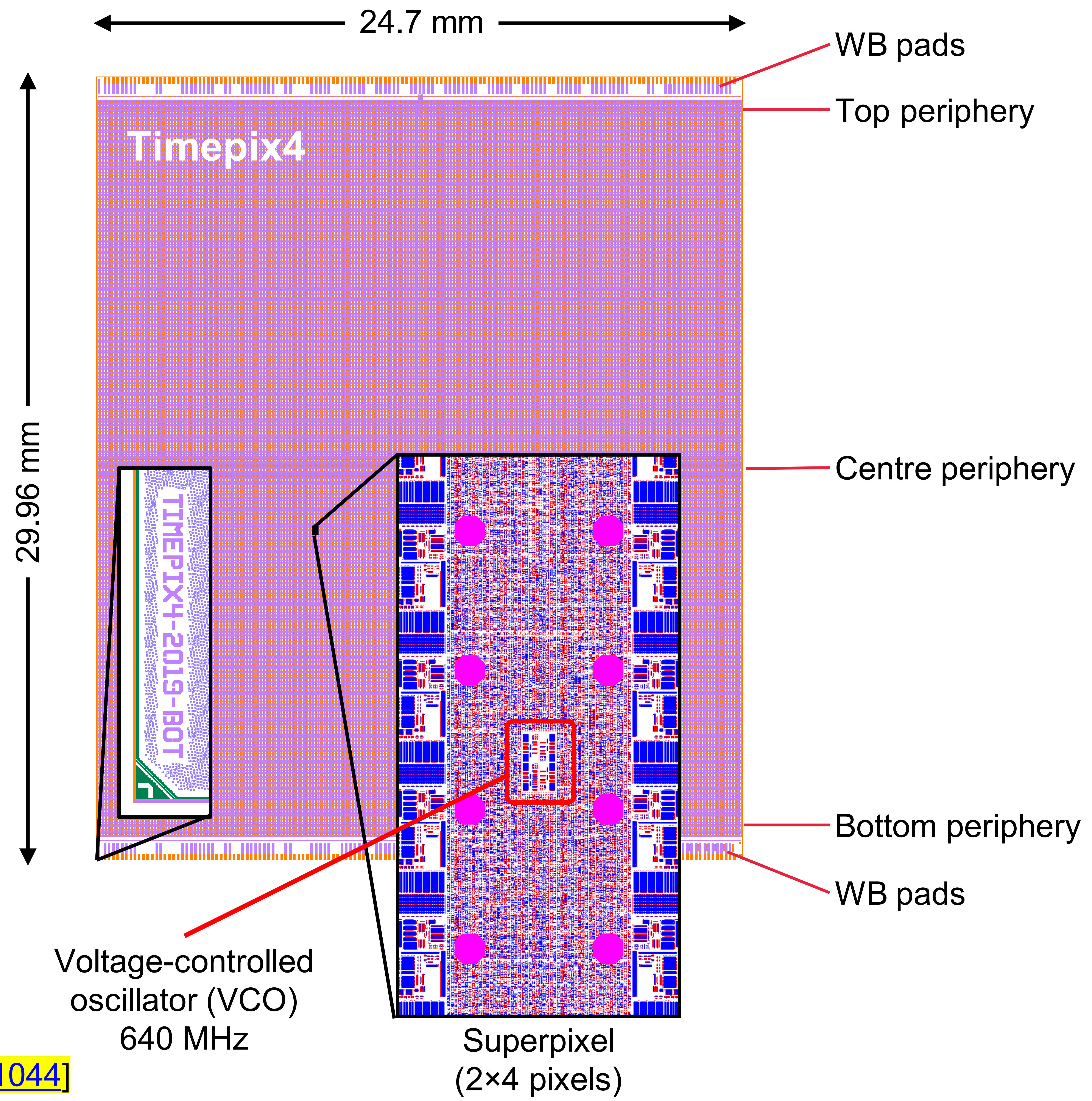
The 31st International Workshop on Vertex Detectors

K. Heijhoff on behalf of
The Medipix4 Collaboration
The Timepix4 Telescope group
and The Fast Timing Group at Nikhef

27 Oct. 2022

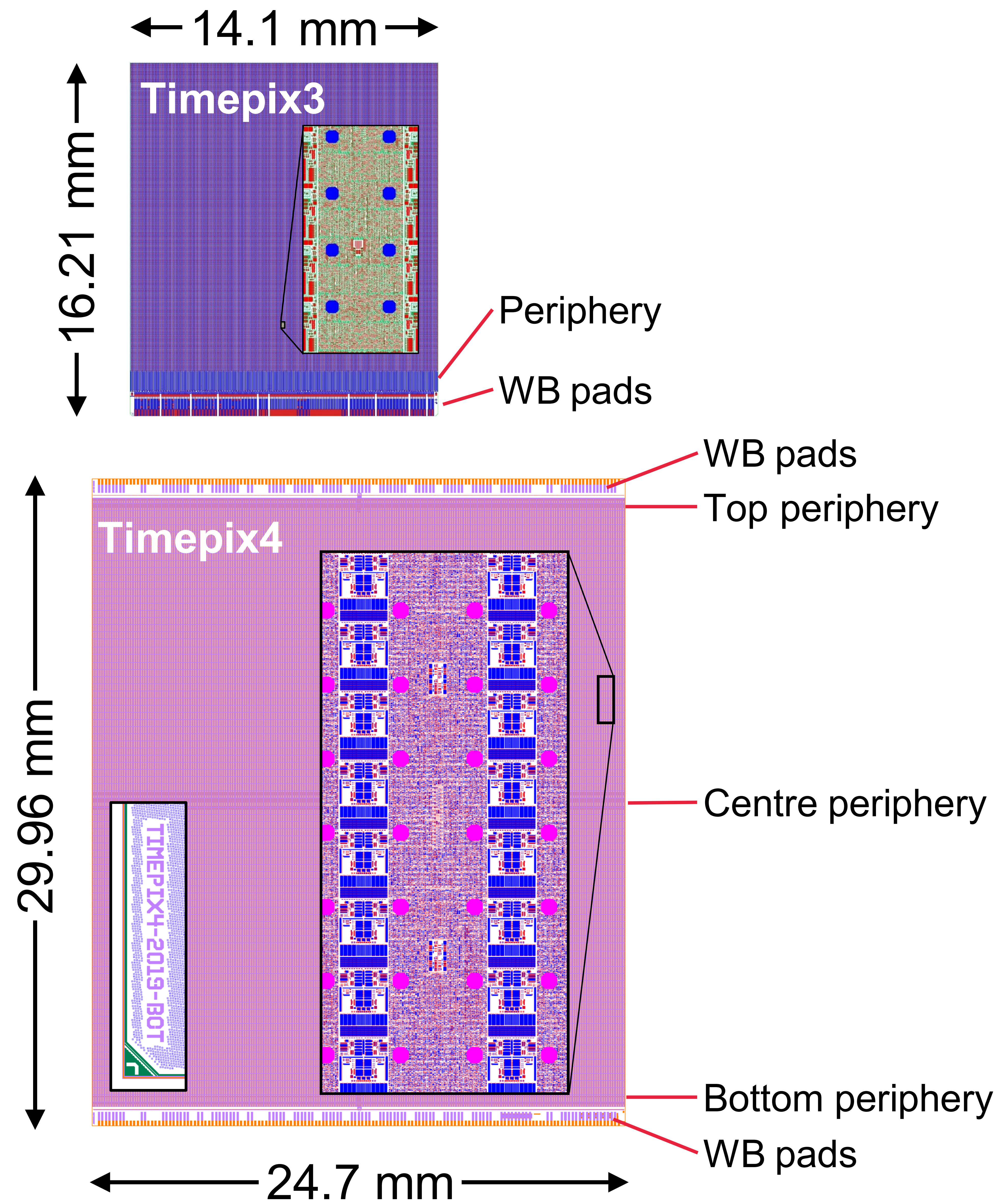
Timepix4: A pixel readout ASIC for hybrid detectors

- Developed by CERN, Nikhef, IFAE, and IEAP
- 65 nm CMOS
- 448×512 pixels, 55×55 μm² pitch
- Can readout positive and negative polarity signals
- Simultaneous measurement of time and charge deposition (by measuring time over threshold)
- Time-bin size of 25 ns/128 ≈ **195 ps**
- Data driven
- Max rate: 360×10^6 hits/cm²/s ~ 20 GB/chip/s
- Four-side buttable (peripheries underneath matrix, TSV option)



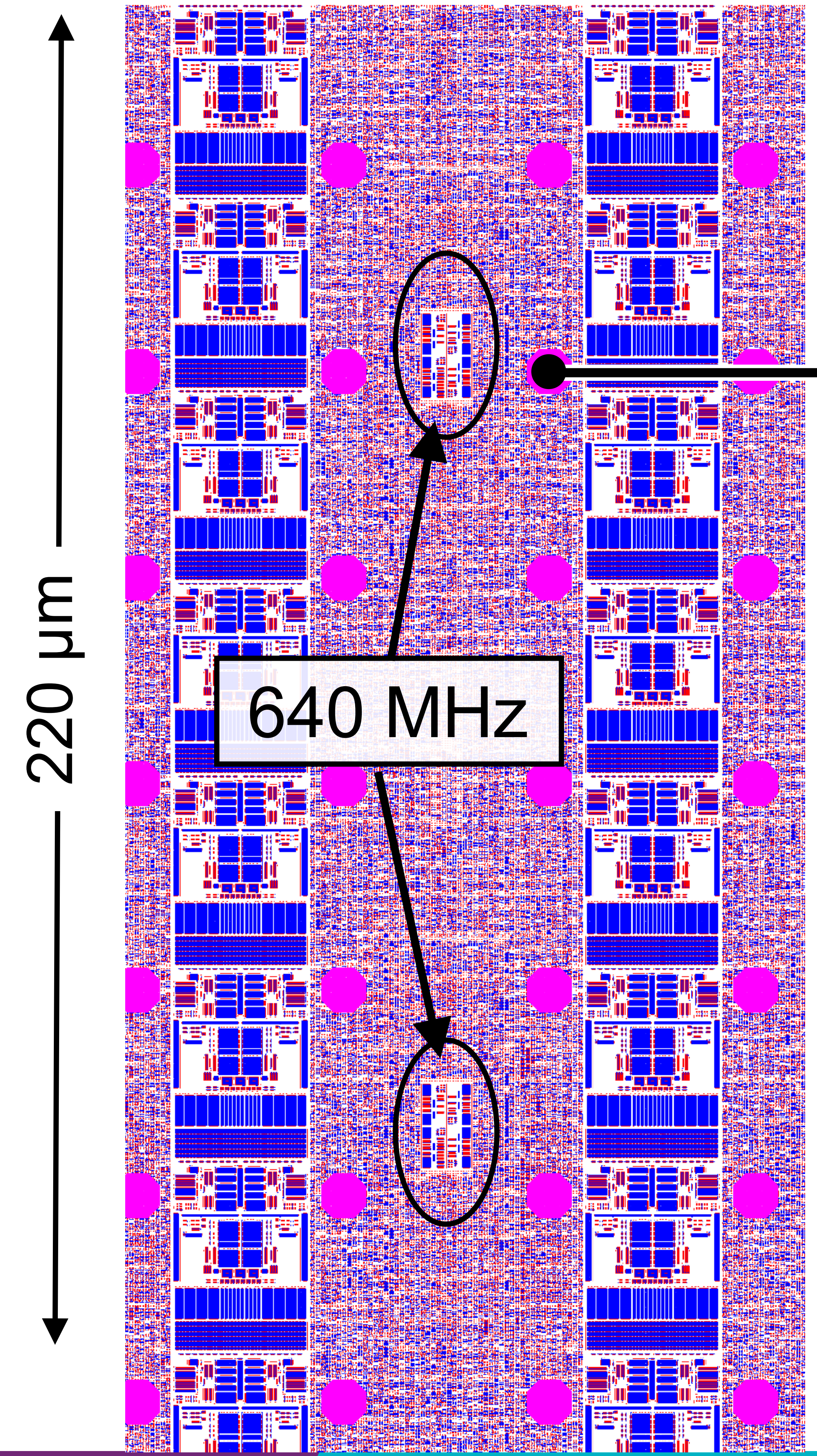
X. Llopart *et al* 2022 *JINST* **17** C01044 [DOI: 10.1088/1748-0221/17/01/C01044]

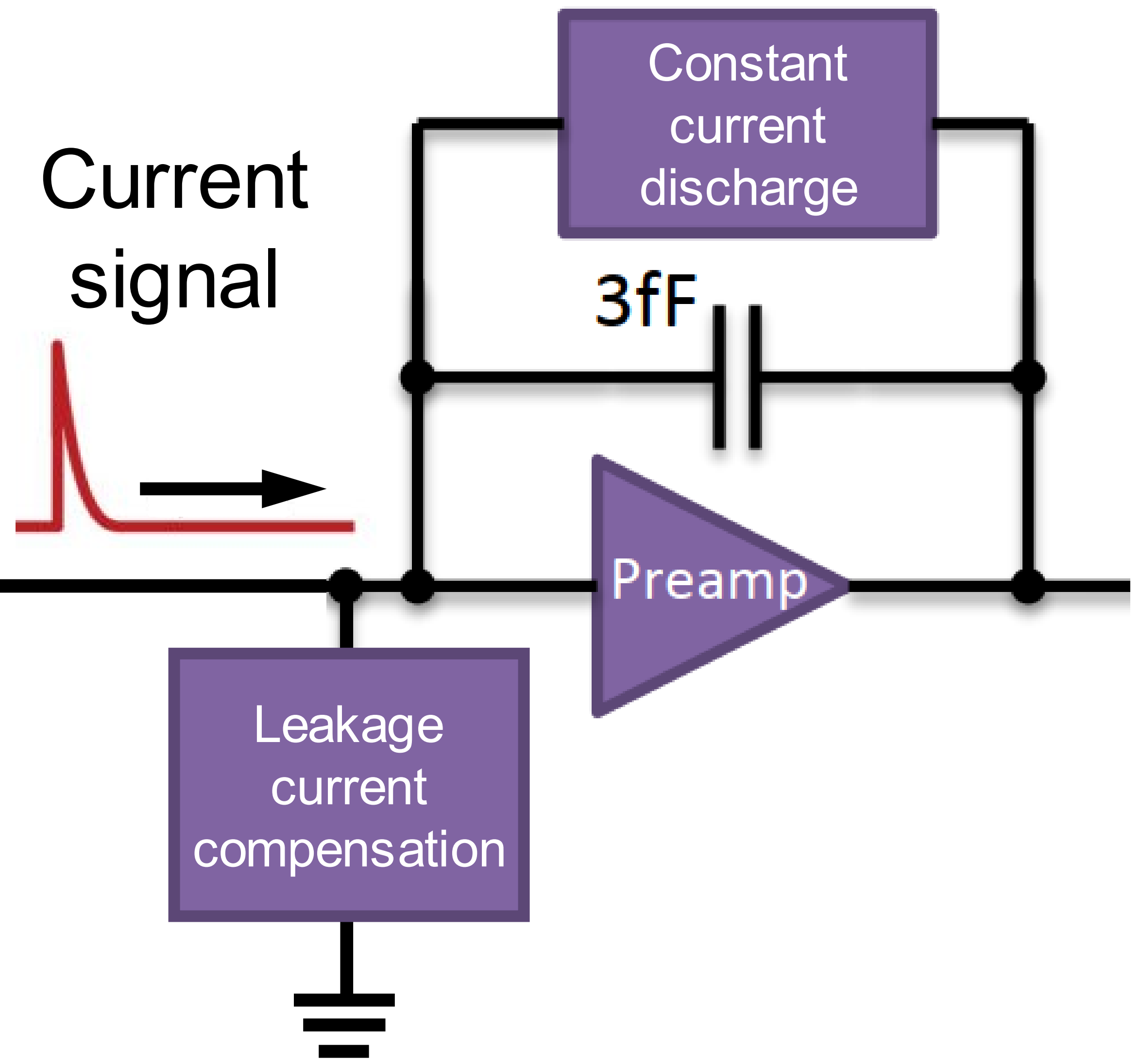
Timepix3 → Timepix4



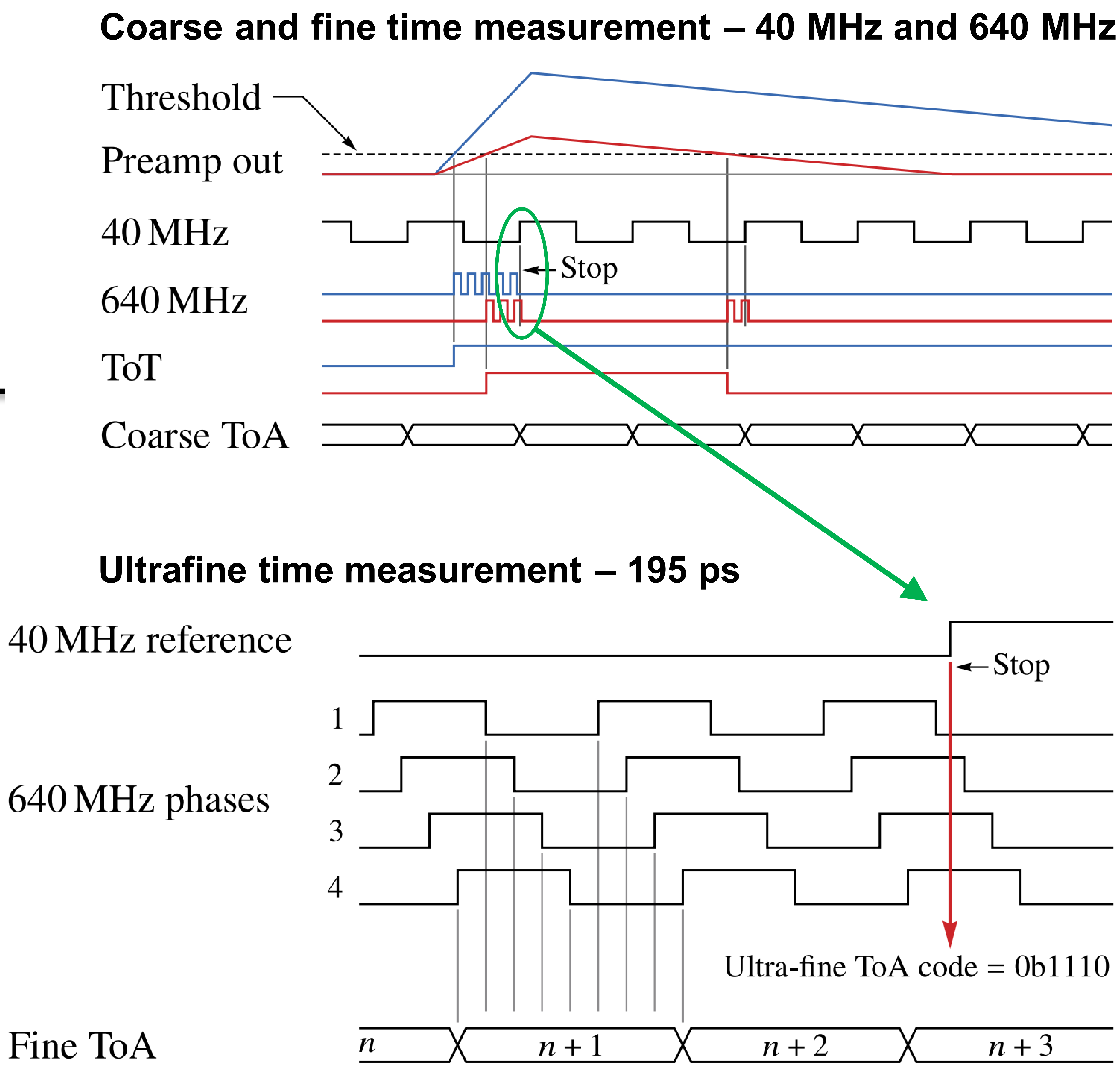
			Timepix3 (2013)	Timepix4 (2019)	
Technology			130nm – 8 metal	65nm – 10 metal	
Pixel Size			55 x 55 µm	55 x 55 µm	
Pixel arrangement			3-side buttable 256 x 256	4-side buttable 512 x 448	**3.5x**
Sensitive area			1.98 cm^2	**6.94 cm^2**	
Readout Modes	Data driven (Tracking)	Mode	TOT and TOA		
		Event Packet	48-bit	64-bit	
		Max rate	0.43×10^6 hits/mm^2/s	**3.58×10^6 hits/mm^2/s**	**8x**
		Max Pix rate	1.3 KHz/pixel	**10.8 KHz/pixel**	
	Frame based (Imaging)	Mode	PC (10-bit) and iTOT (14-bit)	CRW: PC (8 or 16-bit)	
		Frame	Zero-suppressed (with pixel addr)	Full Frame (without pixel addr)	
		Max count rate	~0.82×10^9 hits/mm^2/s	~5×10^9 hits/mm^2/s	
TOT energy resolution			< 2KeV	**< 1Kev**	
TOA binning resolution			1.56ns	**195ps**	**8x**
TOA dynamic range			409.6 µs (14-bits @ 40MHz)	**1.6384 ms** (16-bits @ 40MHz)	
Readout bandwidth			≤5.12Gb (8x SLVS@640 Mbps)	**≤163.84 Gbps (16x @10.24 Gbps)**	**32x**
Target minimum threshold			<500 e^-	<500 e^-	

Time measurement in Timepix4



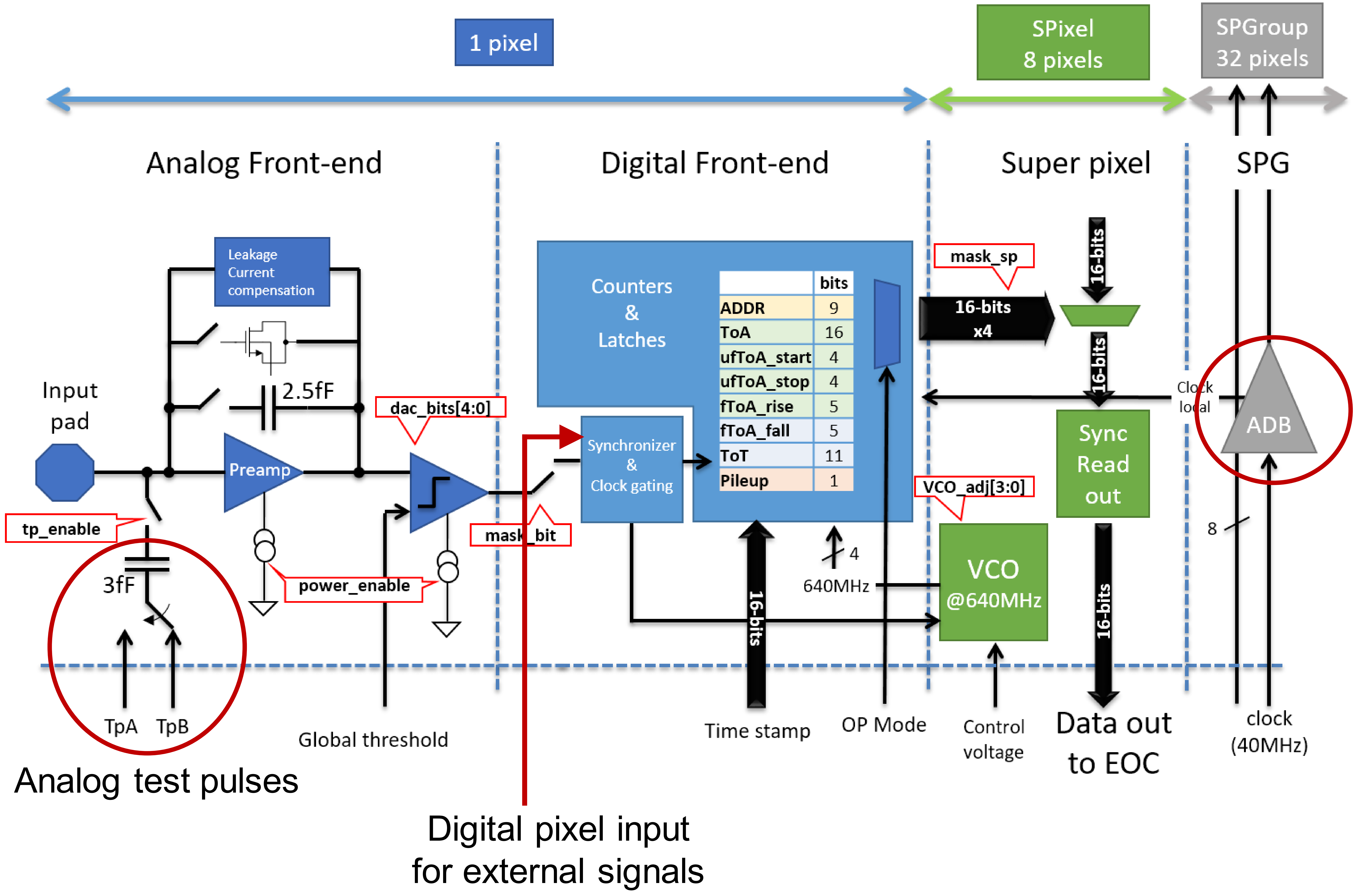


- Nominal TDC resolution: 195 ps/$\sqrt{12}$ = 56 ps
- Time over threshold (ToT) measures signal charge



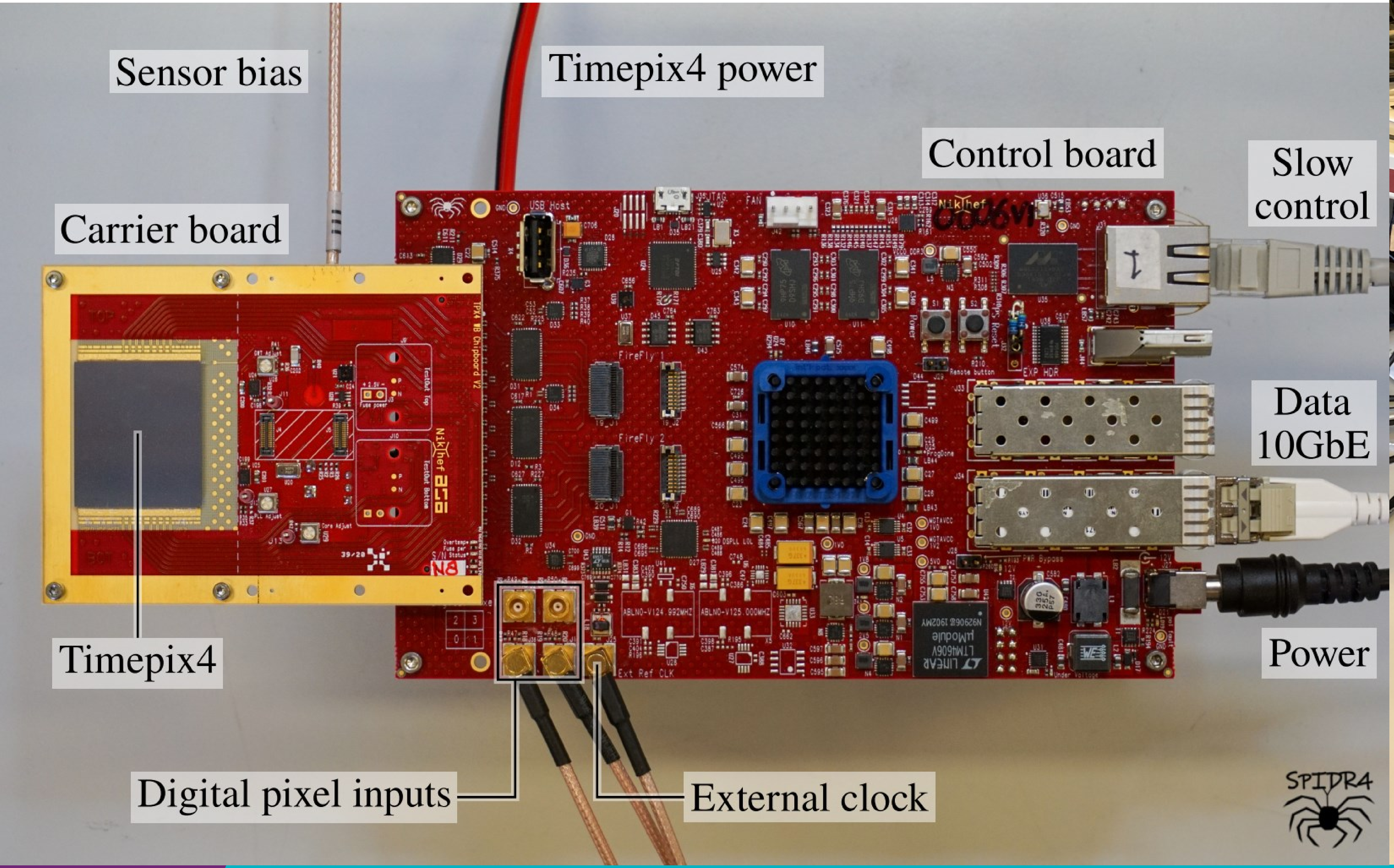
Timepix4 front-end

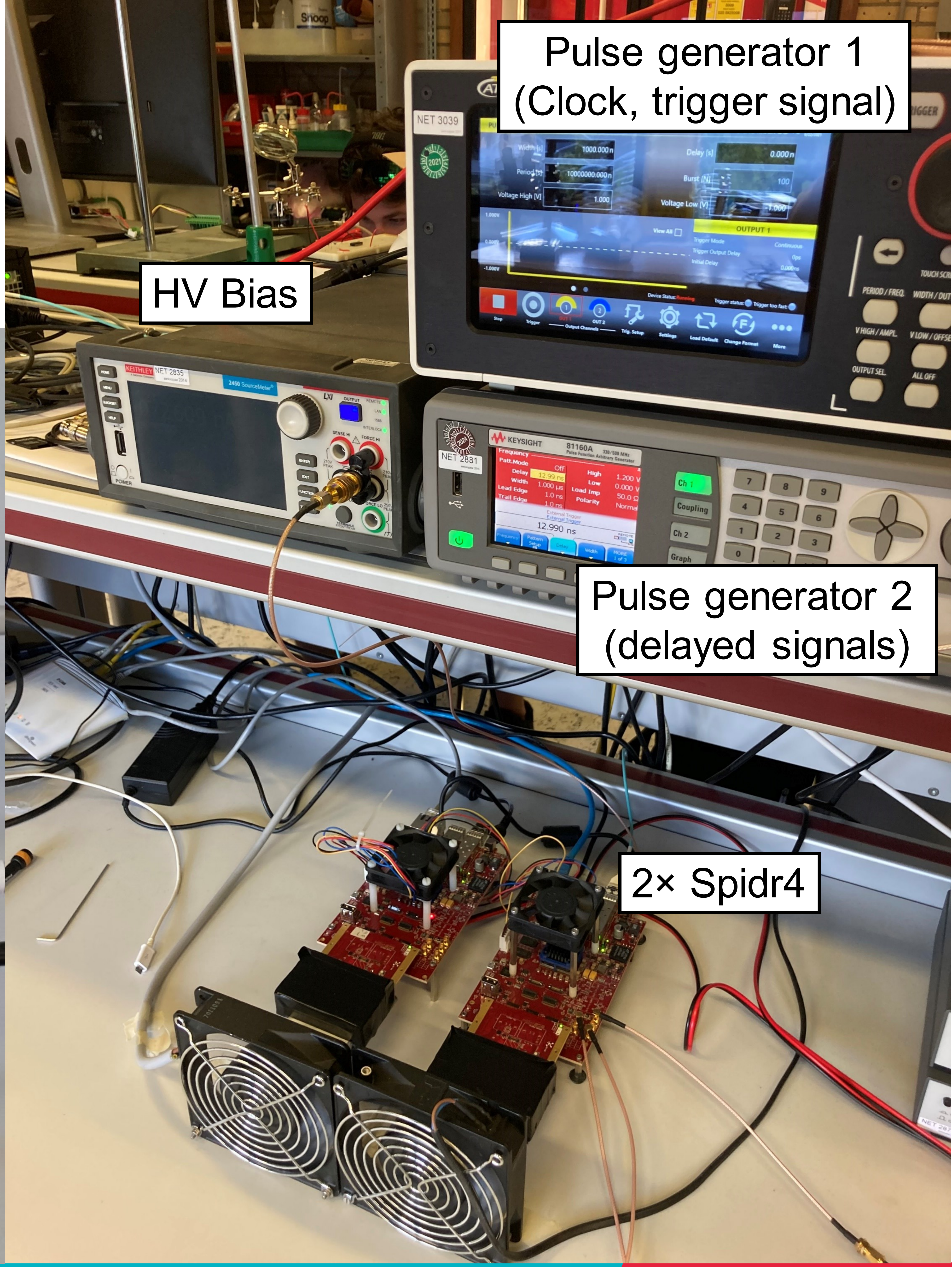
- Analog test pulses were used to characterise the analog front-end jitter
- The relative arrival time of analog test pulses was scanned by delaying the system clock in steps of 20 ps
- Digital pixel inputs: Edge pixels can be triggered with external signals
- Digital pixel inputs were used to characterise the TDC



SPIDR4 / Measurement setup

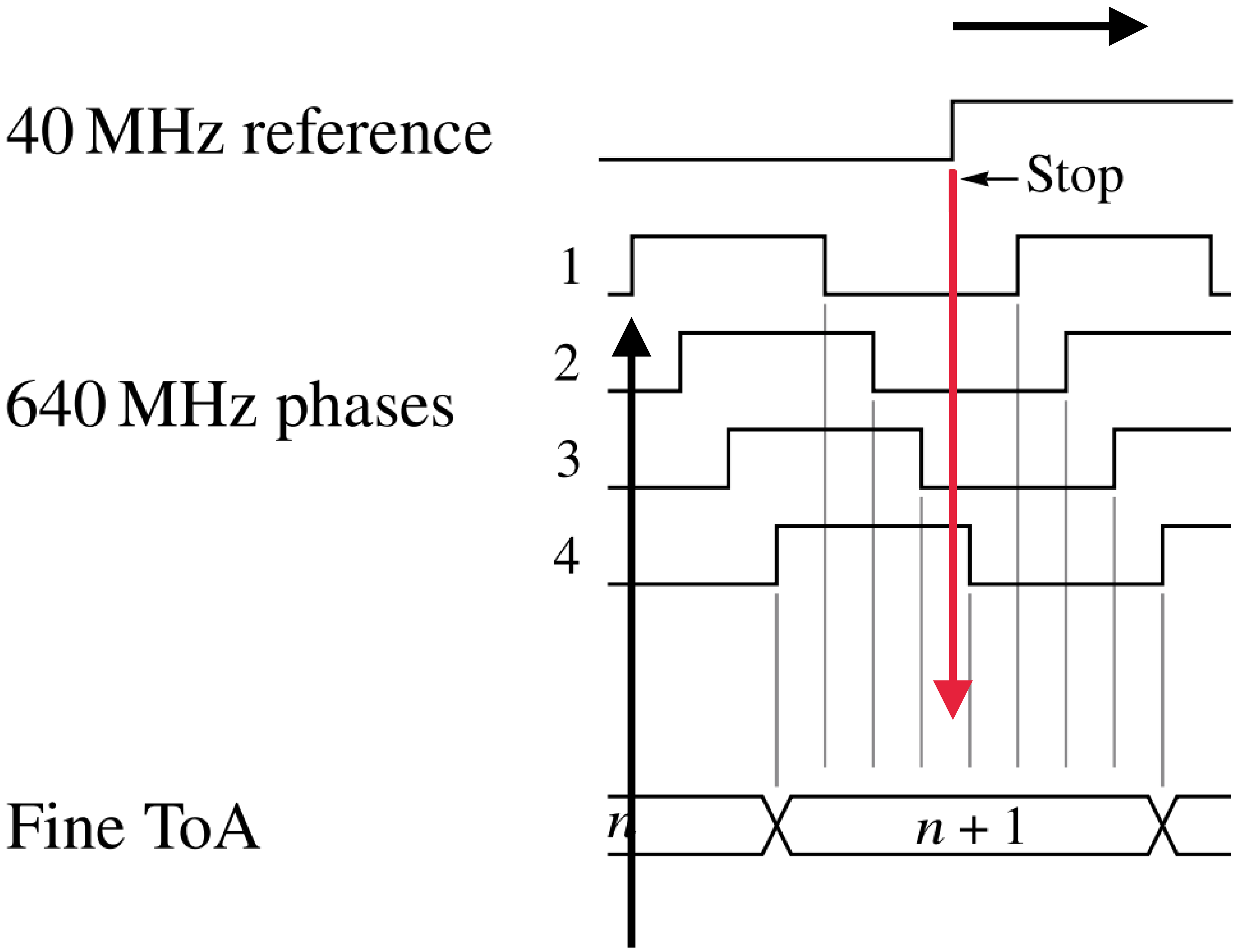
- Readout system for Timepix4 developed at Nikhef: SPeeDy Pixel Readout module 4 (SPIDR4)



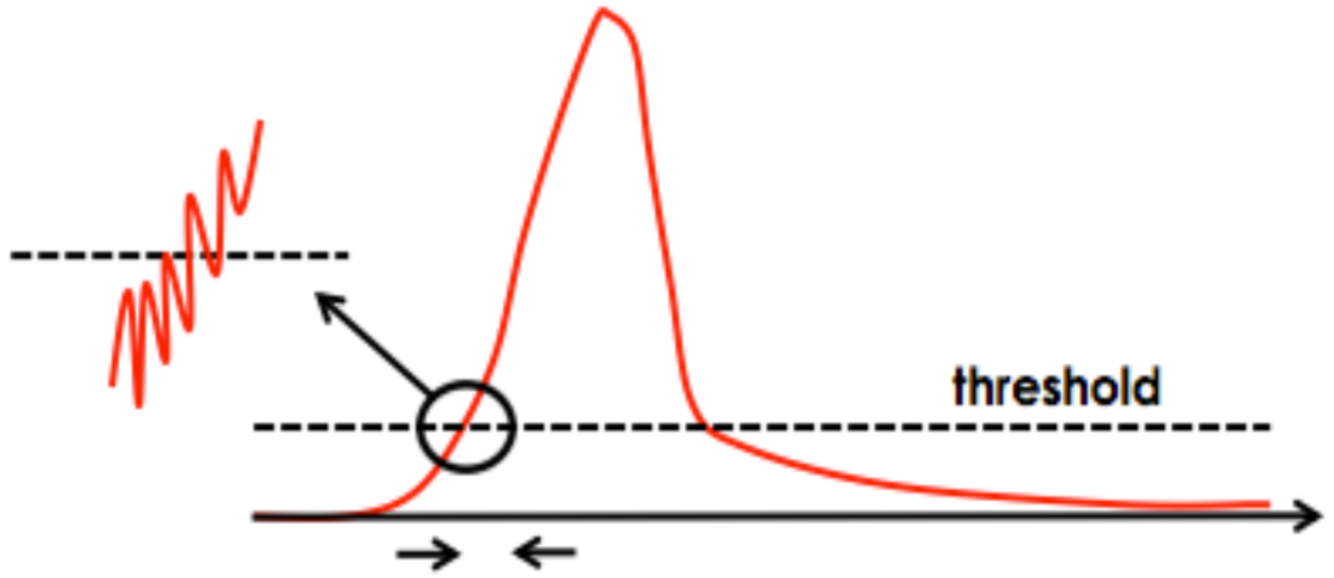


Analog front-end time resolution measurement

Scan clock phase of pixel in steps of 20 ps

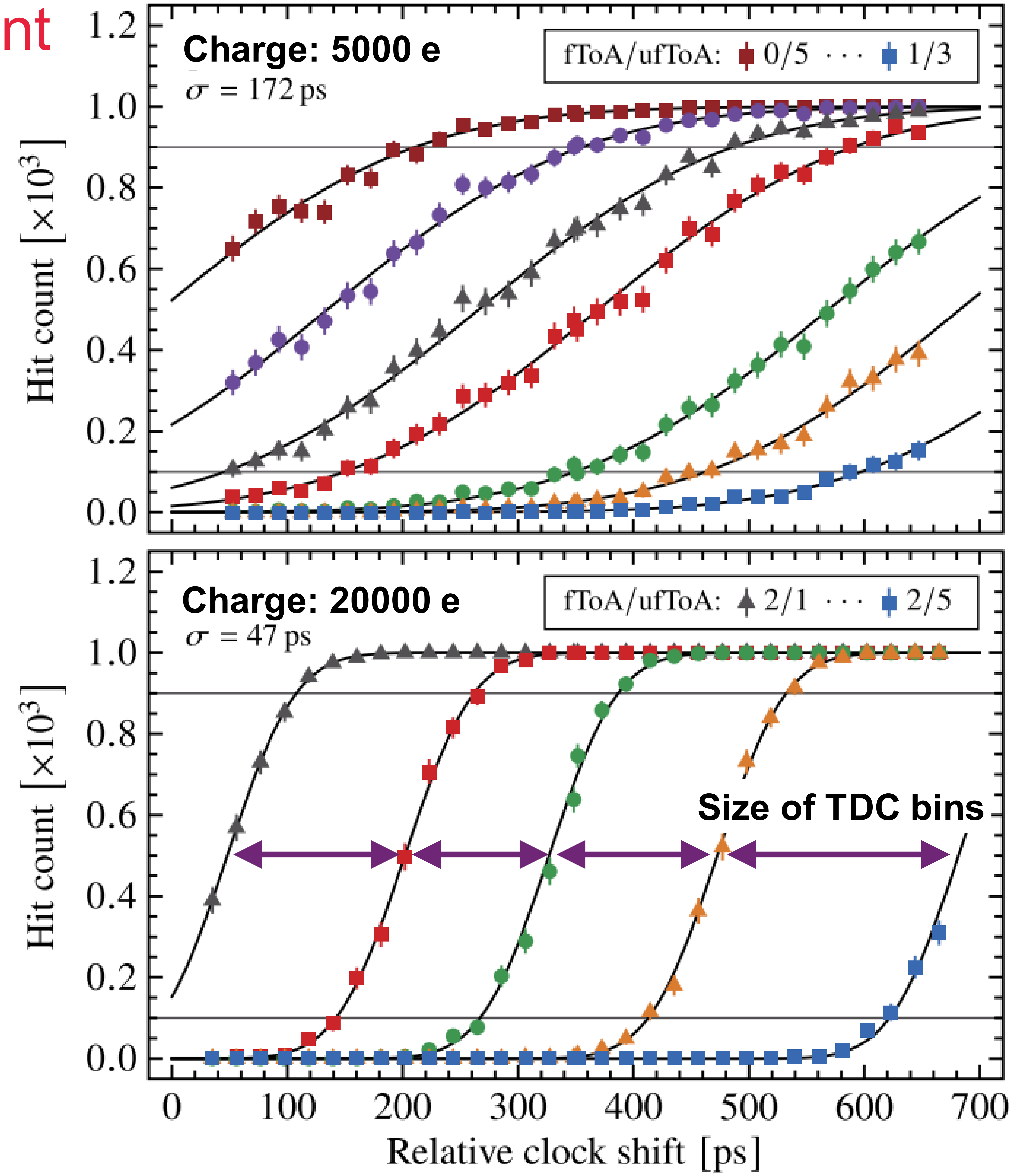


Discriminator starts the VCO
after an analog test pulse



$$\frac{N_{\mathrm{tp}}}{2}\left[1+\mathrm{erf}\left(\frac{t_{\mathrm{delay}}-t_n}{\sqrt{2}\,\sigma_{\mathrm{j}}}\right)\right]$$

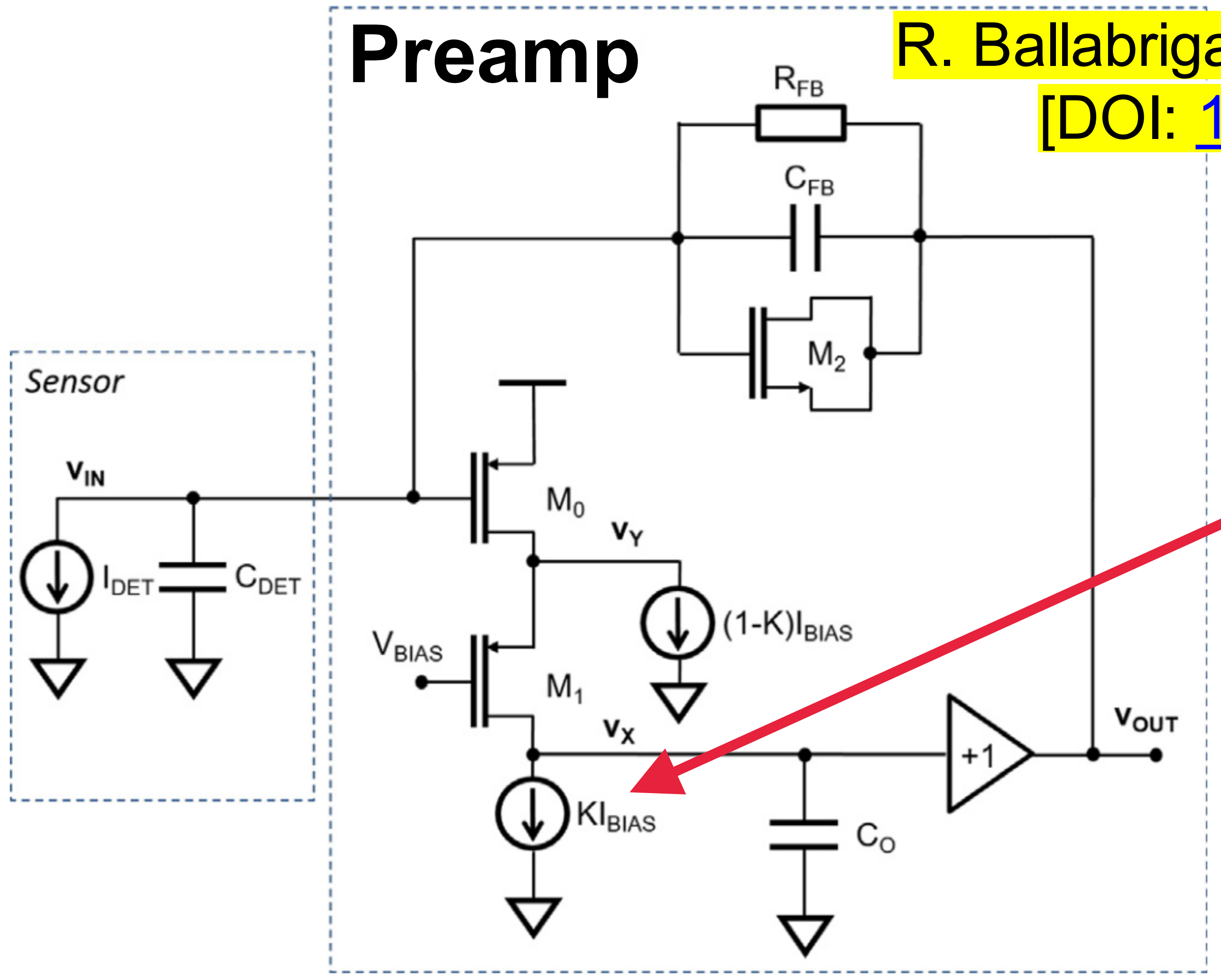
Time resolution from s-curve fit



Analog front-end time resolution

- Time resolution in h^+ mode limited to 75–105 ps depending on DAC settings
- Pixel capacitance worsens the time resolution
  (Also see reference in the top-right corner of this slide)

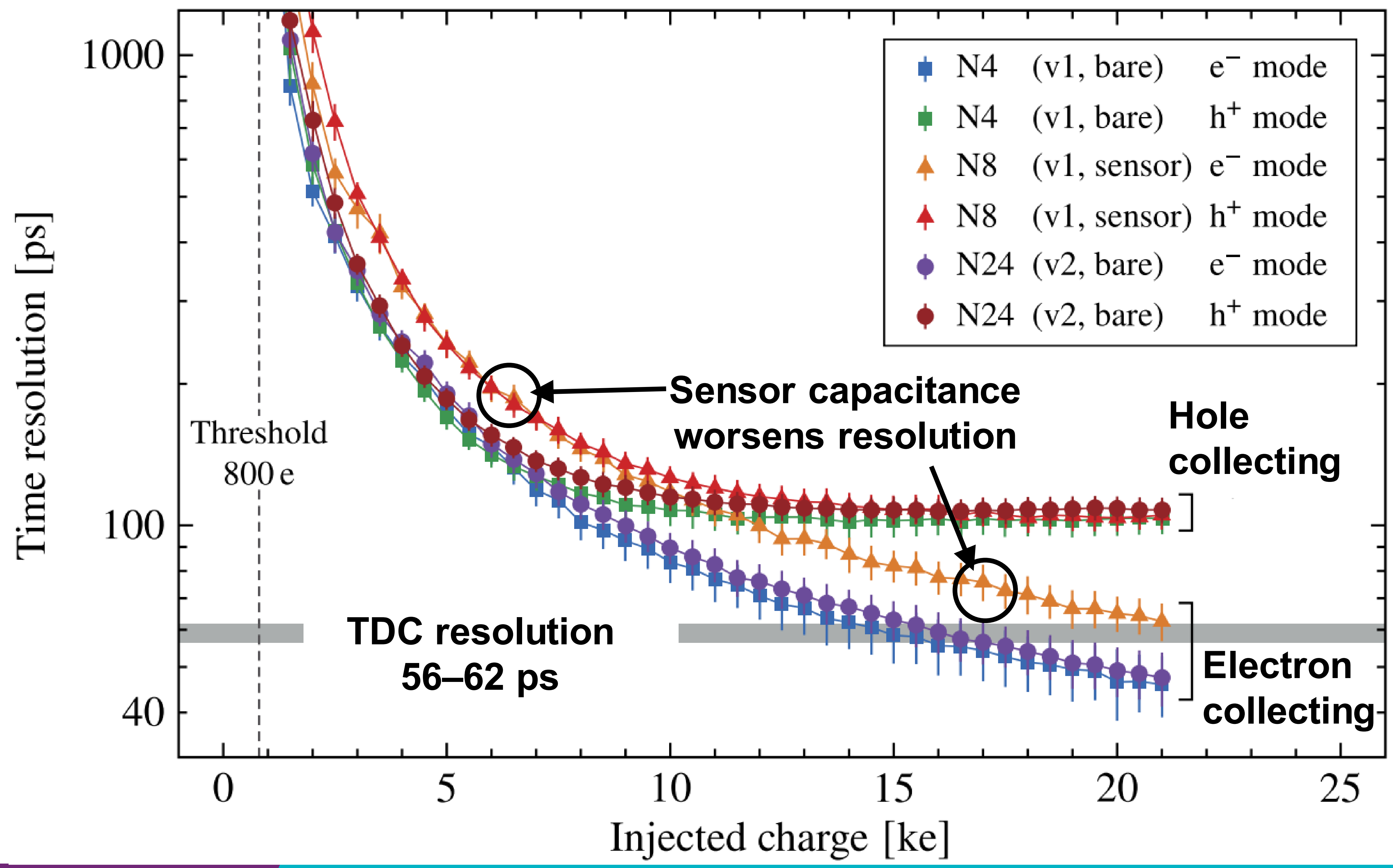
R. Ballabriga *et al* **NIM** A 1045 (2023) 167489 [DOI: 10.1016/j.nima.2022.167489])

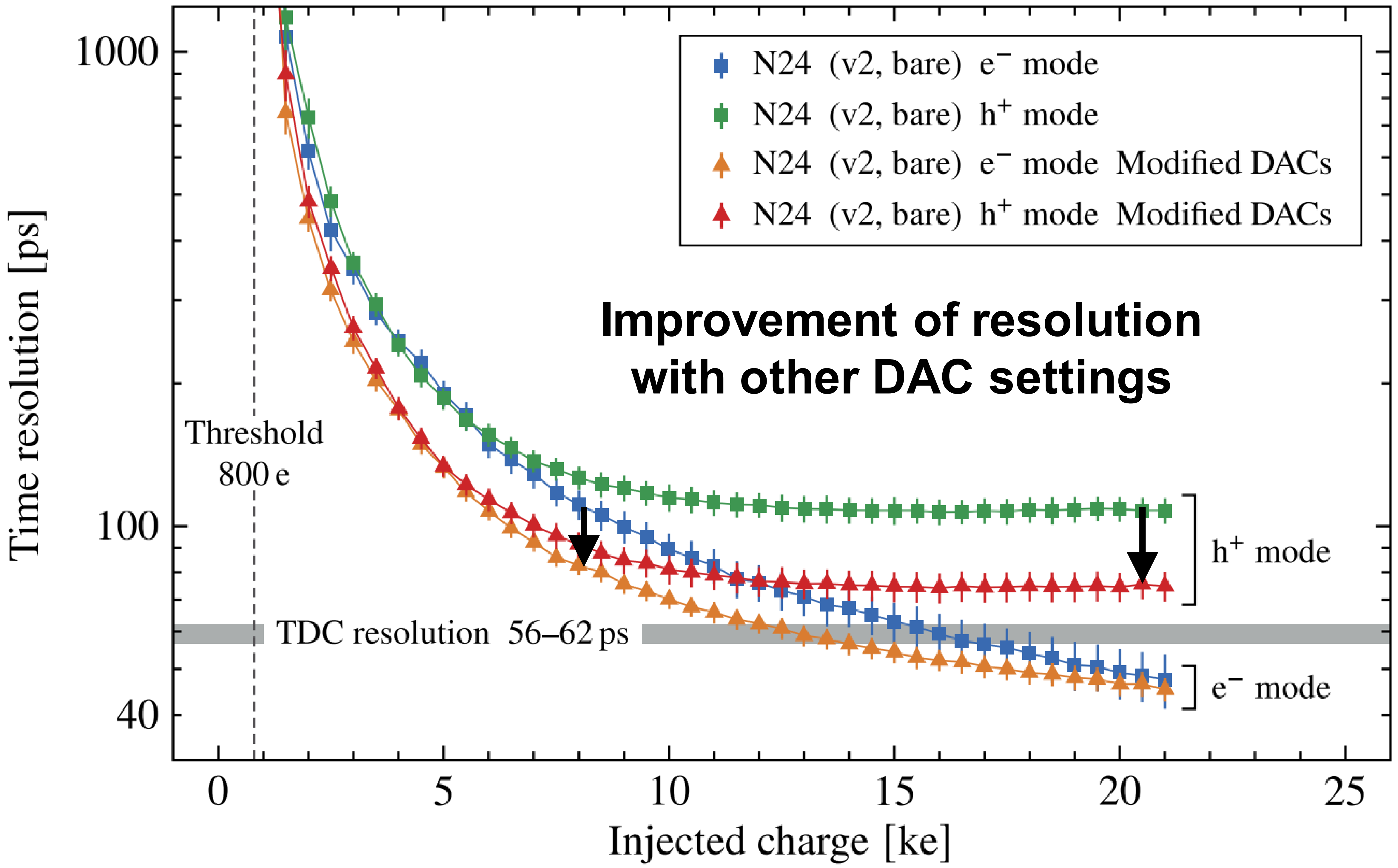


- For positive input signals the output slew rate is limited by the preamp bias current

K. Heijhoff *et al* 2022 *JINST* **17** P07006 [DOI: 10.1088/1748-0221/17/07/P07006]

Anolog front-end time resolution vs signal charge

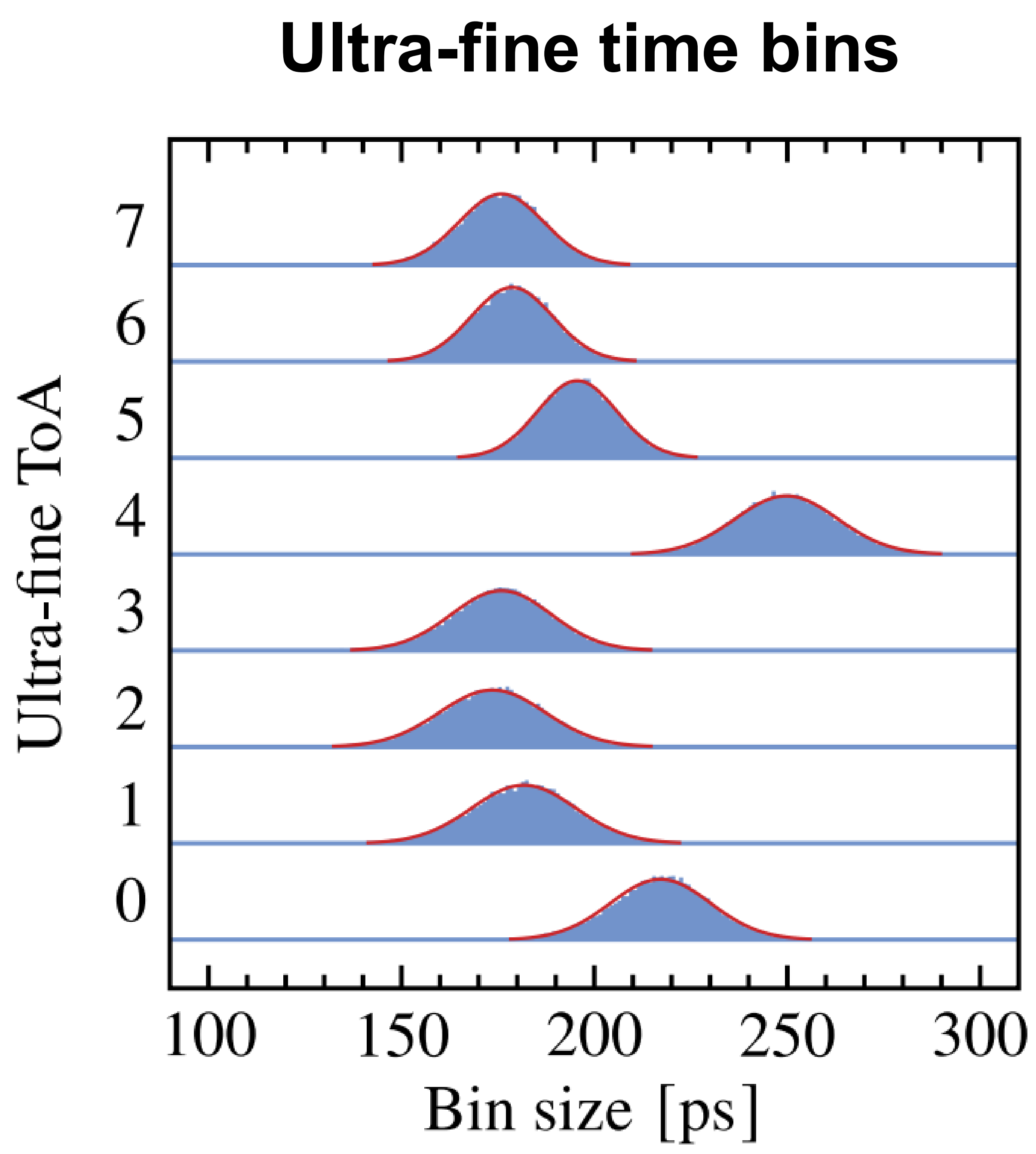


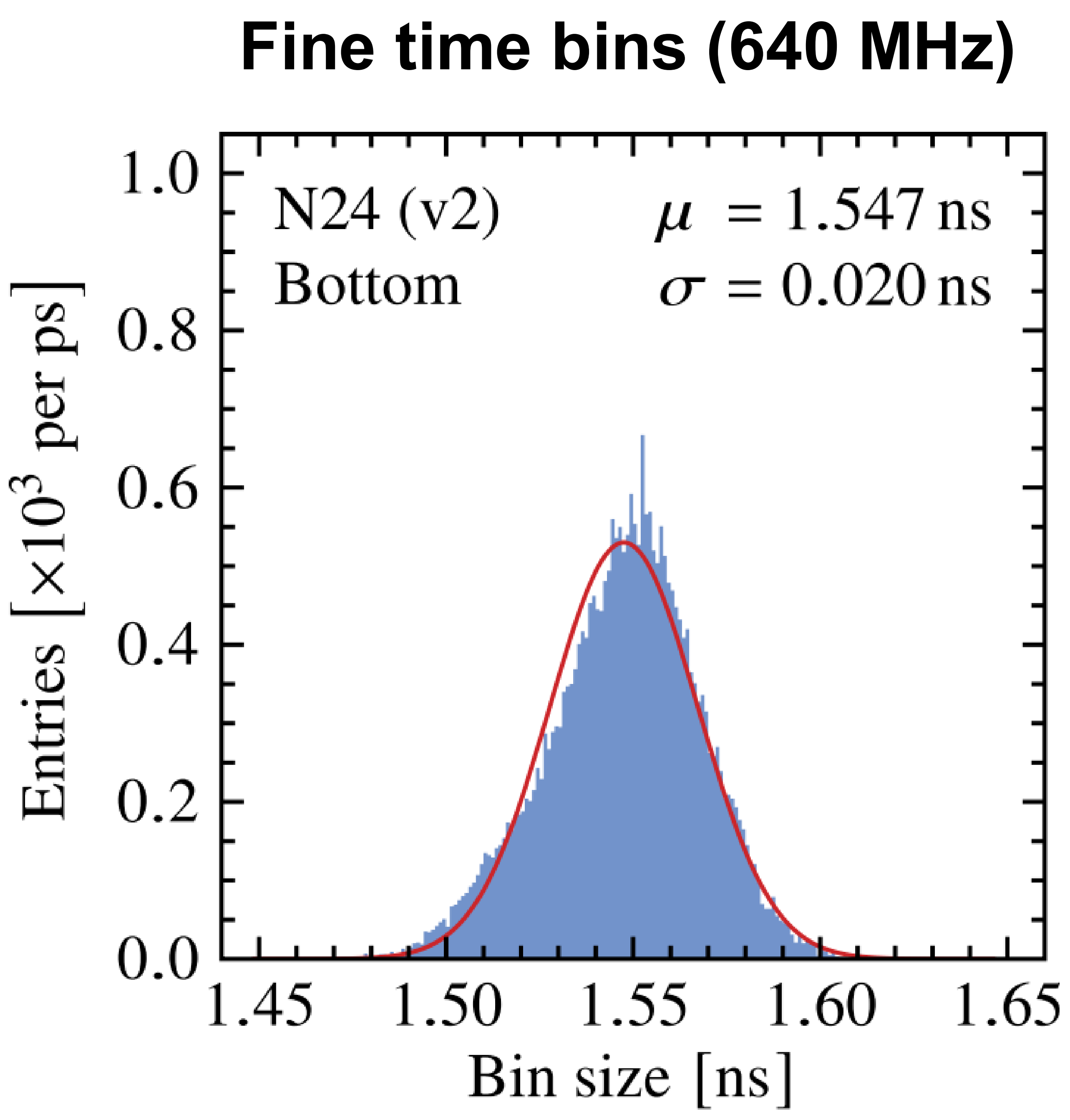


K. Heijhoff *et al* 2022 *JINST* **17** P07006 [DOI: 10.1088/1748-0221/17/07/P07006]

Digital front-end time resolution

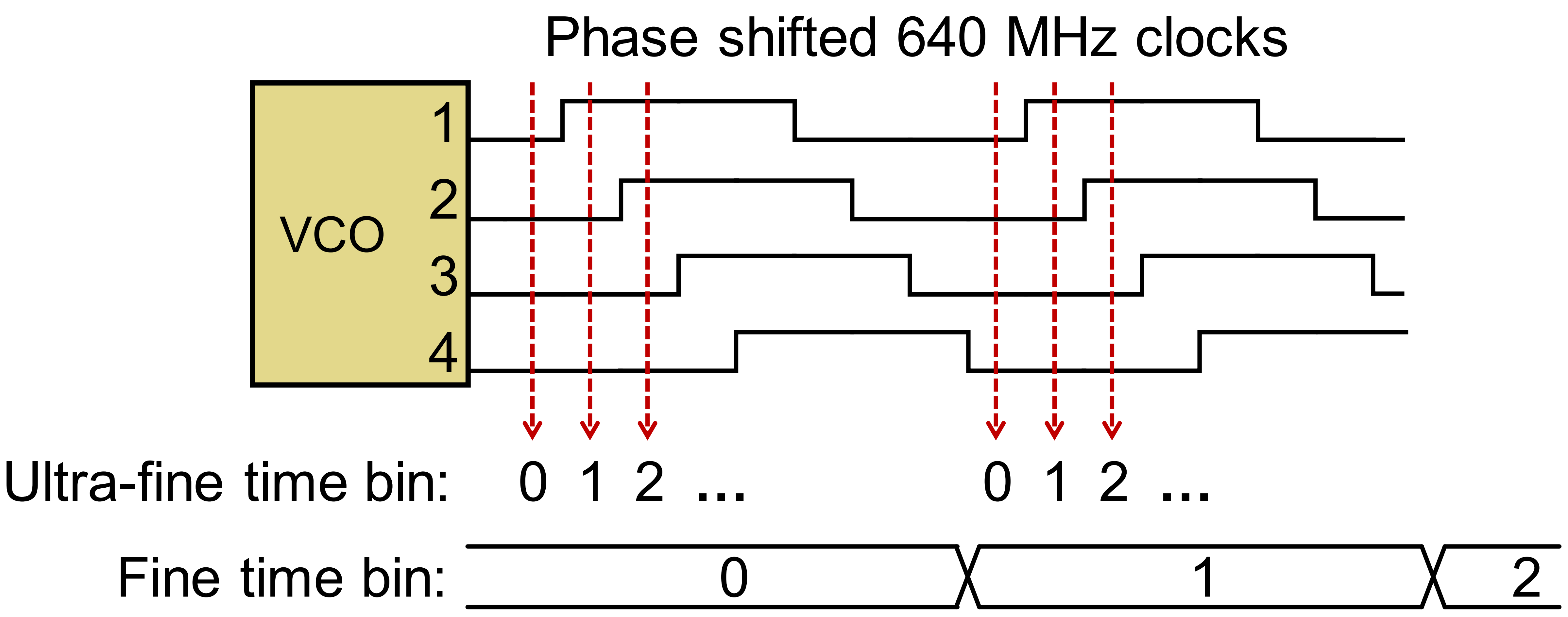
- Structure in ultra-fine time bins has a small impact on TDC resolution (few %)
- Variation in the VCO frequency over the pixel matrix observed:
  Bottom half: 1.547 ns ± 20 ps
  Top half: 1.583 ns ± 14 ps
- We have estimated the TDC resolution for correction methods of increasing complexity





Expected TDC resolution for various correction methods

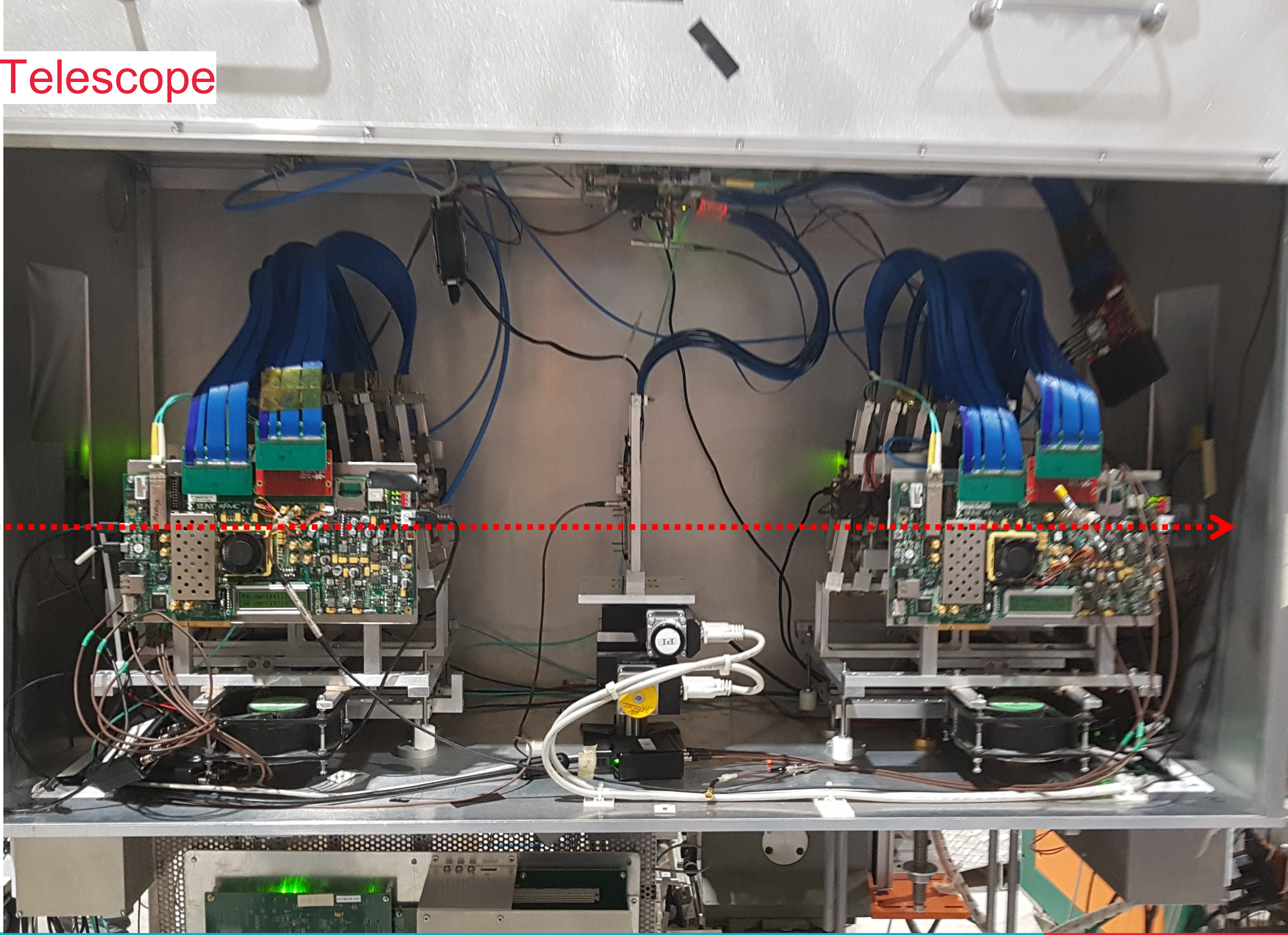
No correction	111	ps
(i) Chip-wide	111	ps
(ii) Per matrix half	80	ps
(iii) Per VCO	61.9	ps
(iv) Per VCO, ufToA	60.3	ps
Best possible	58.3	ps
Ideal bins	56.4	ps

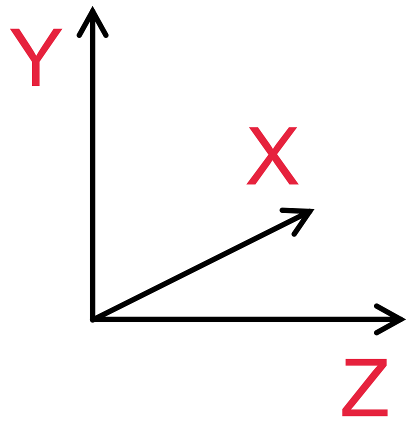


LHCb VELO Timepix**3** Telescope

- Systematic timing errors have been studied in detail using the Timepix**3** telescope.
- Understanding the combined time resolution of large systems will be vital for future 4D trackers

Beam



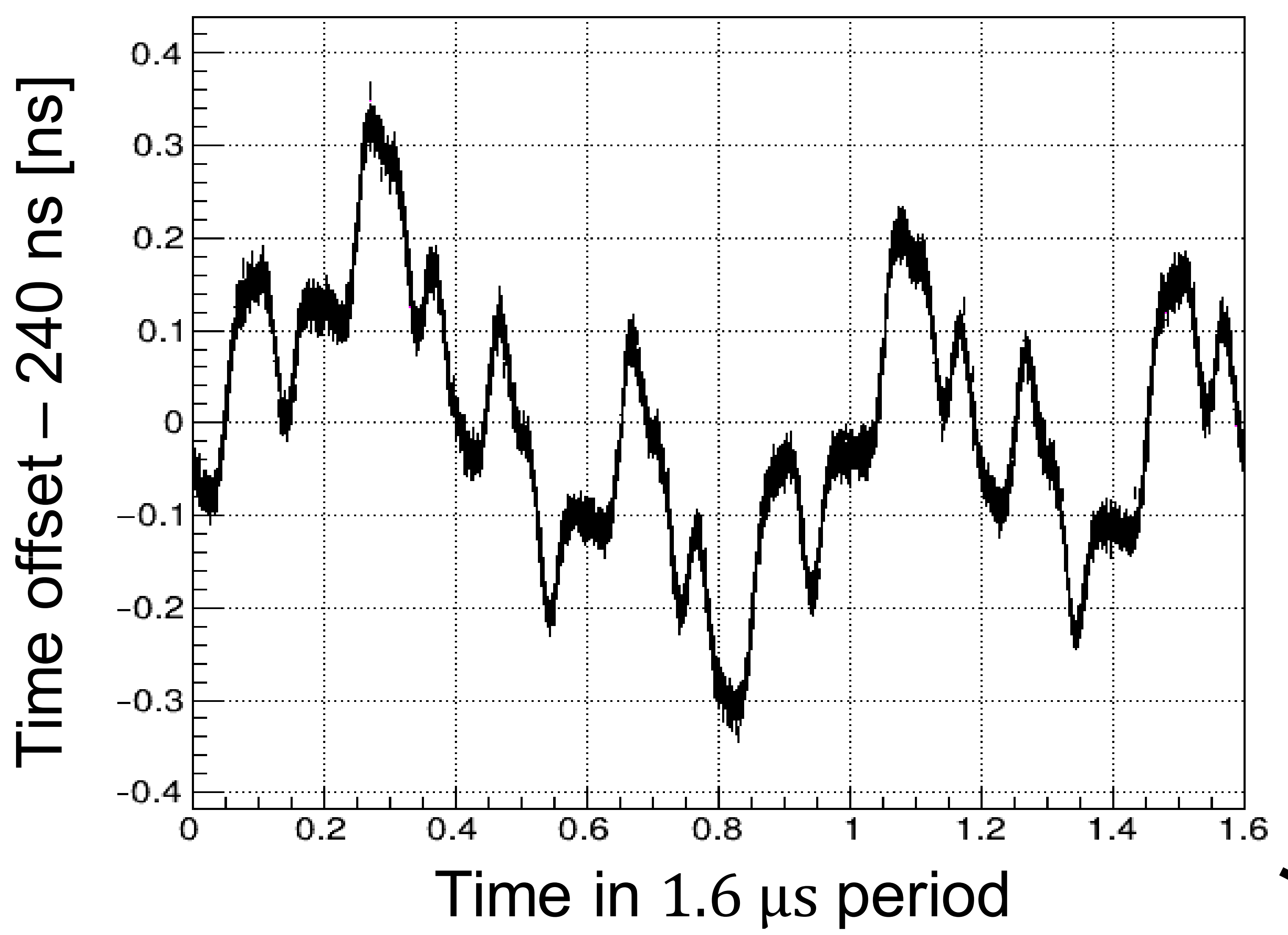


K. Akiba *et al* 2019 *JINST* **14** P05026
[DOI: 10.1088/1748-0221/14/05/P05026]

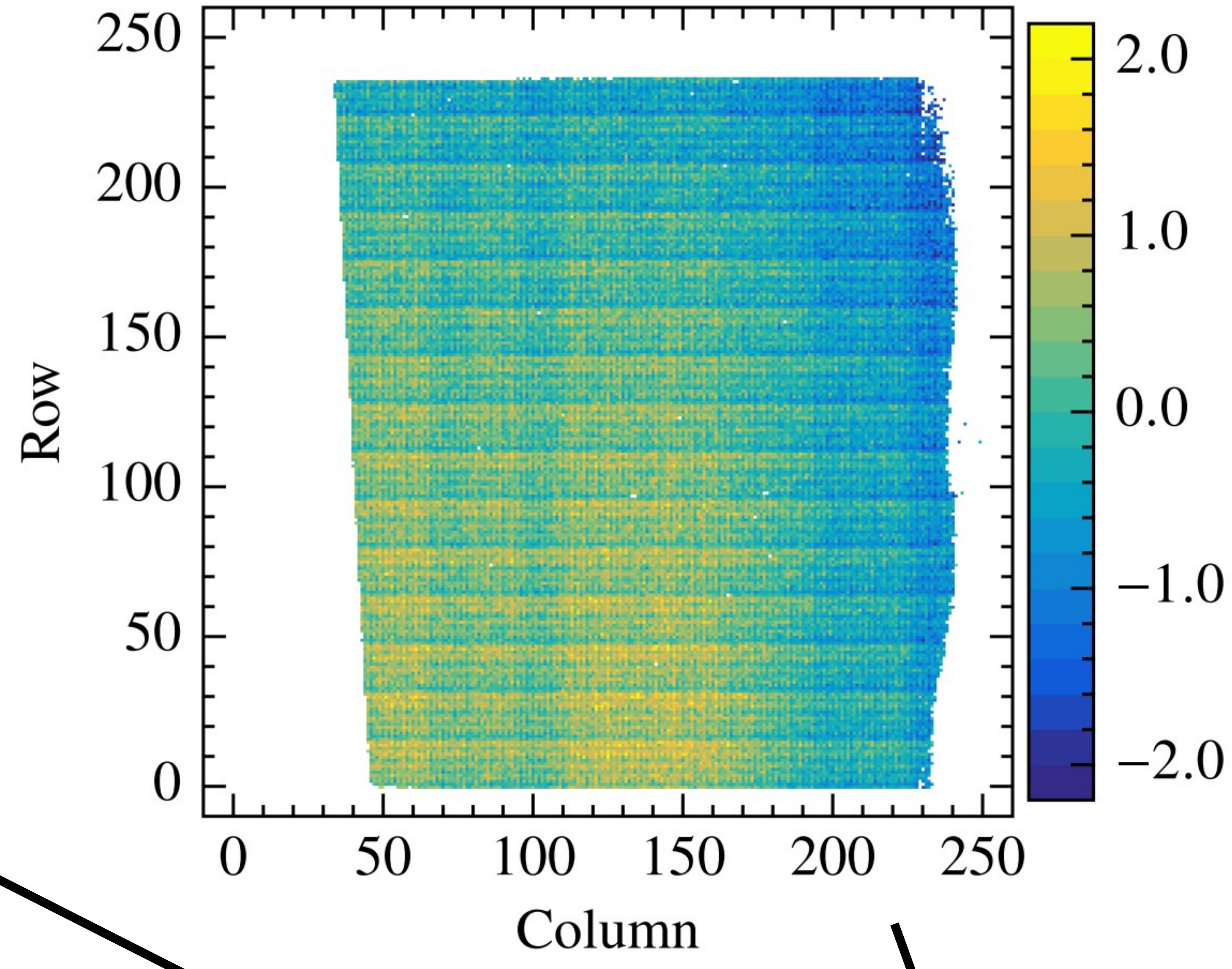
K. Heijhoff *et al* 2020 *JINST* **15** P09035 [DOI: 10.1088/1748-0221/15/09/P09035]

Timing systematics in the LHCb VELO Timepix**3** Telescope

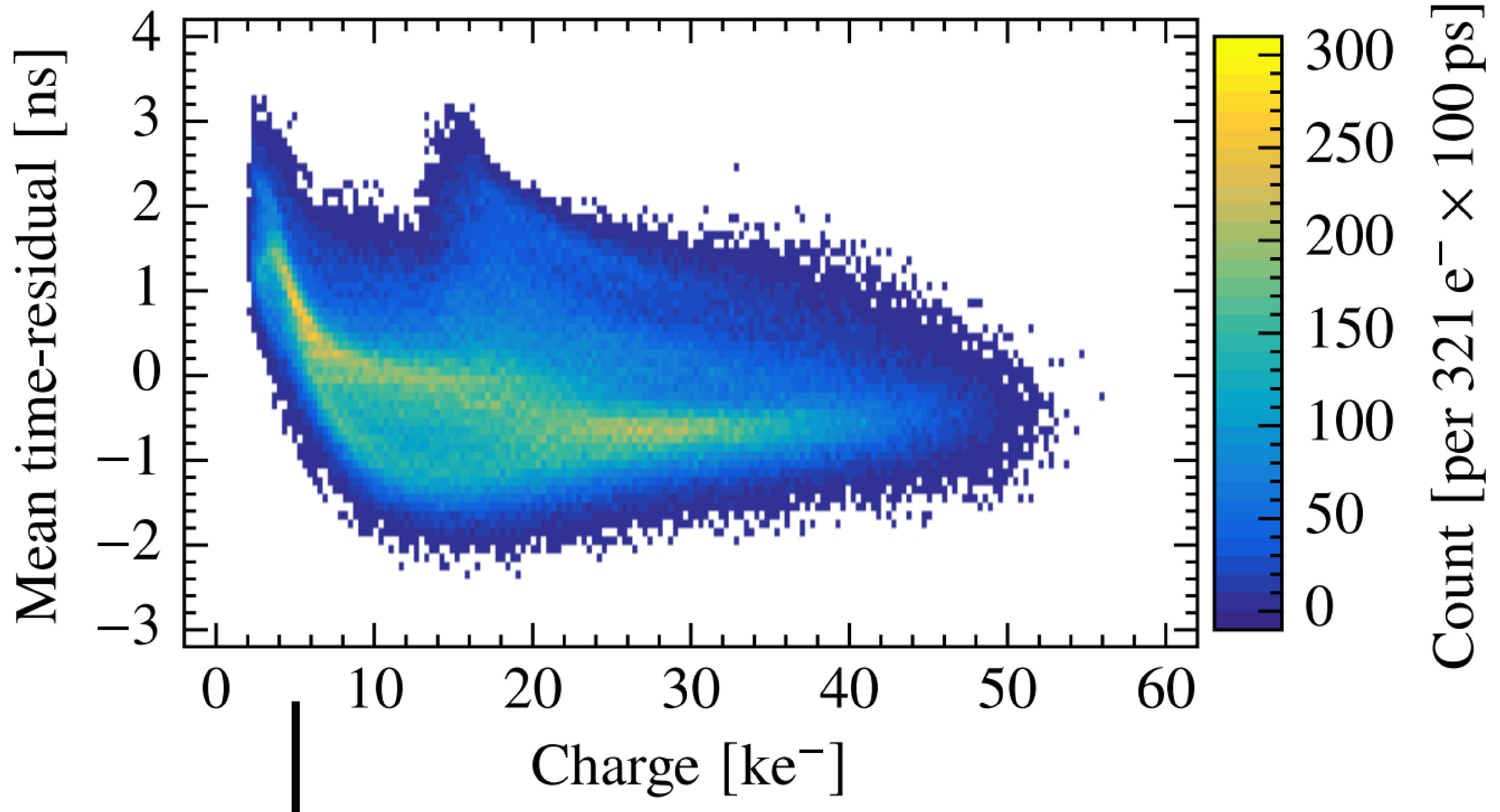
Clock frequency variation



Pixel / TDC systematics

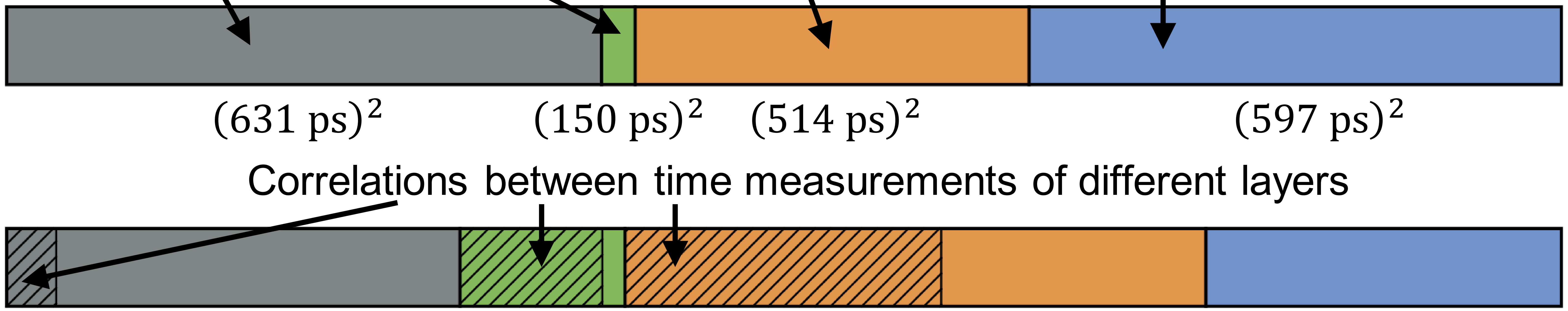


Timewalk and signal induction time in sensor



Analog front-end / TDC / Other

Single-hit time:



$(631\ \mathrm{ps})^2$ $(150\ \mathrm{ps})^2$ $(514\ \mathrm{ps})^2$ $(597\ \mathrm{ps})^2$

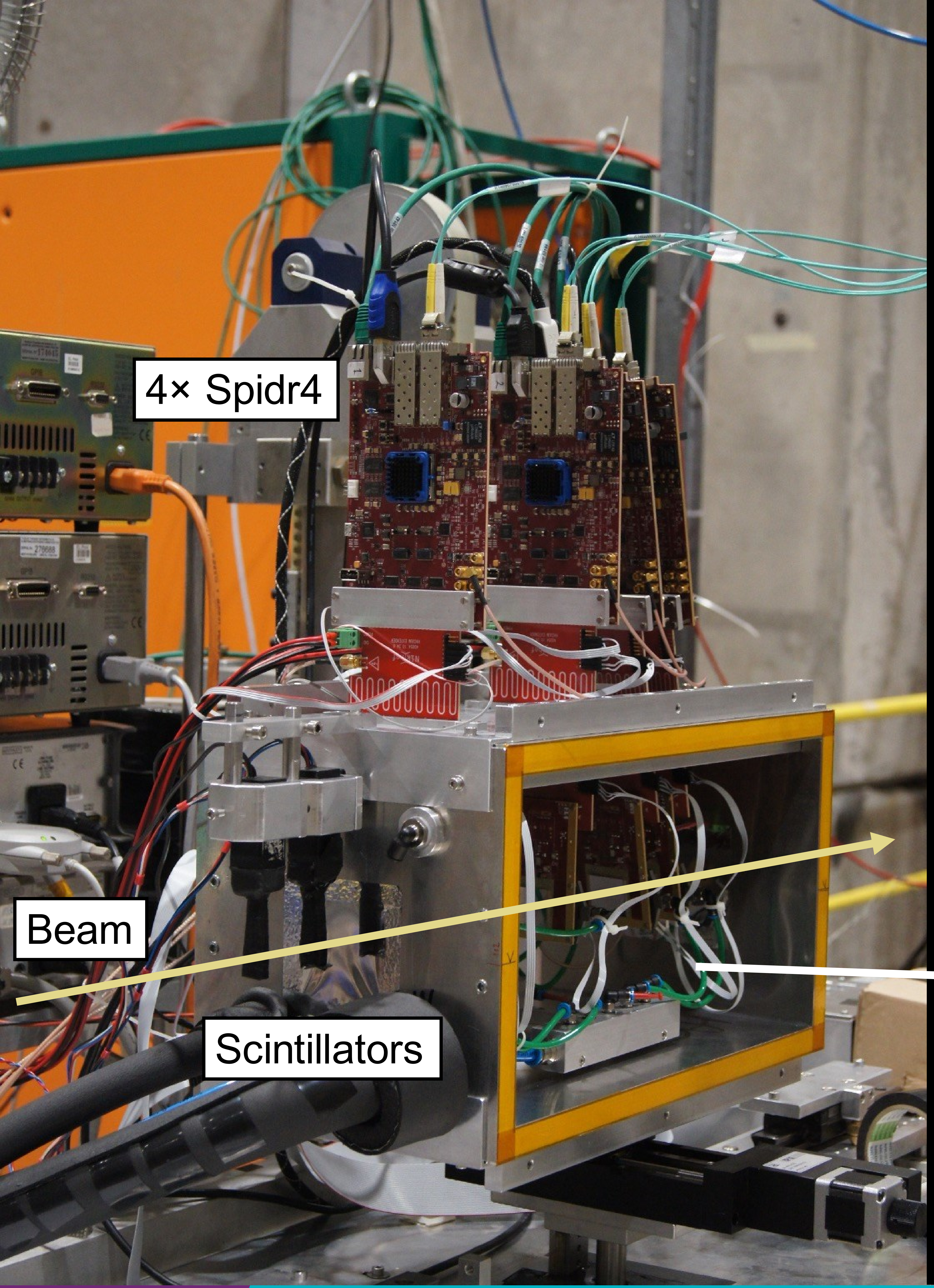
$\sigma_t = 1\ \mathrm{ns}$

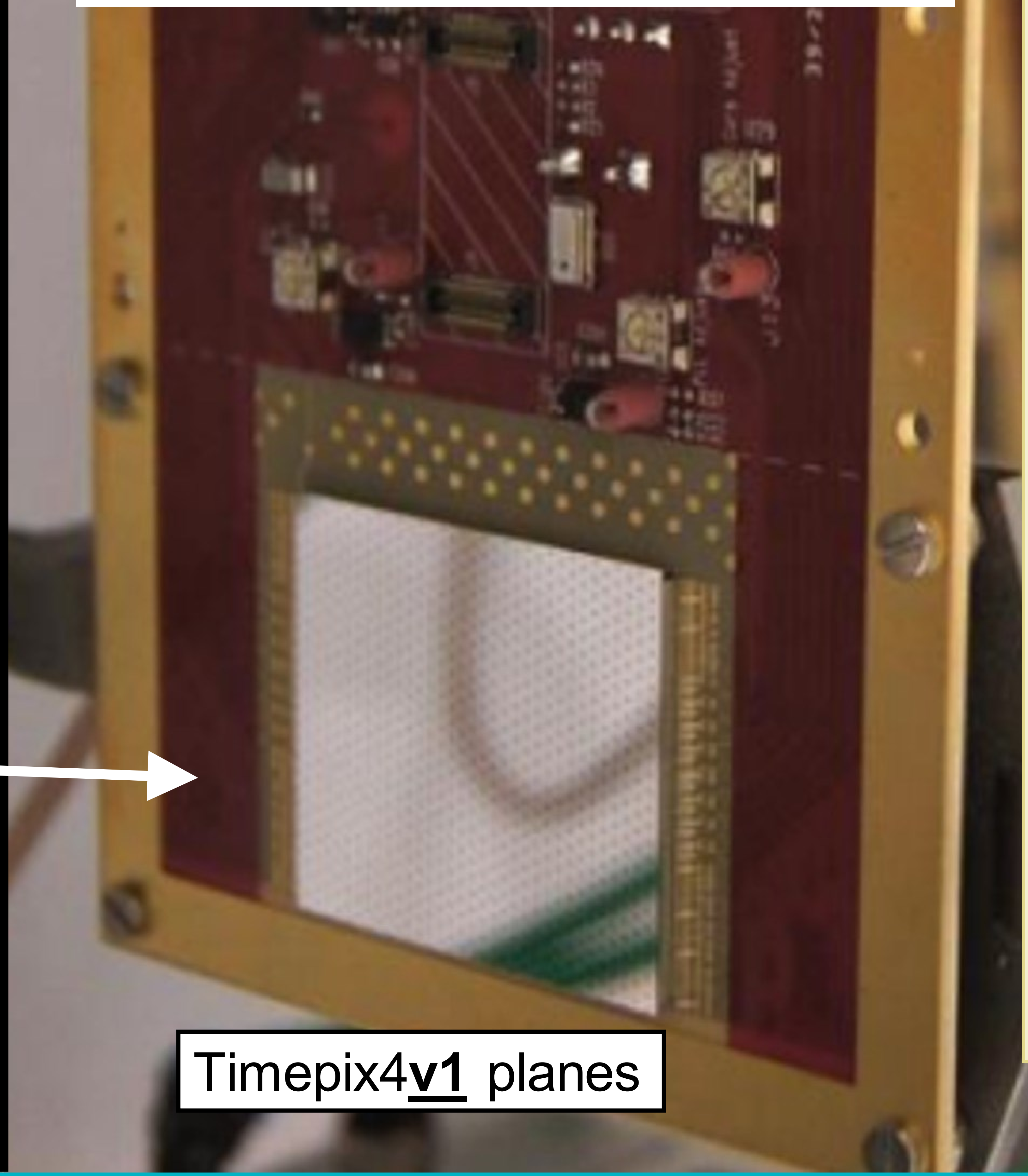
Correlations between time measurements of different layers

Track time:
(mean of 8 hits)

$(236\ \mathrm{ps})^2$ $(209\ \mathrm{ps})^2$ $(268\ \mathrm{ps})^2$ $(209\ \mathrm{ps})^2$

$\sigma_t = 438\ \mathrm{ps}$



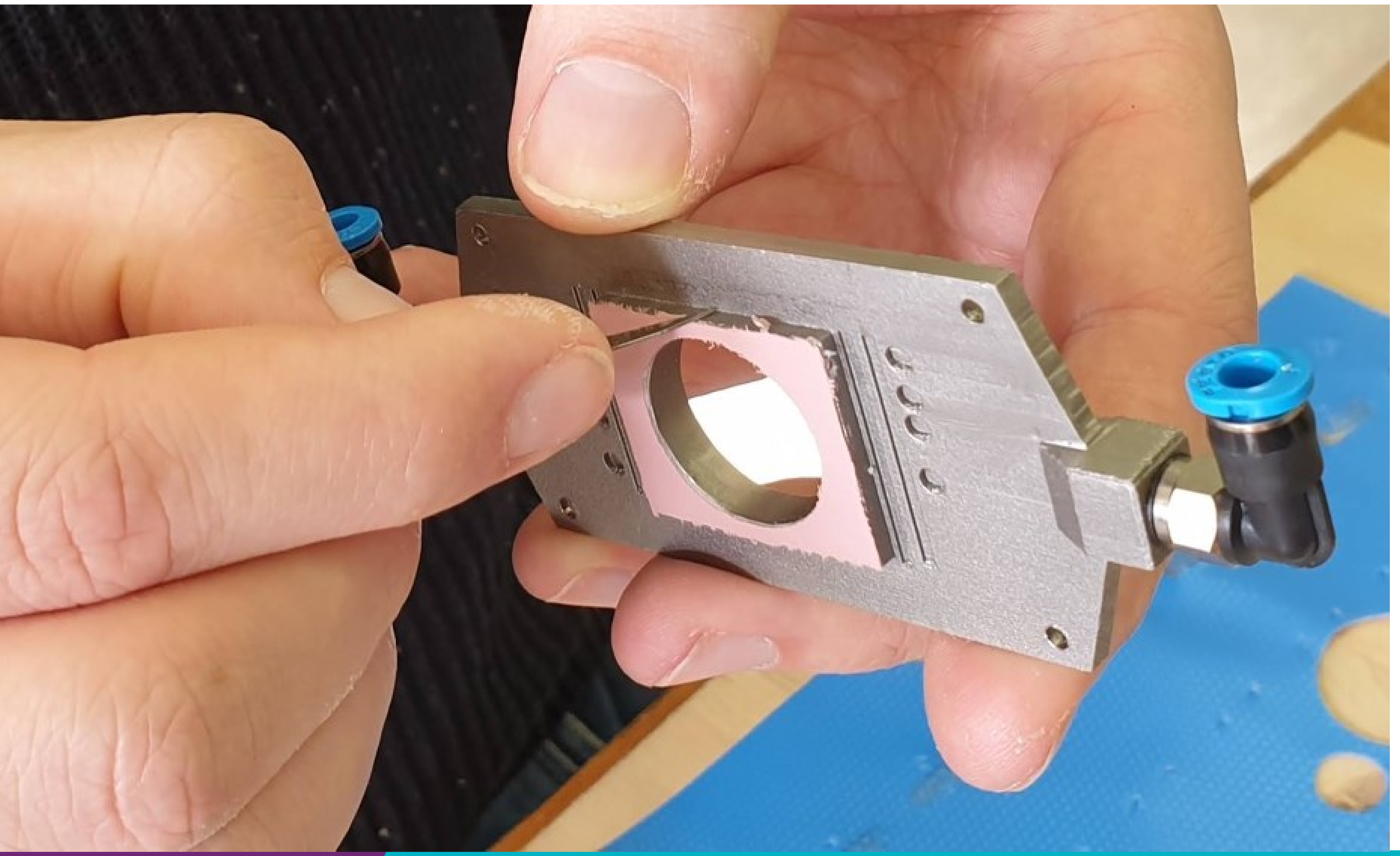


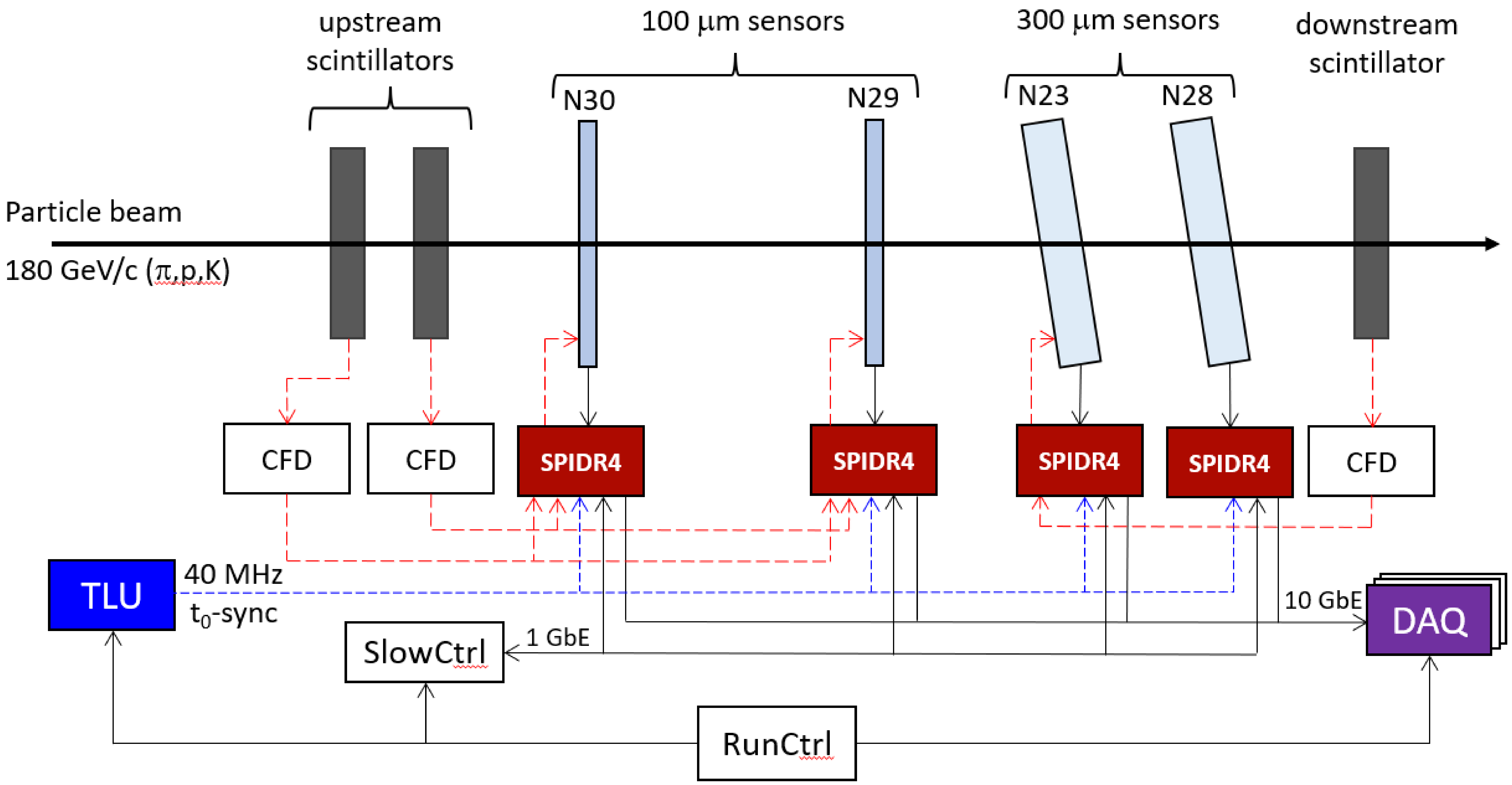
Timepix4 Telescope

- Currently a new telescope based on the Timepix4 ASIC is in the early stages of operation
- Final telescope will have 8 layers of Timepix4
- It will be the ideal tool to investigate fast detectors that can handle enormous rates
- In the context of 4D tracking, we want to investigate the timing characteristics of this telescope
- Results shown are obtained with 4 Timepix4 layers in a 180 GeV/c mixed hadron beam at the CERN SPS

Timepix4 Telescope setup

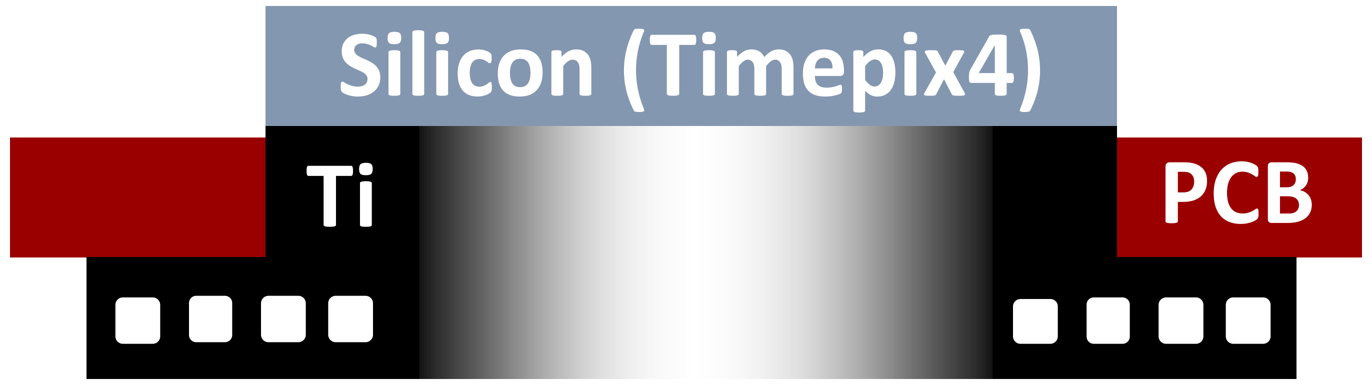
- 2 × 100 µm planar n-on-p sensors for time resolution (perpendicular to beam)
- 2 × 300 µm planar n-on-p sensors for spatial resolution (angled for charge sharing)
- All chips are cooled to room temperature using a titanium cooling block (3D printed) through which glycol is circulated.





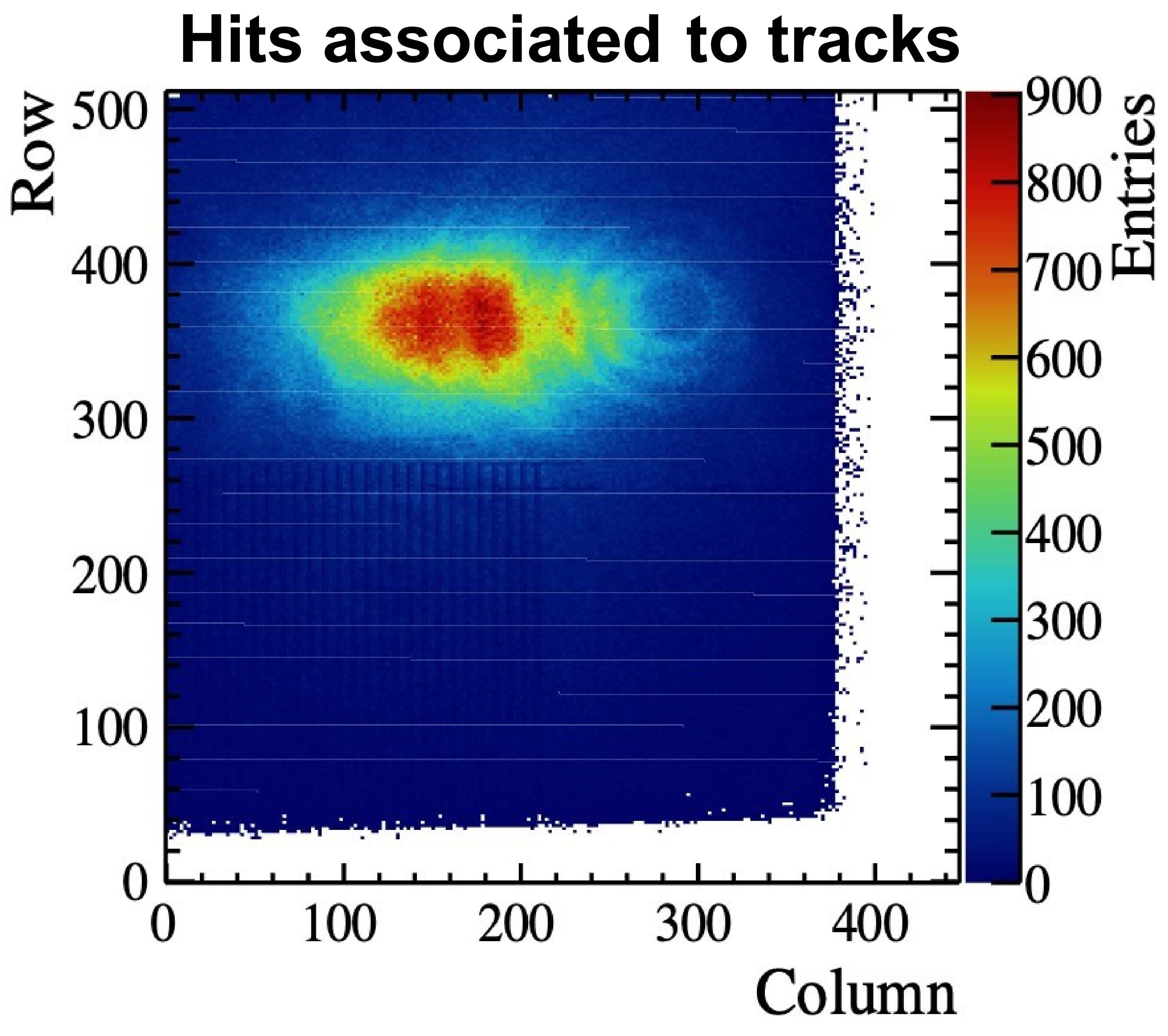
Current cooling:

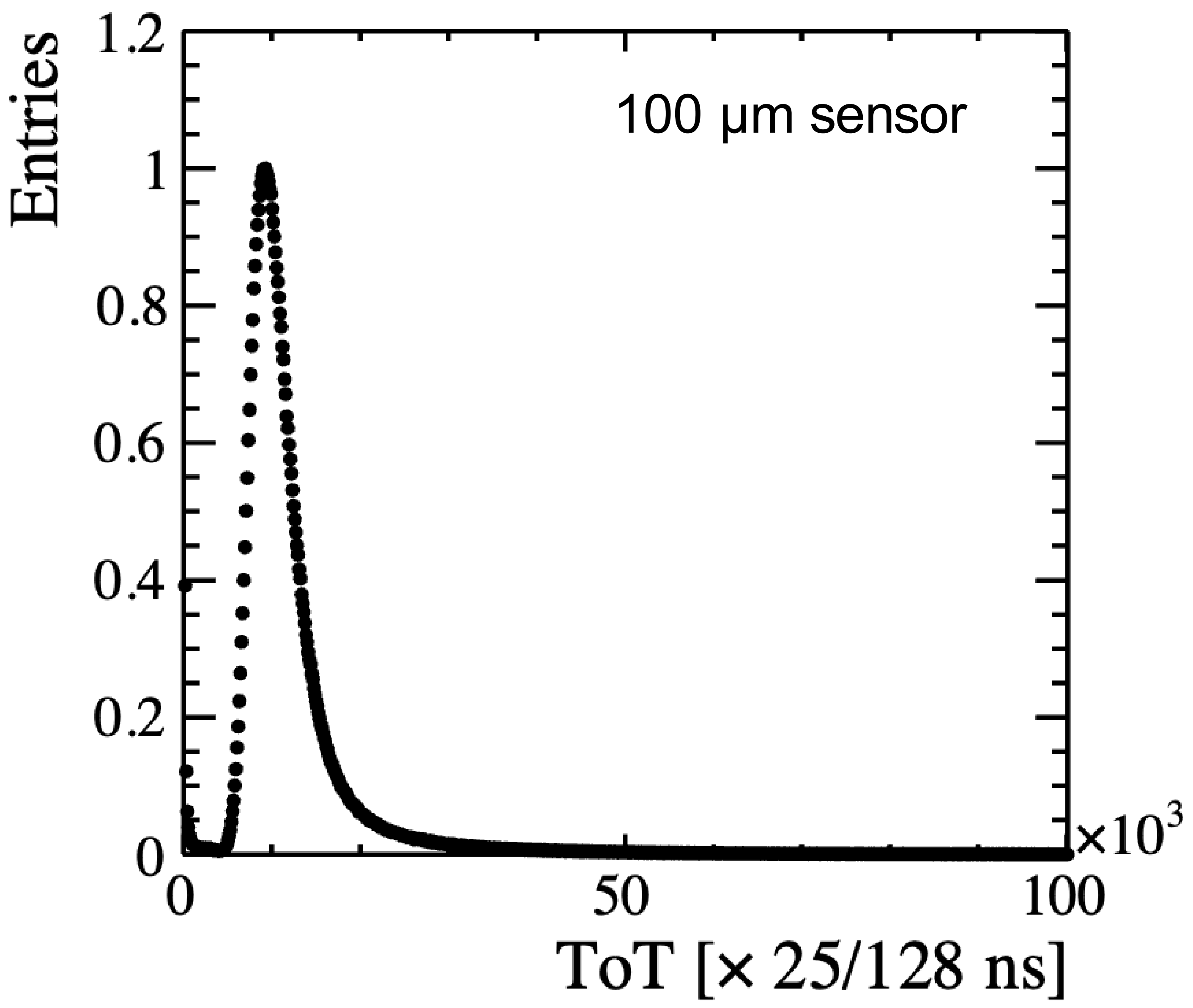
Envisioned cooling:

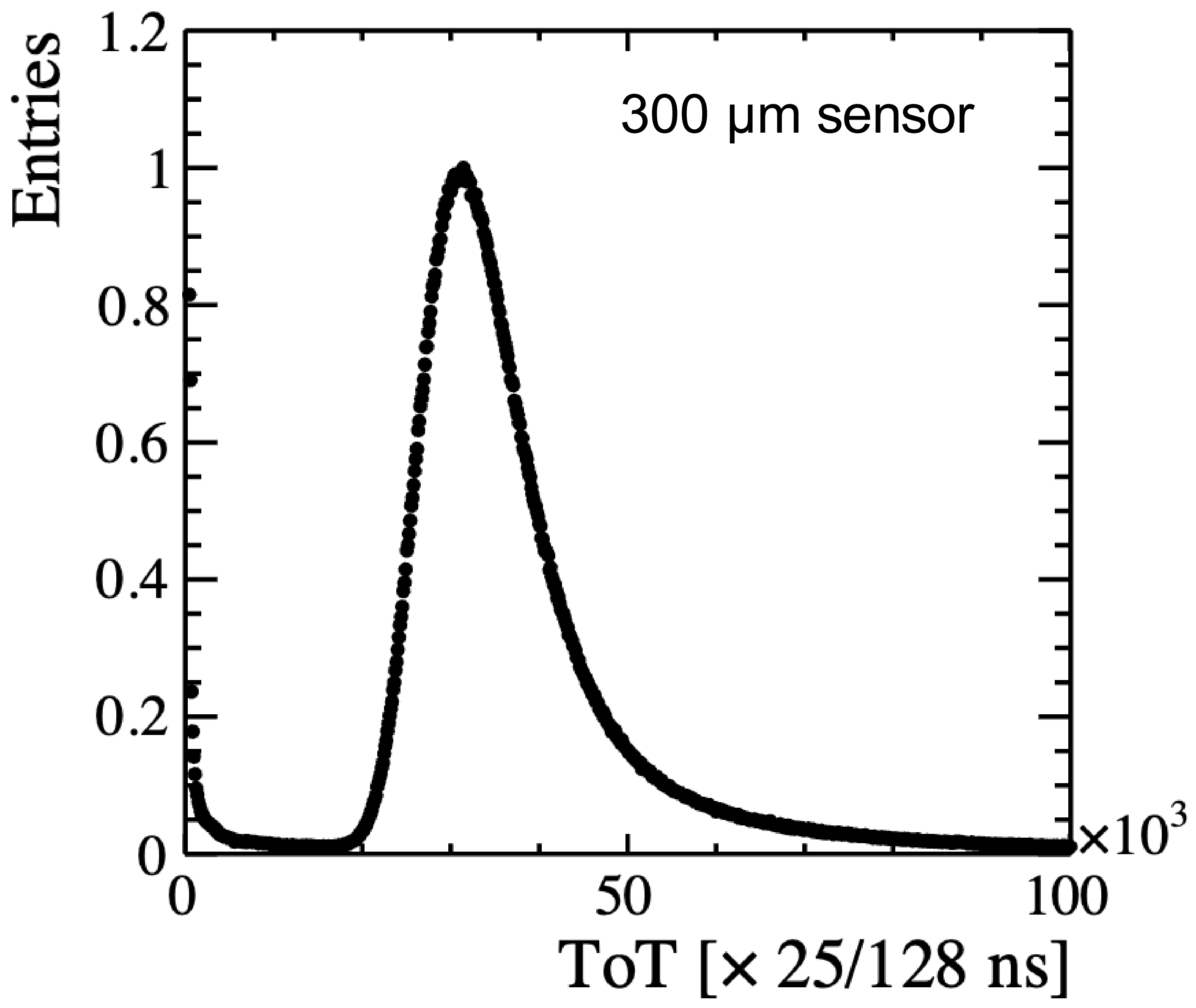


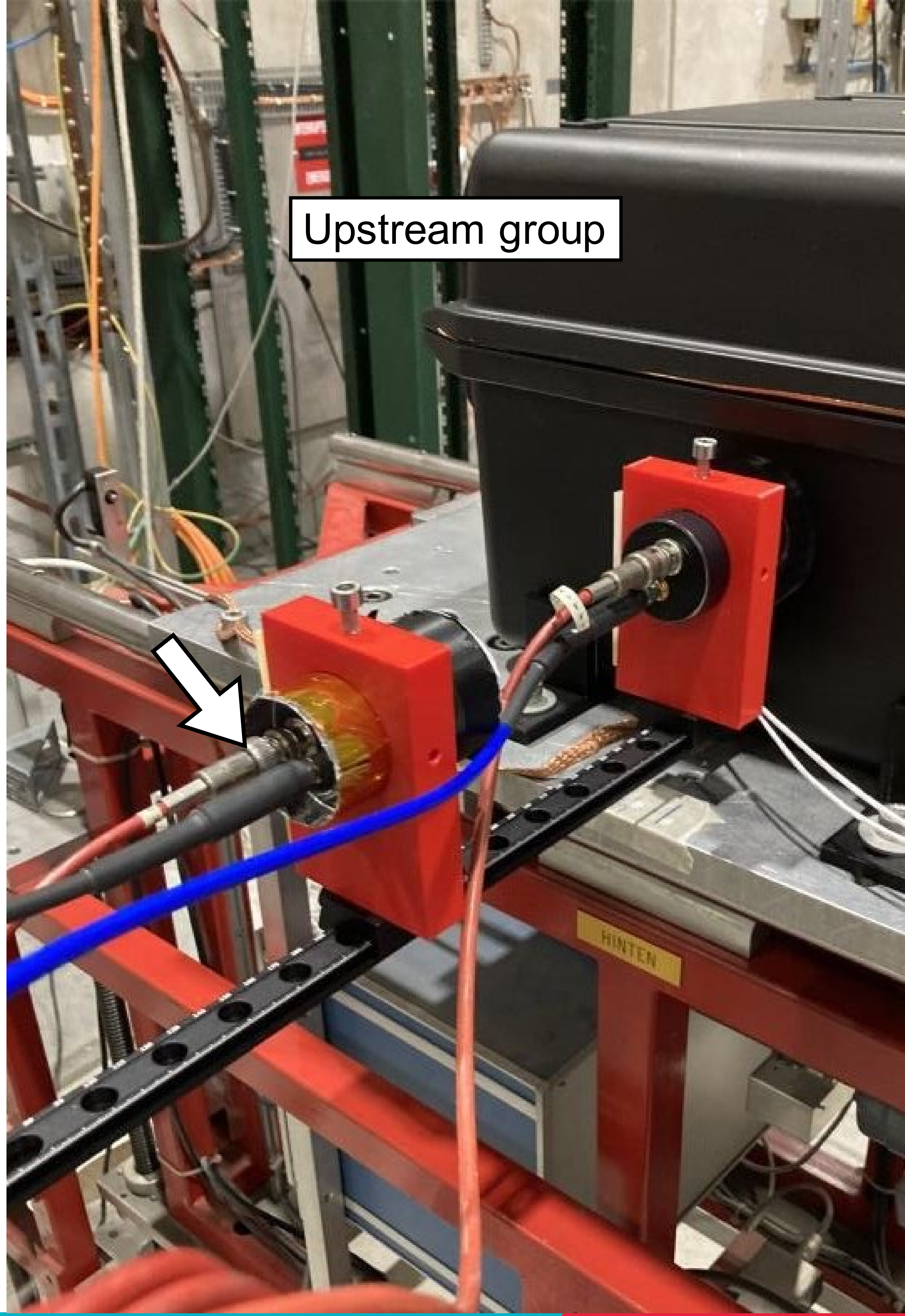
First beam

- First hitmap data on the online monitoring looked puzzling
- Other histograms look as expected
- Offline analysis is performed using the LHCb Kepler framework





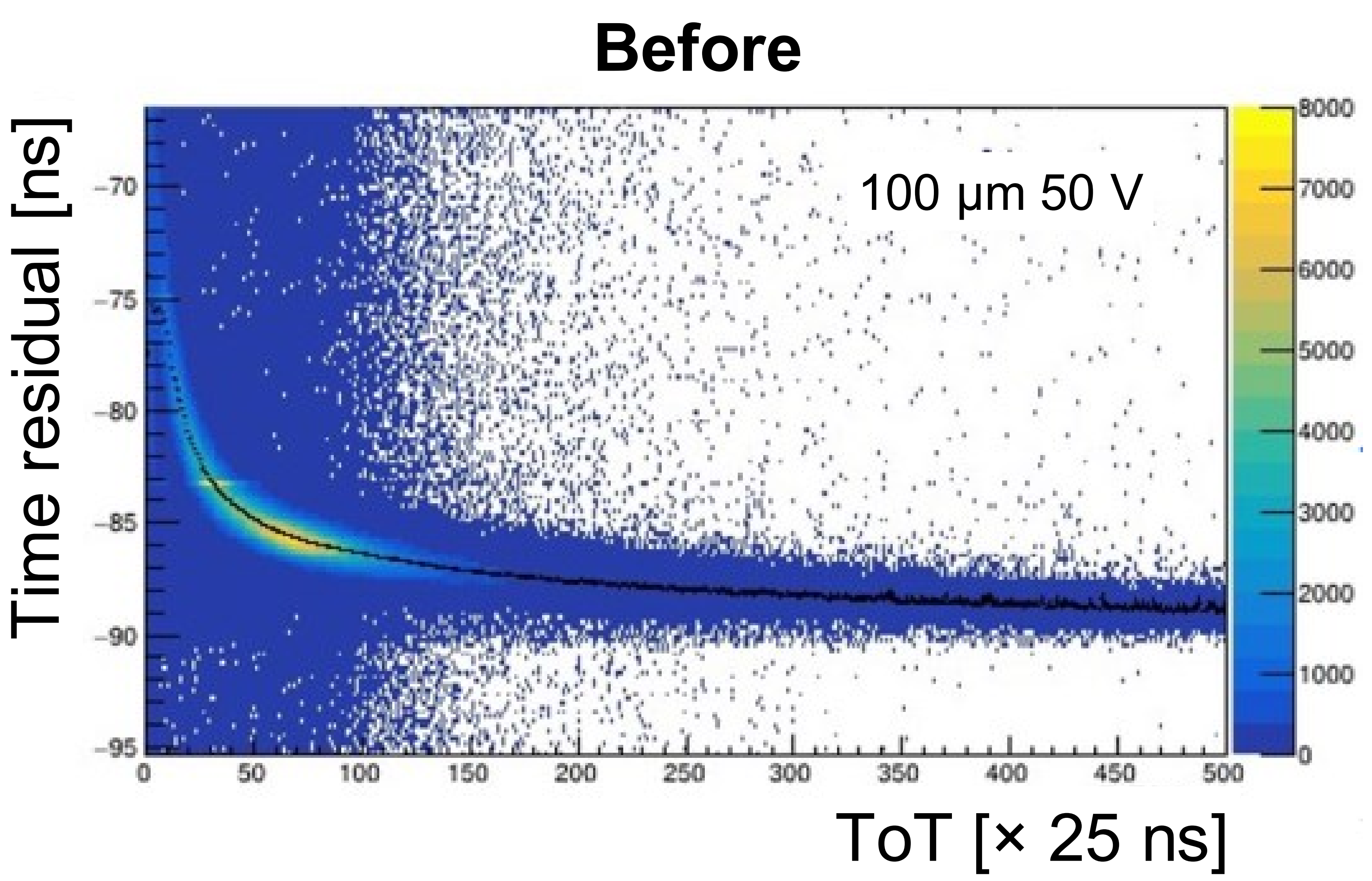


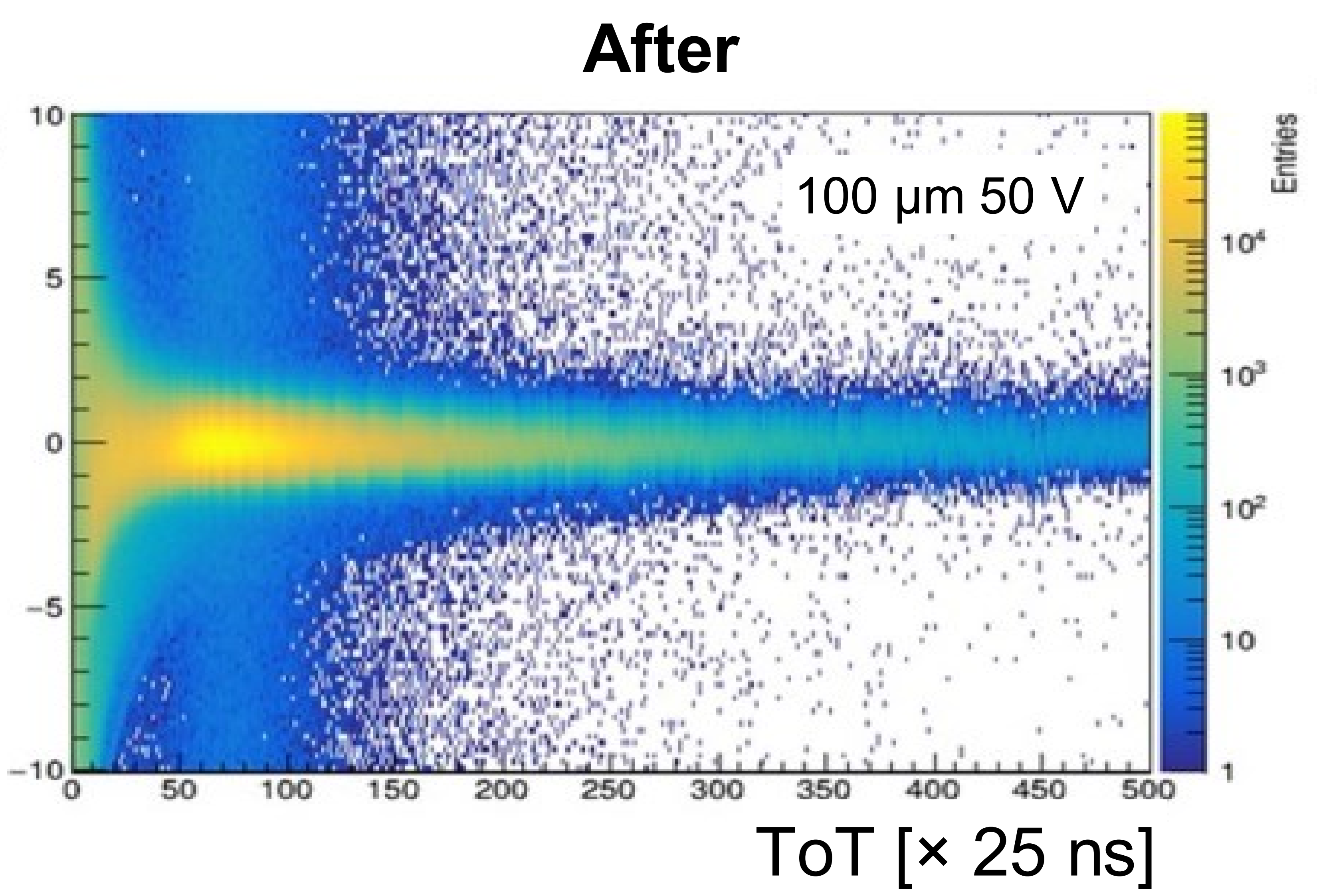


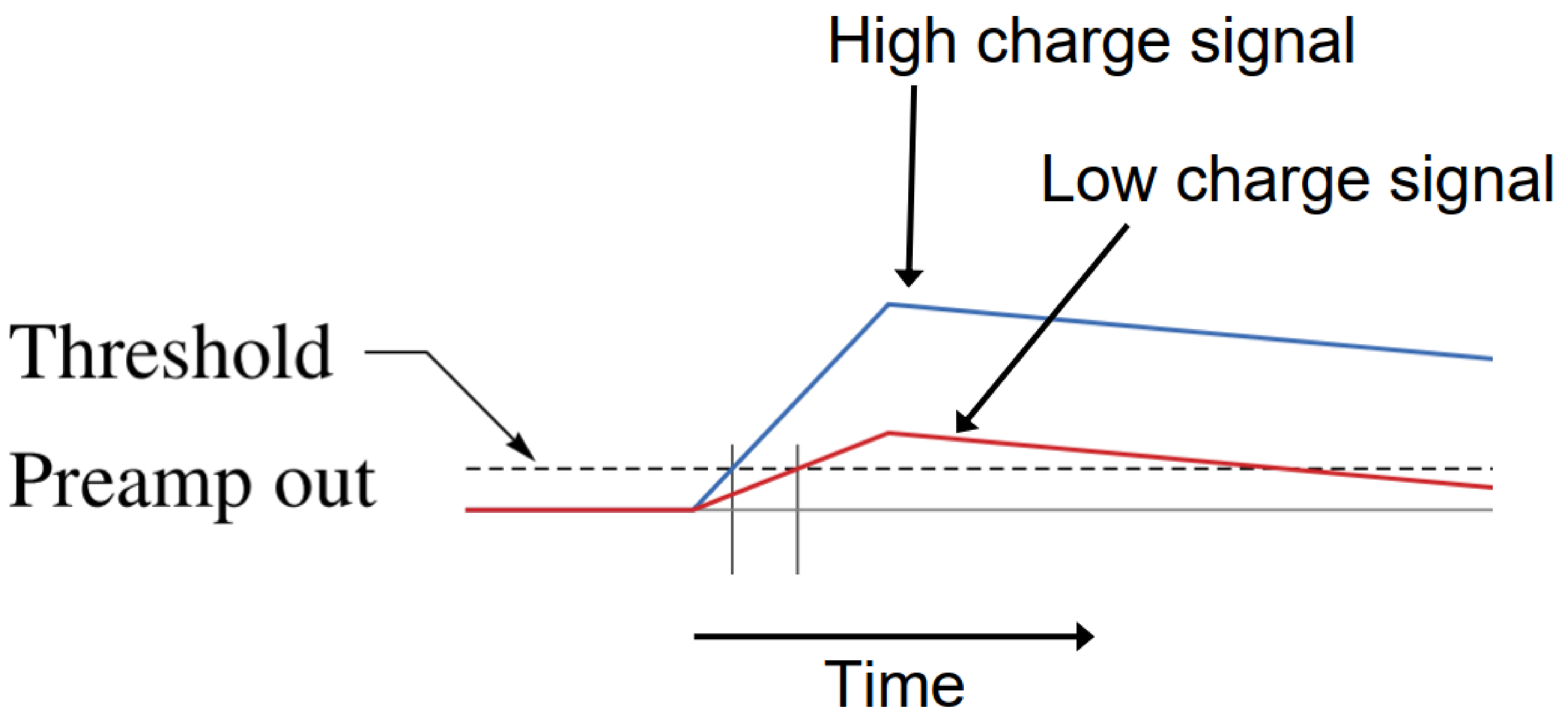
Timewalk correction

- 100 μm sensors give signals of ~8ke for MIPs
- The ToT measurement is used to apply a timewalk correction
- Current track time resolution: σ_t = 340 ps (4 layers)
- Lots of room for improvement:

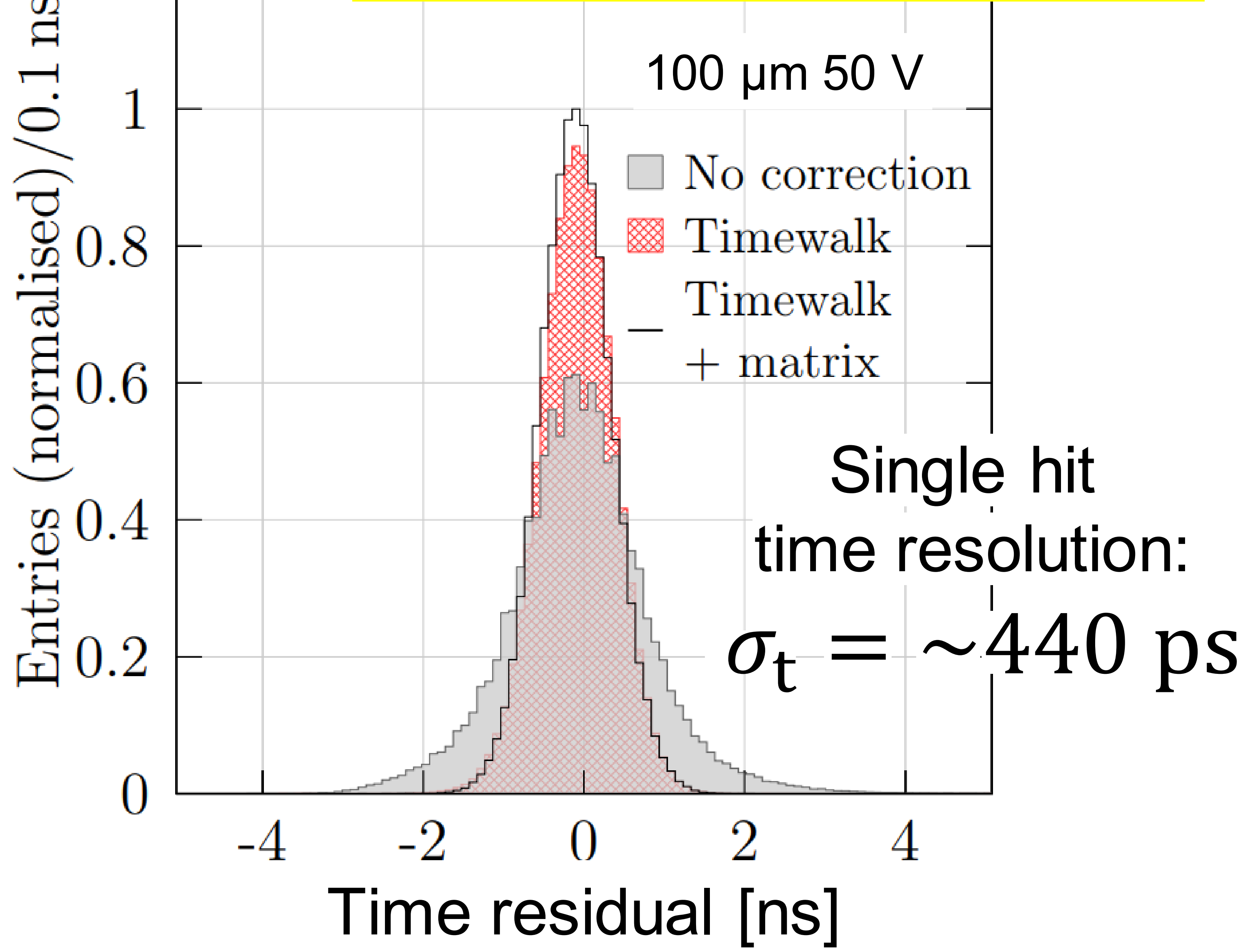
1. Problems with external clock
2. VCO not locked to 40 MHz in Timepix4v1
3. Pixel variation in discharge current affects timewalk correction. (Charge calibration will fix this.)





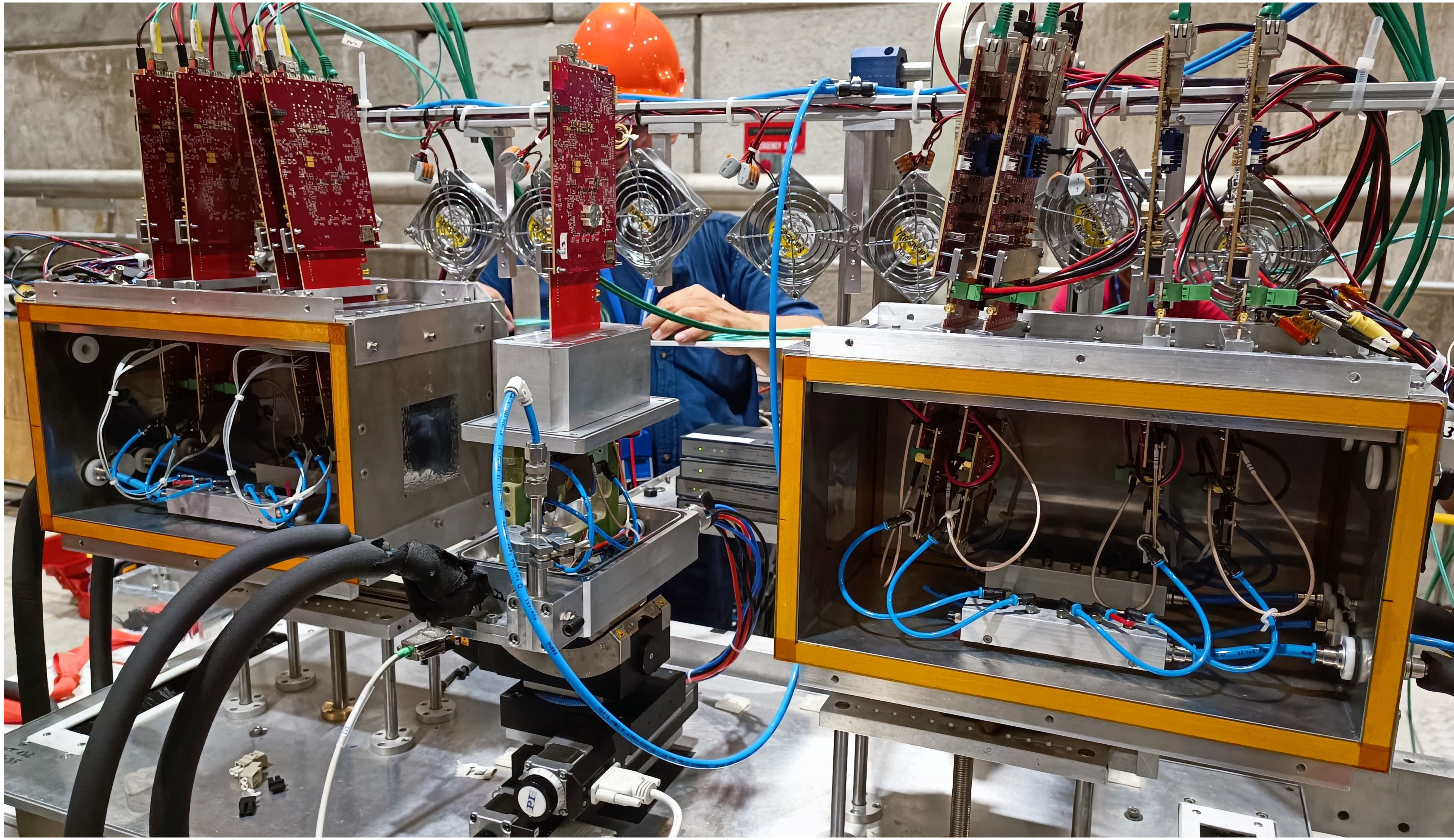


K. Akiba *et al* [arXiv: 2210.01442]



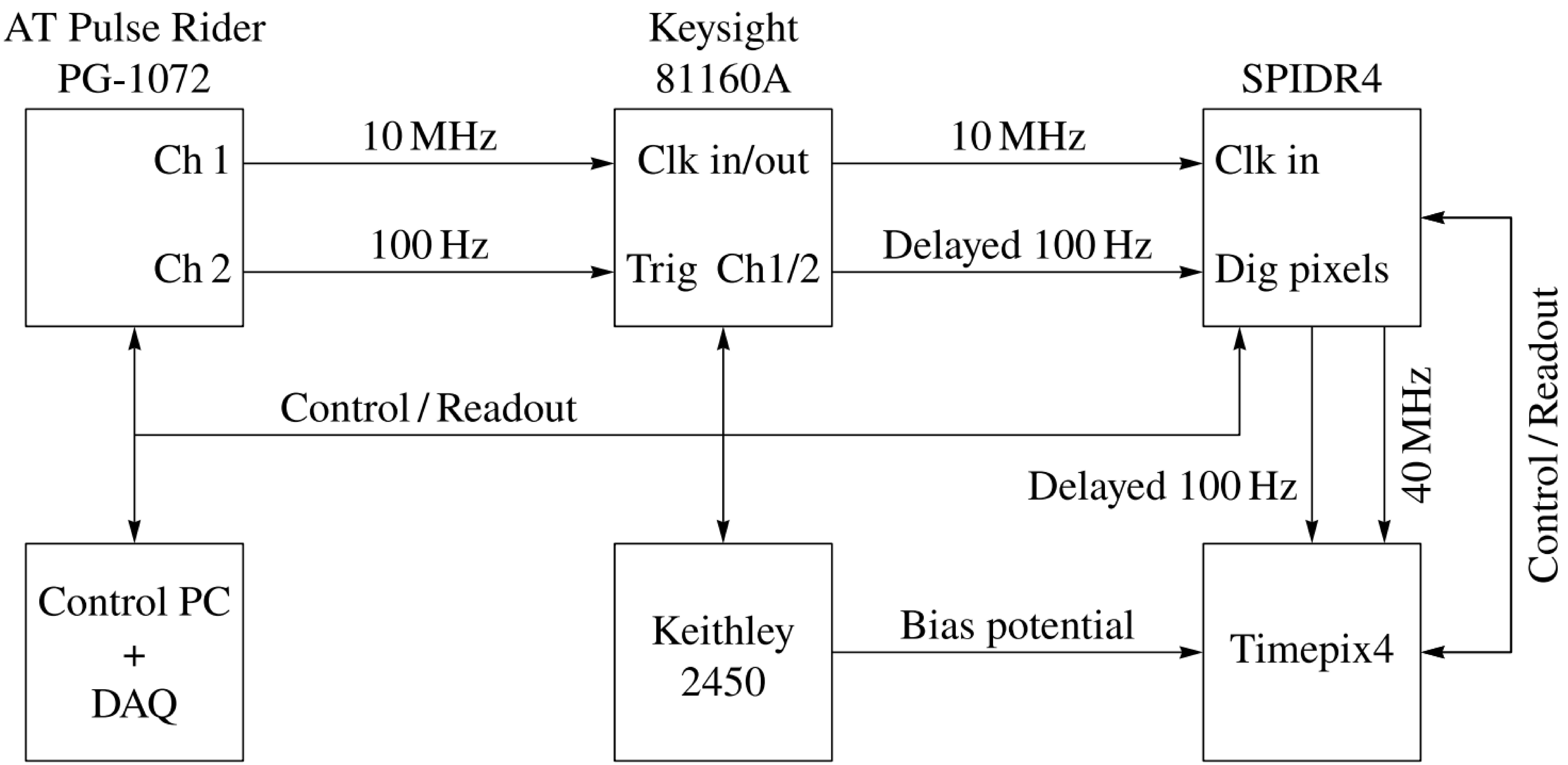
Conclusion and Outlook: Towards Fast Timing and 4D tracking

- We have set a challenging benchmark time resolution using test-pulse measurements
- Proof of concept: Track reconstruction with 4-layer Timepix4 Telescope.
- Testbeam with 8 layers + DUT has taken place earlier this month:
  - Planes have been upgraded to Timepix4v2
  - Time reference system has been upgraded to an MCP + PicoTDC (σ_t < 20 ps)
- Faster sensors are anticipated: LGAD, 3D, …



Backup slides

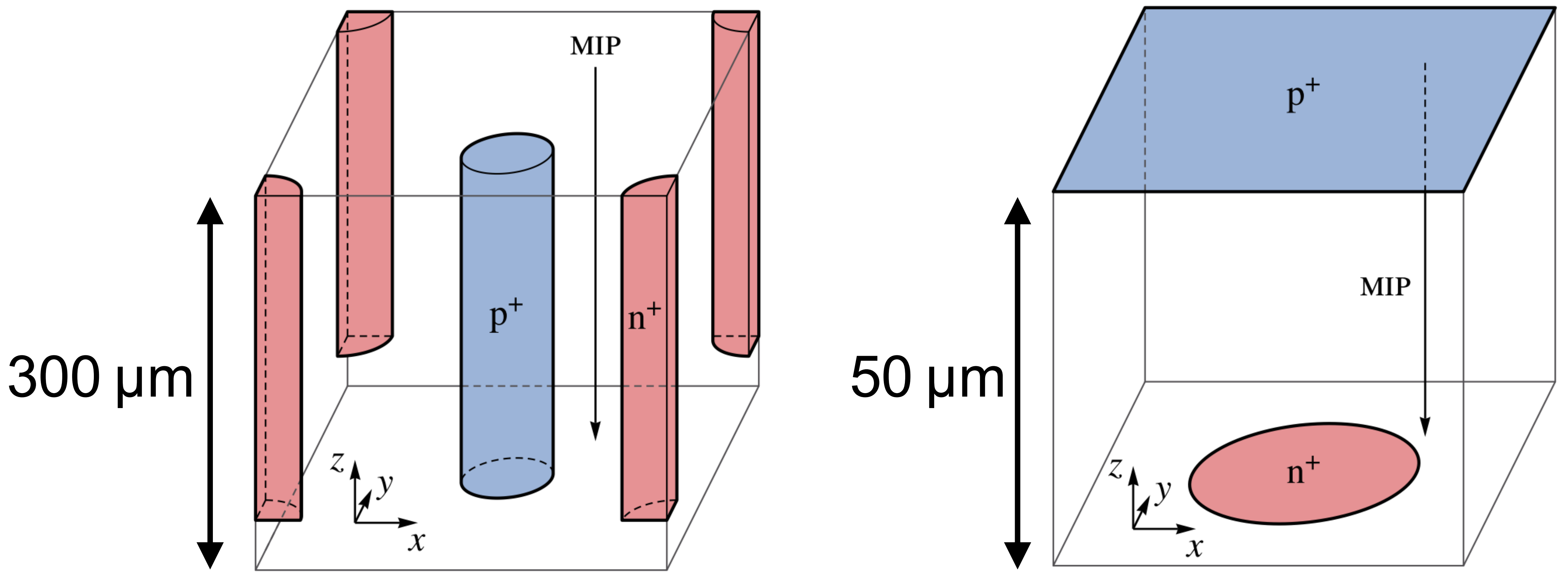
Timepix4 test-pulse measurement setup



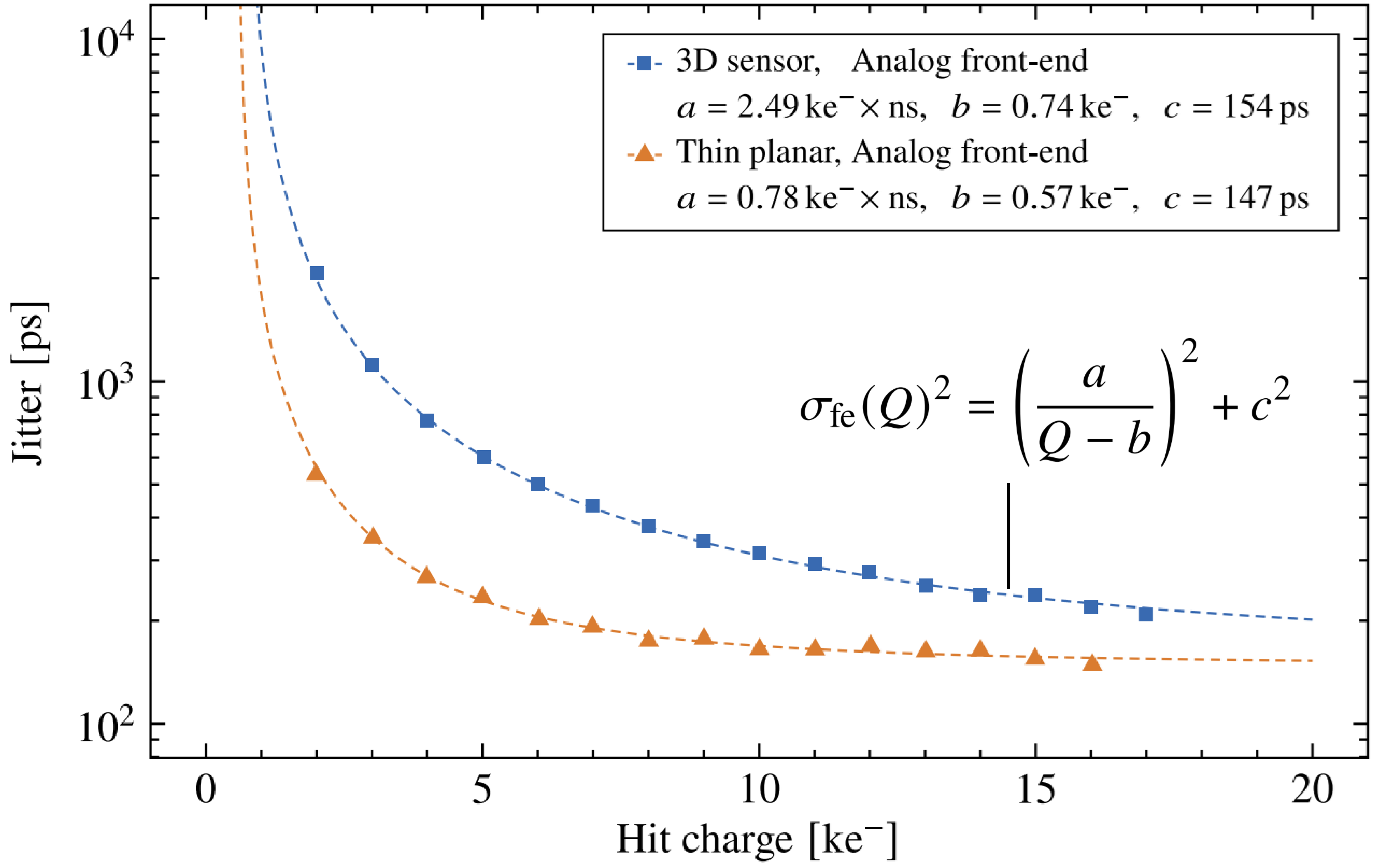
Pixel capacitance and front-end resolution

K. Heijhoff *et al* 2021 *JINST* **16** P08009 [DOI: 10.1088/1748-0221/16/08/P08009]

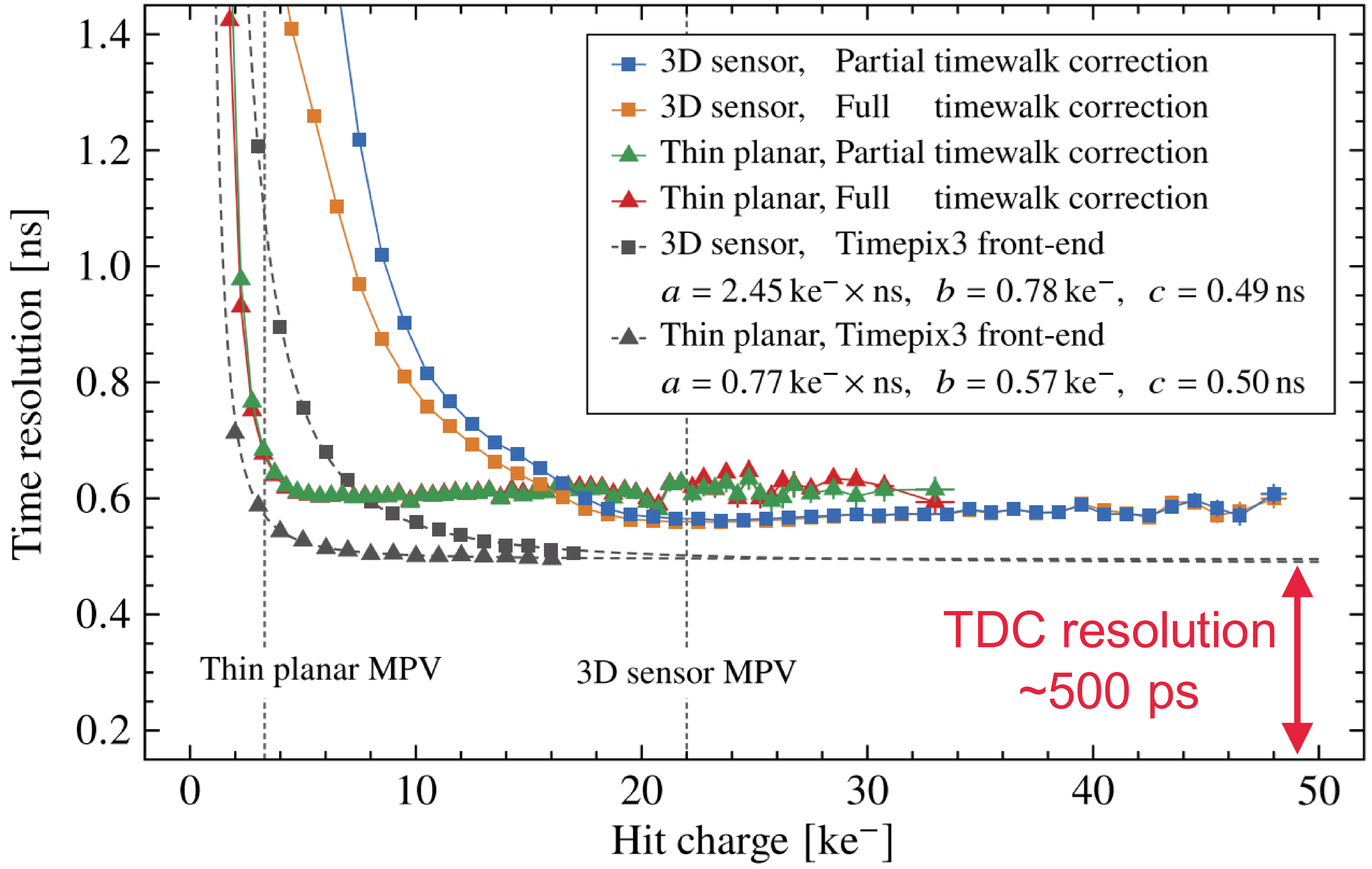
- Higher input capacitance of 3D sensor leads to worse jitter at low signal charge
- 3D sensor still has better time resolution because of 6x higher signal charge



Analog front-end jitter



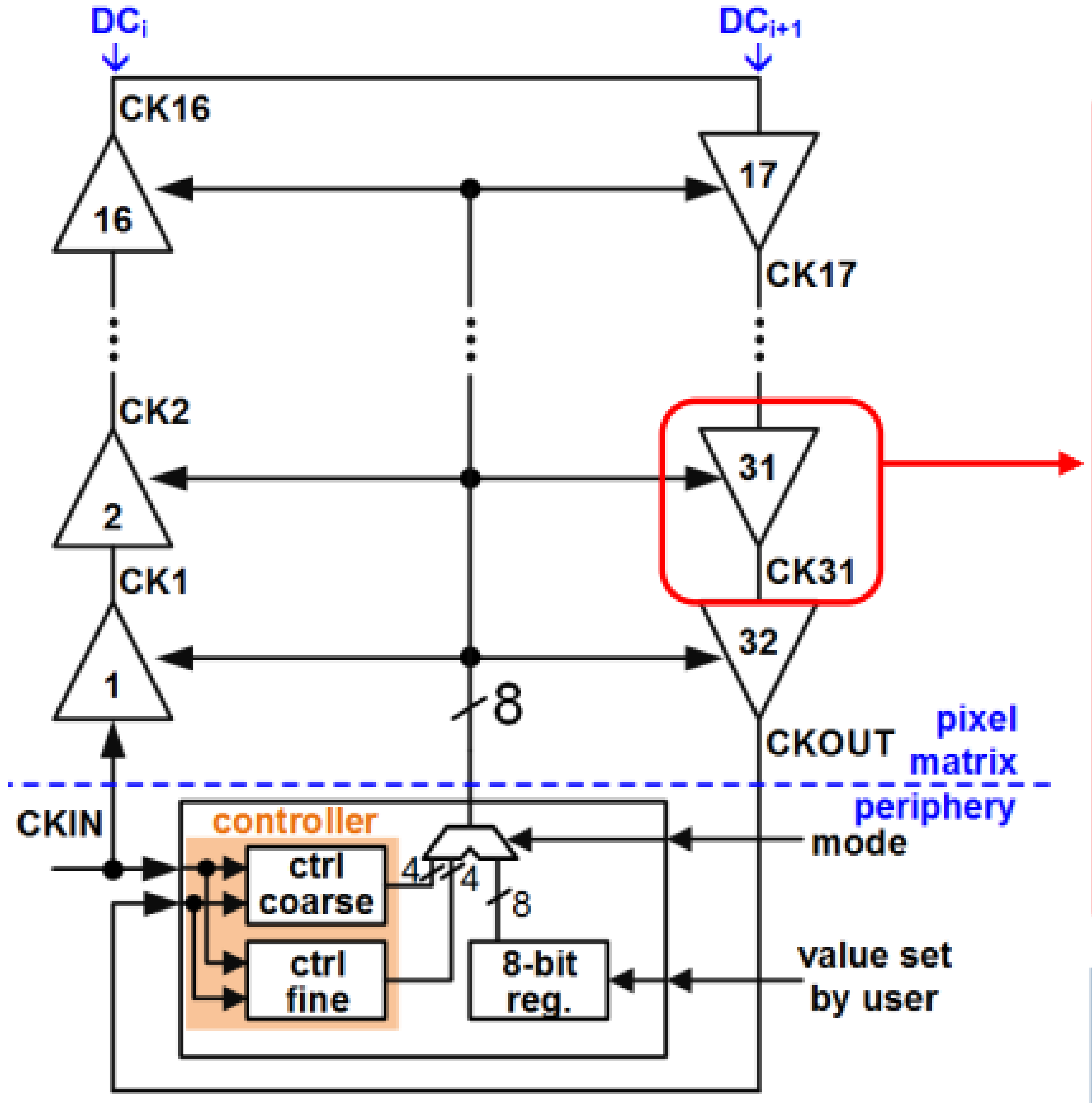
Total time resolution

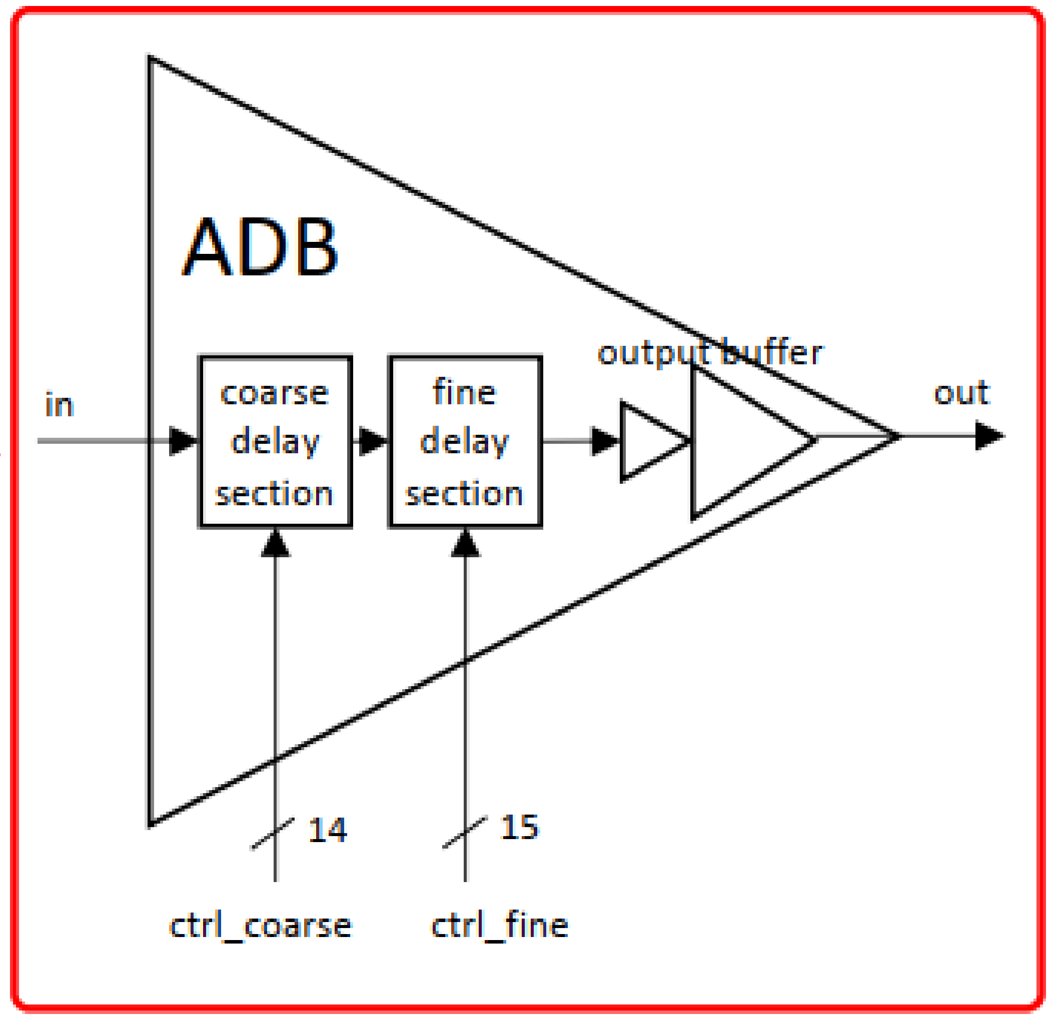


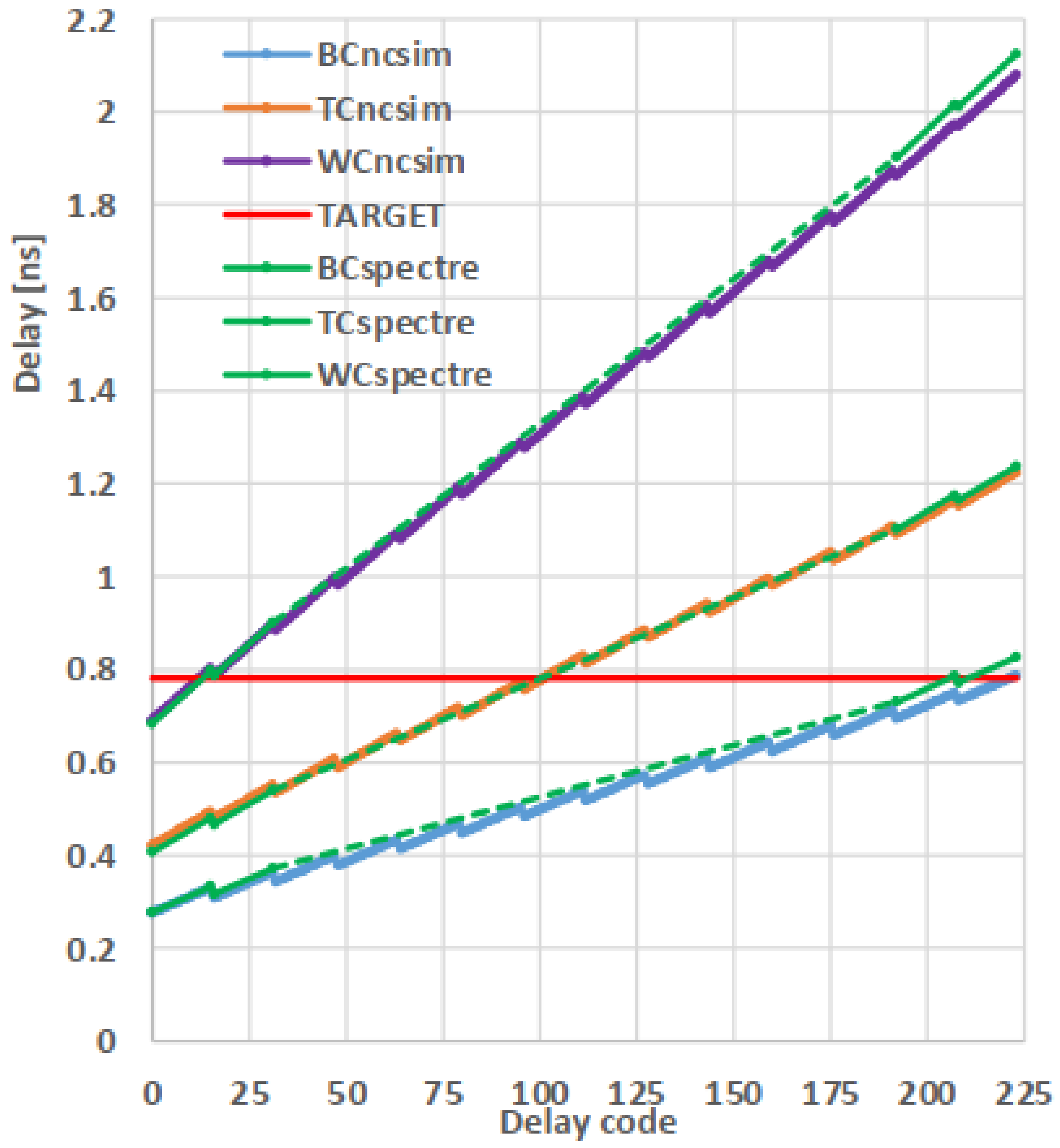
iWoRID 2018
X. Llopart et al 2019 JINST 14 C01024

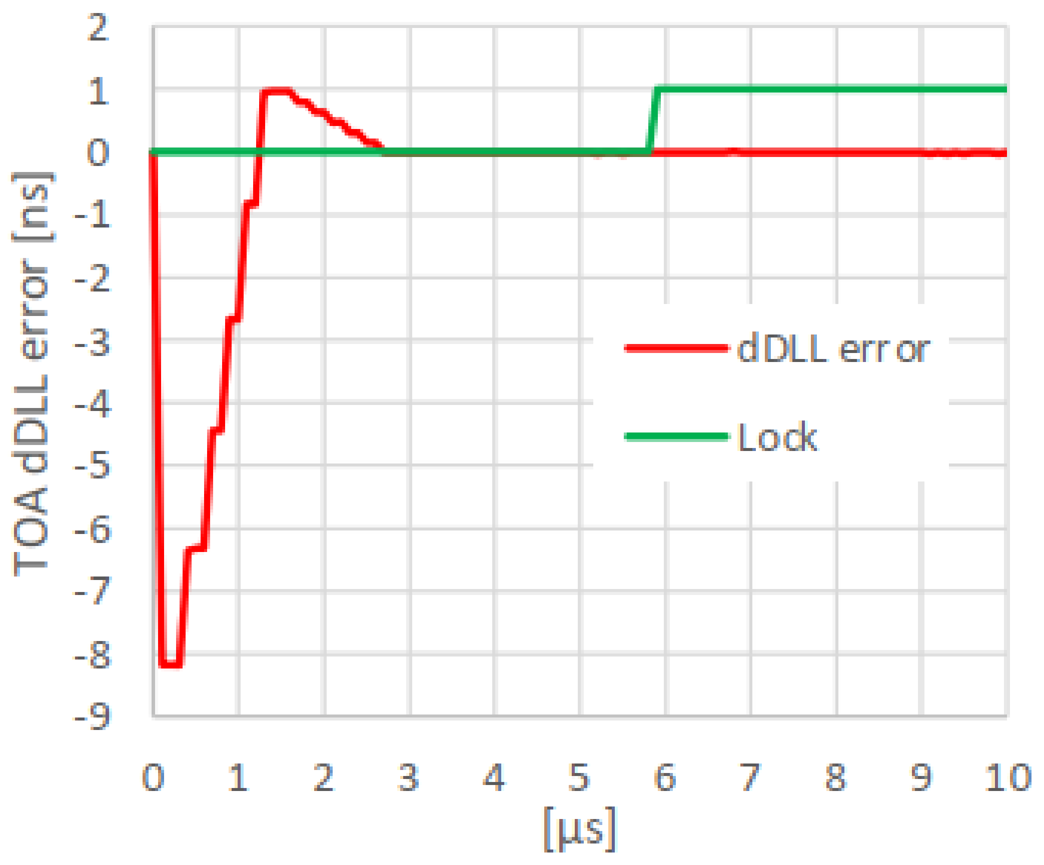
Clock distribution – Column digital locked look (DLL)

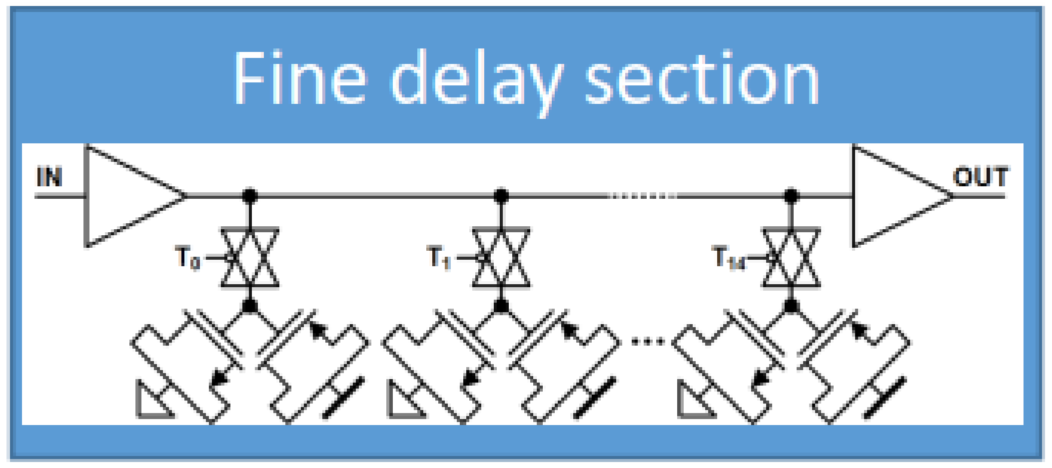
- The column DLL distributes the clock along the columns
- The adjustable delay buffers (ADBs) precisely define the clock phase in each pixel group
- Controller tunes the total delay to 25 ns
- Possible to set the delay manually
- Individual ADB stations can be bypassed

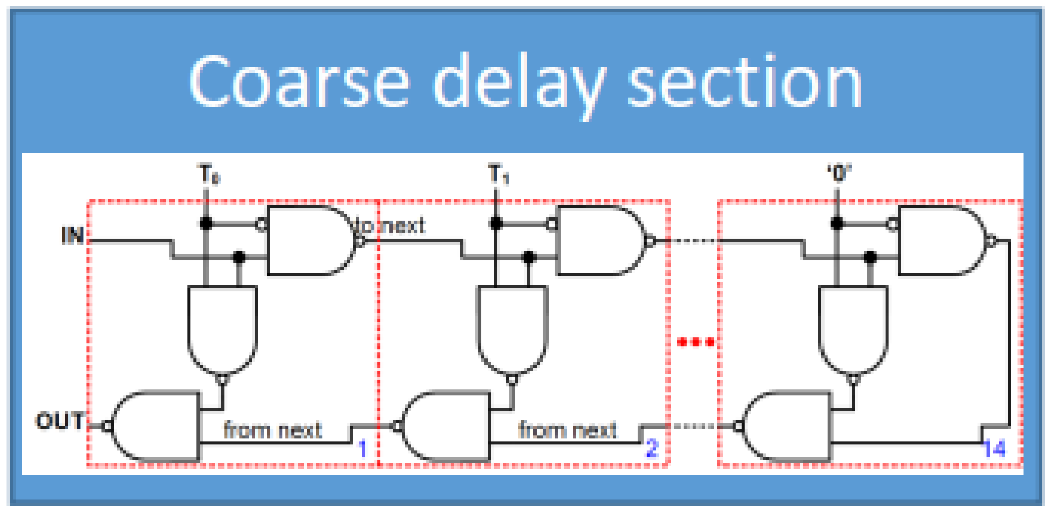










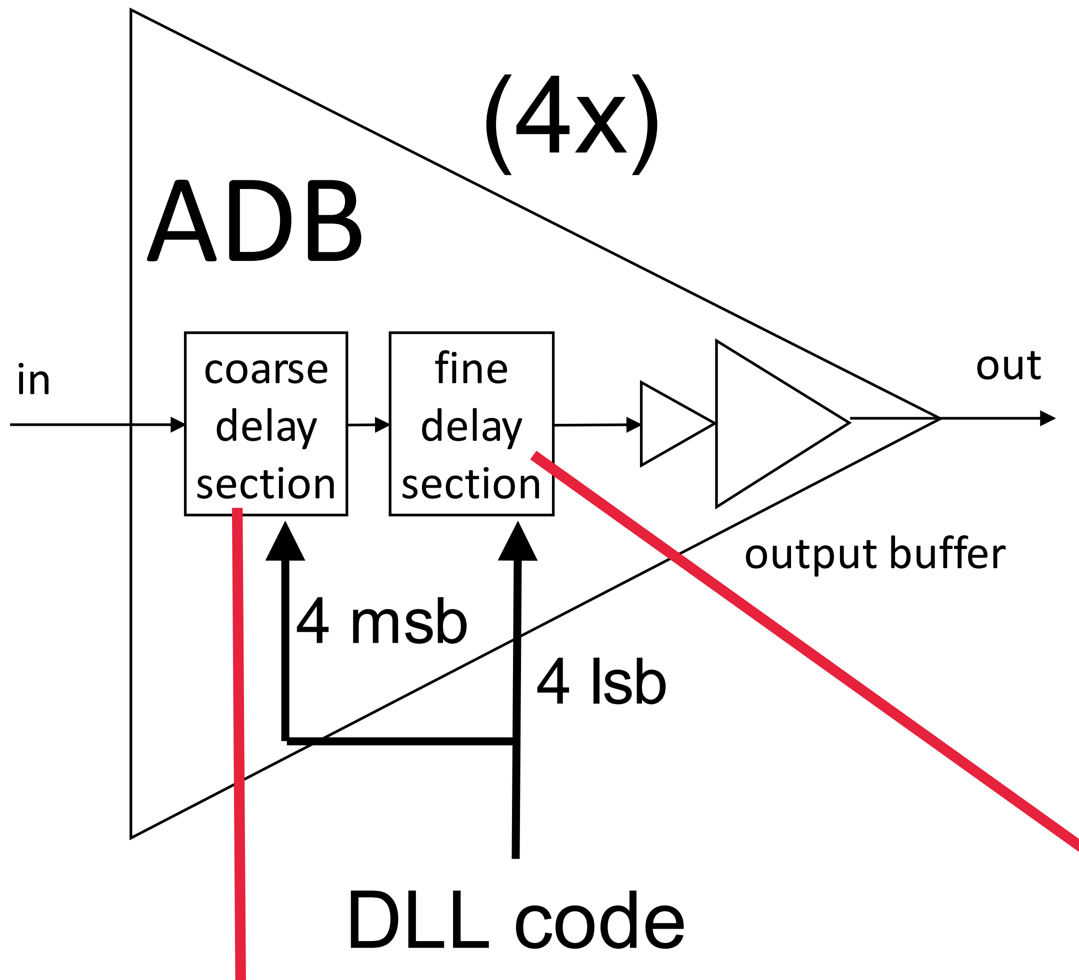


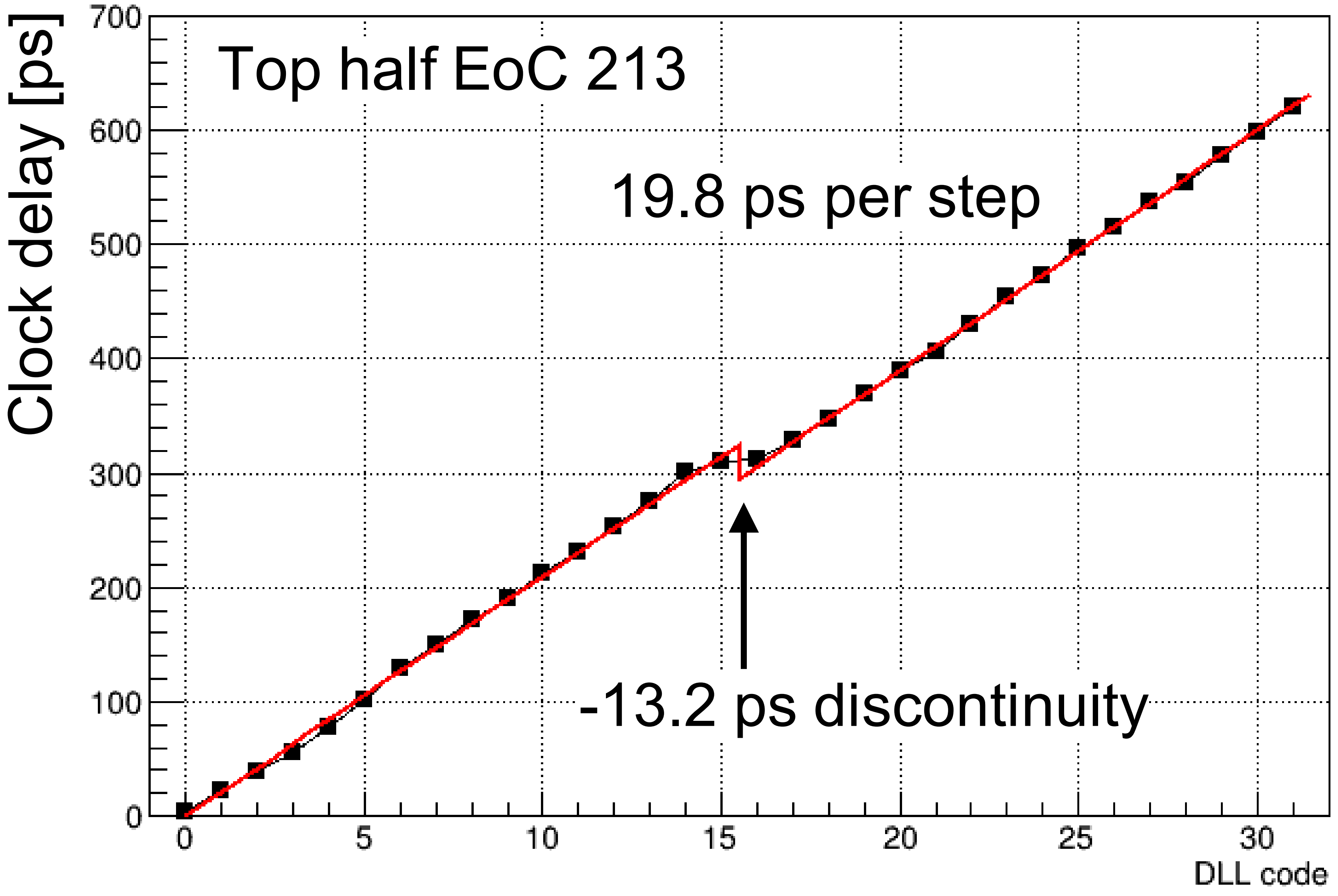
~22.7 mW/cm² to distribute a 40 MHz clock with a 100 ps$_{rms}$

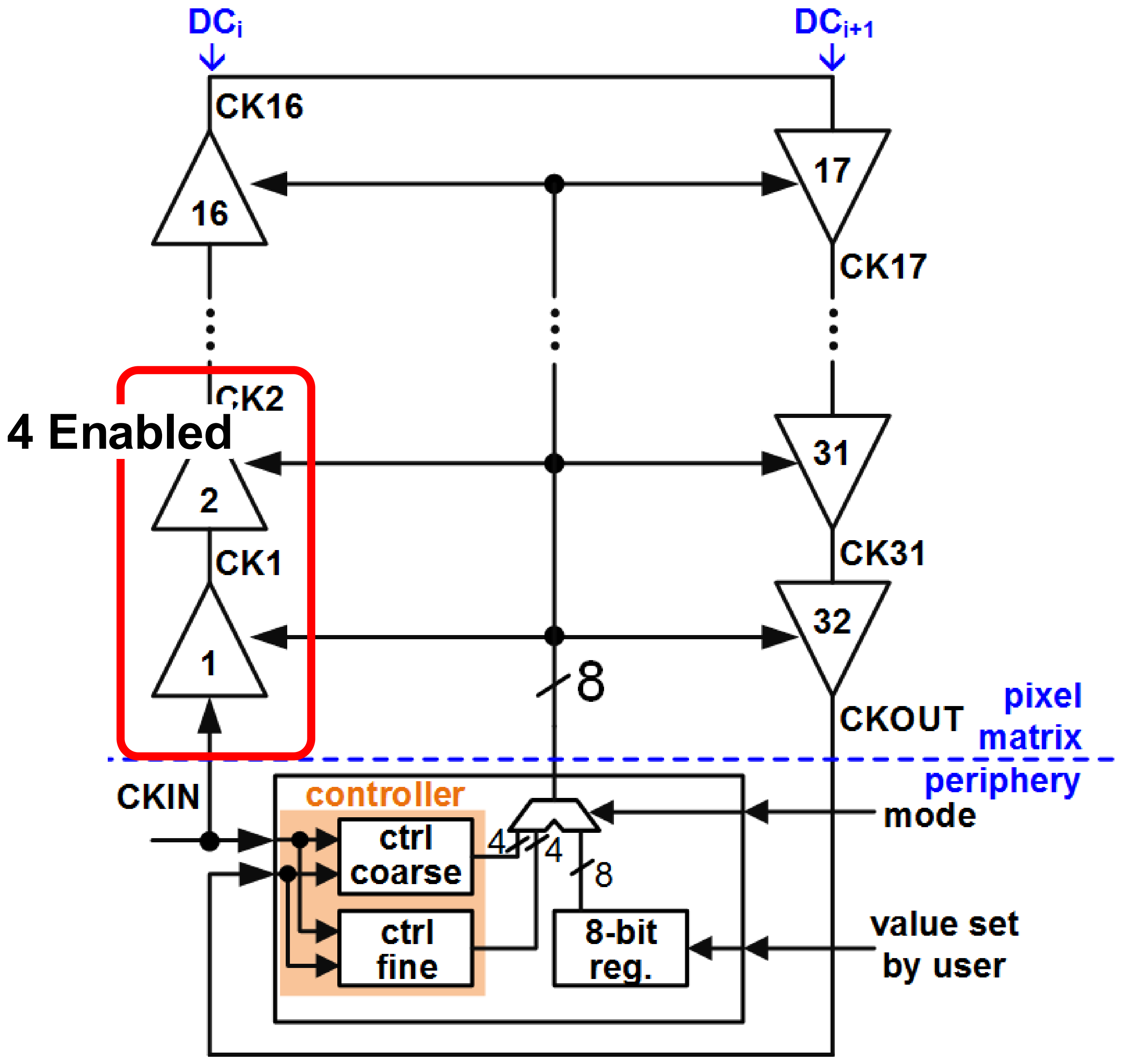
Nikhef

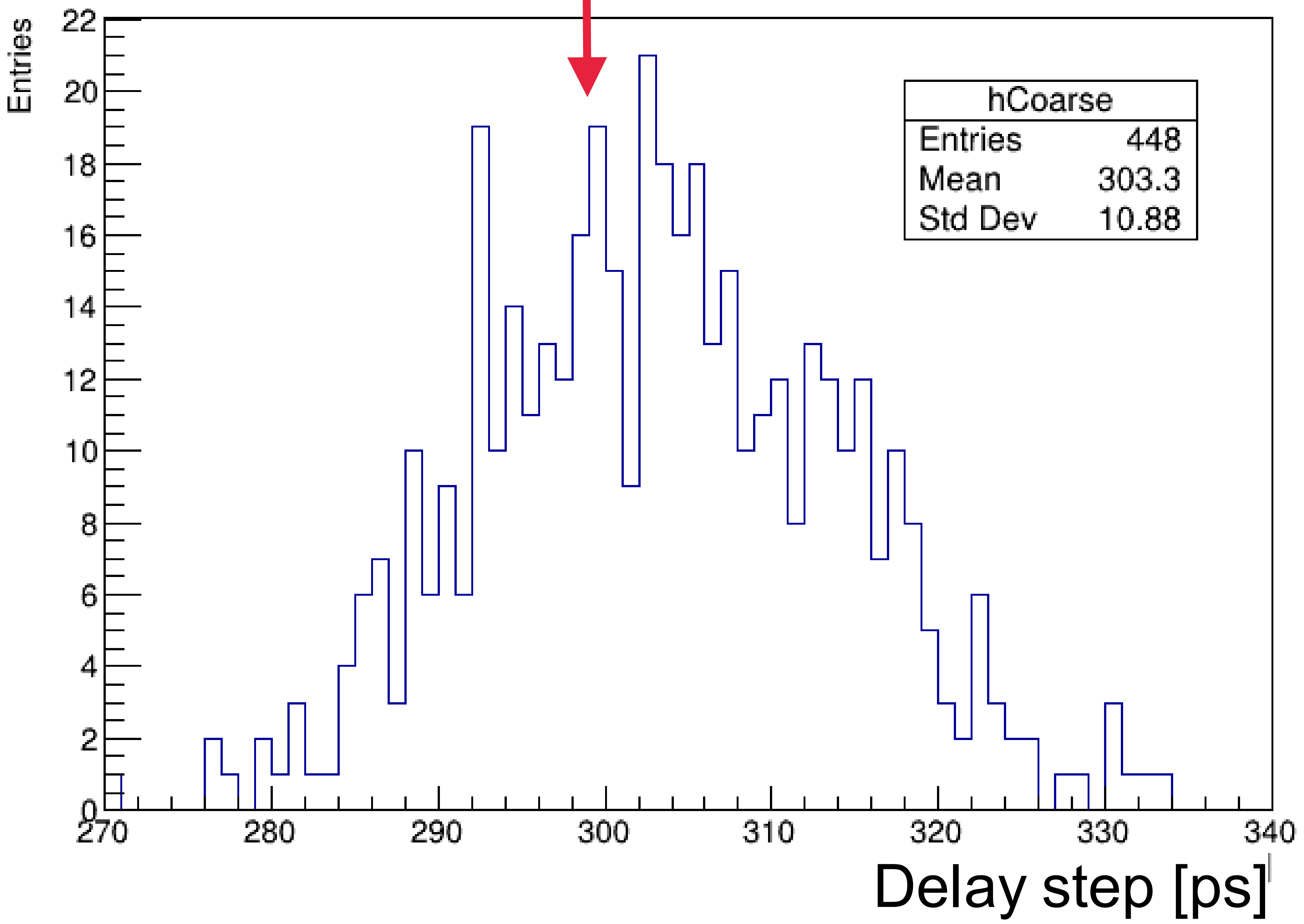
Analog delay buffer (ADB) calibration

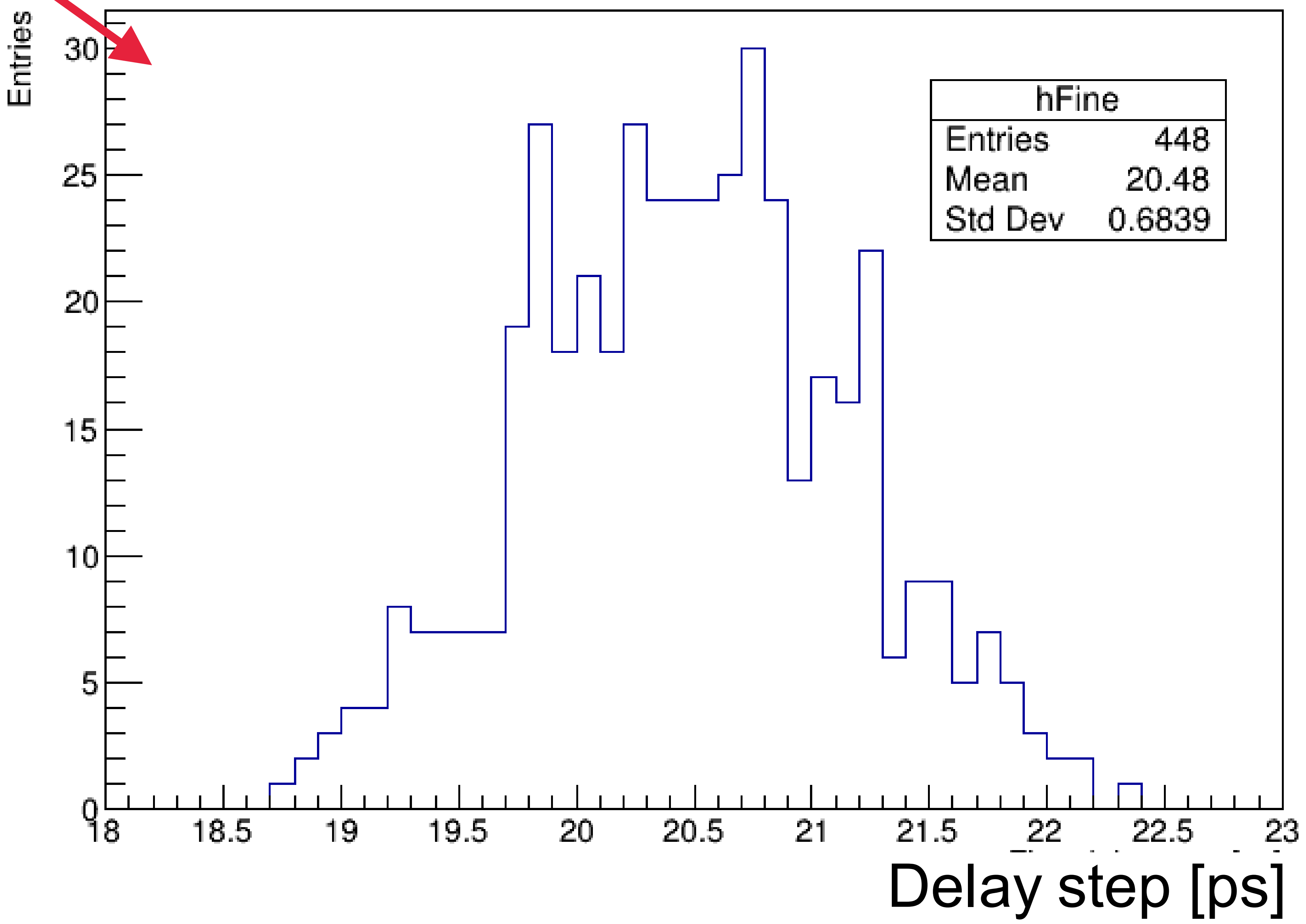
- Here the ADB stations are used to control the phase of analog test pulses
- Mean delay step size 20.5 ps (5.1 ps per ADB station)





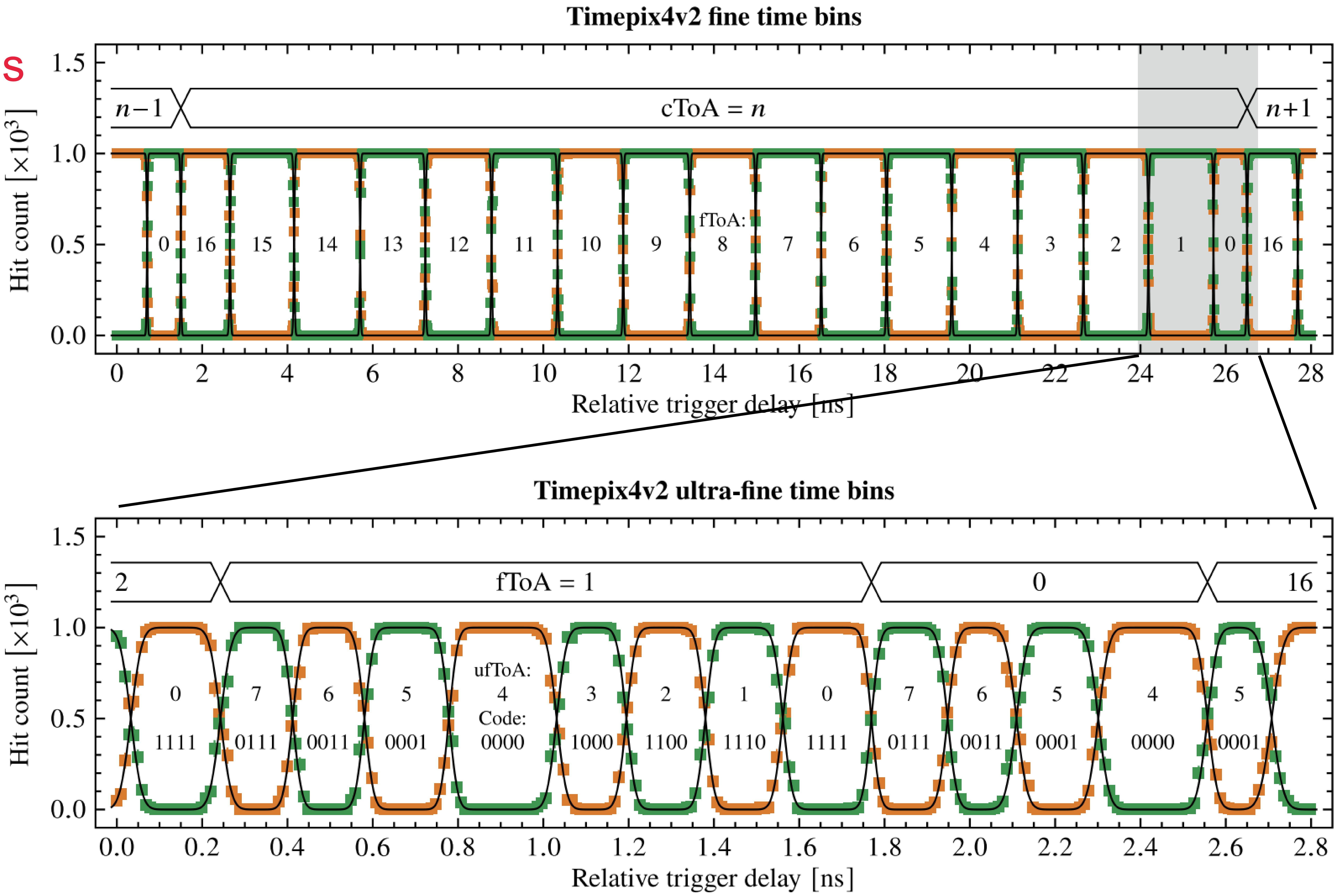






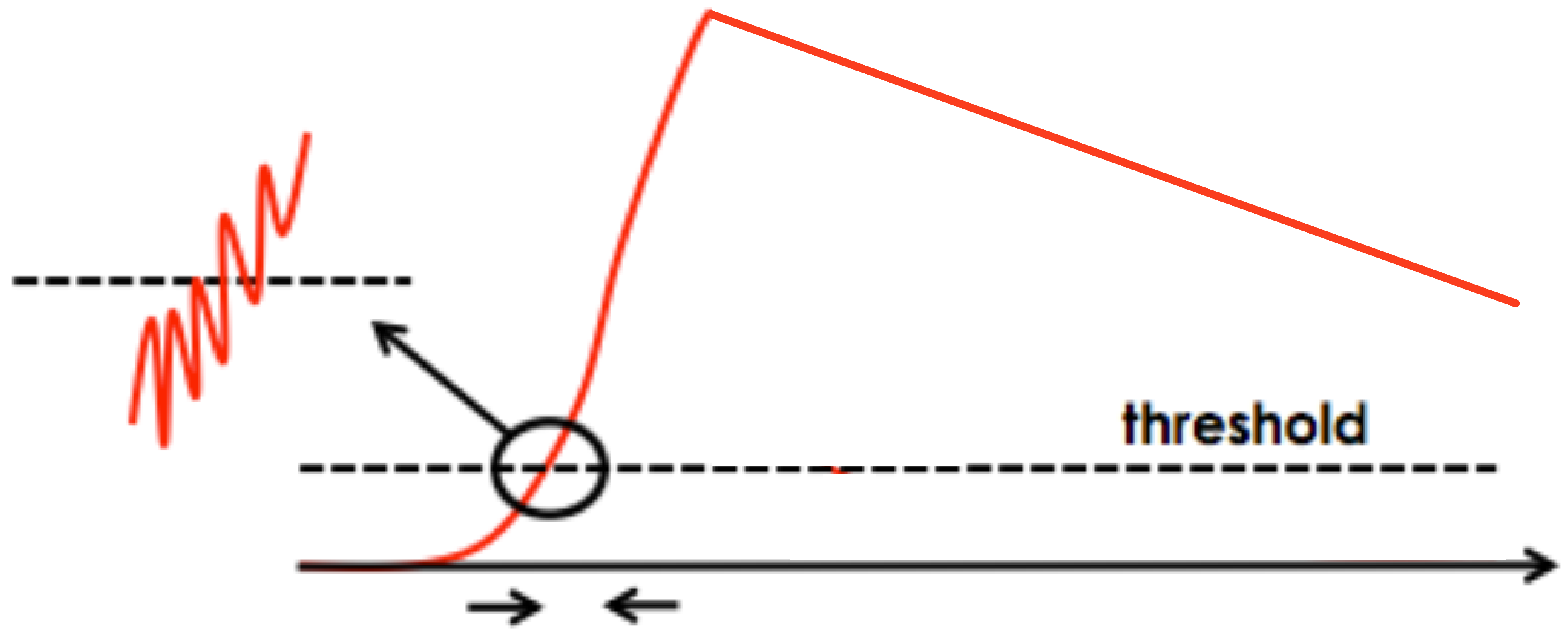
Timepix4 TDC bins

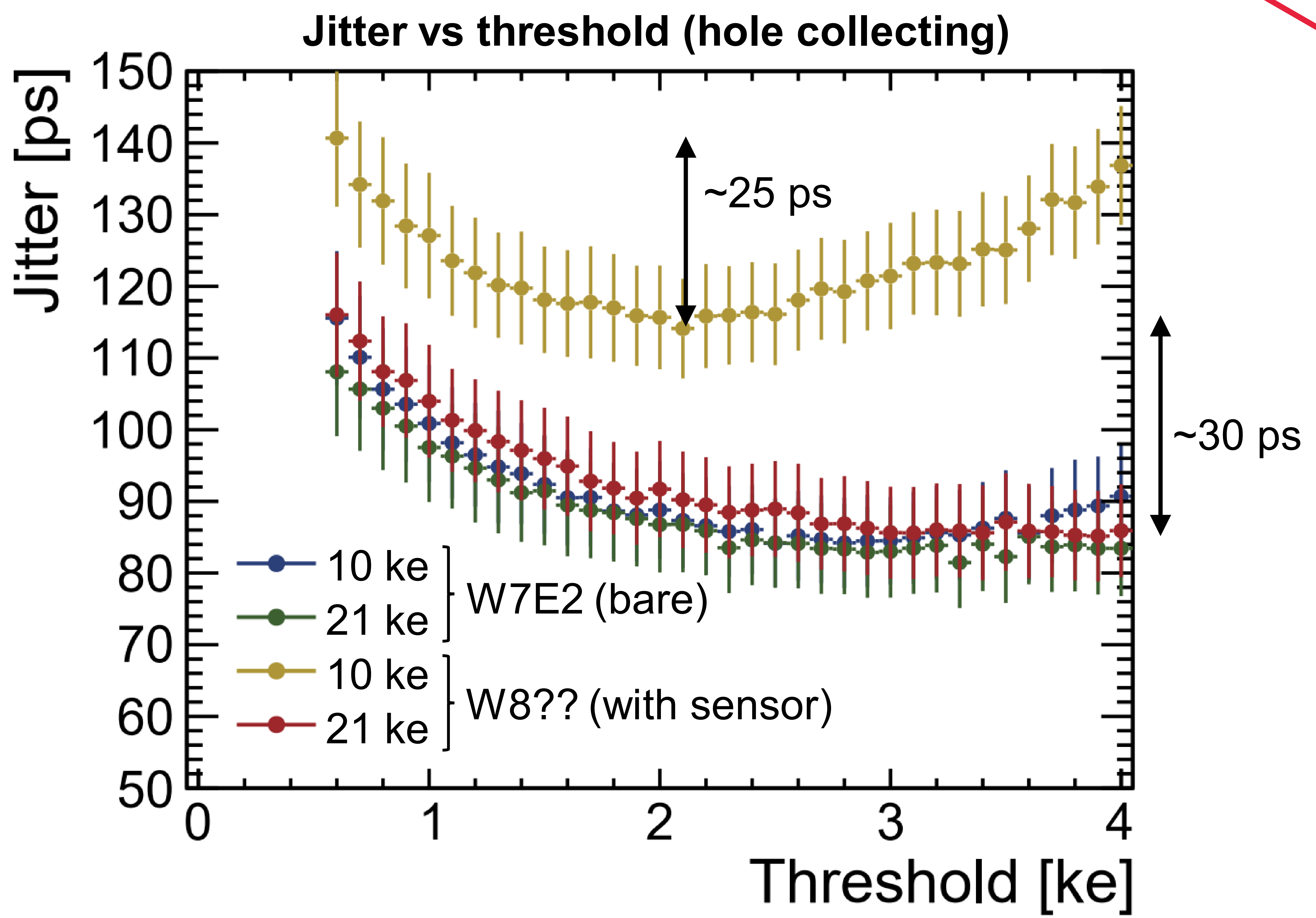
- Time bins measured using digital pixel inputs
- Timepix4v2

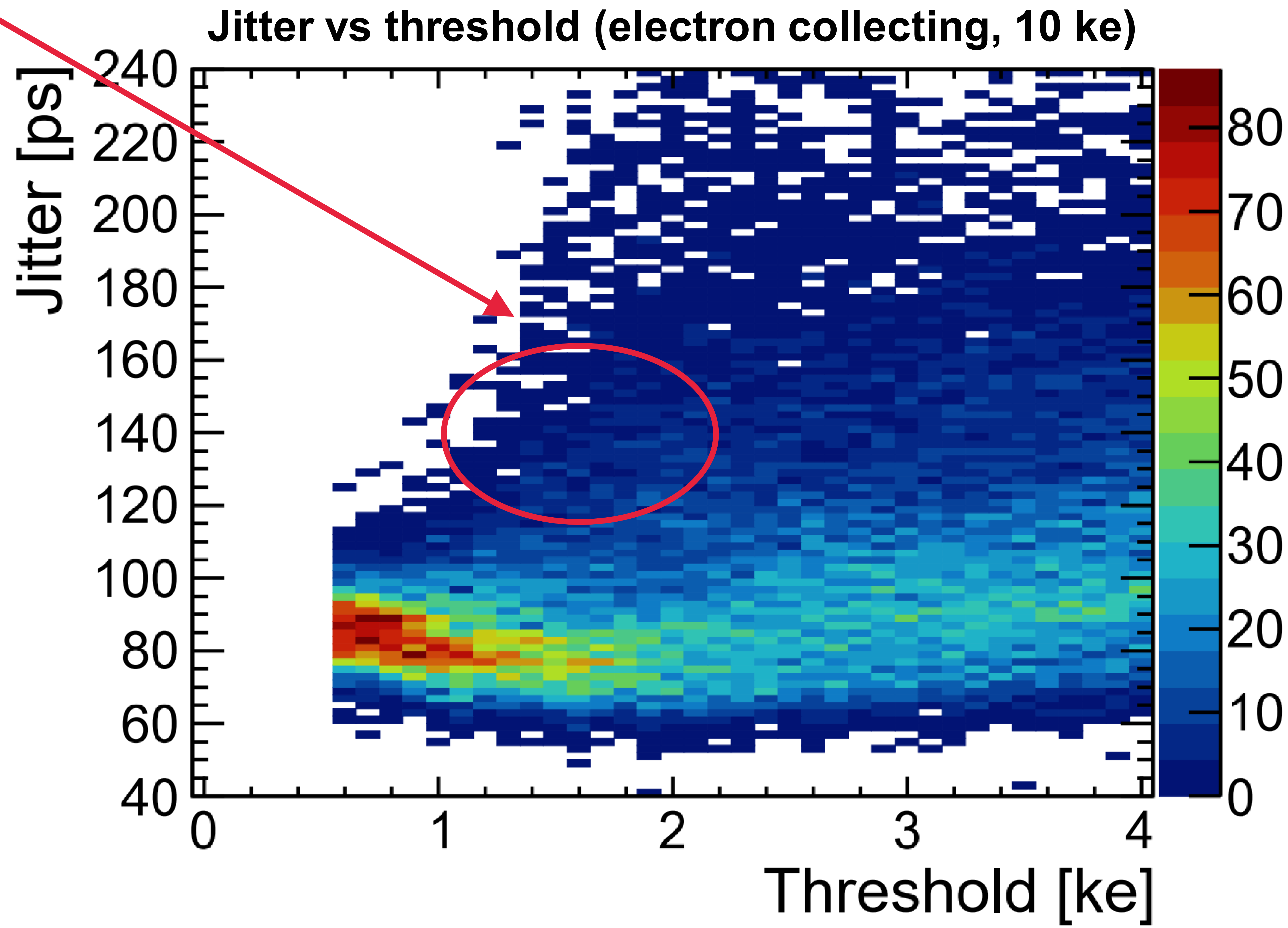


Timepix4 – Jitter vs threshold

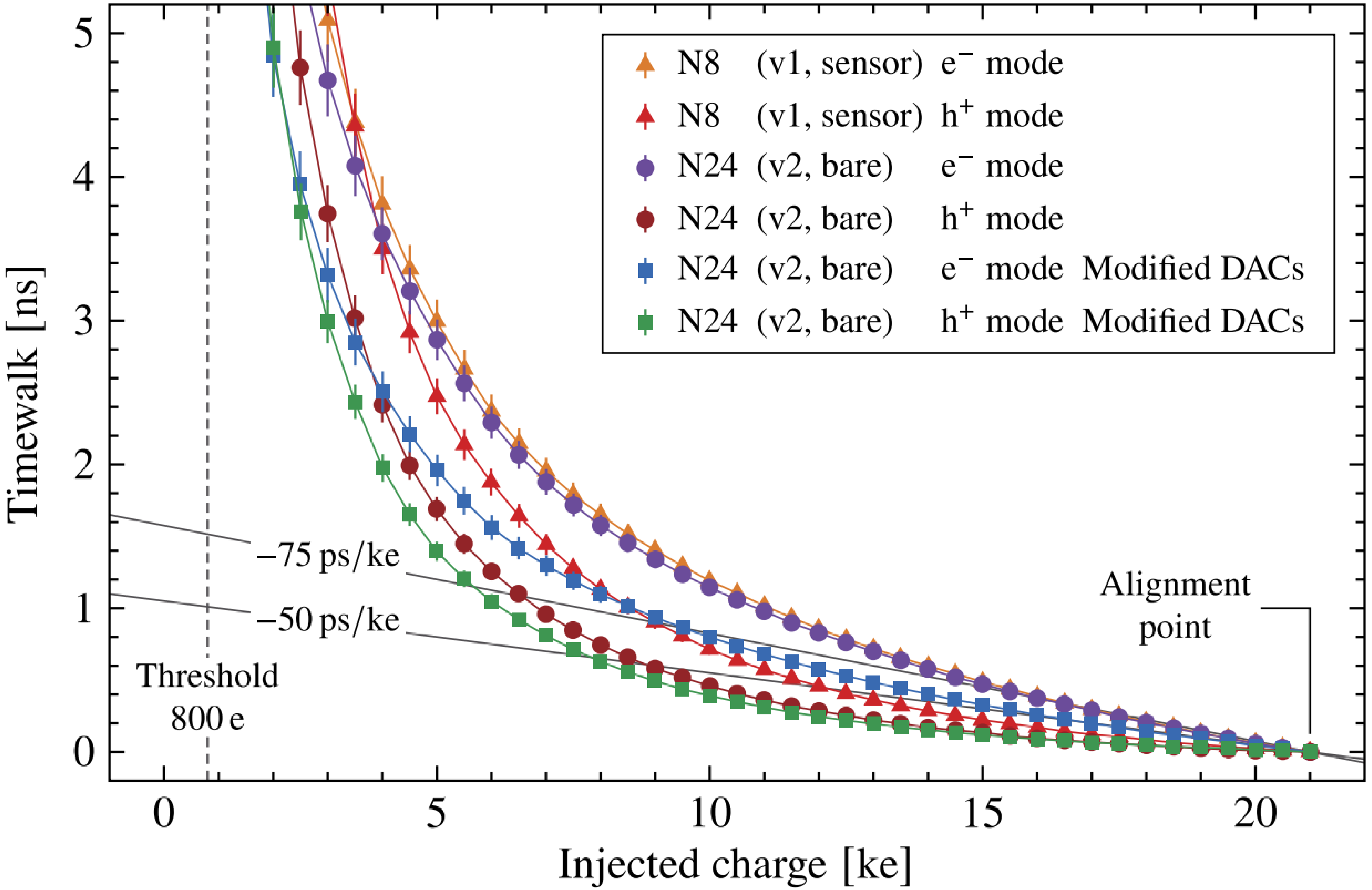
- Jitter depends on threshold
- Tail at high thresholds in electron-collecting mode not understood



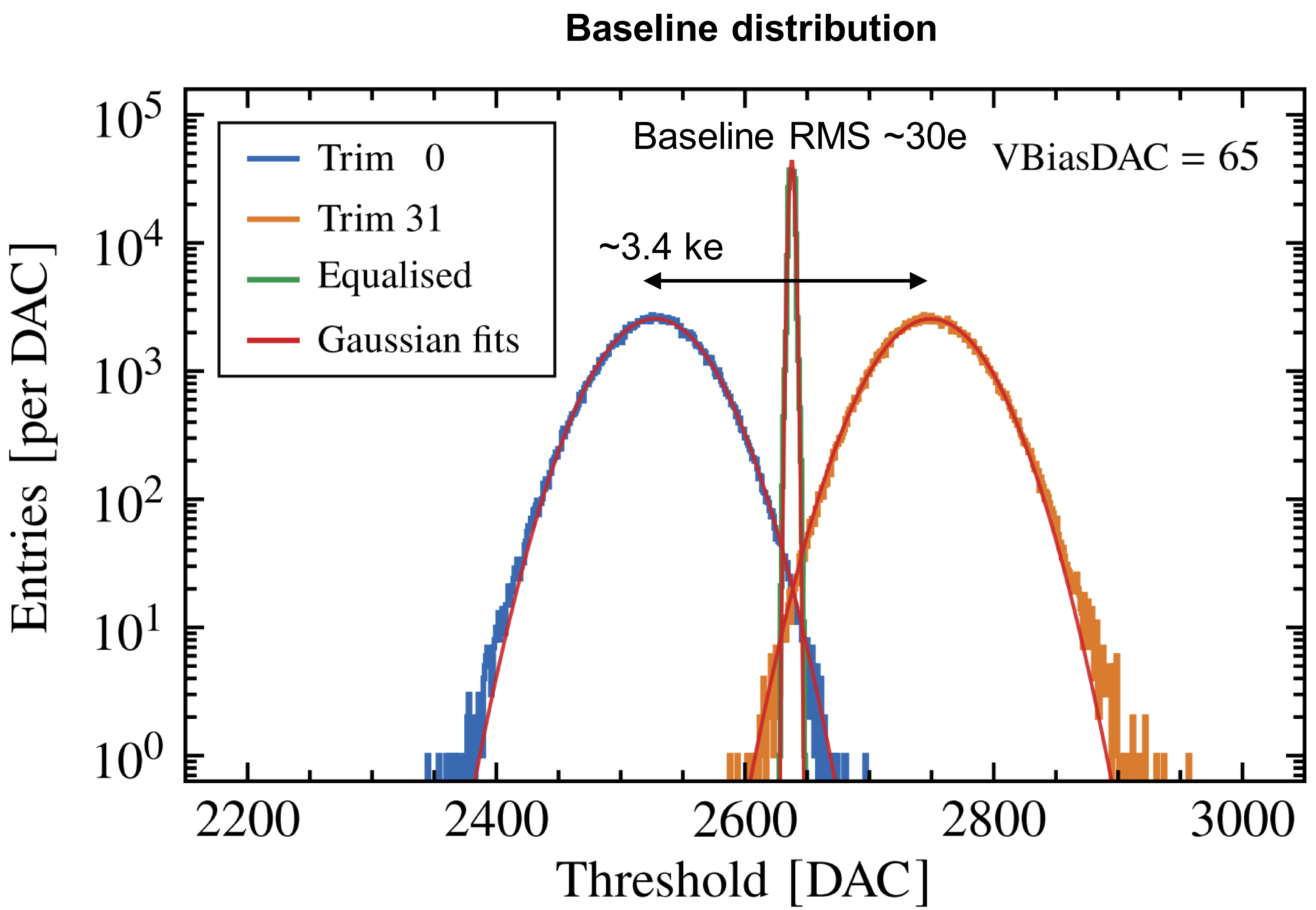




Timepix4 Timewalk measured with test pulses

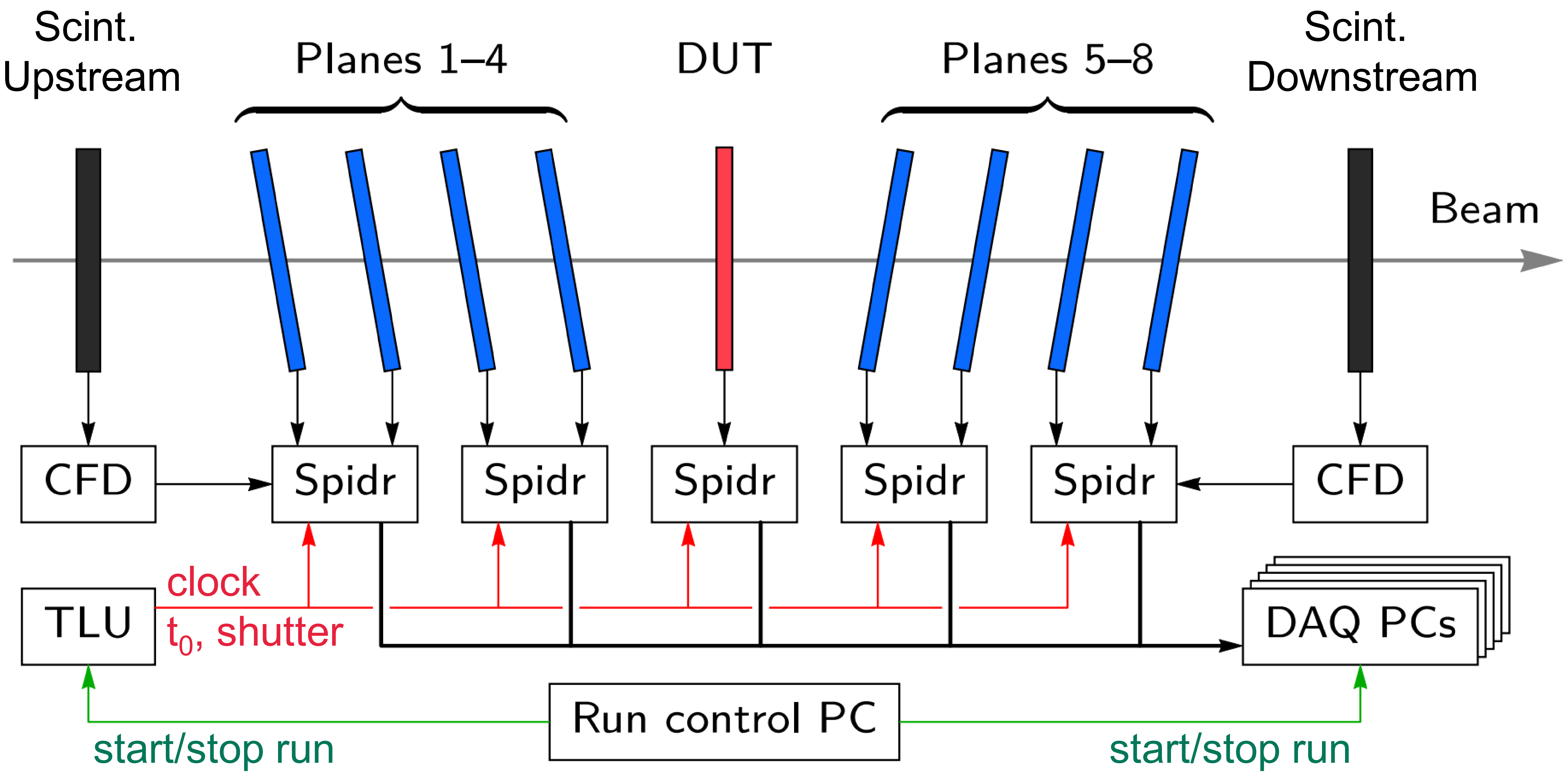


Timepix4 pixel equalisation



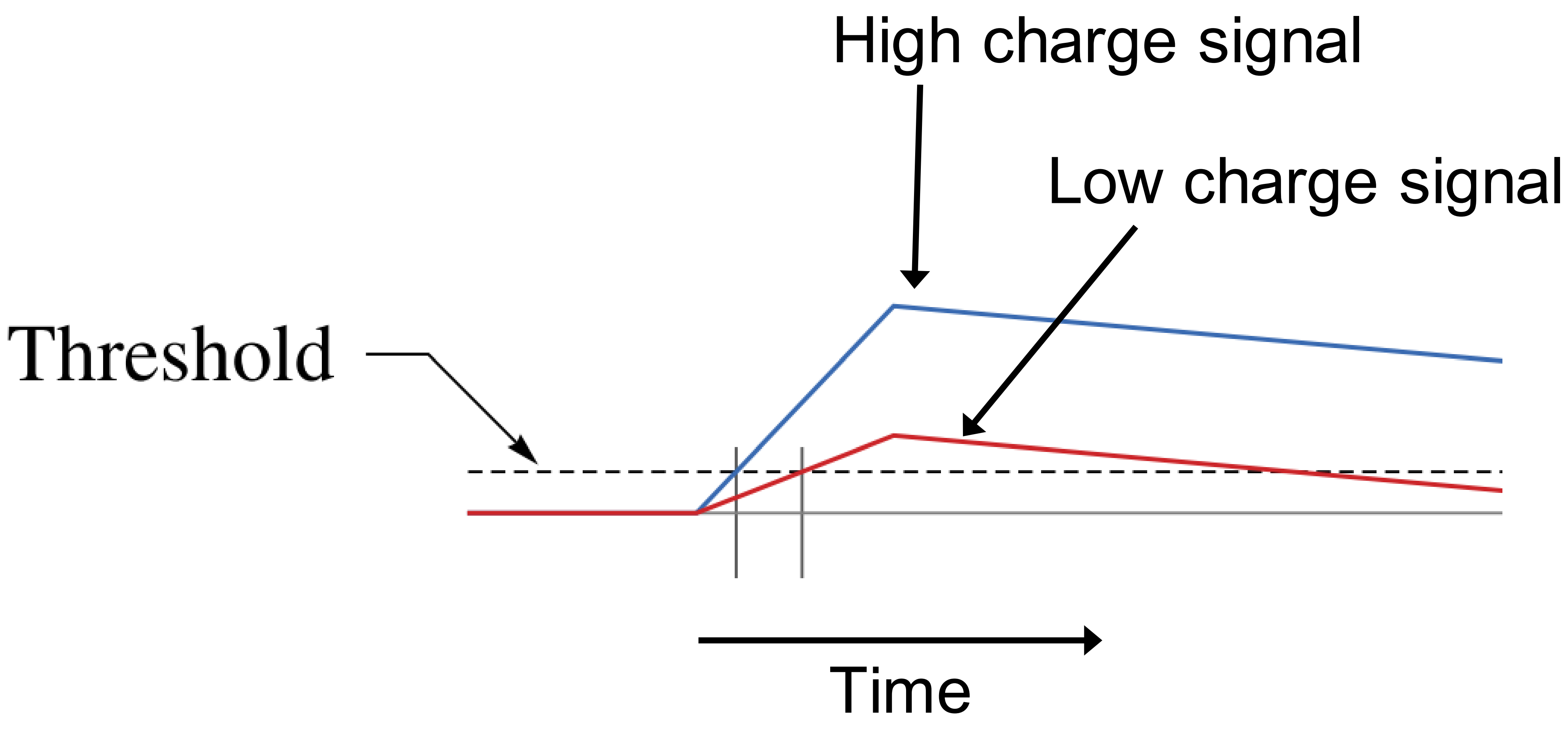
Timepix3 telescope

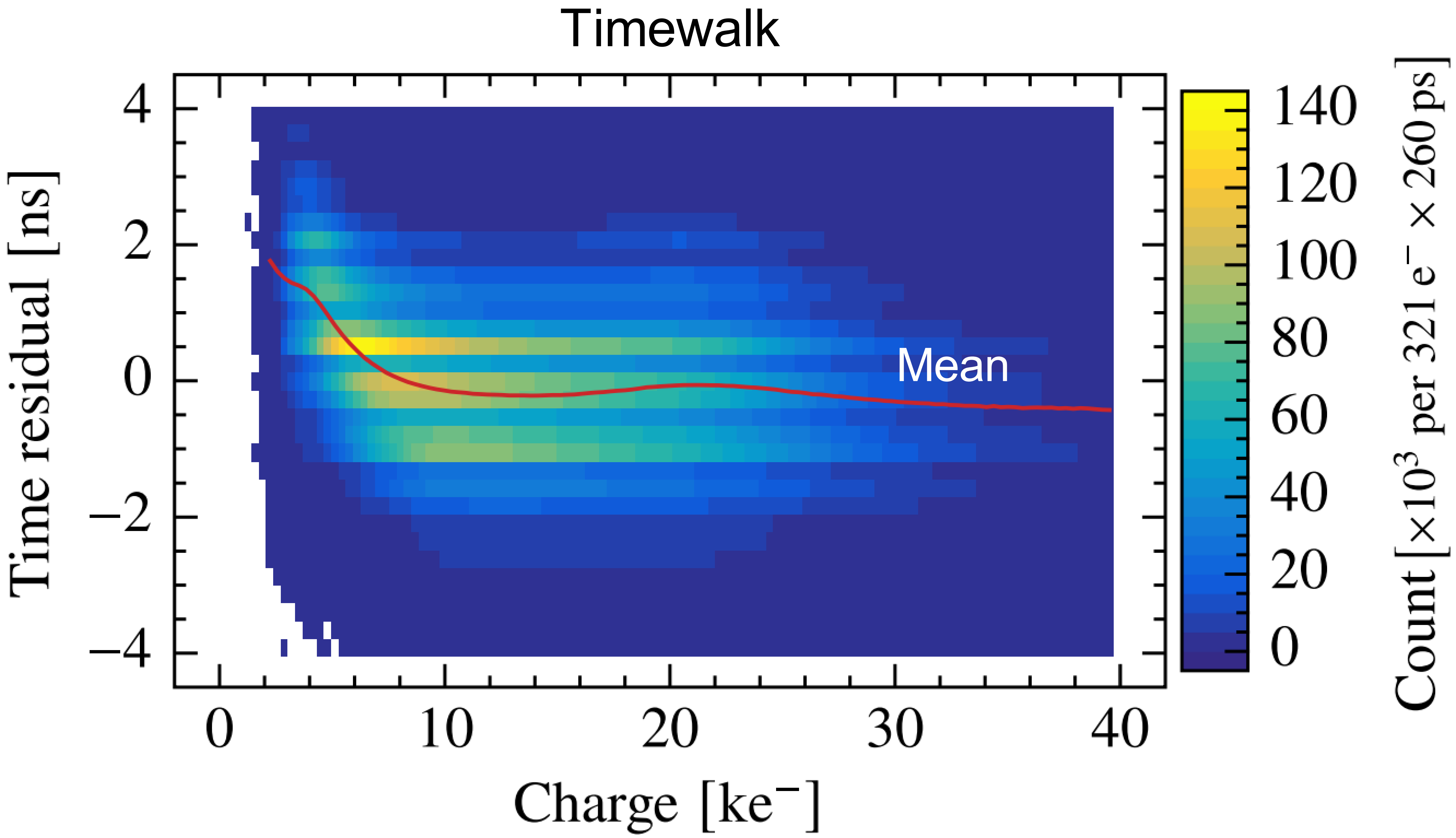
- Eight planes with Timepix3 + sensors
- Planes rotated to optimise spatial resolution
- Scintillators provide a reference time
- Constant fraction discriminators (CFDs) reduce timewalk effects
- All planes run on a common 40 MHz clock



Timewalk

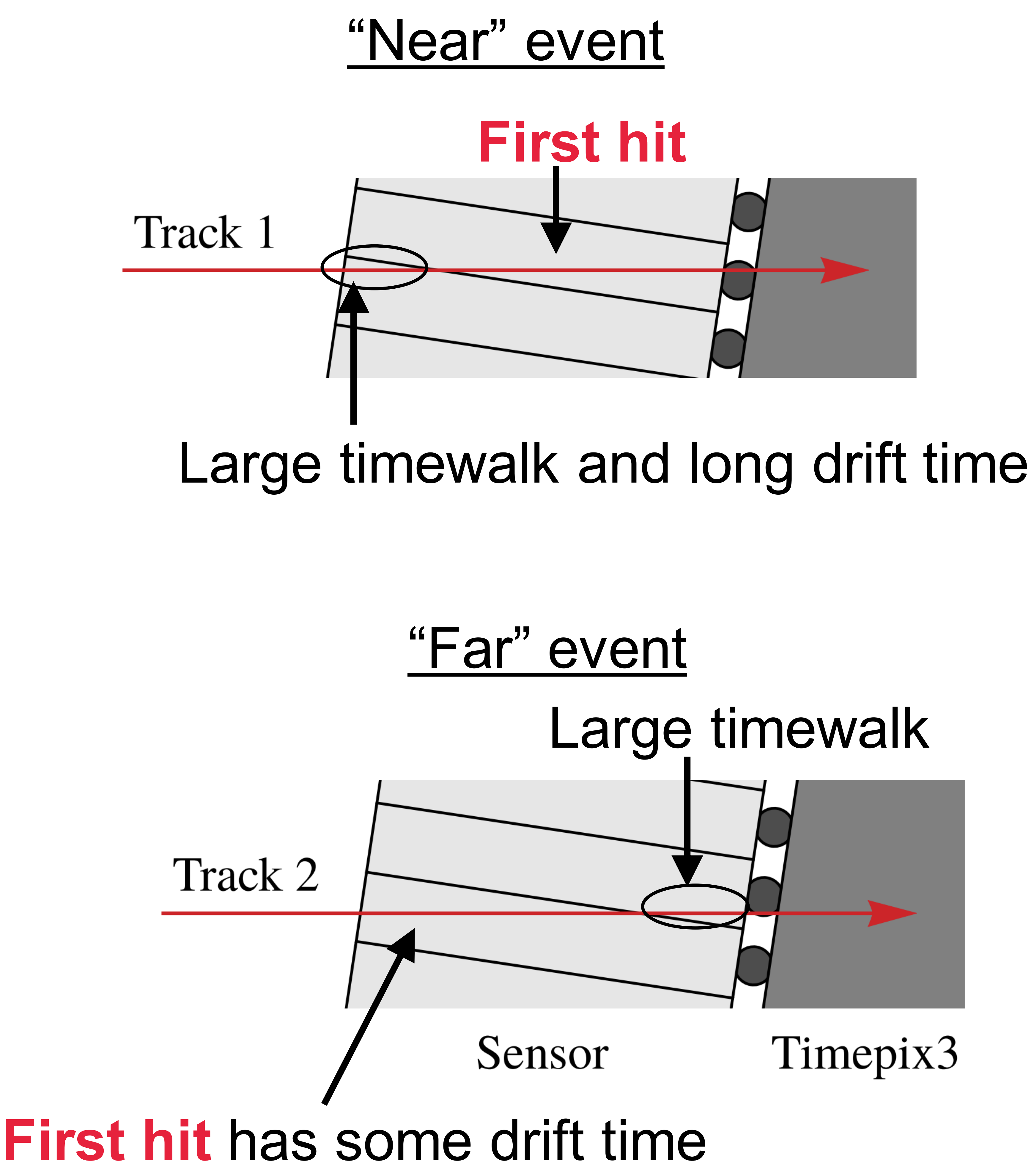
- Cluster time set by earliest hit in cluster: cuts out most timewalk
- Correction improves track resolution: $\sigma(\text{track}) = 438\text{ ps} \rightarrow 415\text{ ps}$
- Atypical timewalk behaviour. A decreasing function of charge is expected.

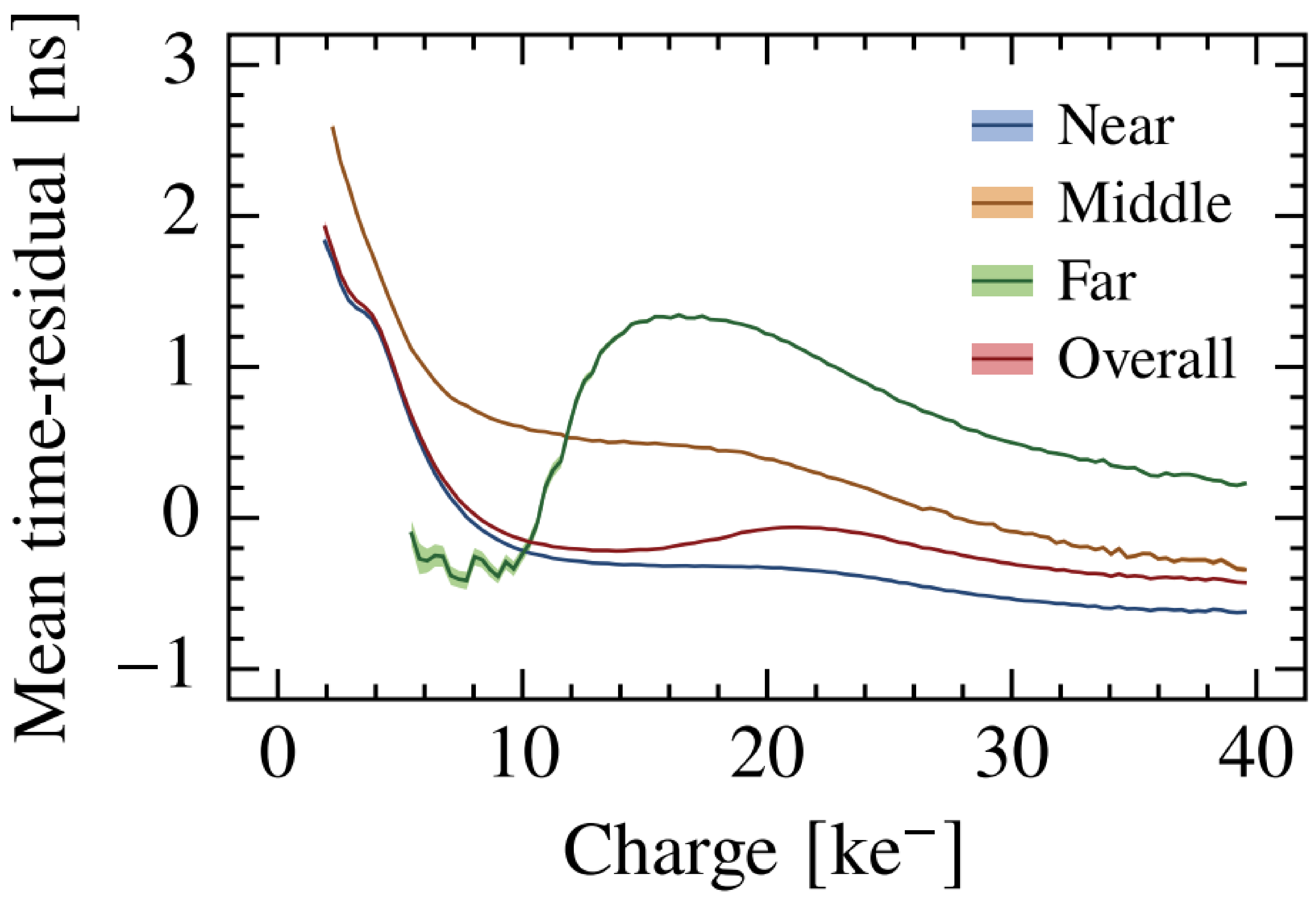


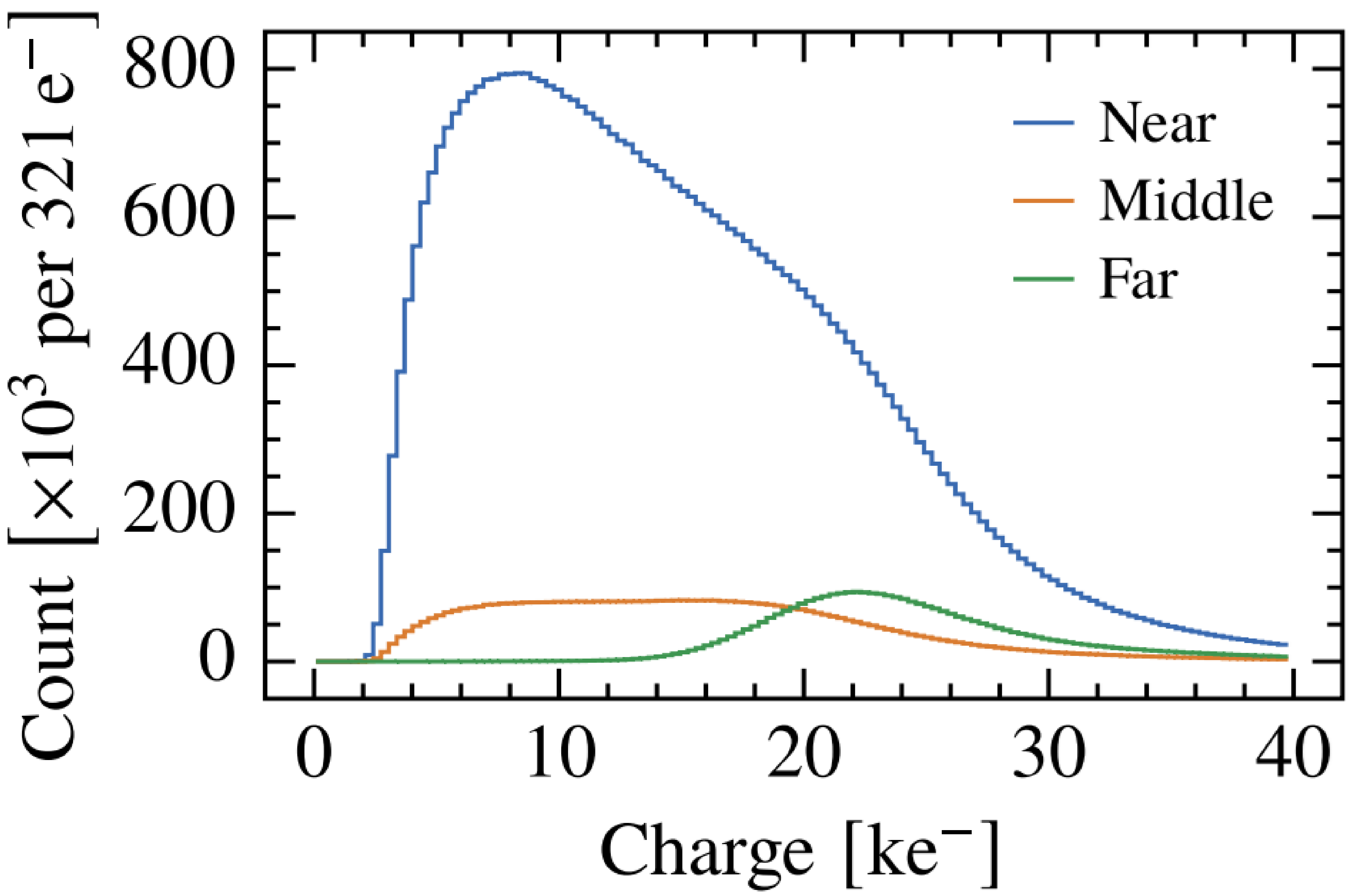


Timewalk and track topology

- Timewalk and sensor effects mixed by track topology

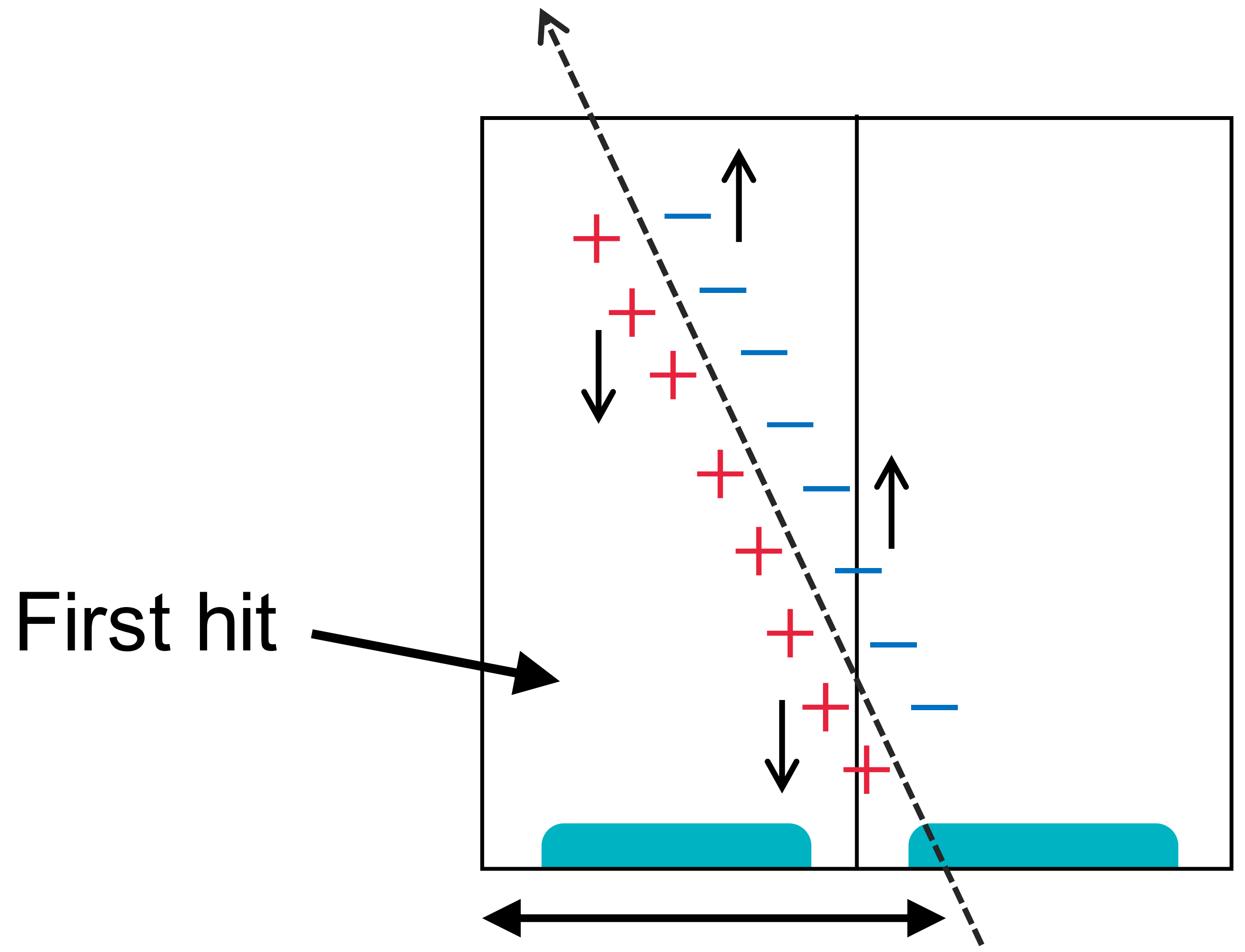


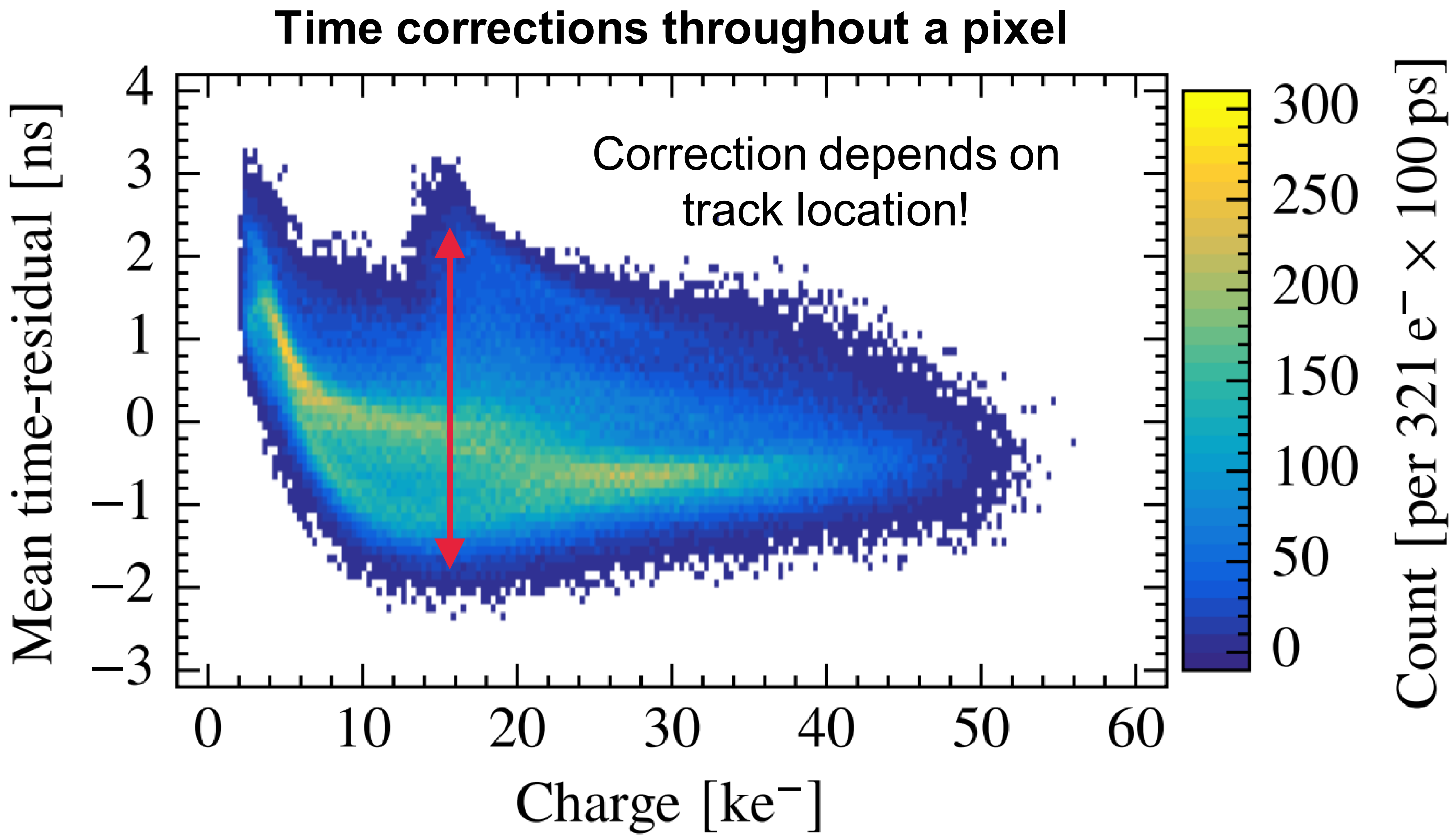


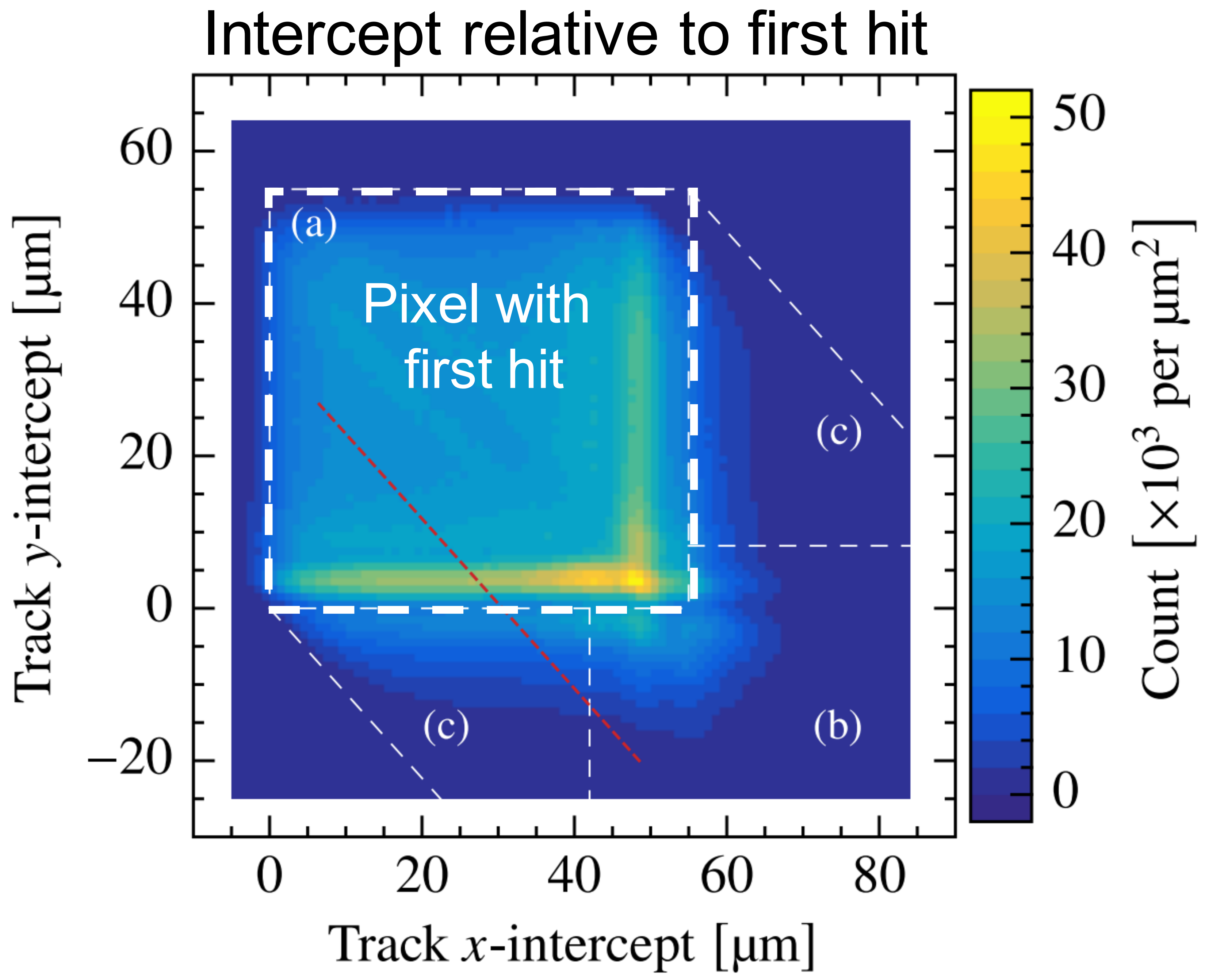


Timewalk and intercept correction

- Use both track intercept and charge to find correction in a lookup table
- Simultaneously corrects for timewalk and signal induction variations
- Improves track time resolution: $\sigma(\text{track}) = 438\ \text{ps} \rightarrow 385\ \text{ps}$



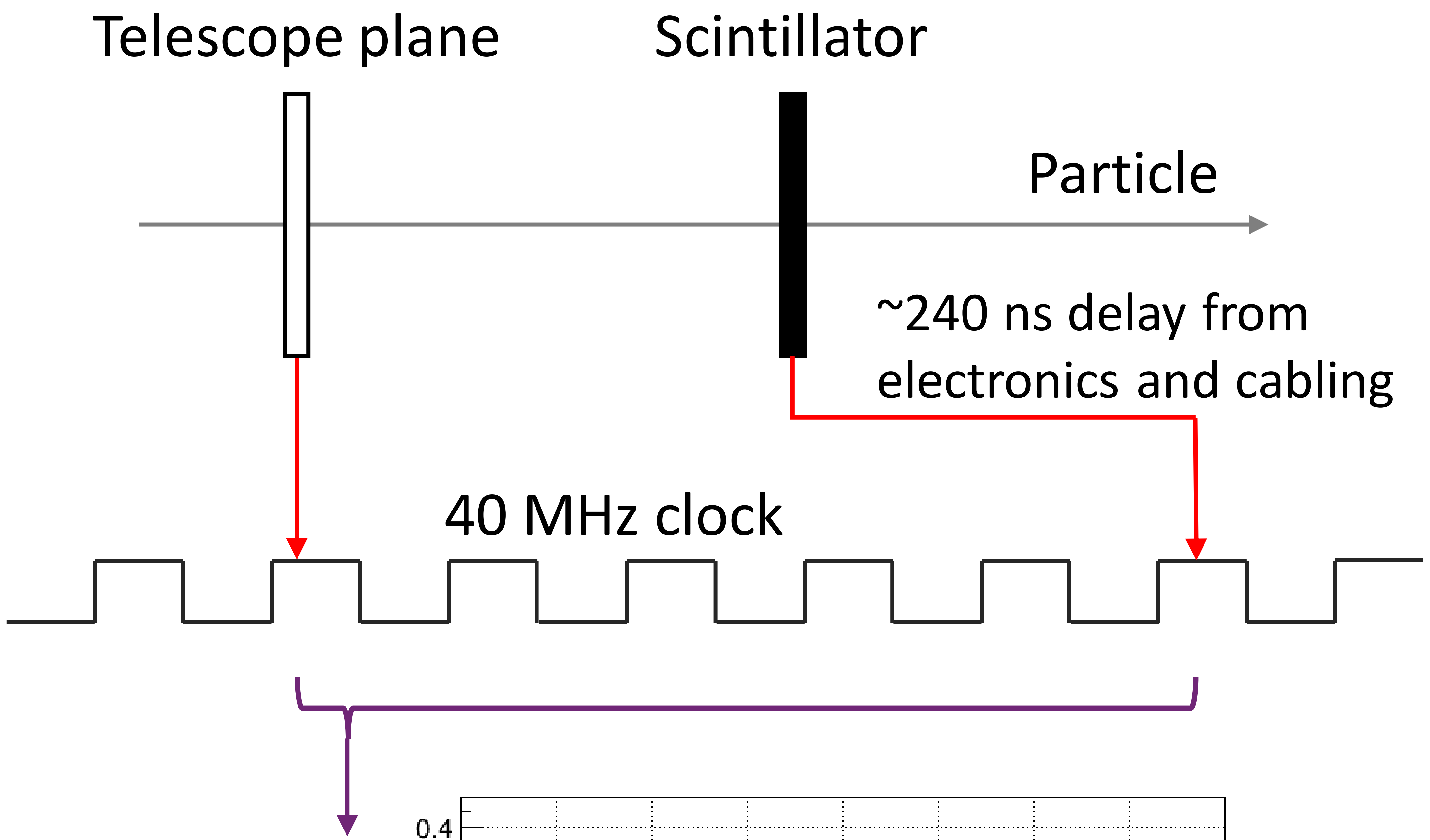


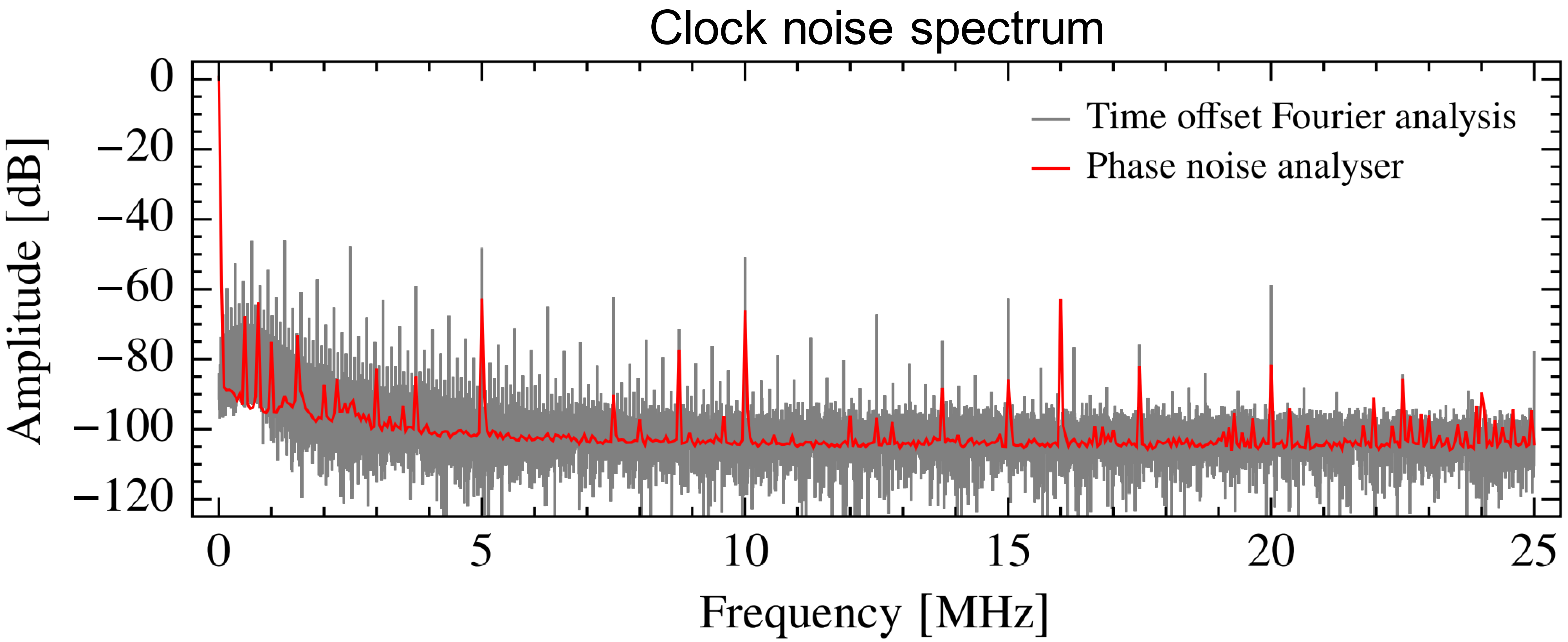


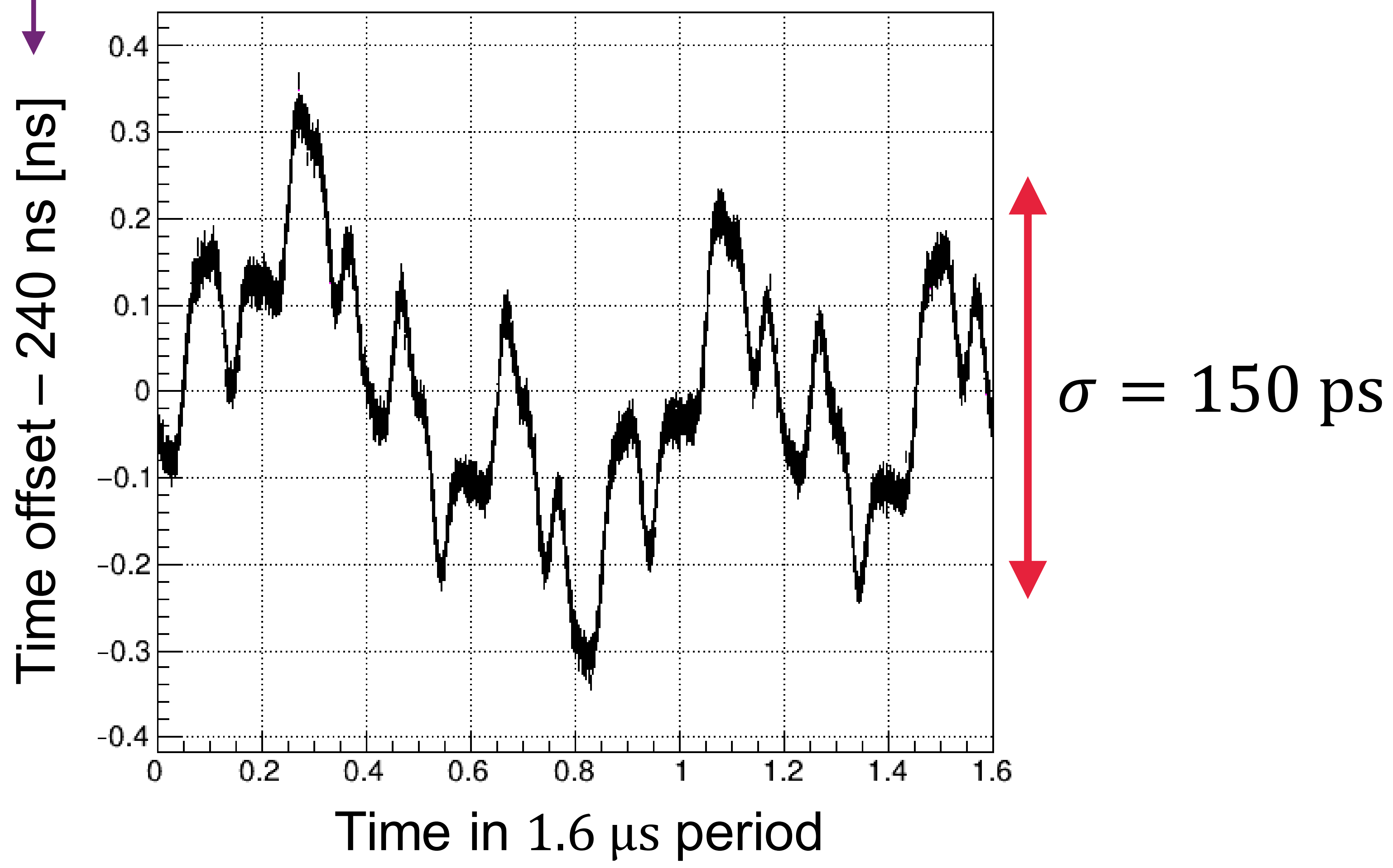
Clock phase noise

- Phase noise in clock modulates time offset between scintillators and telescope planes.
- Contributes $150\ \mathrm{ps}$ to cluster time resolution. Small compared to timewalk and pixel effects: $597\ \mathrm{ps}$ and $514\ \mathrm{ps}$ resp.
- Improves track time resolution:

$$\sigma(\mathrm{track}) = 276\ \mathrm{ps} \rightarrow 236\ \mathrm{ps}$$







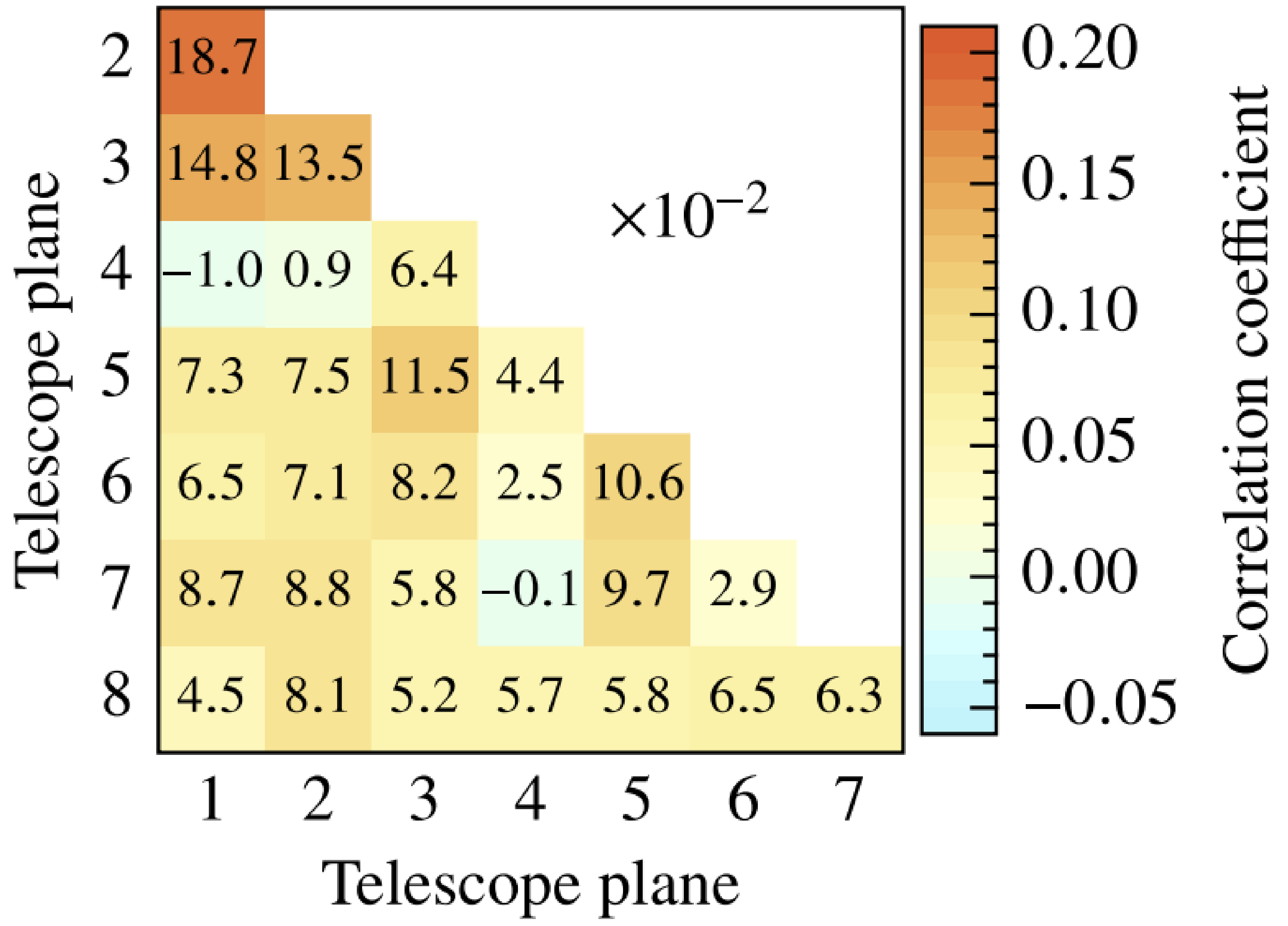
Plane time correlation

- Measured as: $\rho_{ab} = \dfrac{\mathrm{cov}(t_a - t_{\mathrm{up}}, t_b - t_{\mathrm{down}})}{\sigma_a\, \sigma_b}$
- Taking into account correlations correctly predicts track time resolution:

$$\sigma_{\mathrm{track}} = \left(\mathbf{1}^{\mathrm{T}} \mathbf{C}^{-1} \mathbf{1}\right)^{-1/2} = 436\ \mathrm{ps}$$ (Measured: $438\ \mathrm{ps}$)

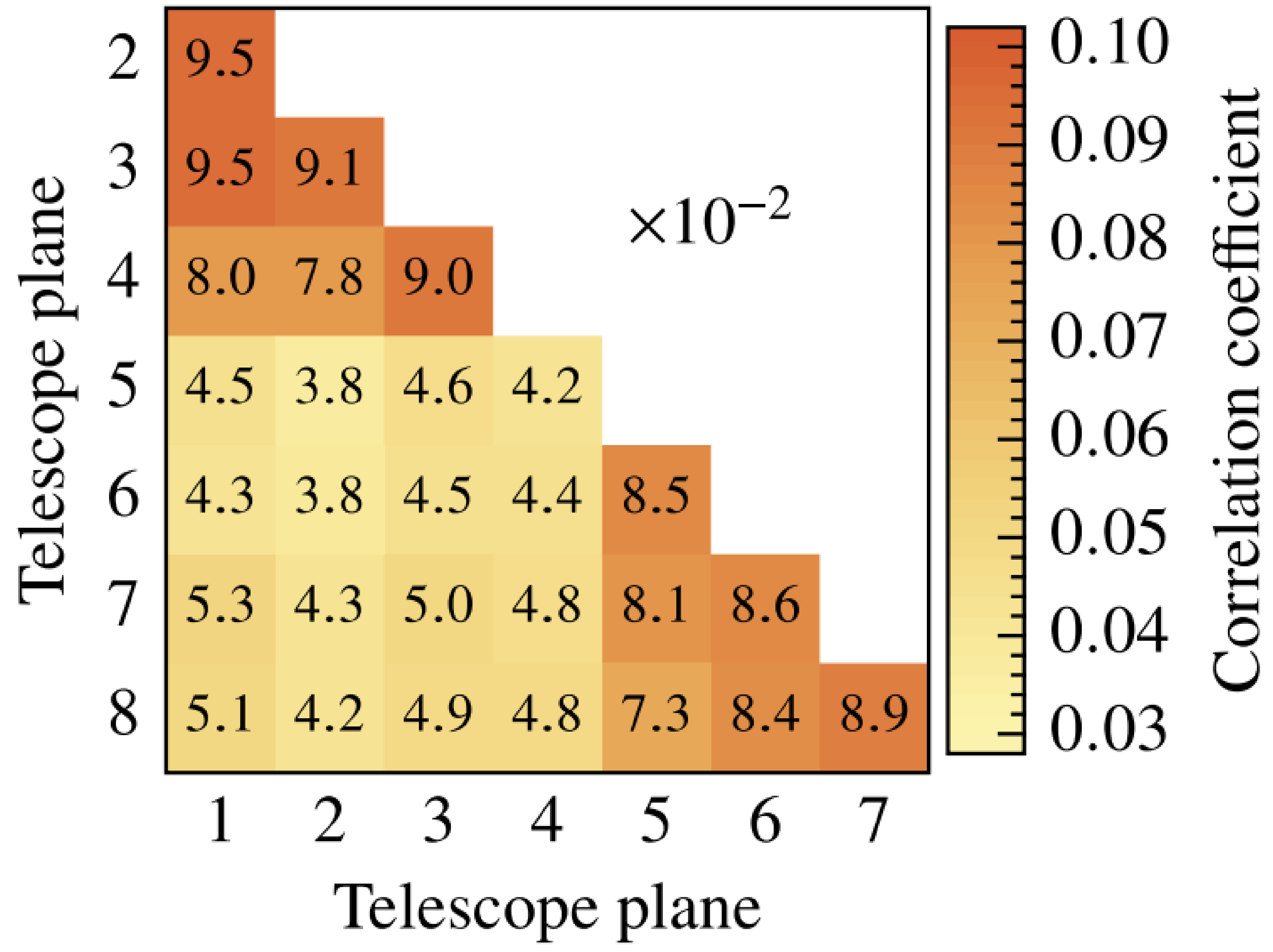
Covariance matrix of plane time measurements

Correlations before corrections

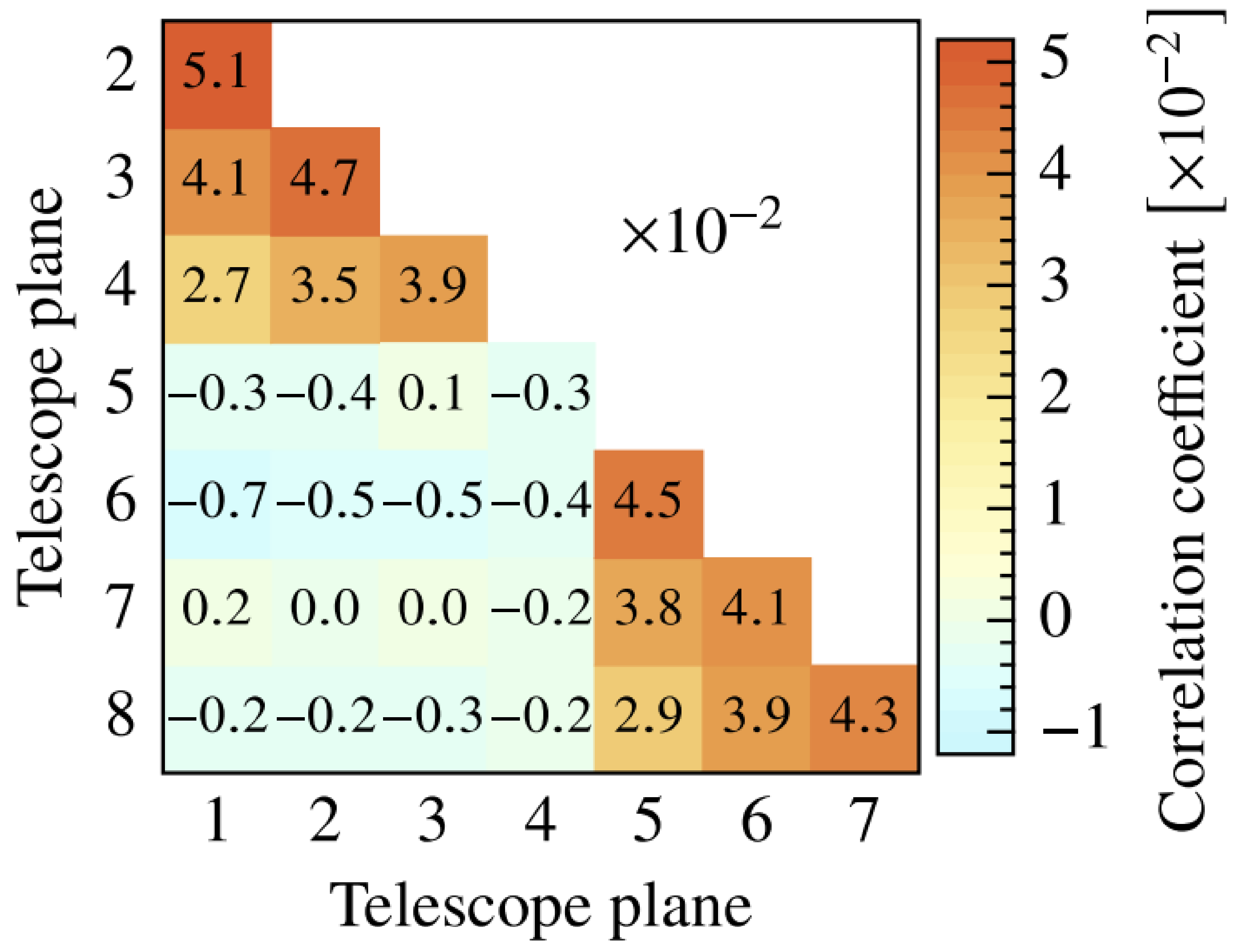


After timewalk and pixel corrections

Without clock correction



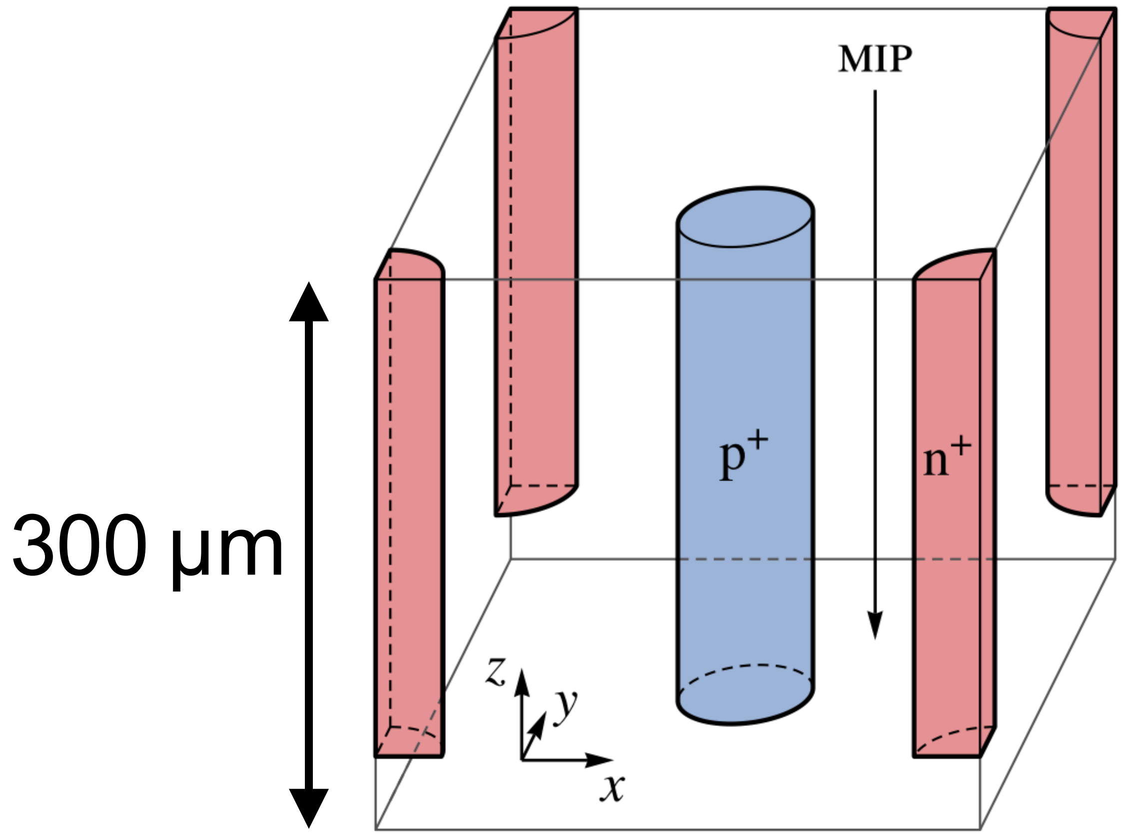
With clock correction

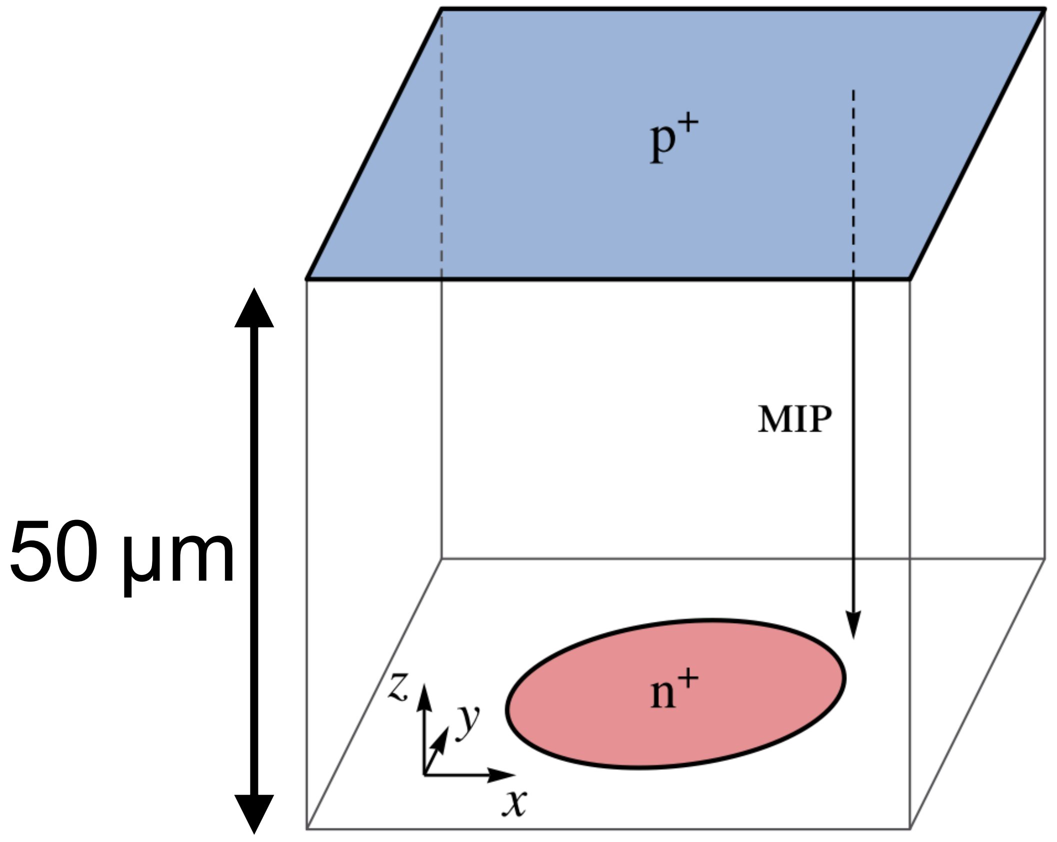


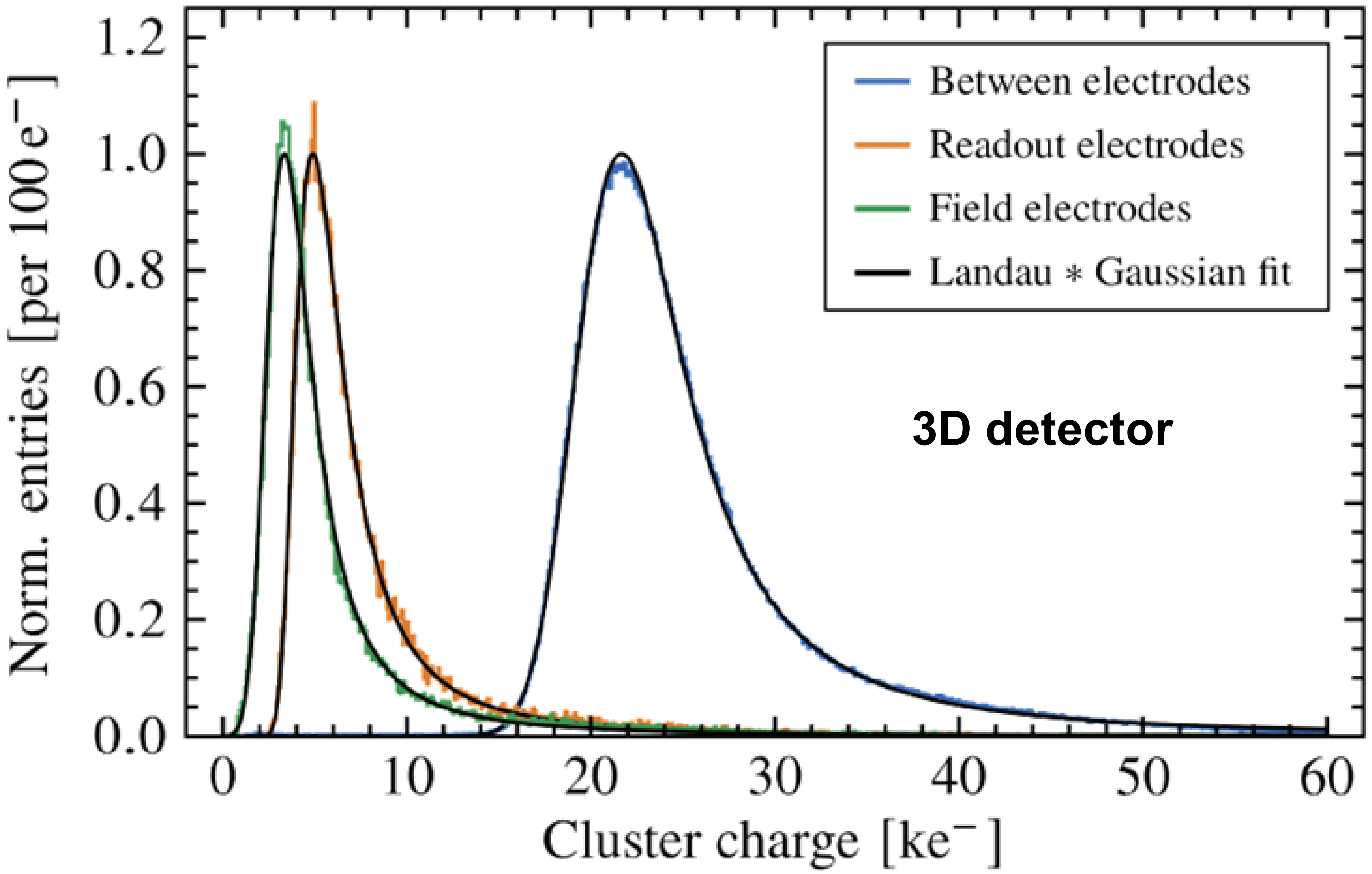
DUT charge distributions

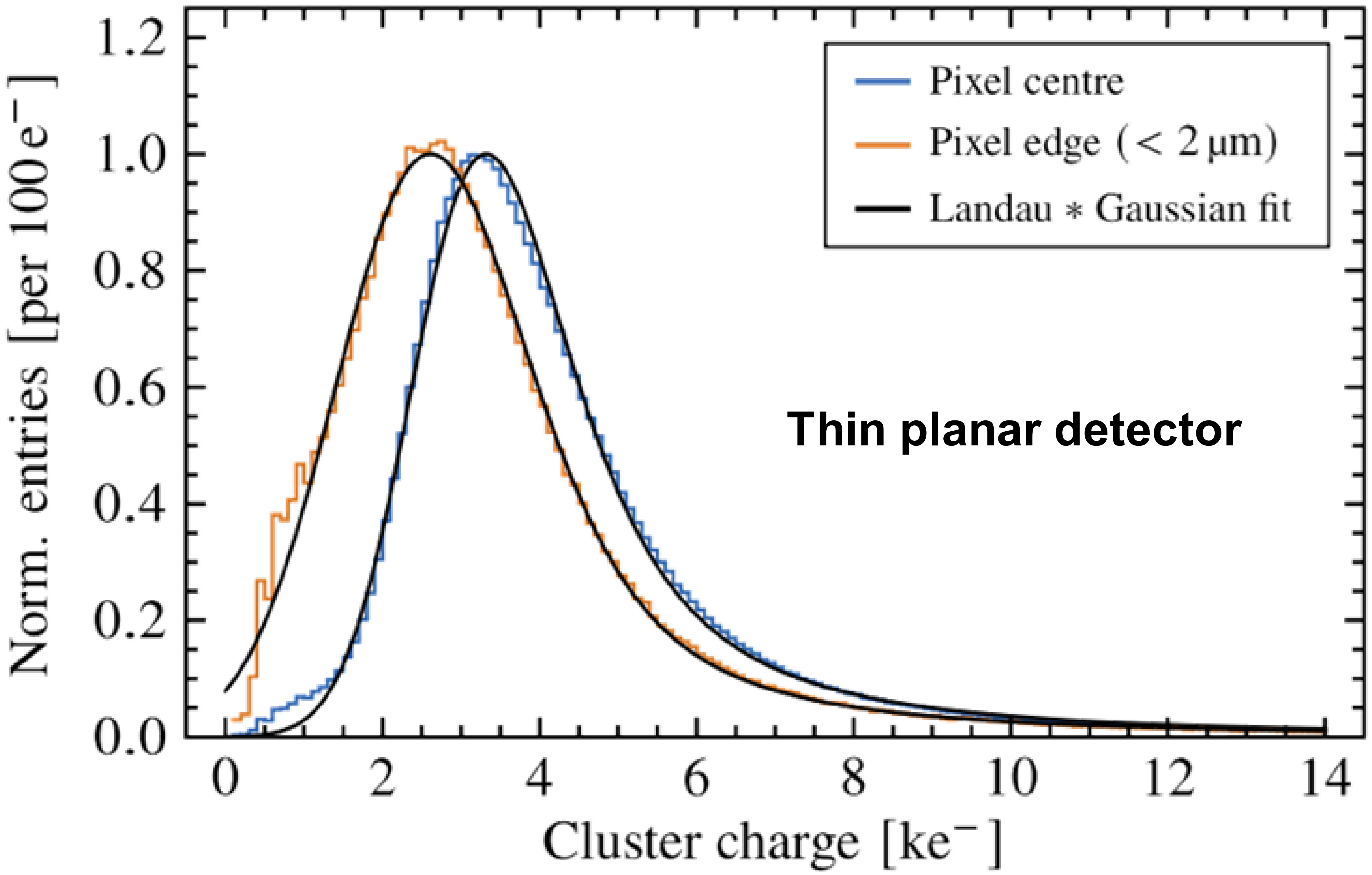
K. Heijhoff *et al* 2021 *JINST* **16** P08009 [DOI: 10.1088/1748-0221/16/08/P08009]

- MIPs going through electrodes of 3D sensor only generate charge in small region



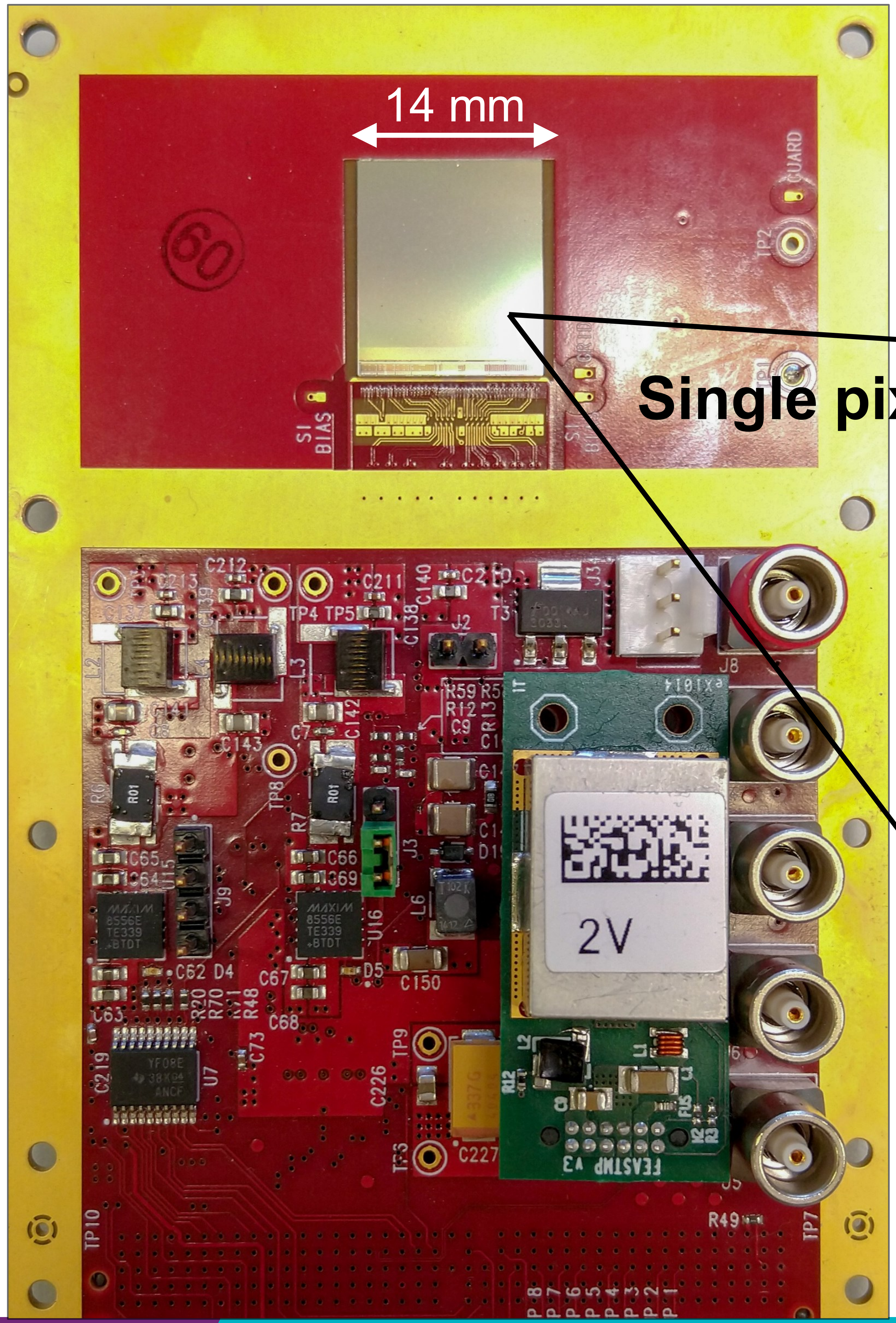




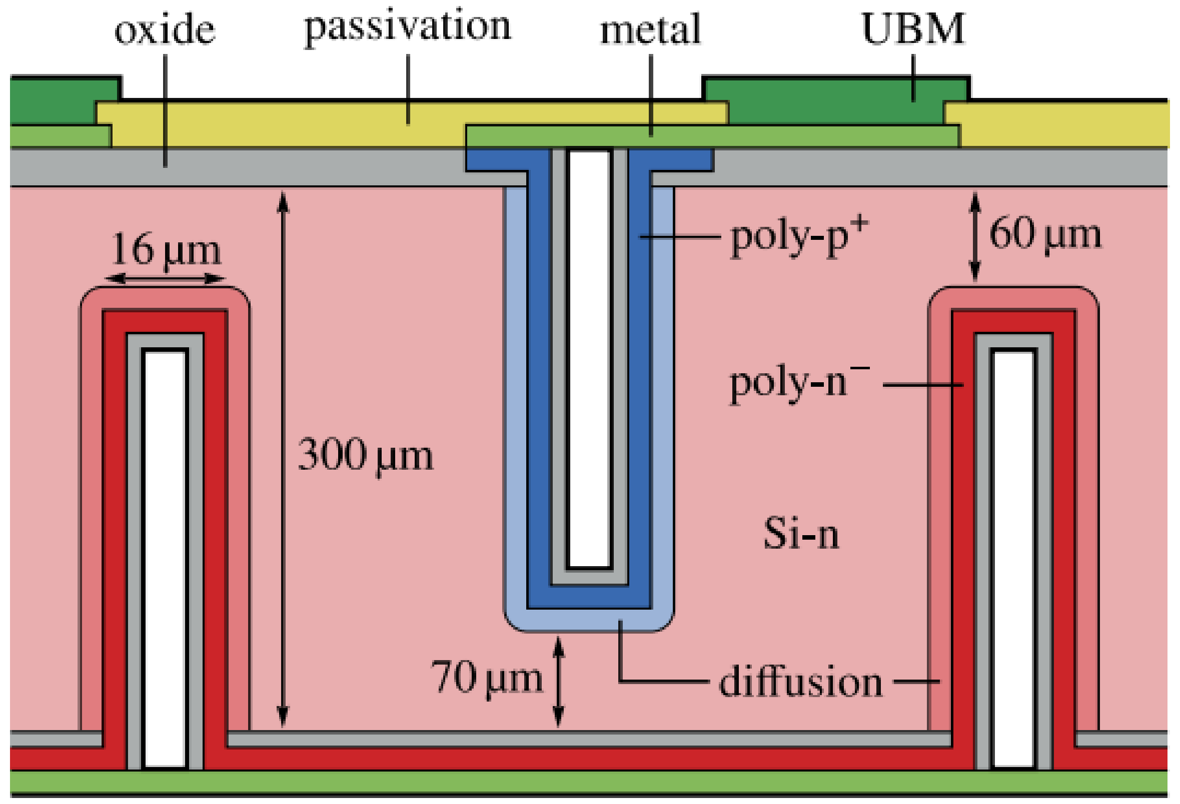


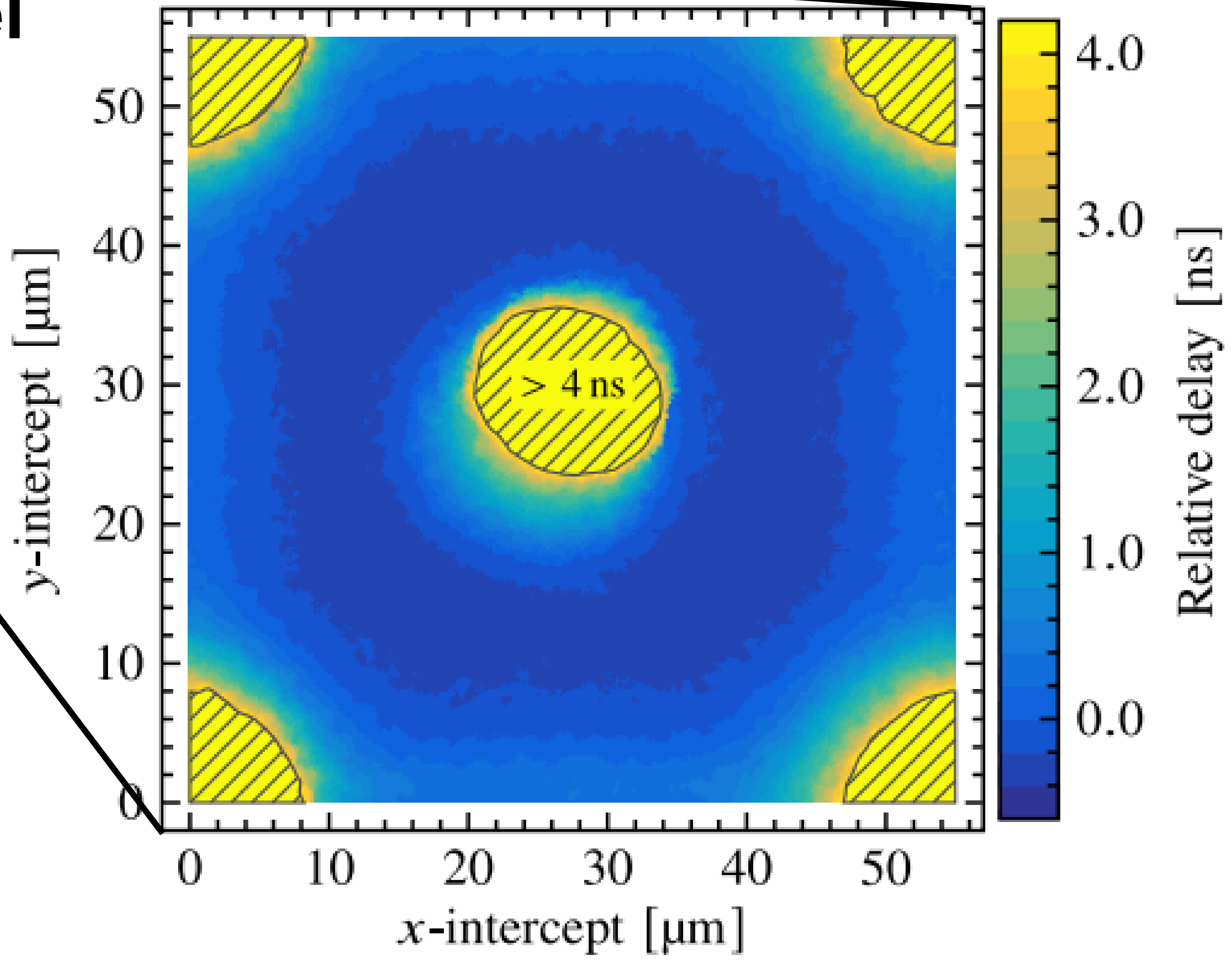
Intrapixel time delay

Timepix3 pixel ASIC + sensor

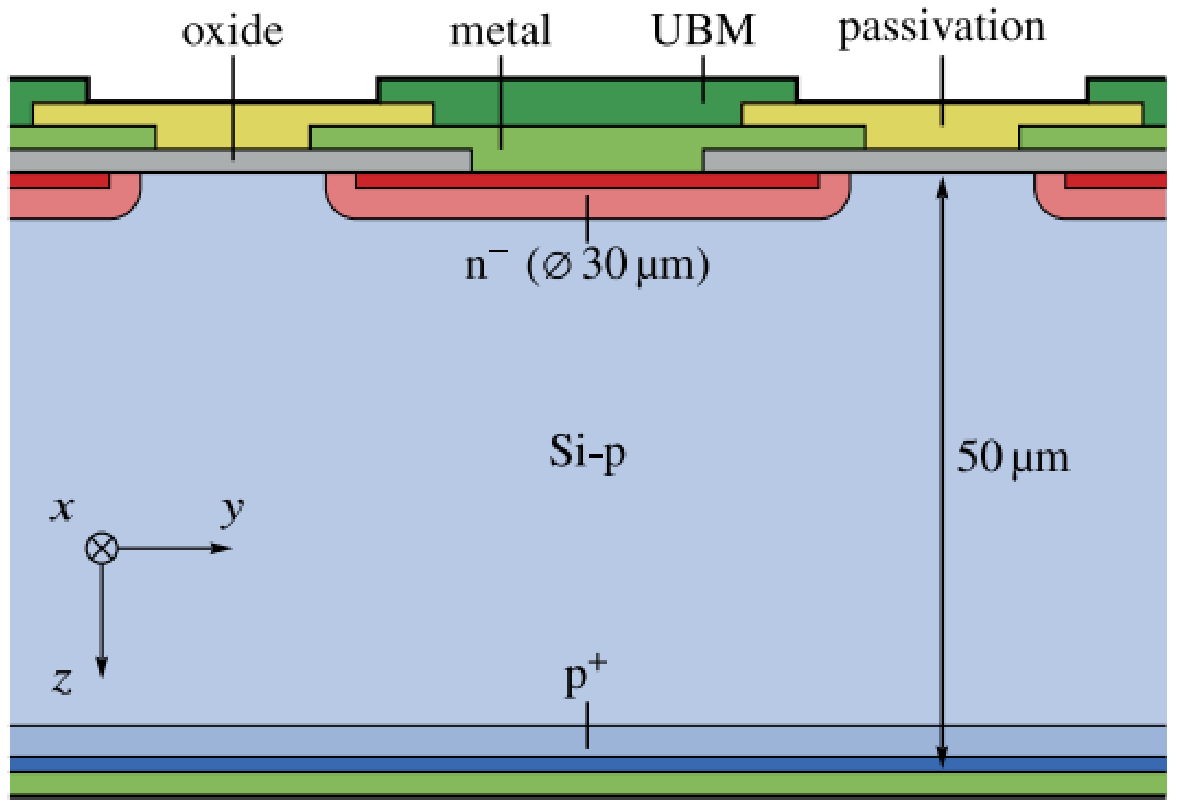


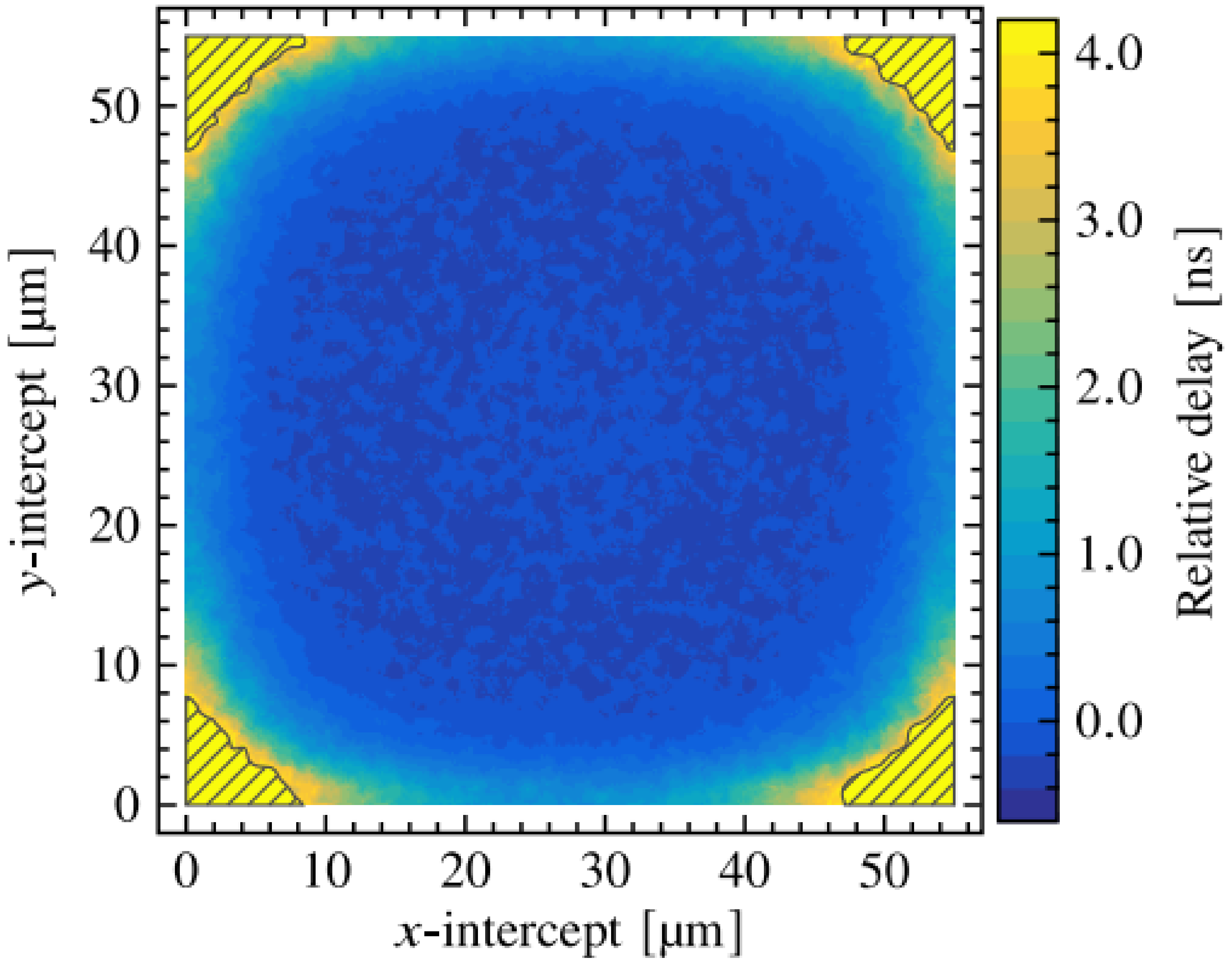
3D sensor technology





Thin planar sensor





K. Heijhoff *et al* 2021 *JINST* **16** P08009 [DOI: 10.1088/1748-0221/16/08/P08009]